Chapter 3

Modified DTBE Technology for Fabricating Thin-Film Devices on Flexible Plastic Substrates

Thin-film transistors on flexible plastic substrates are of considerable interest because of several advantages including light weight, thinness, flexibility, shock resistance, and low cost. In *Chapter 2*, we had discussed several device transfer methods including a successful demonstration of DTBE technology by CMP and wet etching [3.1]. The thinning process of backside silicon through CMP may apply to rigid substrate for polishing backside Si to a thickness around 20 ~ 40 μm. However, since the Si itself becomes flexible when its thickness below 100 μm, the large mechanical stress accompanied with the polish step could damage the plastic, ultra-thin glass or TFT backplanes; samples would probably be scratched by colloidal slurry or even break after CMP. Besides, we supposed that a deformable substrate, like the polish pad used in CMP equipment, could contribute to undesired side effects such as planarization uniformity. To help understanding, Fig. 3-1 depicts the imaginary consequences exaggeratedly when the samples on flexible substrates were polished by CMP. Based on these reasons, a backside thinning process employs full, or at least dominantly wet chemical etching was developed.

In this chapter, we investigated the etching properties of KOH and HNO_3/HF mixture. Besides, in order to improve the etching speed, etching uniformity and consumption of chemicals, a novel concept of "spin etching" was examined. A modified DTBE technique with full chemical etching was demonstrated. Finally, except transferring poly-Si, an idea of transferring crystal Si from a conventional Si wafer by spin etching was also discussed in this chapter.

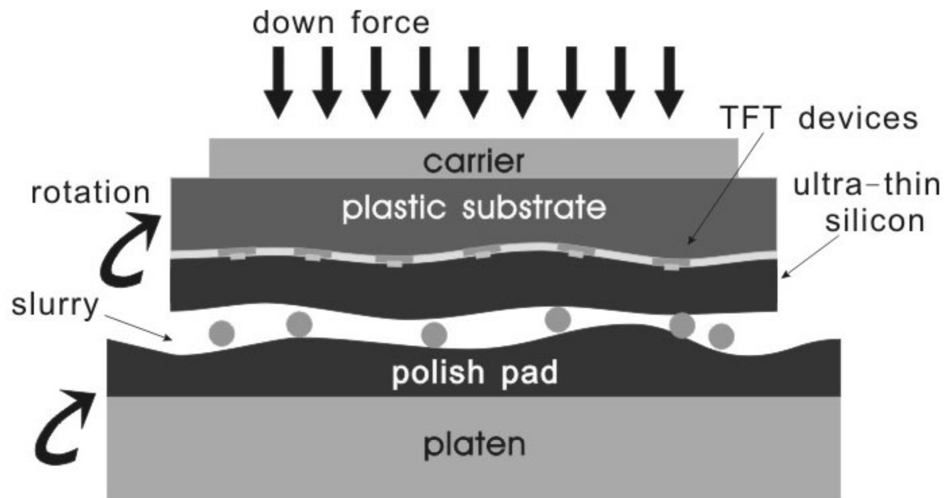


Figure 3-1 Schematic diagram for samples on a flexible substrate being polished by CMP process

3.1 Introduction to Wet Chemical Etchant of Silicon

3.1.1 Etching Mechanism of KOH

Aqueous alkaline solutions are commonly used in silicon etchants such as KOH, NaOH, TMAH (Tetra Methyl Ammonium Hydroxide) and NH_4OH. An electrochemical model for the reaction mechanism has been described and is believed to be useful for all types of alkaline solutions [3.2]. The reaction is redox (reduction and oxidation) process and the key reaction species is the HOH/OH^- redox couple in the etching solution. In the oxidation reaction, a silicon atom is removed from the surface by reaction with four OH^- ions:

$$Si + 4OH^- \rightarrow Si(OH)_4 + 4e^- \quad (3.1)$$

The neutral Si(OH)4 can readily diffuse away from the silicon surface into the solution. The four free electrons generated from the reaction above are located in the silicon very close to the surface. In the reduction reaction, these electrons leave the silicon surface and react with HOH molecules close the silicon surface:

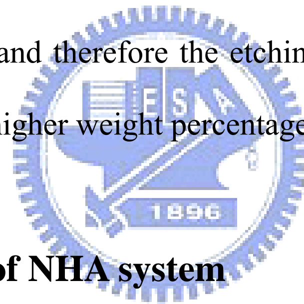
$$4HOH + 4e^- \rightarrow 4OH^- + H_2 \quad (3.2)$$

Only these OH^- ions generated at the silicon surface are considered to be the main reacting species. The OH^- ions from the bulk of the etching solution experience a repulsive force from the negatively charged silicon surface and therefore do not play a major role in the reaction.

On the other hand, the etching mechanism of silicon dioxide by aqueous alkaline solutions was described in [3.3]:

$$SiO_2 + 2OH^- \rightarrow Si(OH)_2^{2-} \tag{3.3}$$

According to the above equation, the etching rate of silicon dioxide depends on the concentration of OH ions in the bulk of the etching solution. A linear dependence of SiO_2 etching rate as a function of the molar KOH concentration can be observed; the maximum etching rate occurs at 35% wt. KOH. Besides, as pH values larger than 2.8, negative charges build up on the oxide surface in the KOH solution, hindering the diffusion of OH^- ions but not for neutral water molecules, and therefore the etching rate decreases with the square of the water molar concentration at higher weight percentages of KOH [3.4].



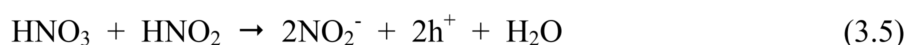
3.1.2 Etching Mechanism of NHA system

Except aqueous alkaline solutions, the etchants most commonly used in the isotropic etching of silicon are mixtures of hydrofluoric acid (HF), nitric acid (HNO_3), and acetic acid (CH_3COOH), the so-called HNA system [3.5], [3.6], also known as poly-etchant [3.7].

The reaction is initiated by promoting silicon from its initial oxidation state to a higher oxidation state:

$$Si + 2h^+ \rightarrow Si^{2+} \tag{3.4}$$

The holes are produced by the following autocatalytic process:



$$HNO_3 + HNO_2 \rightarrow 2NO_2^- + 2h^+ + H_2O \tag{3.5}$$

$$2NO_2^- + 2H^+ \rightarrow 2HNO_2 \tag{3.6}$$

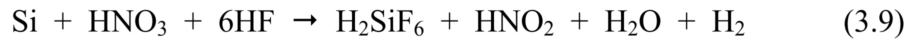
Si^{2+} combines with OH^- (from the dissociation of H_2O) to from $Si(OH)_2$ which subsequently liberates H_2 to form SiO_2:

$$Si(OH)_2 \rightarrow SiO_2 + H_2 \tag{3.7}$$

SiO_2 then dissolves in HF:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + H_2O \tag{3.8}$$

The overall reaction can be rewritten as:



$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2 \tag{3.9}$$

Here, the acetic acid acts as a buffer agent, which controls the dissociation of the nitric acid and preserves the oxidizing power of HNO_3 over a wide range of dilutions during etching. At very high HF and low HNO_3 concentrations, the etching rate is controlled by [HNO_3], because there is excess HF to dissolve any formed SiO_2. Contrarily, at low HF and high HNO_3 concentrations, the etching rate is controlled by the ability of HF to remove SiO_2. The latter etching mechanism is isotropic, that is, the etching rate not sensitive to crystalline orientation. The etching rate of HNA system is affected by the mix ratios, temperature, the level of agitation, and the dopant material/doping concentration in the Si wafer [3.8].

3.2 Experimental: Device Transfer by Backside Si Thinning with Conventional Wet Chemical Etching

3.2.1 Sample Preparation

To reduce the period of device fabrication, we designed a simple test structure with Al strips on oxidized silicon wafers in this experiment. Specifically, a 1.2 μm thermally grown SiO_2 layer was formed on the 4" Si wafers by furnace at 1050°C. Then aluminum of 500 nm was evaporated and patterned. After bonding to the plastic substrates, a passivation layer of TEOS SiO_2 by PECVD was capped. Figure 3-2 shows the cross-sectional view of this test structure. In this structure, the thick SiO_2 was regarded as an etching stop layer while the patterned Al lines can be inspected conveniently by OM after DTBE process.

We also designed poly-Si resistors for examining the uniformity of DTBE technique.

These resistors were also fabricated first on an oxidized silicon wafer. The poly-Si layer of 300 nm was deposited by LPCVD with SiH_4 source at 620°C, 120 mtorr. Then a phosphorus implantation with dosage of 2×10^{15} cm^{-2} was performed at 60 keV. After the activation process by furnace at 950°C for 30 min, the poly-Si layer was patterned, followed by the 500 nm Al evaporation and metallization. The cross-sectional view of a poly-Si resistor was depicted in Fig. 3-3.

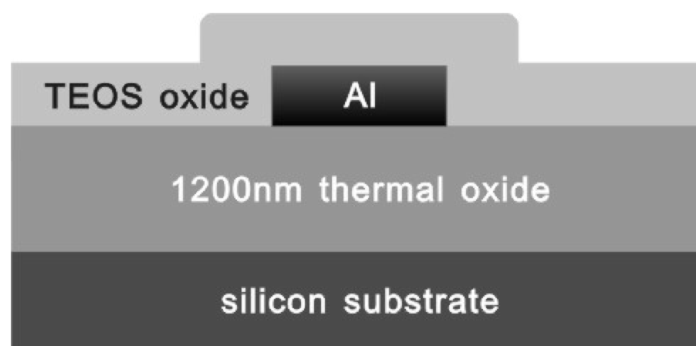


Figure 3-2 Cross-sectional view of a test structure with Al strips on an oxidized Si wafer for DTBE experiment

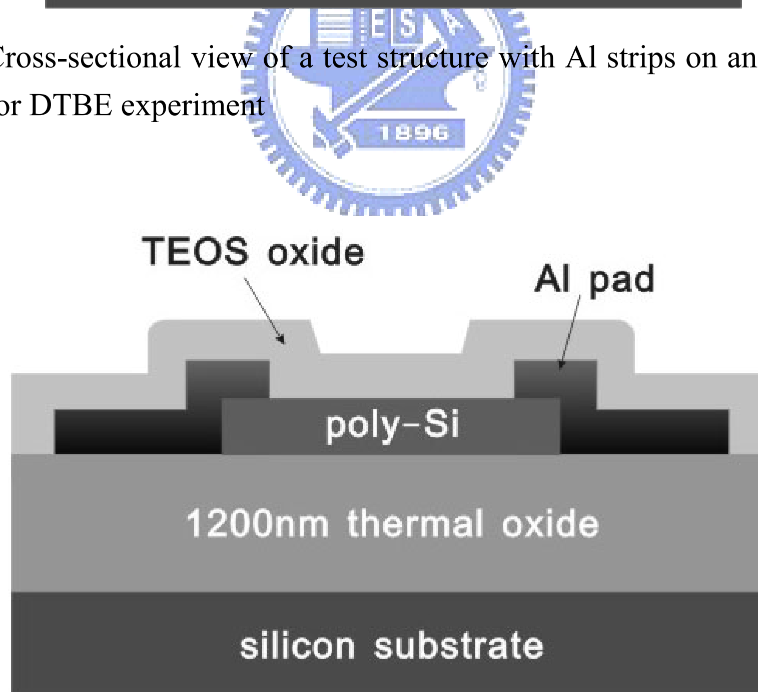


Figure 3-3 Cross-sectional view of a poly-Si resistor

3.2.2 The Choice of the Plastic Substrate

The mCOC backplane used in *Section 2.4* is as thick as 700 μm and not flexible. Therefore, the ARTON™ film made by JSR Corp. was adopted as the plastic substrate in this work. Figure 3-4 shows the chemical structure of ARTON™ film [3.9], which is a new kind of cyclic olefin polymers (COP) functionalized with the ester side chain (COOR) to control T_g [3.10], [3.11]. Some of the important features of ARTON™ film were listed below:

1. High total light transmittance above 93%
2. High heat resistance with glass transition temperature = 170°C
3. Low water absorption of 0.4% (unknown testing conditions)
4. Good adhesion to layers such as hard coating, printing inks and ITO, etc.

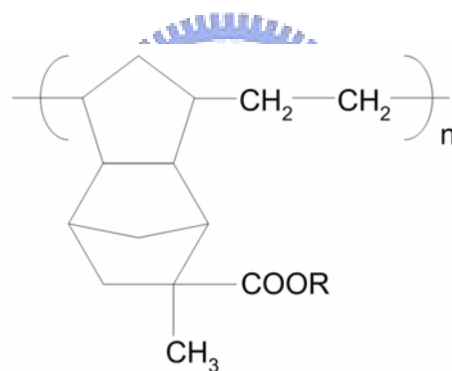


Figure 3-4 The chemical structure of ARTON™ film. This film is a new kind of cyclic olefin polymers functionalized with the ester side chain to control T_g

Moreover, the transmittance and reflectance of glass, PC, PET and ARTON™ films were compared with each other, as illustrated in Fig. 3-5. The thickness of these plastic films was all 100 μm and that of glass was 1.1 mm. Incident angle of light with various wavelengths was 12 degree. One can find the transmittance of ARTON™ is the highest while the reflectance was the lowest among those plastic substrates, and its performance is even better than glass. Additionally, the ARTON™ film has good resistance to most chemicals used in the semiconductor fabrication such as ACE, IPA, TMAH (developer), KOH, HF, etc.

and moderate resistance to HNO_3 (becoming slightly yellowish after immersion in it for a long time). Although the requirements for plastic substrates in DTBE process is not strictly constrained, we still chose ARTON™ film as the substrate in this work.

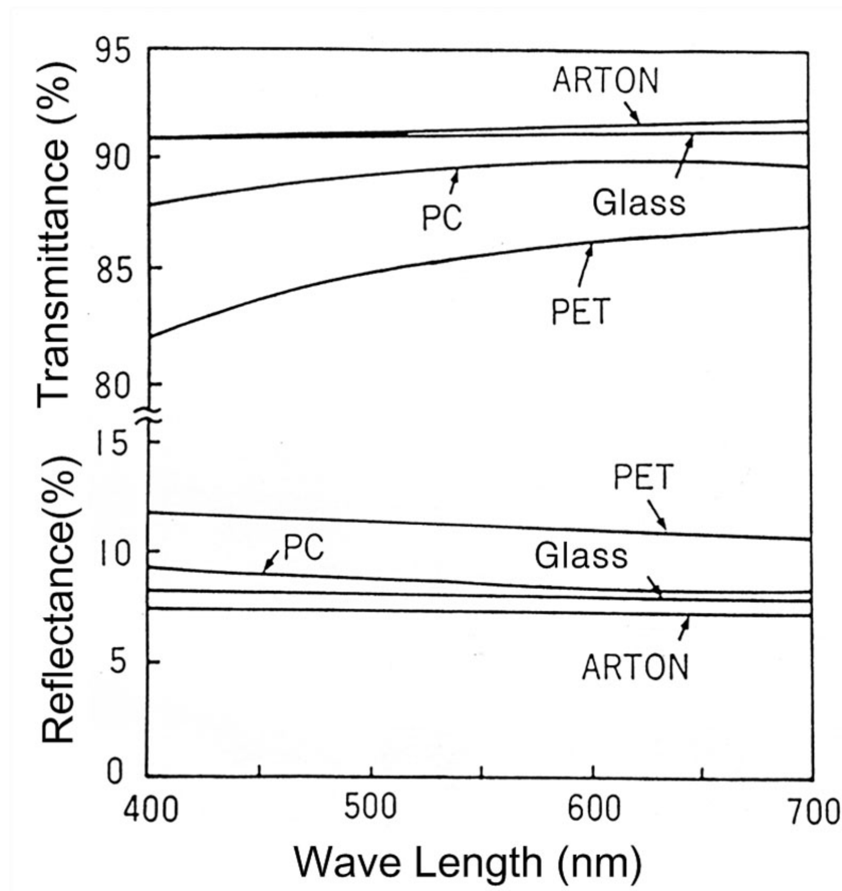


Figure 3-5 ARTON™ film offers superior optical properties in comparison with PC, PET and glass substrates

3.2.3 Bonding Process

To reduce the deformation of plastic substrates during thermal cycles, the ARTON™ films were pre-baked at 150°C for 30 min by hot plate. During the baking process, another heavy stuff such as a Si wafer was placed above the plastics to prevent it from curling up.

The adhesive used for wafer bonding was still EPO-TEK 301-2. However, EPO-TEK 301-2 is specially designed to bond the optical glass lens, and therefore its viscidity is poorer when utilized to bond the plastic substrate. So we deposited 5 ~ 100 nm SiO_2 on the surface

of plastics before bonding process by Dual E-Gun evaporation or by LPD-SiO_2 at room temperature. Furthermore, thermal solidification method must be used to increase the bonding intensity.

3.2.4 One-step Backside Si Etching by Wet Chemical Etching

For HNA system, different compositions of chemicals were tested. First, we started from the traditional poly-Si etchant. According to the etching results, D.I. water was then added and also the process temperature were modulated from 10 ~ 50°C. Besides, different weight percentages of KOH ranged from 17% to 28.5% at 70°C or 100°C were examined. Detailed etching conditions and the results will be discussed later.

3.3 Results and Discussion: Device Transfer by Backside Si Thinning with Conventional Wet Chemical Etching

ES 1896

3.3.1 Characterization of Different Si Etchant Composed by HNA System

Table 3-1 summarized various wet etching formula and the related etching rate of Si by HNA system.

Solution 1a is usually used for etching poly-Si film but it is too slow to be applied for DTBE. When the samples were etched with the solution of group 1b, violent reaction occurred and large quantity of NO_2 gas burst out because of rising of the process temperature. The etching rate was estimated to reach 18 μm/min and became too fierce to be controlled. Although the etchants of group 5a ~ 5c were put in the water bath with temperature of 10 ~ 50°C for 1 hr beforehand, exothermal nature of the chemical reaction still cause the efforts of temperature control by water bath ineffective. By adjusting the concentration of diluter such as H_2O and CH_3COOH, the etching rate can be varied from 80 ~ 4000 nm/min. With increasing the concentration of acetic acid, the dissociation of nitric acid would be effectively

suppressed and thus the etching rate reduced. On the other hand, adding water also decreased the etching rate but the NO_2 gas, one of the etching products, tends to adhere on the surface of Si and contributed to large surface roughness after backside etching, as shown in the AFM photograph of Fig. 3-6.

Table 3-1 Wet etching formula and the related etching rate of Si by HNA system

Number	Solution	Prescription	Etching Rate (nm/min)*
1a	$H_2O + HNO_3 + NH_4F$	33:64:3	200
1b	$HNO_3 + CH_3COOH + HF$	20:7:6	N/A
2a	$H_2O + HNO_3 + CH_3COOH + HF$	67:20:7:6	~0
2b	$H_2O + HNO_3 + CH_3COOH + HF$	33:20:7:6	200 ~ 280
2c	$HNO_3 + CH_3COOH + HF$	20:21:6	600
2d	$HNO_3 + CH_3COOH + HF$	20:42:6	80 ~ 100
3a	$H_2O + HNO_3 + CH_3COOH + HF$	16:20:14:6	520
3b	$H_2O + HNO_3 + CH_3COOH + HF$	10:20:14:6	1380
4a	$H_2O + HNO_3 + CH_3COOH + HF$	5:20:14:6	4000
5a	$HNO_3 + CH_3COOH + HF$	20:7:6	700@10°C
5b	$HNO_3 + CH_3COOH + HF$	20:7:6	6800@23°C
5c	$HNO_3 + CH_3COOH + HF$	20:7:6	>10000@50°C

* The etching rate were estimated for the first 10 min of etching process

For each case of HNA etchants, the etching rate depends closely on the temperature of etchants, the volume of Si to be etched, the continuous consumption of etching species and the etching period, so that finally the etching rate became unstable, hardly to be controlled. To make matters worse, the ARTON^{TM} film as well as the optical adhesive would degrade if being immersed in the nitric acid for a prolonged time. We concluded that the conventional wet etching by HNA system is not suitable for backside thinning process of DTBE.

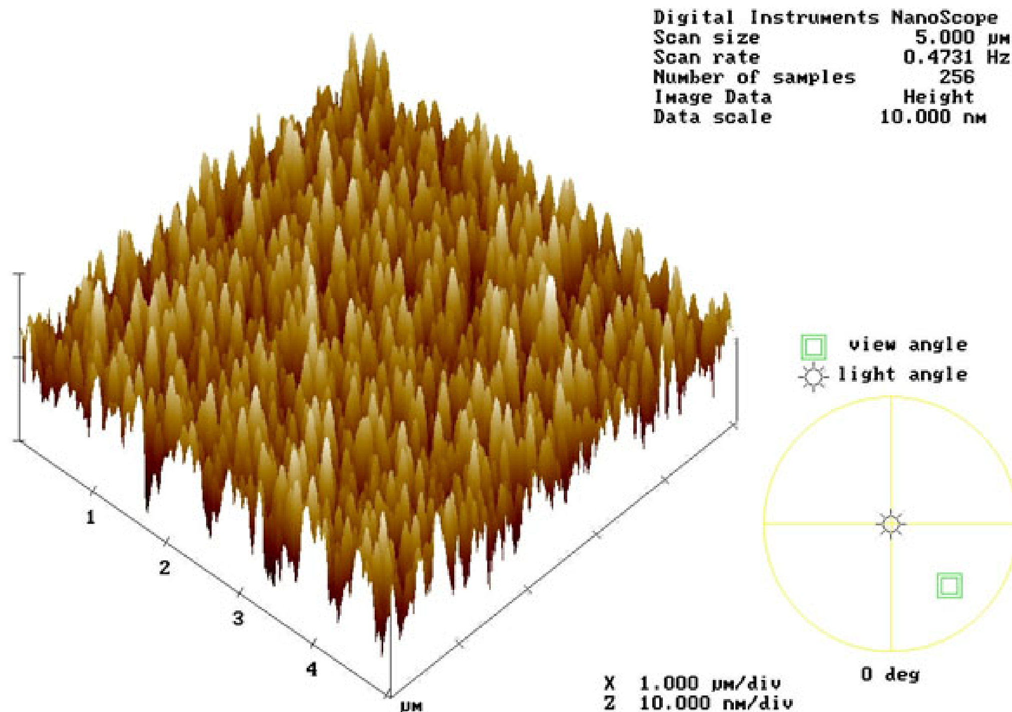


Figure 3-6 Surface roughness of Si etched by HNA solution for 15 min; rms value = 2.174 nm

3.3.2 Characterization of Si etching by KOH

High temperature potassium hydroxide solution has been used to etch Si for many years. Figure 3-7 exhibits the etching rate of Si and etching selectivity to SiO_2 by KOH at different temperature. The etching rate of 21.25 wt.% KOH at 100°C reaches 3.42 µm/min while a high Si/SiO_2 selectivity can be maintained above 100. Moreover, by reducing the reaction temperature to 70°C, the Si/SiO_2 selectivity can exceed 180. Thus a two step wet etching process seems feasible, that is, thinning the backside Si with high temperature KOH etching to reduce the etching time and then removing the residual Si without seriously damaging the etching stop layer by a low temperature KOH etching with a high Si/SiO_2 selectivity. The AFM photograph of Fig. 3-8 also exhibits a satisfactory surface roughness after KOH etching.

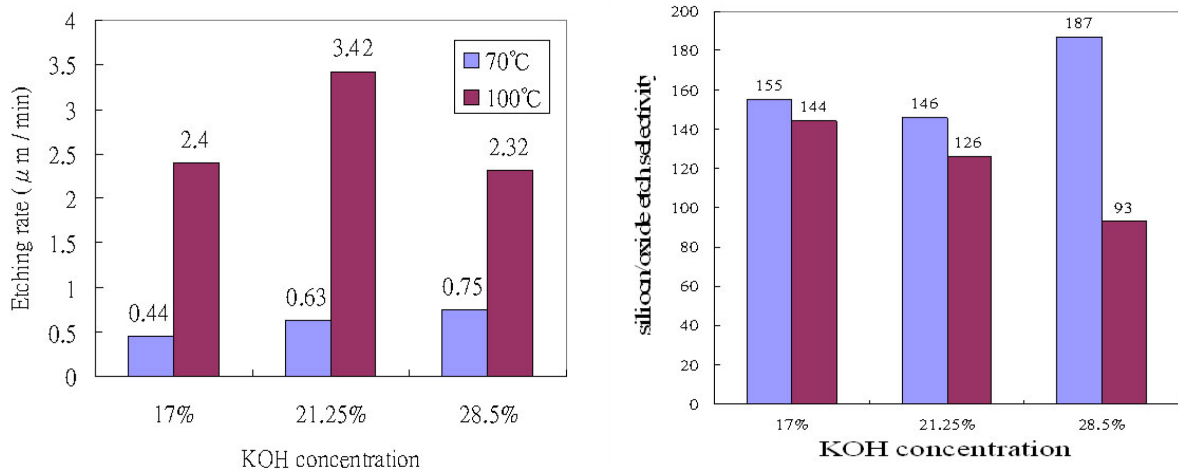


Figure 3-7 Etching rate of Si and etching selectivity to SiO_2 by KOH at different temperature

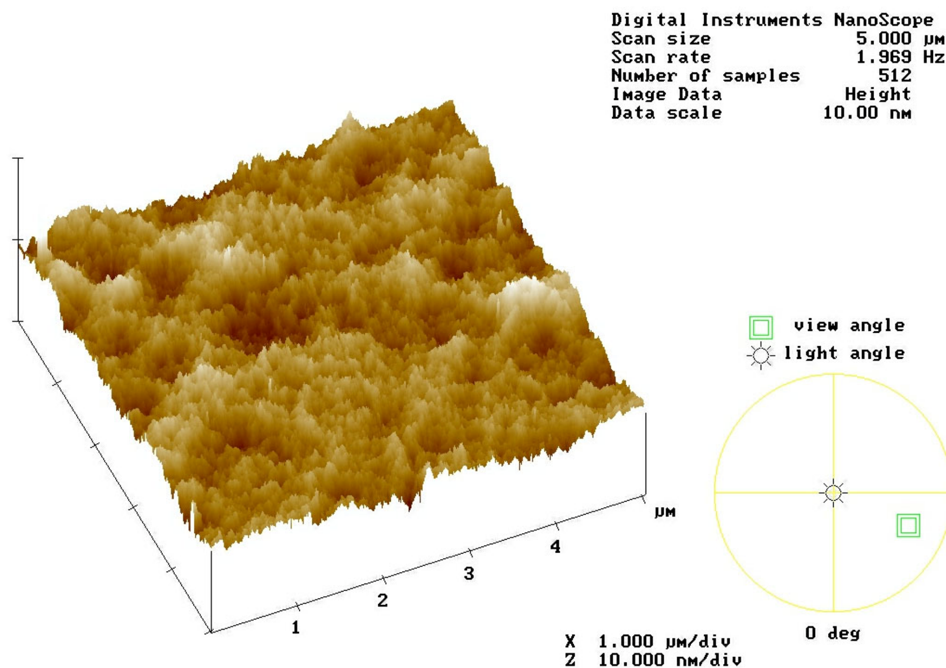


Figure 3-8 Surface roughness of Si etched by KOH for 15 min; rms value = 0.68 nm

3.3.3 Observation after DTBE with Wet Chemical Etching

According to the experimental results discussed in *Section 3.3.1 and 3.3.2*, 21.25 wt.% KOH at 100°C seems quite suitable for backside etching process. However, we found that the bonded samples peeled off from the plastic substrate after being etched with KOH for an hour,

as shown in Fig. 3-9. We believed that the thermal stress and the poor bonding intensity between optical adhesive are responsible for the failure. Therefore, we strengthened the bonding strength by pre-coating a SiO_2 layer on the plastic substrate. Besides, after performing backside thinning process in 21.25 wt.% KOH for 1.5 ~ 2 hr at 100^oC, we turned off the heater and let the chemical temperature reduce naturally to 25^oC, which can prevent from an abrupt change of surface temperature as the samples (still very hot) soaked immediately in the D.I. water at room temperature. Next, we kept on etching the samples with HNA mixtures at room temperature for another 10 ~ 40 min until the transferred patterns can be seen.

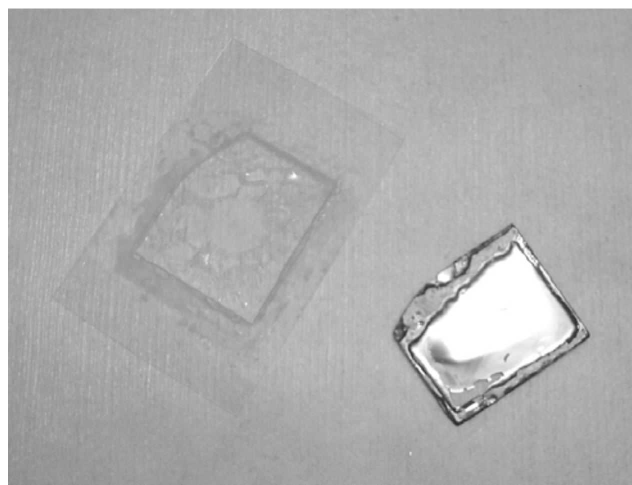
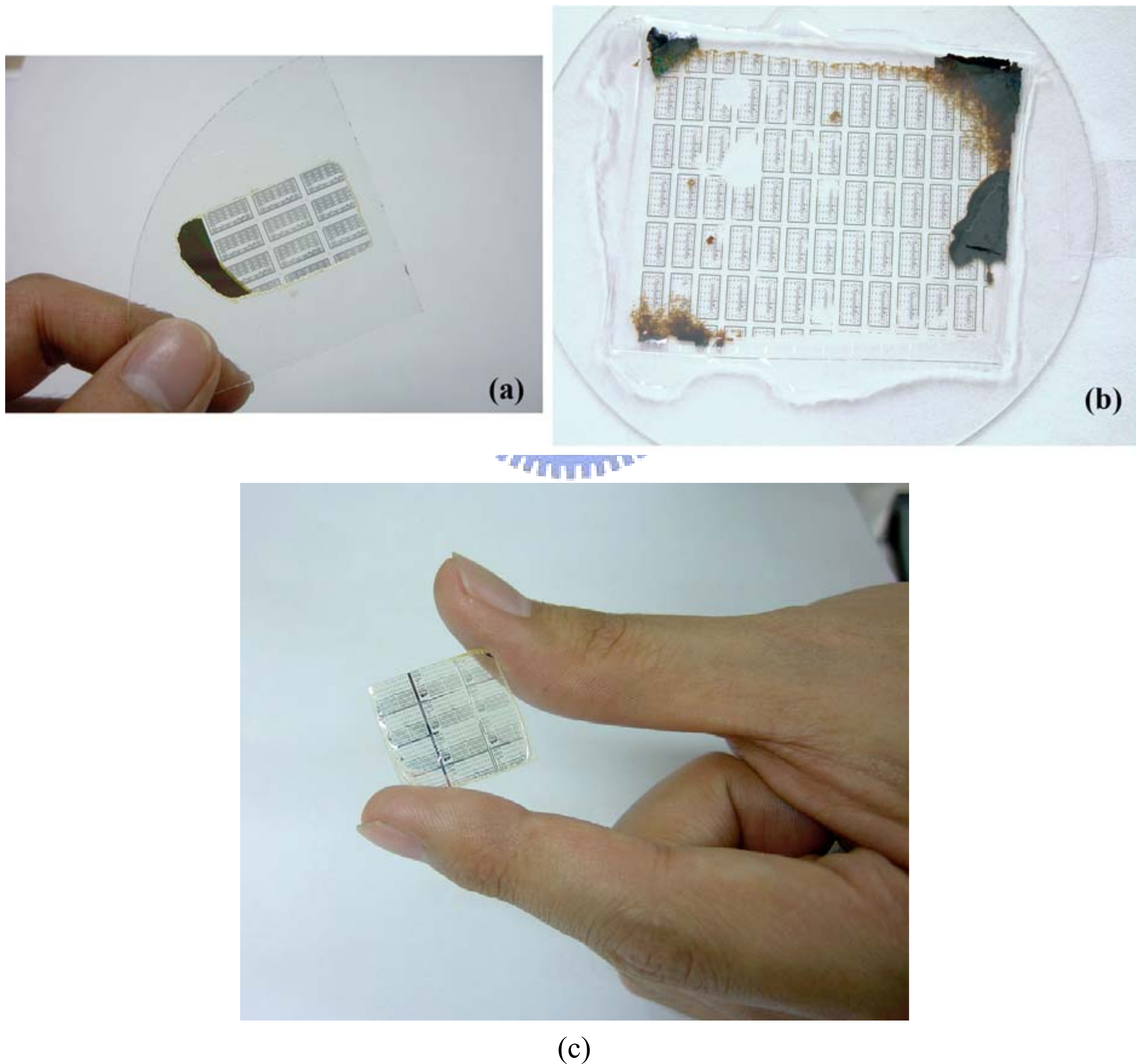


Figure 3-9 Failure sample after being etched in 21.25 wt.% KOH at 100^oC for 1 hour

Figure 3-10(a) and (b) show the thin-film devices manufactured by full wet chemical etching process on the glass while Fig. 3-10(c) exhibits the transferred TFTs on the flexible ARTON^{TM} substrate. Except the contour of the samples, no physical damage was found, indicating the thick SiO_2 etching stop layer plays an important role during DTBE, especially for a thinning process by full wet etching. Test patterns as large as 4 inch in diameter can be transferred to glass by backside etching with KOH. In addition, the resistance distributions of poly-Si resistors between DTBE processes are depicted in Fig. 3-11, where poly-Si resistors

with two different sizes (W/L = 10 μm/60 μm and 20 μm/60 μm) were compared. Slight deviation between these distributions before and after DTBE may result from the self-heating phenomenon because the poly-Si resistors on plastics were capped by a thick SiO_2 layer while both plastics and SiO_2 are poor thermal conductors. Since dissipated power is inversely proportional to resistance (where applied voltages swept from -30 V to +30 V), the samples with lower resistance value (i.e. W/L = 20 μm/60 μm) exhibits larger fluctuations after DTBE.



(c)

Figure 3-10 Successful results of device transfer by full wet chemical etching on the (a) (b) glass and (c) flexible ARTON^{TM} substrate

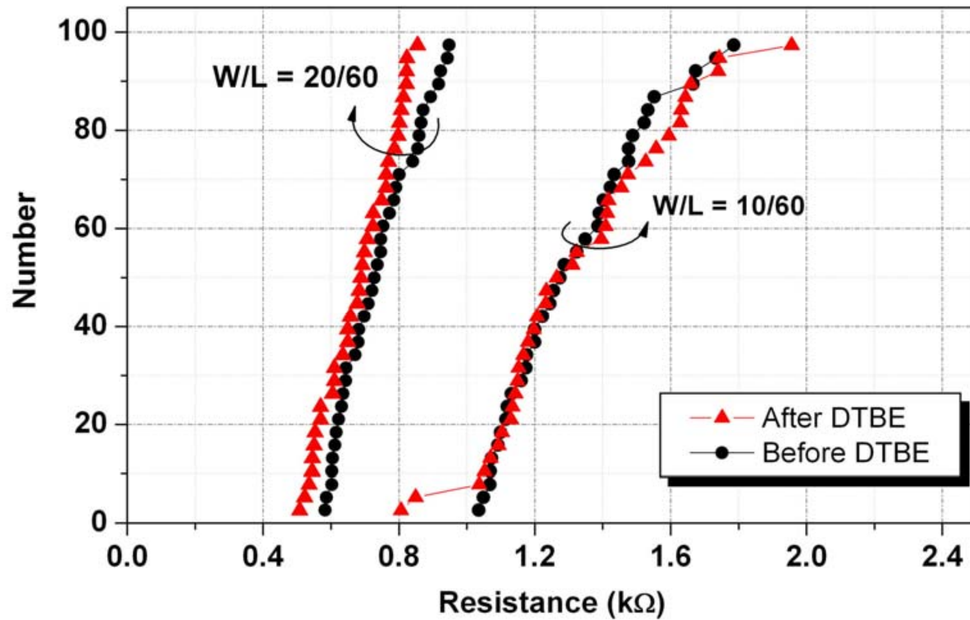


Figure 3-11 Resistance distributions of poly-Si resistors before and after DTBE process

3.4 Spin-Etching Technology

The spin etching technique has been used in the electronic industry for the cleaning of electronic substrates and even for global planarization of dual-damascene metal interconnects [3.12], [3.13]. In this section, the CMP or conventional wet etching steps in the previous DTBE method were replaced by the spin-etching process. In contrast to CMP, the spin-etching process exerts little mechanical stress or thermal stress on the sample, enabling the device to be transferred to a thin flexible backplane. Unlike CMP, spin-etching technique does not utilize colloidal slurry so that the surface after polish contains no scratch and it needs no special cleaning process to remove those embedded SiO_2 or Al_2O_3 particles after the etching process. Besides, spin etching consumes fewer chemicals than conventional wet etching; fresh chemicals keep supplying to the sample during spin etching, so the etching rate is high and the throughput is comparable to conventional wet etching. In this section, we will examine the spin-etching properties and its etching mechanism.

3.4.1 Experimental

Before the backside silicon are removed and the thin-film devices are transferred to a plastic substrate, the properties of the spin-etching process, including the etching rate, the uniformity and the selectivity, etc. should be clarified. Figure 3-12 schematically depicts the spin-etching equipment; the etching chemicals were dropped into the spinner through a manual valve in a funnel at an adjustable flow rate. The spinner was made of Teflon and was manufactured by Laurell Technologies Corp. A mixture of hydrofluoric acid (HF), nitric acid (HNO_3) and some acetic acid (CH_3COOH) was used as the main etchant for silicon. The spin speed of the samples varied from 1000 to 4000 rpm, while the flow rate of the etchant ranged from 100 to 333 ml/min.

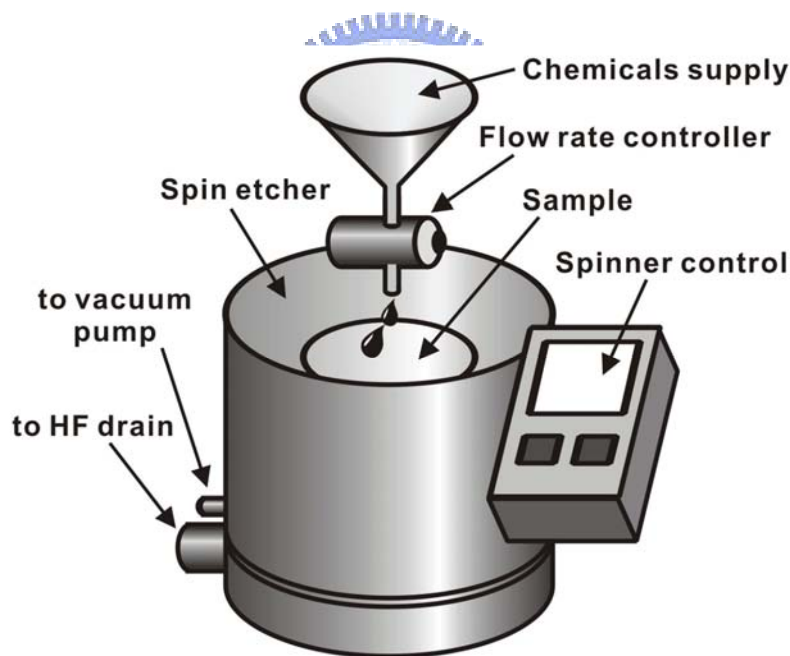


Figure 3-12 The schematic diagram of spin-etching equipment

The etching rate of silicon was calculated from the difference between the sheet resistances R_S of a 4-inch wafer before and after spin-etching process, i.e. the change in wafer thickness can be expressed as

$$\Delta \text{ thickness (T)} = \rho/R_{S\text{-before}} - \rho/R_{S\text{-after}} \quad (3.10)$$

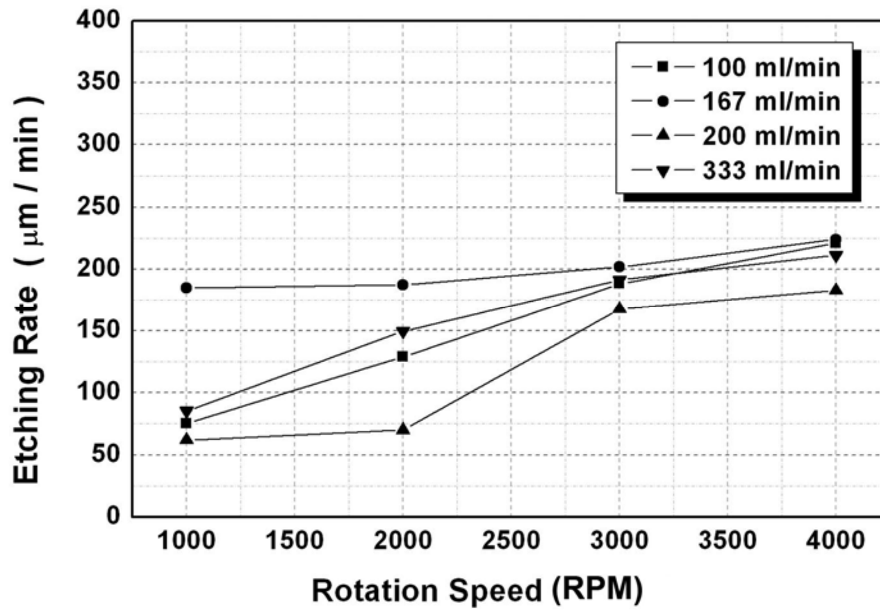
where ρ is the resistivity of a Si wafer.

In order to test the etching selectivity of Si to silicon nitride or silicon dioxide, a layer of 2300 Å Si_3N_4 or a 6000 Å thick SiO_2 was formed on a Si substrate by LPCVD and wet oxidation, respectively. Both the etching selectivity and the etching uniformity were accurately measured using an ellipsometer.

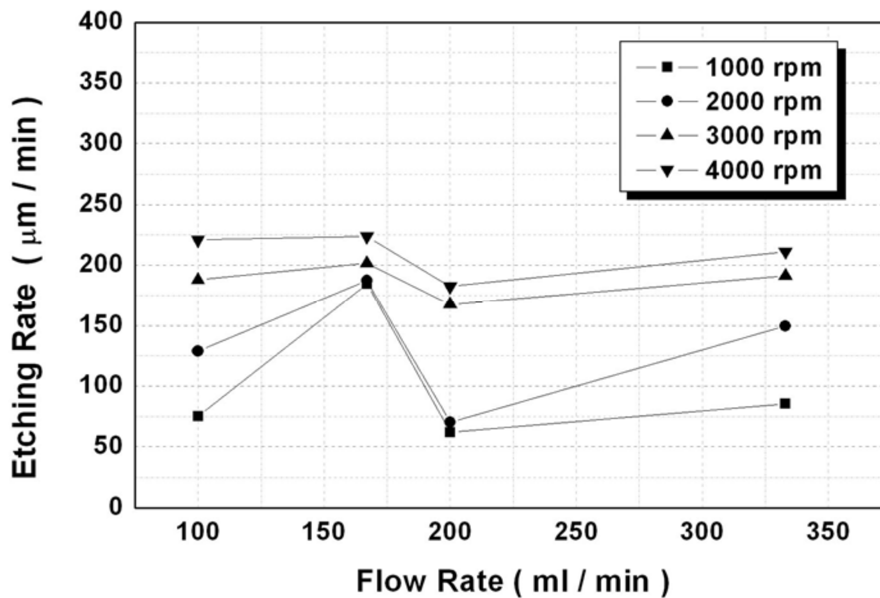
3.4.2 Results and Discussion: Spin-Etching Mechanism, Etching Rate, Selectivity, and Uniformity

The most serious problem encountered during backside etching concerns the process temperature. Since the thermal expansion coefficients of Si and the polymeric materials are significant, the plastic substrate easily rolls up and cause the Si to peel away from the plastic during the exothermic reaction of backside etching process. Moreover, several plastic substrates and adhesives are eroded by hydrofluoric or nitric acid, so the conventional wet etching cannot be applied to them. In spin etching, however, the sample is spun at a high speed, while the fresh cooling chemicals are supplied continuously to the wafer surface; accordingly, the influence of temperature is almost eliminated and the plastic substrate or adhesives are not damaged.

Figures 3-13(a) and (b) plots the curves of etching rate versus rotation speed and flow rate, respectively. Figure 3-13(a) reveals that the etching rate increases with the rotation speed, and that the maximum etching rate exceeds 200 μm/min at the highest spin speed of 4000 rpm and a chemical flow rate of 167 ml/min. Consequently, spin etching is a very efficient process compared to conventional wet etching (~2 μm/min @ 25℃). Given a 4-inch wafer with a thickness of 550 μm, the DTBE process can be completed in 3 ~ 5 min. Nevertheless, Fig. 3-13(b) shows no apparent relationship between the etching rate and the flow rate at a fixed spin speed. Specifically, the etching rate reaches a maximum at the flow rate of 167 ml/min and considerably declines above a flow rate of 200 ml/min.



(a)



(b)

Figure 3-13 Etching rate vs. (a) rotation speed and (b) chemical flow rate

A simple mechanism of spin-etching process depicted in Fig. 3-14 is proposed to further explain the observed phenomenon. The etching procedure involves three steps as following:

(a) First, a boundary layer is formed near the silicon surface where the etching species are rapidly consumed. All of the reactants diffuse through this boundary layer to support the reaction (mass transport control).

(b) The reaction species at the surface, e.g. HNO_3 and HF, will react with Si, in a process that depends strongly on the temperature (surface reaction control).

(c) The reaction products diffuse through the boundary layer and return to the bulk of the liquid (product diffusion control).

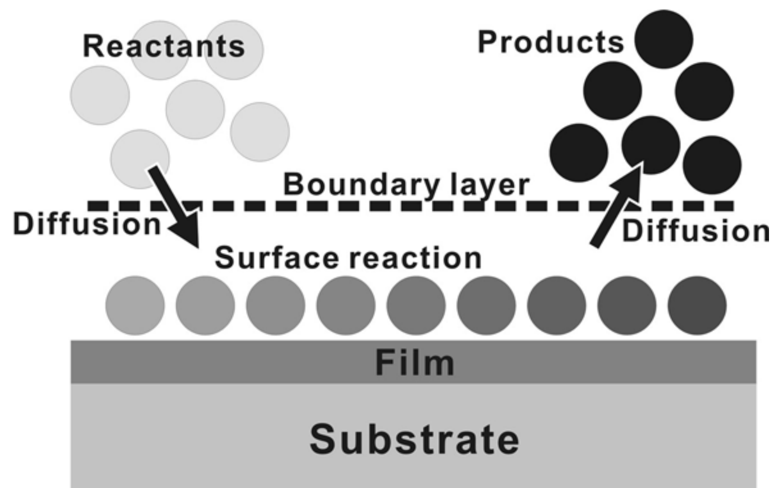


Figure 3-14 The proposed mechanism of spin-etching process

In spin-etching, the spin speed mainly affects steps (a) and (c), because a higher rotation speed yields a thinner boundary layer and thus a faster diffusion rate of both reactants and products. Accordingly, as shown in Fig. 3-13(a), the etching rate keeps increasing with spin speed at every flow rate and gradually saturates when the rotation speed larger than 3000 rpm, implying that the system is then in the *surface reaction control* regime. In this regime, increasing the flow rate of etching chemicals may cool the surface of the sample and slightly change the reaction rate.

At a low rotation speed (<2000 rpm), however, the total process is more like a conventional wet etching rather than a spin etching. Without help from the centrifugal force, the reaction products near the silicon surface would now be repelled by the supplied chemicals so that the etching rate increases with the flow rate from 100 to 167 ml/min, as shown in Fig. 3-13(b), indicating that the system is in the *diffusion control* regime. Moreover,

the system leaves the diffusion control regime and enters the surface reaction control regime as the flow rate increases. The etching speed then decreases significantly owing to the cooling effect of chemicals.

Figure 3-15 exhibits the etching rate with respect to the etching uniformity for Si_3N_4. A 4-inch wafer with a Si_3N_4 layer of 2300 Å was spun and etched by the poly etchant for totally 360 sec; every 120 sec, the etching process was terminated and the film thickness of Si_3N_4 was measured using an ellipsometer. The rotation speed was 4000 rpm and the flow rate was 100 ml/min. From Fig. 5, we can find that not only was the etching rate from the wafer center to the edge very uniform, but the etching repeatability was also satisfactory. (Data on the thickness of the film near the wafer edge could not be obtained using our equipment.) The etching selectivity of Si to Si_3N_4 is larger than 10^4, indicating that the silicon nitride formed by LPCVD is an ideal etching stop layer against poly etchant.

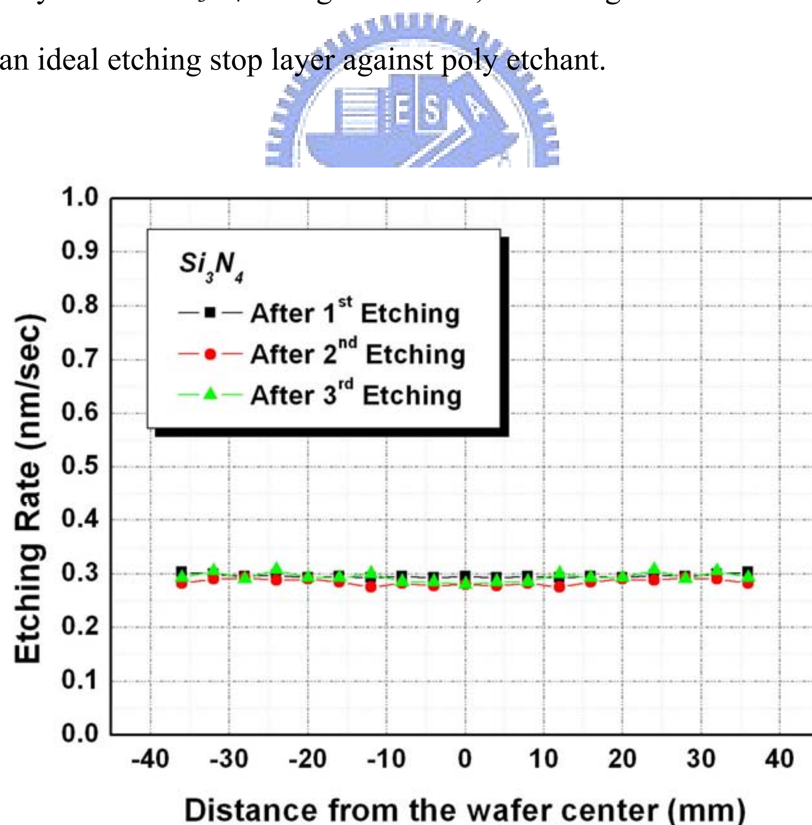


Figure 3-15 The spin-etching uniformity of the silicon nitride film obtained by poly etchant

The etching characteristics of poly etchant for SiO_2 were also investigated. As shown in

Fig. 3-16, the etching rate increases with the flow rate, and gradually saturates at a flow rate above 200 ml/min. Since the relative concentration of hydrofluoric acid was low in our poly etchant and the hydrofluoric acid was consumed very quickly during etching, the etching mechanism is diffusion-controlled and this mechanism depends on the chemical refresh rate. Additionally, the rotation speed negligibly influences to etching rate, except at 1000 rpm. It is notable that the etching rate greatly increases at the lowest flow rate (100 ml/min) and rotation speed. We presumed that the temperature at the surface had arisen, resulting in the increment of surface reaction rates. The etching selectivity of Si to SiO_2 is larger than 150. Although this value is inferior to that of silicon nitride, a thick SiO_2 stop layer with lower stress than Si_3N_4 can be formed through wet oxidation and patterned easily with HF. Consequently, we chose SiO_2 rather than Si_3N_4 as an etching stop layer in DTBE process.

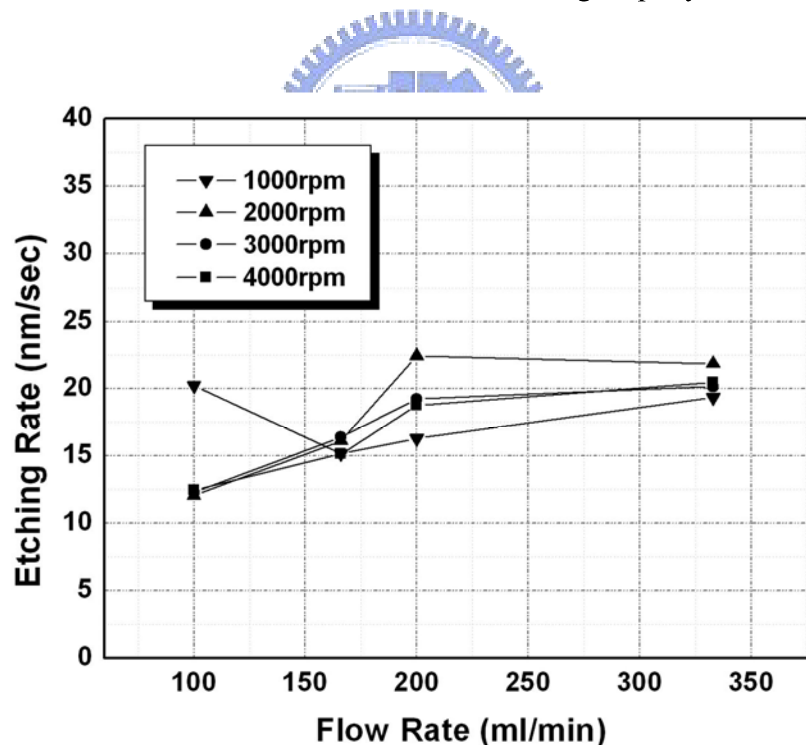
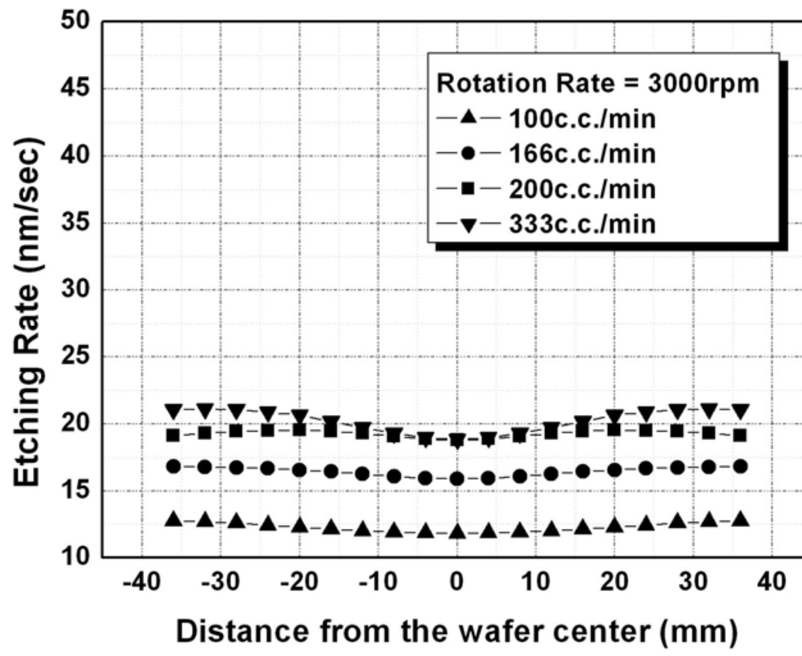


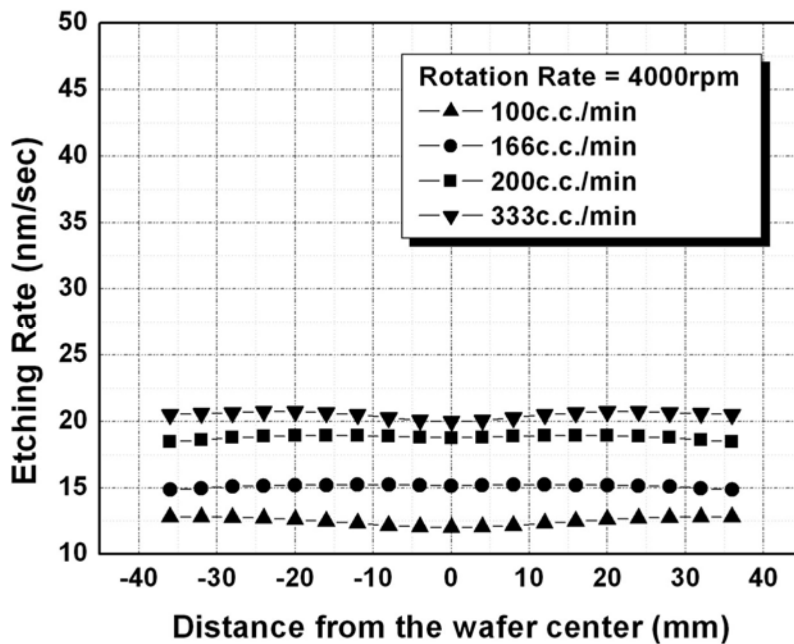
Figure 3-16 The spin-etching rate of silicon dioxide versus chemical flow rates under different spin speed

Figures 3-17(a) and 3-17(b) compare the etching uniformity for SiO_2 with different rotation speeds. From Fig. 3-17(a), we can observe a U-shaped curve of etching uniformity,

but the etching uniformity can be improved by increasing the rotation speed, as indicated in Fig. 3-17(b). A similar phenomenon can also be found during backside Si etching, which will be discussed in the next section.



(a)



(b)

Figure 3-17 The spin-etching uniformity of silicon dioxide obtained at a spin speed of (a) 3000 rpm and (b) 4000 rpm

3.5 Manufacturing TFTs on Flexible Substrate by Modified DTBE with Spin-Etching Technology

In this section, optimal spin etching recipe acquired from the previous section would be utilized to remove the backside Si during DTBE. The electrical characteristics of TFTs after being transferred to flexible ARTON^{TM} films were closely examined, including a bending test that explores the effect under a deliberately applied extrinsic stress.

3.5.1 Fabrication of Thin-Film Devices

In the DTBE process, both poly-Si resistors and thin-film transistors were fabricated on the 4" wafers. First, a 1.5-μm thermal oxide layer was grown on a Si substrate as an etching-stop layer against poly etchant. Then, a 1000 Å amorphous Si layer was deposited by LPCVD at 550°C and patterned to form an active region. A TEOS-SiO_2 layer by PECVD with a thickness of 1000 Å and a poly-Si layer by LPCVD at 620°C with a thickness of 250-nm were then deposited as gate insulator and gate electrodes, respectively. Self-aligned phosphorous implantation at a dosage of 5×10^{15} cm^{-2} with an energy of 60 keV was carried out to generate the source/drain areas.

After the passivation oxide was deposited by PECVD and the contact holes were opened, a 5-nm Ni layer was evaporated onto the contact windows and then the samples were annealed at 550°C in a furnace for 48 hrs to recrystallize the channel region. Next, in order to further increase the grain size and active the dopants simultaneously, the samples were annealed in an N_2 ambient at 900℃ for 1 hr, resulting in the so-called "secondary crystallization" effect [3.14]. Afterward the samples underwent a standard backend process to form the source/drain and gate metallization. Finally, a passivation process using NH_3 plasma was performed for one hour [3.15]. The cross-sectional view of the finished TFT was shown in Fig. 3-18(a). Before the thin-film devices were transferred to the plastic substrate, the

electrical characteristics of the TFTs and poly-resistors were measured using Agilent 4156 semiconductor-parameter analyzer. Except poly-Si TFTs, we also prepared poly-Si resistors and test patterns composed by Al strips for DTBE, as described in *Section 3.2.1*.

The detailed process flow was listed below:

1. Initial RCA cleaning
2. 1500 nm SiO_2: thermal wet oxidation at 1050^oC
3. 100 nm a-Si: LPCVD, SiH_4 source at 40 sccm, 550^oC
4. Mask #1: Active area definition
5. Dry etching of active area: SAMCO® RIE-200L system with SF_6 and O_2 at 10 Pa
6. RCA cleaning
7. 100 nm gate oxide: PECVD TEOS-SiO_2, TEOS 7 sccm, O_2 200 sccm, 250 W
8. 250 nm poly-Si gate: LPCVD, SiH_4 source at 40 sccm, 620^oC
9. Mask #2: Gate electrode definition
10. Dry etching of gate electrode: SAMCO® RIE-200L system with SF_6 and O_2 at 10 Pa
11. RCA cleaning
12. Ion implantation: P^{31}, 60 keV, 5×10^{15} cm^{-2}
13. RCA cleaning
14. 500 nm passivation layer: PECVD TEOS SiO_2
15. Mask #3: Contact hole definition
16. Wet chemical etching for contact hole formation: buffered oxide etcher (NH_4F : HF = 6 : 1)
17. 5 nm Ni: Duel E-Gun evaporation system, 0.5 Å/sec at room temperature, base pressure below 2×10^{-6} torr
18. P.R. lift-off: ACE with ultra-sonic vibrations
19. Metal-induced lateral crystallization and dopants activation: furnace annealing, 48 hr, 550^oC in N_2 atmosphere

20. Residual Ni removal: hot SPM solution at 150°C for 20 min

21. Furnace annealing for *secondary recrystallization*, 900°C, 1 hr

22. Native oxide removal: diluted HF, 20 sec

23. 500 nm Al: thermal coater, base pressure below 4×10^{-6} torr

24. Mask #4: metallization

25. Wet chemical etching for Al etching: H_3PO_4, HNO_3, CH_3COOH, H_2O mixture

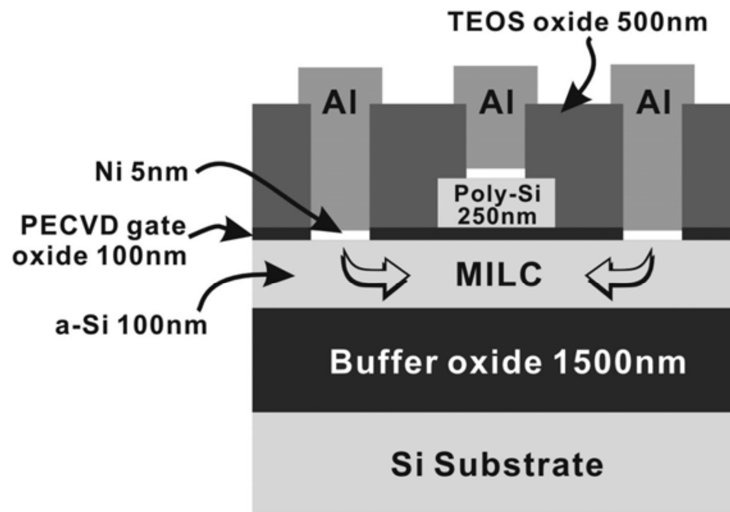
26. Al sintering at 400°C, 30 min in N_2 atmosphere

27. Defect passivation: PECVD, NH_3 70 sccm, 400 mtorr, 20 W, 350°C

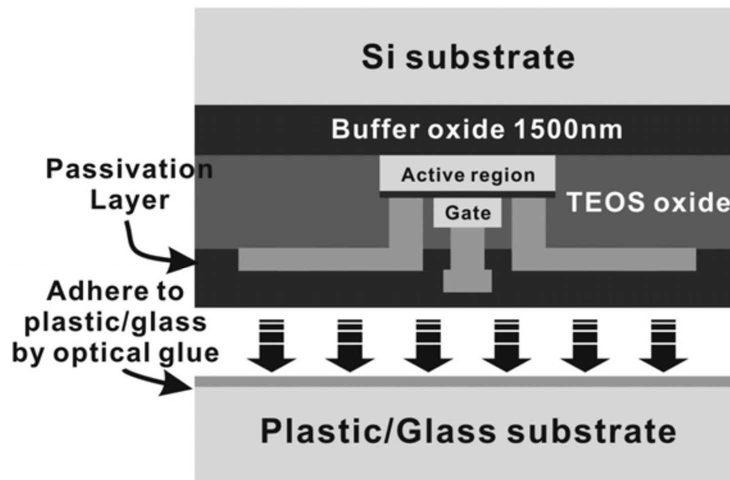
3.5.2 Bonding Process and Backside Si Etching by Spin Etching

After the device characteristics were measured, a 3000 Å TEOS-oxide was deposited on the surface to protect the TFTs from damage by the organic adhesive. Next, as shown in Fig. 3-18(b), the wafer (with devices on it) was bonded to a flexible ARTON^{TM} plastic substrate with a thickness of 110 μm by the optical adhesive and then cured at 80°C for three hours on a hot plate. Afterward, spin-etching process with Si etchant was applied to remove the backside Si. As the thickness of the backside Si was reduced, the flexible plastic substrate tended to deform because it had a low Young's modulus. Accordingly, a supporting glass substrate had to be attached below the plastic substrate to prevent the samples from cracking during the etching process of backside silicon.

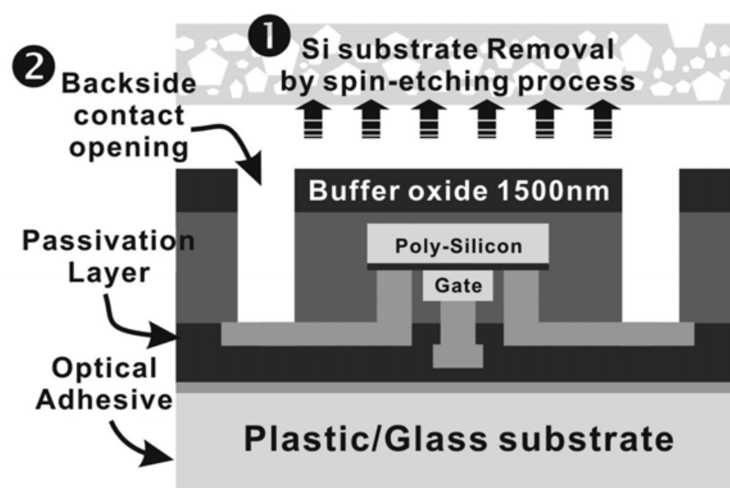
The spin etching step automatically stopped because the Si etchant has a high etching selectivity of 150 to the etching-stop layer, SiO_2. Finally, a photo-lithography process was performed to open the contact pads, as indicated in Fig. 3-18(c). Again the electrical characteristics of TFTs or poly resistors were measured to examine the influence of DTBE.



(a)



(b)



(c)

Figure 3-18 The process flow of device transfer by backside etching technique

3.5.3 Observation after DTBE with Spin Etching Technique

Figure 3-19 shows a photograph of Al test patterns after they were transferred to another plastic substrate by DTBE technique at a spin speed of 4000 rpm and a flow rate of 167 ml/min. The test patterns were originally fabricated on a 4-inch (10 cm in diameter) wafer. During spin-etching, the etching rates near the wafer edge and that at the wafer center were higher than that in other areas, so the patterns that had been in these areas were destroyed by poly etchant even when a protecting oxide stop layer was present. Finally, the transferred devices formed a ring-shaped pattern with a diameter of 5 cm. To solve this problem of non-uniformity, the nozzle structure should be modified to spray the etchant more evenly to make the etching rates equal all over the wafer. Efforts to transfer larger samples using the DTBE technique are under way. In this work, we transferred TFTs or poly resistors from a 4 cm $\times$ 4 cm chip of a Si wafer for a better yield of experiments.

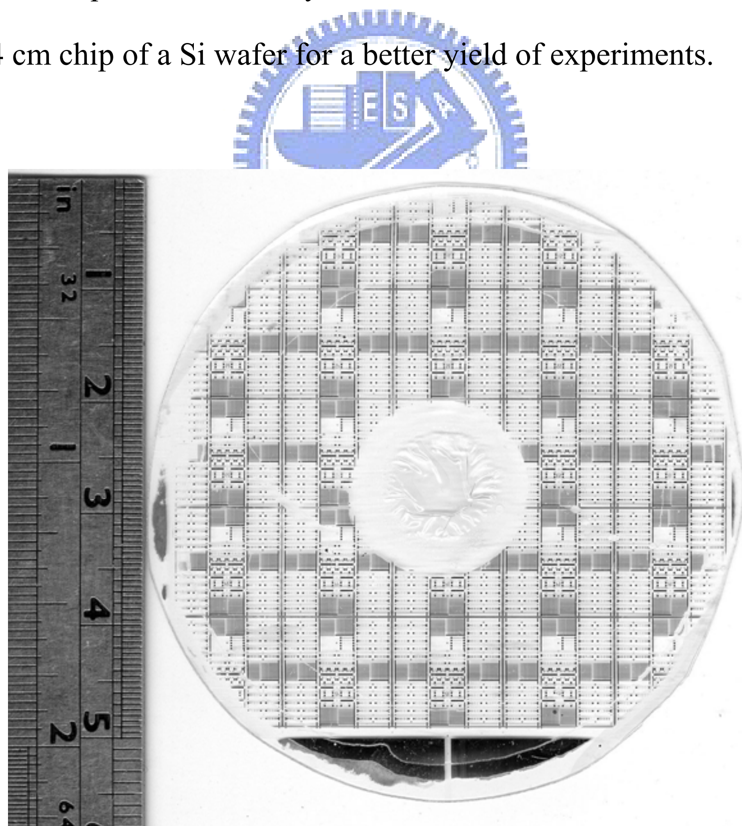
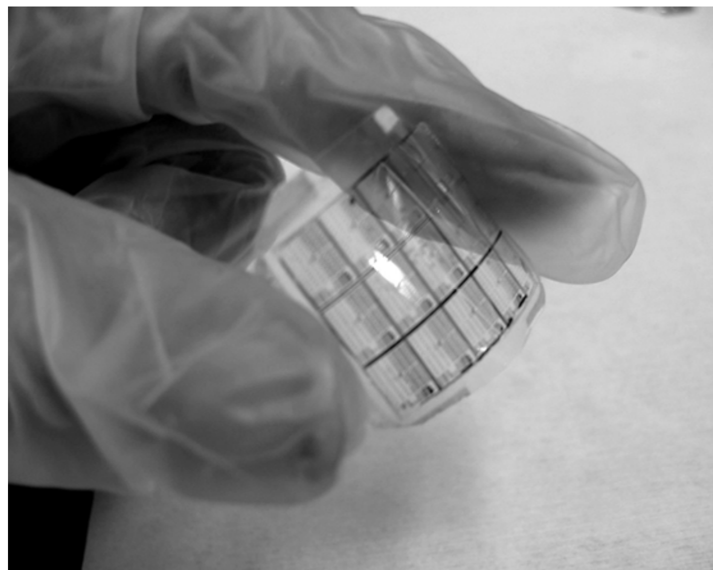
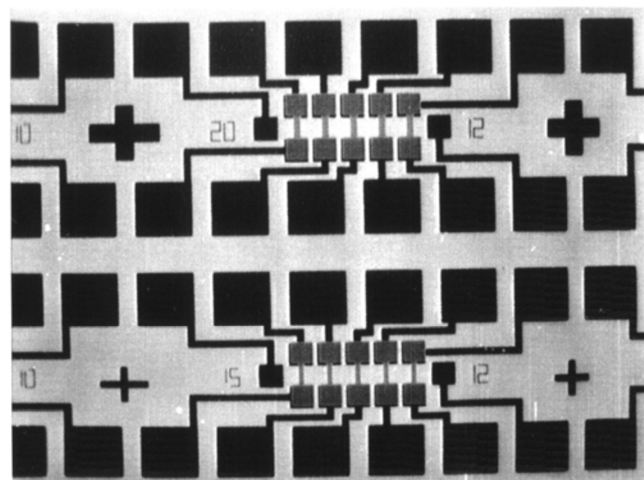


Figure 3-19 A ring-shaped pattern with a diameter of 5 cm formed by DTBE

Figure 3-20(a) presents a flexible ARTON^{TM} substrate on which the thin-film devices had been transferred successfully. The finished die size was 3 cm × 3 cm. The optical microscope image of these devices observed with back light source is shown in Fig. 3-20(b). The dark regions represent aluminum pads, poly-Si gates and S/D electrodes, which are all opaque, while the white area is the transparent plastic substrate, adhesive and SiO_2. The backside Si had been thoroughly removed during spin-etching process and no physical damage was observed.



(a)



(b)

Figure 3-20 (a) Photograph of several TFT arrays transferred to a flexible plastic substrate, and (b) photograph of optical microscope observed with back light source

3.5.4 Electrical Characteristics of Thin-Film Devices after DTBE

Figure 3-21 illustrates the I_D-V_{GS} and field-effect mobility curves of a TFT before and after DTBE. Notably, the DTBE process does not degrade the electrical characteristics of TFTs, such as threshold voltage, mobility, ON/OFF current ratio and subthreshold swing. The field-effect mobility is 43 cm^2/Vs, as determined by the following equation:

$$\mu_{FE} = \frac{L}{C_{ox} \cdot W \cdot 0.1} \times g_m \tag{3.11}$$

where L is the channel length, W is the channel width, C_{ox} is the gate oxide capacitance and g_m is transconductance. The ON/OFF current ratio is larger than 10^6 when the threshold voltage is around 10 V. The variation of electrical properties was not observed, especially the anomalous improvement of field-effect mobility and subthreshold swing found in *Section 2.5.3*. Here, the samples were all passivated by NH_3 plasma and the trap states in the grain boundary were not affected when the capping oxide layer was deposited.

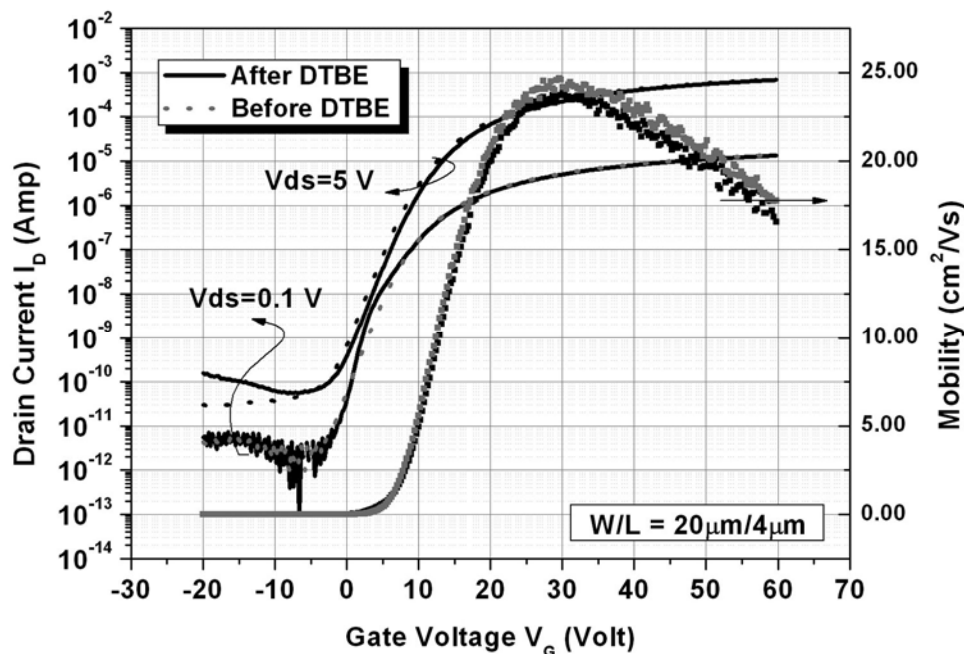


Figure 3-21 I_D - V_G curves and mobility curves of TFTs before and after DTBE process

The electrical characteristics of devices on a bending substrate in a flexible display should not be degraded. Statistically, Fig. 3-22 summarized several key electrical properties of TFTs with different gate length (while gate width = 20 μm) before and after transfer. Each data point was averaged by at least three devices and then normalized to the value of the gate length equal to 8 μm. For example,

$$\text{Normalized mobility:} \quad \mu_{W/L=20/10}^{norm} = \frac{\mu_{W/L=20/10}}{\mu_{W/L=20/8}} \times 100\% \qquad (3.12)$$

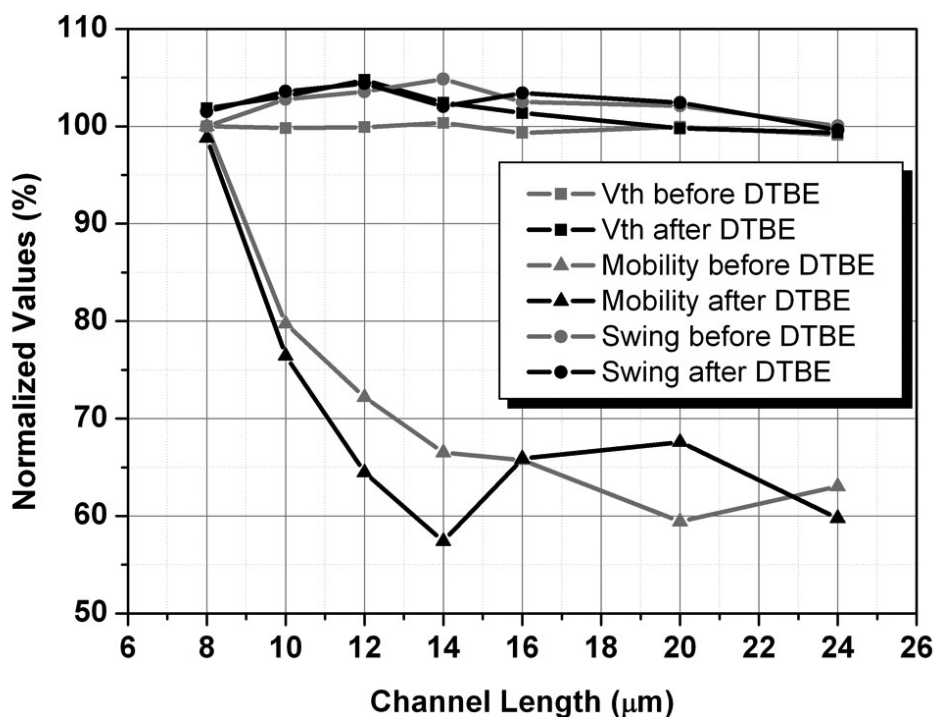


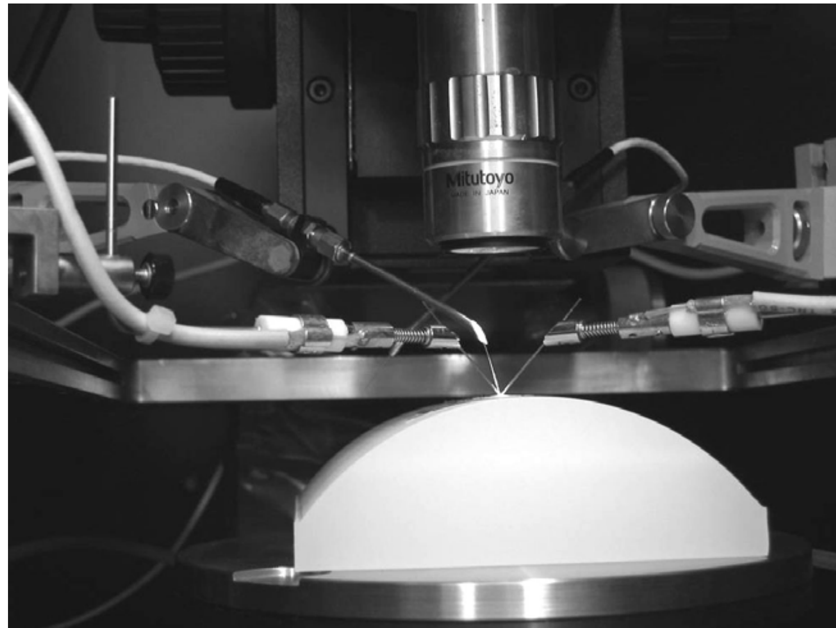
Figure 3-22 Normalized electrical characteristics of TFTs after DTBE process versus channel length

It can be found that both the threshold voltage and subthreshold swing exhibit no dependence on the channel length while the field-effect mobility decreases with increasing the gate length, because the efficiency of Ni-induced lateral recrystallization initiated at the source/drain contacts becomes poorer for a longer distance of silicide diffusion. The TFTs with short gate length thus occupy fewer defective grain boundaries and contribute to high

field-effect mobility. Besides, for DTBE technique, the devices on a wafer underwent several bonding (annealing of the optical adhesive), etching and photo-lithography processes; accordingly, the electrical characteristics of TFTs would be influenced slightly by heat, organic contaminants or moisture generated in these steps, resulting in a larger deviation of electrical characteristics than those before the transfer processes.

In order to examine the influence of mechanical stress on the device performance, several testing bases with various radii of curvature were made; the poly resistors or TFTs after transfer were fixed to the testing base and the electrical characteristics were measured, as shown in Fig. 3-23. Figure 3-24 plots the confidence interval (CI) of poly resistance in different bending cases. The average resistance dose not change after DTBE even at the smallest bending curvature of 2 cm, but the distribution of resistance is wider than those before transfer. Additionally, Fig. 3-25 illustrates the electrical properties of TFTs with W/L = 20 μm/8 μm under various radii of bending curvature, where parallel bending means that the direction of strain is parallel to the current path. And the devices under bending tests all suffer *compressive* stress since the TFTs after DTBE were upside-down attached to the testing base. The experimental data are normalized to the value before DTBE. According to the research of S. Wagner et al., the mobility of amorphous Si TFTs would slightly decrease with increasing the compressive strain because of possible variation of optical band gap of a-Si:H under compression [3.16]. Nevertheless, no significant correlation between the electrical properties of TFTs and different bending curvatures can be found in Fig. 3-25. We speculated that the elastic optical adhesive as well as thick etching stop/capping oxide layers may absorb the extrinsic stress during bending tests, and therefore the thin-film devices sandwiched between these layers suffer lower stress. Actually, when low modulus, small thickness substrate, and encapsulation are used, the thin-film approximation breaks down and the whole structure can be bent to extremely small radii, even being folded like a map [3.17], [3.18].

(a)



(b)

Figure 3-23 (a) The testing base with different radius of curvatures, and (b) the bending measurement with the testing base

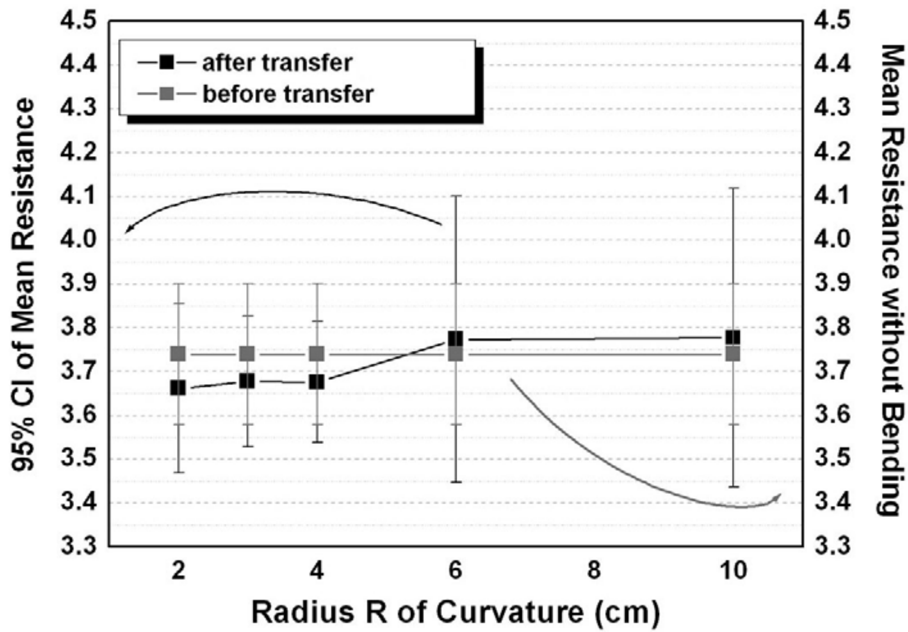


Figure 3-24 Resistance of poly resistors measured under different bending curvatures

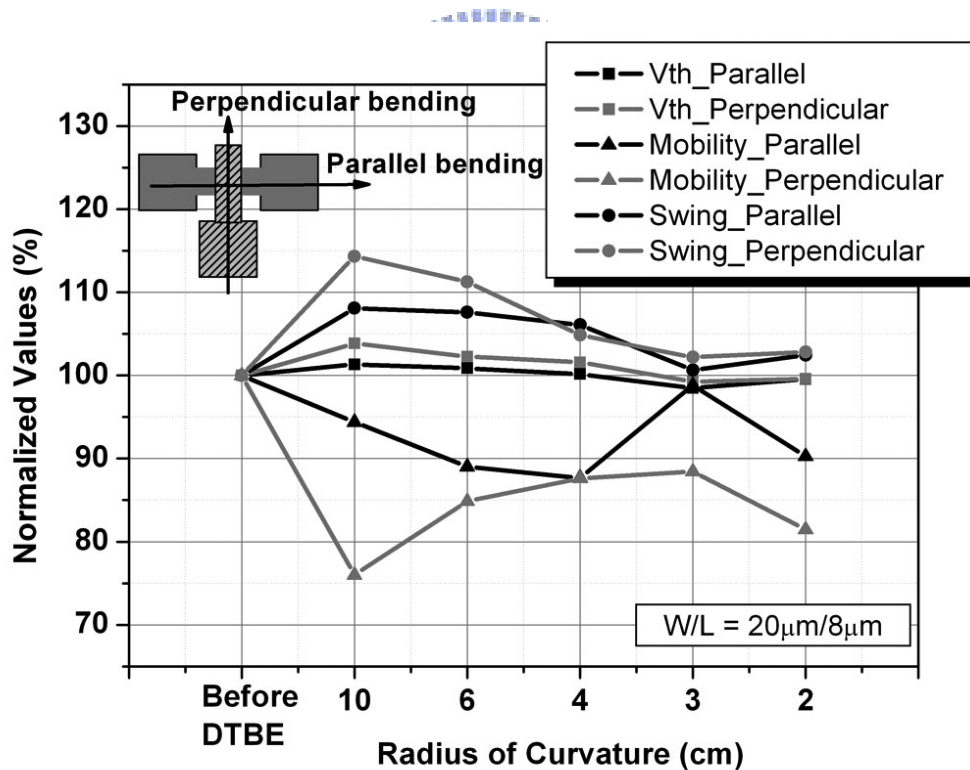


Figure 3-25 Comparison of electrical properties of TFTs before DTBE and that measured at various bending curvatures after DTBE

3.6 Single Crystal Si on Glass/Plastic Substrates by DTBE

There are particular demands for fabricating c-Si on another host substrate; these applications include sensor/actuator system, radio-frequency devices, optical transducers, and three-dimensional integrated circuits, etc [3.19]. Actually, from the mid 80's to 90's a few methods for transferring devices had been studied such as liquid crystal projector, SOI devices, and multi-chip module (MCM) assembly technique [3.20]-[3.23]. More discussion about transfer technique of single crystalline Si can be found in *Section 2.3.3*.

Although high temperature poly-Si TFTs or epitaxial c-Si devices have been fabricated directly on quartz substrate for years, the extremely high cost of quartz (at least ten times higher than a Si wafer with the same size) limits its application and popularity. In contrast, the ability of the modified DTBE with spin etching technique is not limited to the transfer of poly-Si TFTs. Utilizing DTBE technique, both high-performance integrated circuits and MOSFET arrays can be easily fabricated by conventional CMOS processes and then transferred from the Si wafer to the other low-melting-temperature substrates. In this section, we demonstrated a procedure that transfers c-Si from conventional Si wafer (rather than expensive SOI wafer) to plastic substrate by DTBE.

3.6.1 Experimental

Figure 3-26 shows the process flow that transfers a bar of c-Si from a Si wafer to glass/plastic substrates by DTBE. First, the thin dry oxide and silicon nitride layers were grown and patterned as the hard mask for anisotropic wet etching. Next, the samples were immersed into the 21.25 wt.% KOH at 110°C to form Si islands as shown in Fig. 3-26(a). The estimated height of each Si islands was 5 ~ 20 μm, depending on the etching time of KOH. After removing SiO_2 and Si_3N_4 hard masks by hot HF and H_3PO_4, a 1500 nm wet oxide followed by a 500 nm Al layer was deposited and patterned to form the dummy metal

interconnections. It should be noted that the lithography step of Al patterning must utilize thick-film photo resist, e.g. AZ4620, because conventional photo resist cannot be coated smoothly to such large steps (5 ~ 20 μm) of wafer surface. The finished testing structure was shown in Fig. 3-26(b).

The testing structures were capped a passivation SiO_2 layer by PECVD. Thereafter, the wafer was bonded to another plastic or glass substrate with optical adhesive and then the backside Si was removed by spin-etching technique. Finally, as shown in Fig. 3-27(c), crystal-Si bars can be successfully transferred.

3.6.2 Results and Discussion

Figure 3-27 shows the OM images of Si islands formed by anisotropic KOH etching and Al interconnections before DTBE. Since the etching rate of KOH is anisotropic depending on the orientation of Si wafer, the distortion of Si islands becomes more serious with increasing the etching time. These distortions change the actual width and length of MOSFETs and should be taken into consideration during photo mask design. However, the distortion of Si islands can be discarded in this experimental structure.

Figure 3-28 shows the OM images of Si islands being transferred to glass/plastic substrate successfully by DTBE. Since the passivation layer and the etching stop layer are all transparent, which are dark in Fig. 3-28 by a top light source, the etching stop point during DTBE can be easily determined. For the transferred testing patterns, no physical damage was found after DTBE.

In conclusion, although we just demonstrated a dummy structure here, more complicated circuits for transfer process can be fabricated in a similar way. Specifically, the MOSFETs can first be manufactured by standard CMOS process followed by a special designed photolithography step to define the Si island region. After deposition SiO_2 or Si_3N_4 as the etching stop layer, the metallization, bonding and DTBE are then carried out. Here,

thermal budget introduced during high-temperature deposition step of etching stop layer may contribute to the other unexpected issues and should be always kept in mind during designing overall process flows.

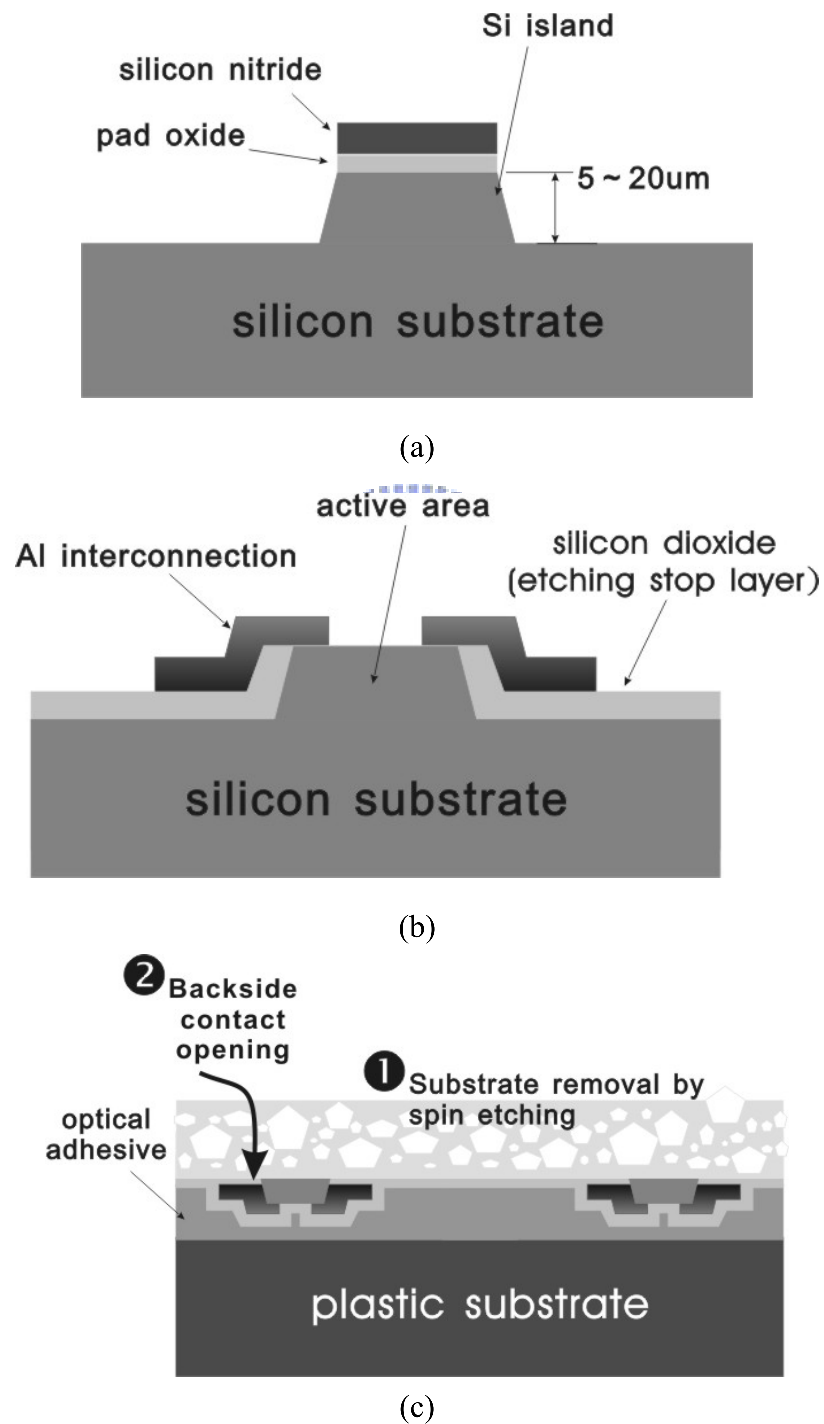


Figure 3-26 Schematic diagram of a process flow for transferring c-Si from a Si wafer to the glass/plastic substrates

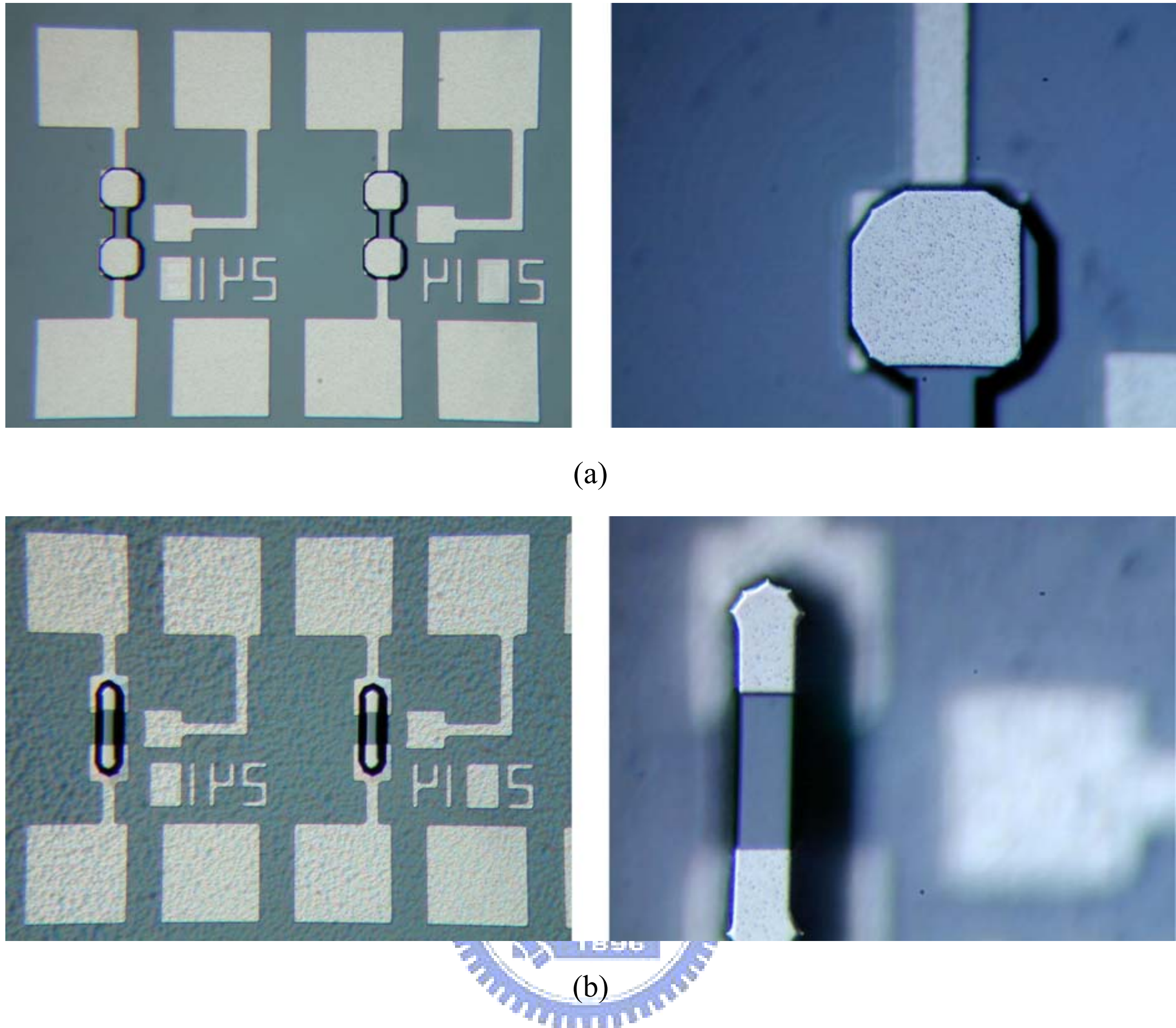


Figure 3-27 OM images of Si islands formed by anisotropic KOH etching and Al interconnections before DTBE. Each step height is (a) 5 μm, and (b) 20 μm

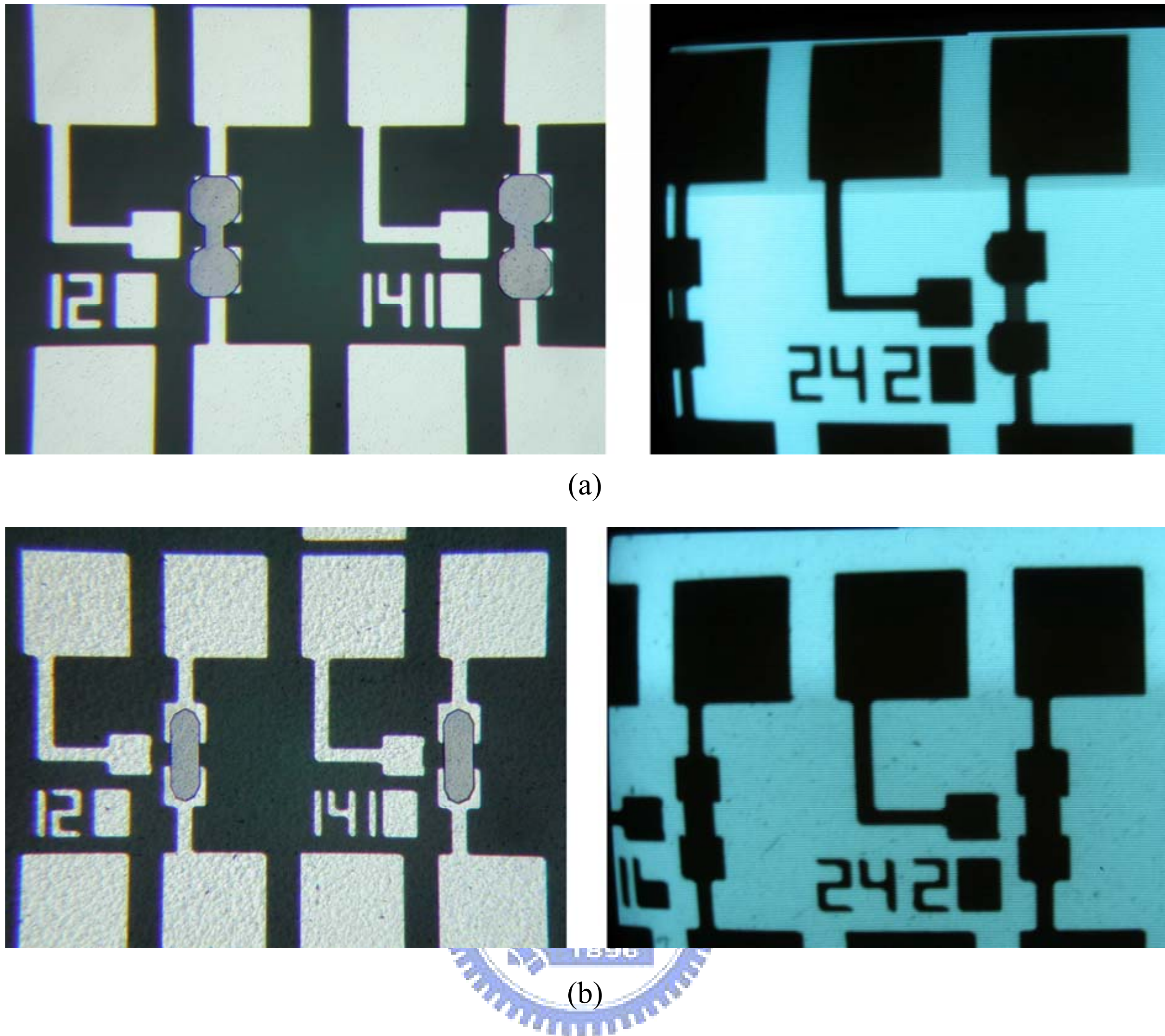


Figure 3-28 OM images of Si islands being transferred to glass/plastic substrate successfully by DTBE. Each step height is (a) 5 μm, and (b) 20 μm

3.7 Summary

In this chapter, we surveyed different kinds of silicon etching chemicals and techniques to find out an optimal method for transfer thin-film devices to flexible substrate without utilizing CMP. The mechanism of spin etching was proposed, and the etching rate, selectivity as well as spin etching conditions were explored. Large samples with diameter of 5 cm had been transferred to flexible ARTON^{TM} film successfully.

Fabricating high-performance thin-film transistors on plastics is extremely challenging.

This work proposed an indirect process for transferring thin-film devices on a silicon wafer to another polymeric backplane. Spin-etching process was applied to overcome the issues about heat and mechanical stress resulted from CMP or conventional wet chemical etching. Moreover, the electrical characteristics of poly-Si resistors or TFTs are not changed after transfer process or the bending measurement, confirming that the device transfer technique with backside spin-etching process a practical means of fabricating thin-film devices on a flexible plastic substrate or fragile glass substrate.

The DTBE technique have been developed and well discussed in *Chap. 2* and *Chap. 3*. For comparison, we listed several key issues about LTPS TFTs and summarized the corresponding solutions with various technologies in Table 3-2.

Table 3-2 Comparison of DTBE technique with the other LTPS poly-Si technology

Issues	**Direct method**	**SUFTLA**	**Sacrificial layer**	**c-Si from SOI wafer**	**DTBE**
Discussion	Section 2.2	Section 2.3.1	Section 2.3.2	Section 2.3.3	Chap.2, 3
Starting material	Glass/plastic substrate	Glass/quartz	Glass	SOI wafer	Conventional Si wafer
Process temperature	<600°C/<200 $^{\circ}$C	<600°C/<600°C*[1]	<600°C	~1100°C	~1100°C
Special Technology	Excimer laser	Excimer laser	Excimer laser	Ion cutting	CMP, spin etcher
Host substrate	Glass/plastic	Unlimited	Unlimited	Glass	Unlimited
Largest size (potential)	60 × 72 cm^2 (G3.5)	Small (ablation uniformity?)	60 × 72 cm^2 (G3.5)	12”	12”
μ_{FE} (cm^2/Vs)	100 ~ 400*[2]	> 100	> 100	> 400	50 ~ 300*[3] or > 400*[4]
Critical dimension	~ 1-2 μm	~ 1-2 μm	~ 1-2 μm	Submicron	Submicron
Compatibility	AMLCD	AMLCD	AMLCD	CMOS	CMOS
Complexity	Low/high	Moderate	Low	Moderate	Moderate
Yield	Moderate to high	Low	Moderate to high	Moderate	Moderate
Mass production cost	Low	Moderate	Low	Extremely high	Moderate
Applications	AMLCD and AMOLED	AMLCD and AMOLED	AMLCD and AMOLED	Niche market	AMOLED, projector, biochip and other niche market

*1: limited by the exfoliation layer even using quartz as a starting material

*2: requiring complicated super-lateral growth mechanism or CW laser

*3: secondary recrystallization after MILC, also depending on the critical dimension

*4: transfer of single crystalline Si if necessary