

Chapter 4

Poly-Si TFTs with Elevated Channel and Gate Overlapped Structure by Excimer-Laser Annealing

Polycrystalline silicon thin-film transistors have found its wide application for active matrix liquid crystal display as switching devices and peripheral circuits [4.1], [4.2]. Besides, poly-Si TFTs utilizing excimer laser crystallization exhibit considerable improvement of the electron mobility over $100 \text{ cm}^2/\text{Vs}$, becoming much more attractive to current-driven organic light-emitting devices and system-on-panel integration [4.3]. However, conventional TFTs are known to present several undesired effects, including large OFF-state leakage current, anomalous drain current increase at high source-drain voltages, the so-called kink effect, and electrical instabilities after long term operation [4.4]. These effects, mostly induced by hot carrier or avalanche multiplication in grain boundary at high electric field, would increase the power dissipation while attenuate the current gain, the common mode rejection ratio and reliability characteristics [4.5].

In this chapter, we will discuss the origin about these undesired effects of poly-Si TFTs and the associated special structure of TFTs in addressing these issues. Next, we proposed a novel elevated-channel thin-film transistor (ECTFT) structure, where the thin channel region is connected to the thicker source/drain area. For ECTFT structure, the selective liquid-phase deposition (S-LPD) technique becomes a key process to planarize the trench area at room temperature without utilizing CMP or additional photo-masks, thus fully compatible for LTPS process on glass substrate. Furthermore, by combining the gate overlapped light-doped drain and elevated channel structures, we examined the electrical properties and reliability characteristics of TFTs and found both device performance and kink phenomenon can be effectively improved.

4.1 Undesired Effects of Conventional Poly-Si TFTs

4.1.1 OFF-State Leakage Current

In AMLCD applications, leakage current represents a limiting factor affecting the time that video information can remain on a pixel before refreshing. To prevent a pixel from losing charge over a frame cycle, the poly-Si TFTs must have very low leakage current (<1 pA) at typical source to drain bias of approximately 10 volts. Poly-Si TFT suffers from more serious leakage current problem than a-Si:H TFT does since the nature of larger channel resistance of a-Si:H at its off-state.

Several effects account for the off-state leakage current, which includes thermionic enhanced emission by the Poole-Frenkel effect (PF), thermally assisted tunneling through the barrier (trap assisted tunneling, TAT), and band-to-band tunneling (BBT) [4.6]. In the case of *low electric field*, the off-current turns out to be almost independent of the gate voltage and it is limited by the conductance of the poly-Si channel between source and drain. In these conditions, the off-current arises from *thermal generation* via the gap states, where the contribution of PF and TAT to the off-current is dominant, so that the leakage current can be eliminated by reducing the amount of traps (density of states, DOS), improving the quality of the active region and decreasing the thickness of the active layer (i.e. reducing the thermal generation volume) [4.7].

At *large electric fields*, however, the off-current becomes almost independent of the material quality. In these conditions, all the generation effects listed above (namely PF, TAT, and BBT) contribute to the off-current [4.6]. Specifically, considering the conduction band energy along the middle of the poly-Si channel from source to drain for two drain bias as shown in Figure 4-1(a) [4.8], the barrier height to electron injection near the source decreases with increasing drain bias; at high V_{DS} , the holes also tunnel out of traps near the drain side and flow along the silicon-oxide interface to the source, lowering the barrier near the source.

Furthermore, as shown in the band diagram of Fig. 4-1(b) and (c) [4.44], both the lateral electric field along the channel and the vertical electric field perpendicular to the gate oxide interface contribute to the trap-assisted tunneling current. As a result, the high field tunneling mechanism, especially BBT, becomes dominant, and minority carriers are generated near to the drain, causing device leakage to depend on the position of the traps within the TFT. A substantial reduction of the leakage current can only be achieved by reducing the electric field within the semiconductor.

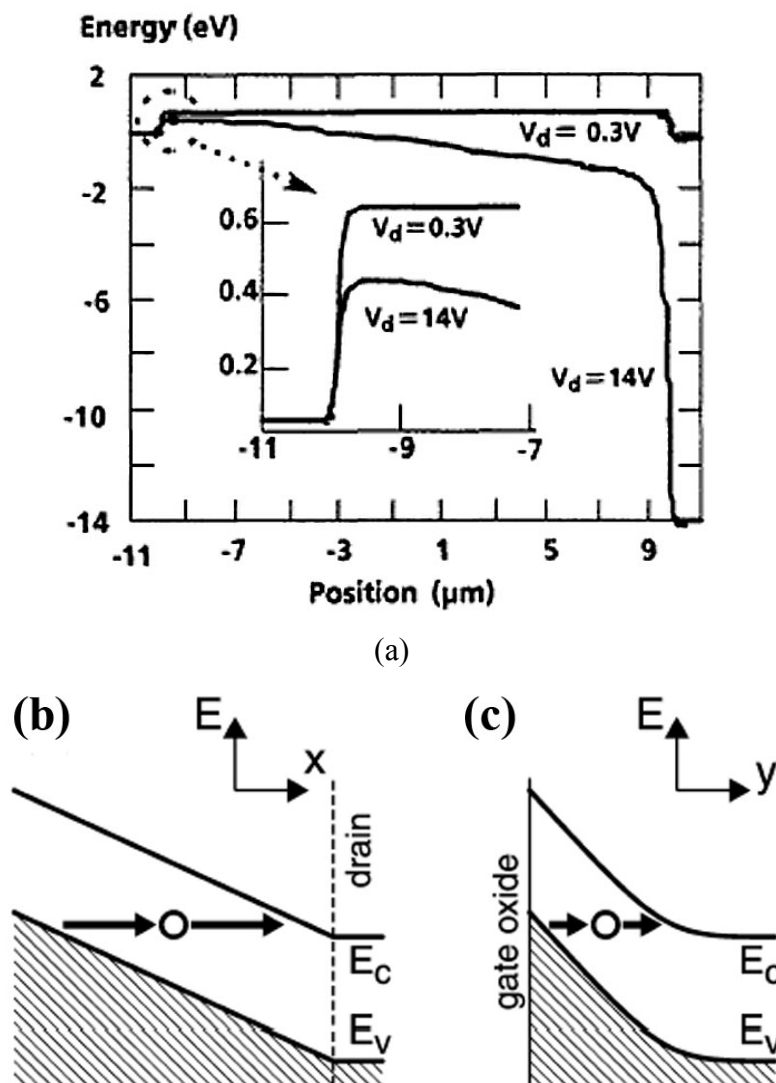


Figure 4-1 (a) Simulated conduction band energy for a 20 μm NMOS poly-Si TFT for $V_D = 0.3\text{ V}$ and $V_D = 14\text{ V}$, (b) band profile along the channel in the vicinity of the drain, and (c) band profile perpendicular to the channel starting from the gate interface

4.1.2 Floating Body Effects

The output characteristics exhibit in fact an anomalous current increase in the saturation regime, the floating body effect is also called “kink” effect due to an analogy with silicon-on-insulator devices [4.9], [4.10]. Basically, because of the impact ionization occurring in the high electric field region at the drain end of the channel, holes are injected into the floating body (base) forcing further electron injection from the source (emitter) and then collected by the drain (collector). This added drain current augments impact ionization which, in turn, forward biases the floating body harder, thereby causing a regenerative action which leads to a premature breakdown. Kink effect results in an increase of the output conductance, and is responsible for degradation of the device characteristics both in digital and in analog circuit applications such as reduced noise margins and available voltage gain, etc [4.11].



4.1.3 Hot Carriers Induced Degradation

The hot carrier effect which originates from the high electric field near the drain junction have been widely investigated in MOSFETs, and it is also an important reliability issue for poly-Si TFTs. For n-channel TFTs, conduction carriers can obtain energy from the high electric field at the drain side and become “hot”; these high-energy electrons can easily break the weak Si-Si or Si-H bonds in the active region, contributing to serious degradation of TFT’s electrical properties.

The g_m degradation in polysilicon TFTs has been attributed to the stress-induced creation of acceptor-like active layer bulk traps and to the increase of interface carrier scattering due to the stress-induced increase of the oxide-trapped charge and the interface trap density, as is mainly the case with MOSFETs [4.12], [4.14]. However, the V_{th} shift is affected not only by the interface degradation but also by charge trapping in the oxide, which is much more evident for the higher vertical field conditions. It is also reported that the

carrier-induced metastable defect creation within the channel (ambipolar states near mid gap) results in a threshold voltage shift of TFTs without significant change in the field-effect mobility [4.13].

On the other hand, the subthreshold swing (SS) depends mainly on intragrain traps distributed uniformly inside the polysilicon film and also on the deep interface states [4.15]. Table 4-1 summarizes the variation of electronic parameters and the corresponding possible degradation mechanics.

Table 4-1 Variation of experimental electronic parameters and the corresponding possible degradation mechanics [4.16], [4.17], [4.45]

Electrical Parameters	Possible degradation mechanisms
After stressing	
$\Delta g_{m,max}$	<ul style="list-style-type: none"> ◆ interface state (deep states from dangling bond) generation ◆ state generation in the grain boundaries (tail states)
ΔV_{th}	<ul style="list-style-type: none"> ▪ charge injected into the gate oxide ▪ interface state generation (deep states) ▪ state generation in the grain boundaries (mid gap states)
ΔS_{wing}	<ul style="list-style-type: none"> ◆ intra-grain defect density generation (bulk states) ◆ interface state generation (deep states)

According to the above table, Δg_m appears to be a reliable parameter in studies of the hot carrier induced degradation since the change of transconductance depends mainly on the generation of interface state.

4.2 Device Architecture for High-Performance Poly-Si TFTs

4.2.1 Active Layer Thinning

Poly-Si active layer generally contains lots of trap states in the grain or in the grain

boundary even if the active region is well recrystallized by excimer laser annealing. These trap states contribute to the OFF-state leakage current and deteriorate the other electrical performance of poly-Si TFTs. One of methods for solving this problem is to reduce the thickness of active layer [4.20]. It has been reported that a poly-Si device with 2-nm-thick channel realizes a quantum-confinement effect and produces a low leakage current value of only 10^{-19} A at room temperature [4.18]. Besides, thinning the active layer is also beneficial for obtaining a higher current drive [4.19], [4.21] while provide a lower overall source to channel barrier that alleviates the kink effect and better immunity to short channel effect for the fully depleted nature of thin body device.

However, simply thinning the active area of TFTs would cause many side effects such as poor drain/source contact, large series resistance, and low drain breakdown. Therefore, one kind of TFT structure with thin channel and thick source/drain region is developed to overcome these side effects while maintaining the benefits of thinning the active area [4.22], [4.23]; this structure is called elevated channel or elevated S/D TFT. The ECTFT concept we proposed in this section also belongs to this architecture. Additionally, the $R_{S/D}$ can also be suppressed by the selective tungsten CVD or silicidation process [4.46], [4.47]. Nevertheless, the conventional elevated channel architecture utilizes CMP to planarize the thin channel region, while the CVD or the silicidation process must be implemented at $300 \sim 500^{\circ}\text{C}$, so these methods are probably not adequate for the fragile glass substrate or plastic substrate with low-melting temperature in AMLCD application.

4.2.2 Reduction of the Drain-Side Electric Field

According to the discussion in *Section 4.1*, the most effective approach to eliminate those undesired effects of poly-Si TFTs is reducing the electric field at the drain side at either ON or OFF state of TFTs. It has been proved that the lightly doped drain (LDD) structure can redistribute the peak electric field, alleviating the OFF-state leakage current and hot

carrier damage at the ON-state [4.24]-[4.26]. However, as shown in Fig. 4-2(a), the LDD structure generally incorporates an additional series resistance to the channel region, so that the ON current as well as the carrier mobility of TFTs with LDD would be a little bit lower.

To solve this problem, the gate-overlapped LDD (GOLDD) architecture is proposed [4.27]-[4.30]. As shown in Fig. 4-2(b), the overlapped gate electrode would induce additional carriers in the n^- region without sacrificing the ON current of TFTs. Consequently, for GOLDD TFTs, ON current was almost independent of n^- density, in contrast to a strong dependence observed in the LDD architecture. The dependence shows that the GOLDD type has a wide process window for high performance. Moreover, it is reported that the hot carrier generation occurs far from the interface between gate oxide and poly-Si for GOLDD structure, and the fixed charges or traps in the n^- layer generated by the hot carrier stress can be screened since the gate electrode overlaps the n^- layer [4.31]. As a result, GOLDD TFTs exhibit high reliability during stress measurements.

The other TFT configurations also show the immunity to the hot carrier stress and kink reduction, such as dual gate (Fig. 4-2(c)) [4.32] and single gate with split channel structure (Fig. 4-2(d)) [4.33], [4.34], where the incorporated n^+ region would recombine the excess holes generated by impact ionization and redistribute the electric field in the channel region; additionally, modifying the channel electric field through gate engineering like field-induced drain [4.35], sub-gate coupling [4.36], and double gate configuration (Fig. 4-2(e)) [4.37], etc. all draw a lot of attention recently.

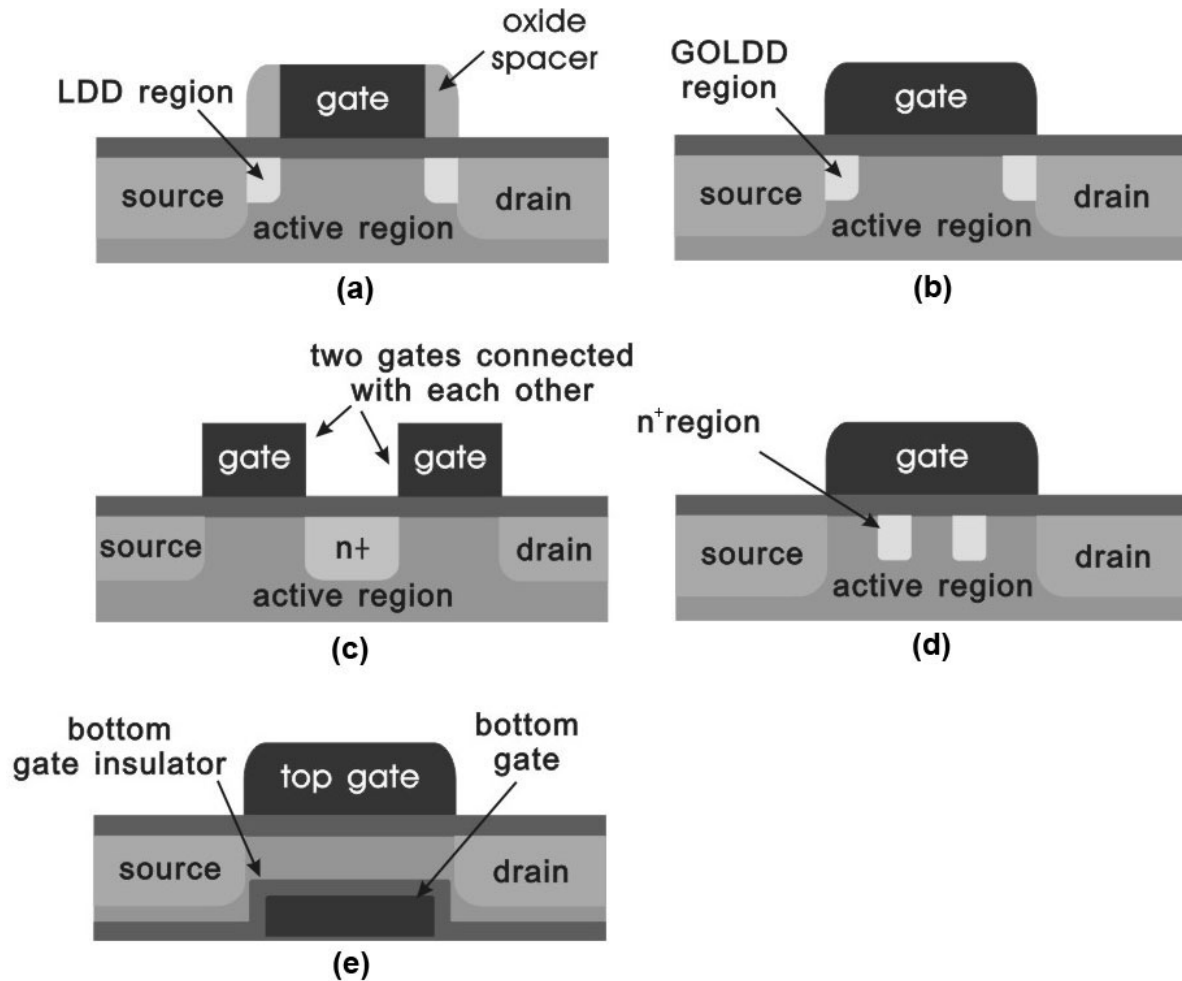


Figure 4-2 Typical structures for alleviating the undesired effects of poly-Si TFTs: (a) LDD, (b) GOLDD, (c) dual gate, (d) split channel, and (e) double gate structure

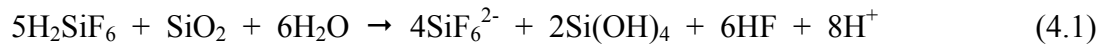
4.3 Experimental: Fabrication of ECTFT with S-LPD and ELA

Process

4.3.1 Selective Liquid-Phase Deposition Technology

The schematic diagram of the apparatus for liquid-phase deposition technology is illustrated in Fig. 4-3. First, 75 g of silica (SiO_2) powder with high purity of 99.999% was mixed with 1200 ml of hydrofluorosilicic acid (H_2SiF_6 , 4 mol/l) and then the solution was stirred in the “saturation tank” at 23°C for 18 ~ 24 hr. The temperature of the LPD solution was controlled precisely by a water chiller. After stirring for tens of hours, the

hydrofluorosilicic acid became saturated, which can be represented by the following equation:



Before starting the deposition process, the pipes, filters, valves, and pumps (driven by compressed dry air, CDA) should be cleaned by diluted HF and D.I. water rinse for several times to ensure the cleanness. This process can be performed automatically through the programmable control of the LPD apparatus. Next, the saturated H_2SiF_6 solution was pumped out of the left saturation tank, filtered through two PTFE filters with pore size of $0.5 \mu\text{m}/0.1 \mu\text{m}$ respectively to remove the undissolved SiO_2 particles, and then flow into the right “deposition tank.” The temperature of the deposition tank was also controlled by the water chiller at 23°C or 25°C .

When the samples were ready for deposition LPD- SiO_2 , we added D.I. water into the saturated H_2SiF_6 solution and thus the equilibrium condition was altered, contributing to a super-saturated state of silicic acid $\text{Si}(\text{OH})_4$. After immersion the samples, the $\text{Si}(\text{OH})_4$ molecules would react with the hydrophilic surface, that is, the surface full of OH bonds, and then the $\text{Si}(\text{OH})_4$ dehydrate into SiO_2 under an acid catalytic polymerization process. For those hydrophobic surfaces such as photo resist or metals (e.g. Ta), the SiO_2 will not deposit on them and an extraordinary selectivity can be obtained as shown in Fig. 4-4. Finally, the two PTFE filters were cleaned again to remove the SiO_2 following the standard cleaning process of LPD apparatus.

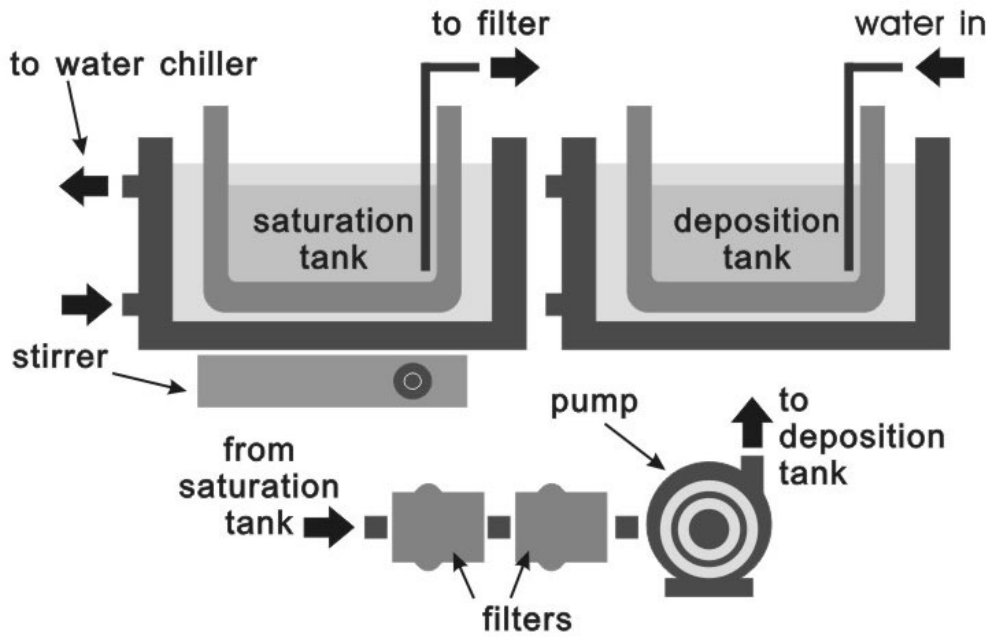


Figure 4-3 The schematic diagram of the apparatus for LPD-SiO₂

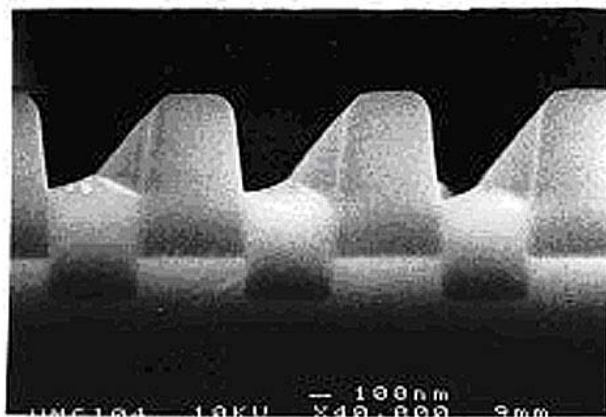


Figure 4-4 SEM photograph for the selective deposition of SiO₂ by S-LPD technology

4.3.2 Device Structure and Fabrication of ECTFT

The key processes for fabricating ECTFT with GOLDD structure are illustrated in Fig. 4-5. At first, a 50-nm amorphous silicon layer was deposited on an oxidized silicon substrate by LPCVD at 550°C. Then the thin channel (trench) region was patterned by photolithography and Si etchant composed of HNO₃, NH₄F and H₂O. Next, without removing photoresist, the samples were soaked into super saturated H₂SiF₆ solution at 23°C; the SLPD-oxide would deposit at the sidewall and the bottom of the trench except the surface of

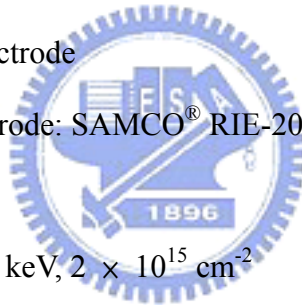
photoresist. Because the wet chemical etching and the deposition of LPD oxide are both isotropic, a planar surface as shown in Fig. 4-5(a) can be established precisely and was checked by surface profiler. After photoresist removal, a phosphorous implantation with a dosage of $1 \times 10^{13} \text{ cm}^{-2}$ at 30 keV was performed to generate lightly doped region.

Next, a 100-nm amorphous-Si layer was deposited by LPCVD followed by the excimer laser (KrF, $\lambda = 248 \text{ nm}$) annealing with energy density of 320 mJ/cm^2 . The energy density of laser annealing had been optimized to stimulate the super lateral growth of active layer, as shown in Fig. 4-5(b). For comparison, control samples with the active layer thickness of 100 nm and 150 nm were also prepared. After the active area was patterned, a 130-nm gate oxide layer by PECVD and 250-nm poly-Si gate electrodes by LPCVD at 620°C were formed. For n-channel transistors, a self-aligned phosphorous implantation with a dosage of $5 \times 10^{15} \text{ cm}^{-2}$ at 60 keV was carried out to generate S/D regions. Figure 4-5(c) schematically depicts the finished ECTFT structure, where d means the gate overlapped length varied from 0 to 3 μm . A passivation oxide was then deposited and the implanted dopants were activated by furnace annealing at 600°C for 24 hours. Thereafter, all samples followed standard back-end processes to form contact holes and Al contact pads. Finally, TFTs were passivated by NH_3 plasma treatment for 1 hour.

Detailed process flow of the proposed ECTFT with GOLDD structure was listed below:

1. Initial RCA cleaning
2. 500 nm SiO_2 : thermal wet oxidation at 1050°C
3. 50 nm a-Si: LPCVD, SiH_4 source at 40 sccm, 550°C , 100 mtorr
4. Mask #1: define the a-Si trench for the thin channel region
5. Wet chemical etching of the a-Si trench: poly etchant (NH_4F , HNO_3 and H_2O mixture) at room temperature
6. 50 nm SiO_2 by S-LPD method: (without removing photoresist) in super-saturated H_2SiF_6 , at 23°C for about 2.5 hr

7. P.R. removal
8. Ion implantation for LDD region: P³¹, 30 keV, $1 \times 10^{13} \text{ cm}^{-2}$
9. RCA cleaning
10. 1000 nm a-Si: LPCVD, SiH₄ source at 40 sccm, 550°C, 100 mtorr
11. Recrystallization of a-Si: 50 shots, 320 mJ/cm², substrate at room temperature, annealed by KrF excimer laser
12. Mask #2: define the active area
13. Dry etching of the active area: SAMCO[®] RIE-200L system with SF₆ at 20 Pa
14. RCA cleaning
15. 130 nm gate oxide: PECVD, TEOS and O₂ source, 350°C, 250 W
16. 250 nm poly-Si gate: LPCVD, SiH₄ source at 40 sccm, 620°C, 120 mtorr
17. Mask #3: define gate electrode
18. Dry etching of gate electrode: SAMCO[®] RIE-200L system with SF₆ at 20 Pa
19. RCA cleaning
20. Ion implantation: P³¹, 60 keV, $2 \times 10^{15} \text{ cm}^{-2}$
21. RCA cleaning
22. 500 nm passivation layer: PECVD TEOS SiO₂
23. Dopant activation: 600°C for 24 hr
24. Mask #4: define contact holes
25. Wet chemical etching for contact hole formation: buffered oxide etcher (NH₄F : HF = 6 : 1)
26. 500 nm Al: thermal coater, base pressure below 4×10^{-6} torr
27. Mask #5: metallization
28. Wet chemical etching for Al etching: H₃PO₄, HNO₃, CH₃COOH, H₂O mixture
29. Al sintering at 400°C, 30 min in N₂ atmosphere
30. NH₃ plasma passivation for 1 hr



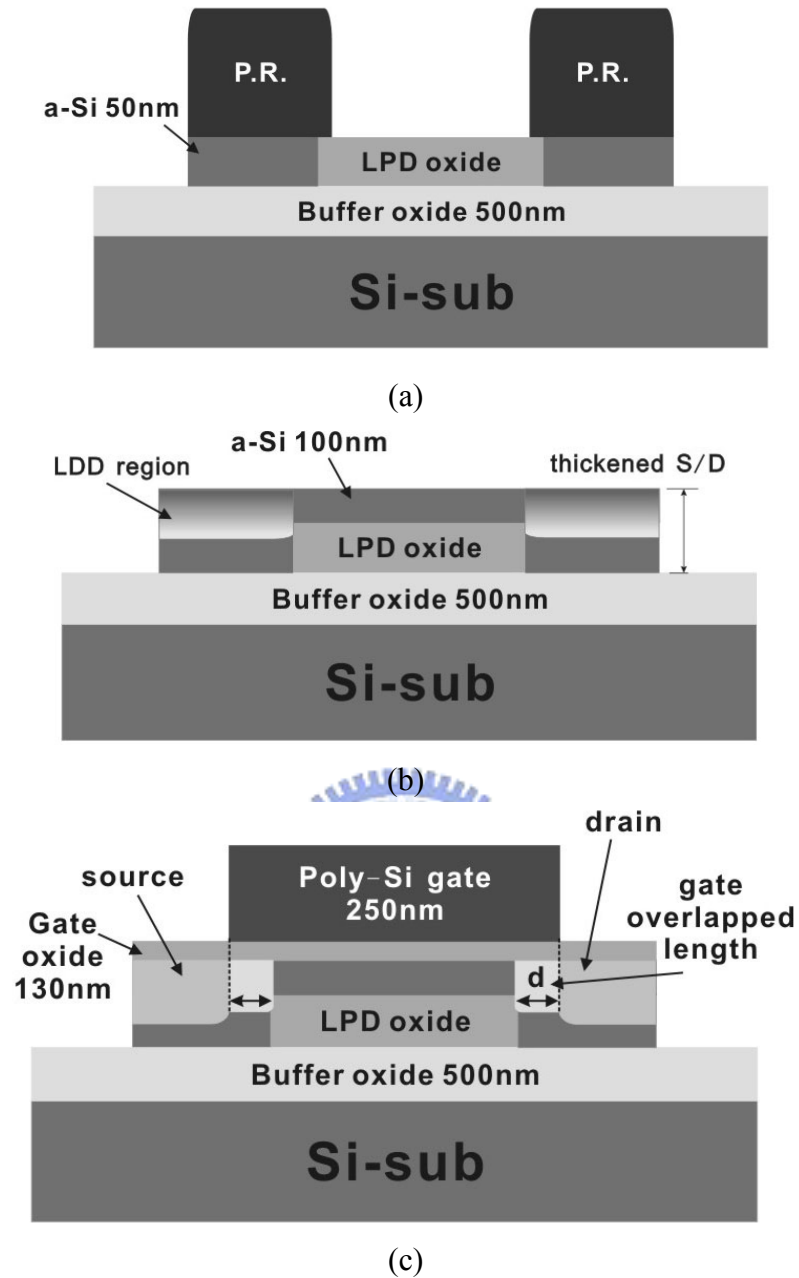


Figure 4-5 Process flow of ECTFT with GOLDD structure

Moreover, in order to find out the optimal conditions for ELA, we prepared samples with a-Si of 100 nm at channel while 150 nm at S/D, and planar samples with a-Si of 100 nm on an oxidized silicon wafer. The laser energy was split from 245 mJ/cm² to 345 mJ/cm², 50 shots.

4.4 Results and Discussion

Figure 4-6 shows a series of SEM photographs at random sites that revealed 100-nm a-Si being recrystallized by ELA with energy density ranging from 245 mJ/cm² to 345 mJ/cm². The grain size was smaller than 500 nm when the laser energy density below 300 mJ/cm², representing that the a-Si was only partially melted. With increasing the laser energy density above 300 mJ/cm², the average grain size of recrystallized poly-Si can reach 1 μm, meaning that the ELA had caused a super lateral growth mechanism. Moreover, Fig. 4-7 exhibits SEM photographs of ECTFT structure recrystallized by ELA with energy density ranging from 245 mJ/cm² to 345 mJ/cm². Interestingly, a super lateral growth mechanism can be easily observed at the channel region for laser energy density above 300 mJ/cm², and the size of large longitudinal grains exceeds 2 μm. It is known that lateral thermal gradient could arise because of the heat generated at moving solid-melting interface [4.38]. When proper laser energy irradiates the active layer of ECTFT structure, the thin channel region is completely melted but the thick S/D is only partially melted, leaving behind islands of solid material. Therefore, the recrystallization process would start at the thick S/D region, utilizing the unmelted Si island as the seed, and then the grain stretch toward the fully melted thin-channel area until the two grain boundaries originated from the opposite sides meet with each other. Figure 4-8 depicts the averaged grain size of conventional and elevated channel TFTs versus different laser energy density. In this figure, the phenomenon of super lateral growth was widely observed for ECTFT as laser energy density larger than 300 mJ/cm² while that for conventional planar TFTs was restricted in an limited laser energy range, implying that a broad process window as well as good device uniformity can be achieved with ECTFT architecture.

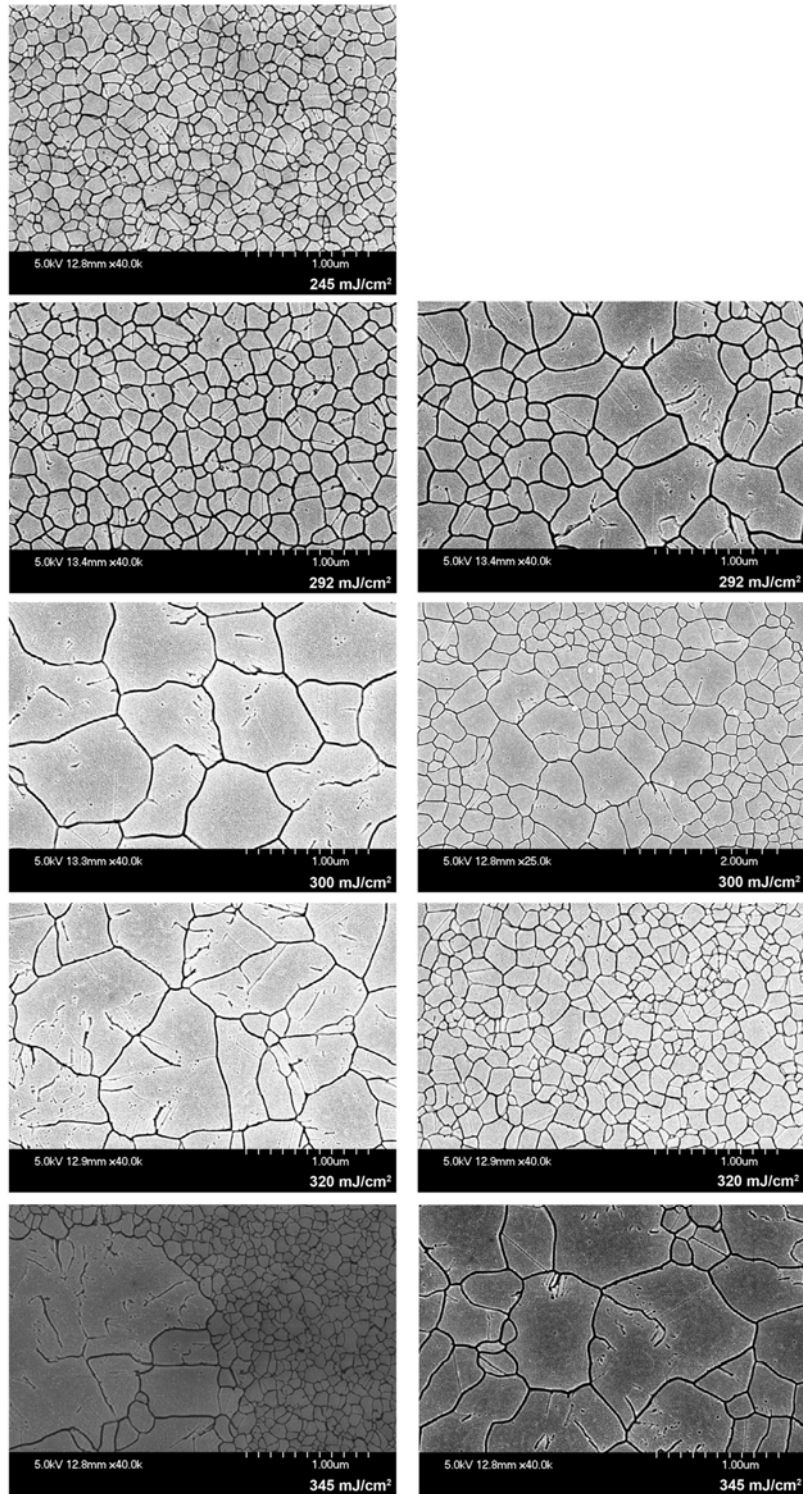


Figure 4-6 SEM photographs of 100-nm a-Si recrystallized by ELA with energy density ranging from 245 mJ/cm² to 345 mJ/cm².

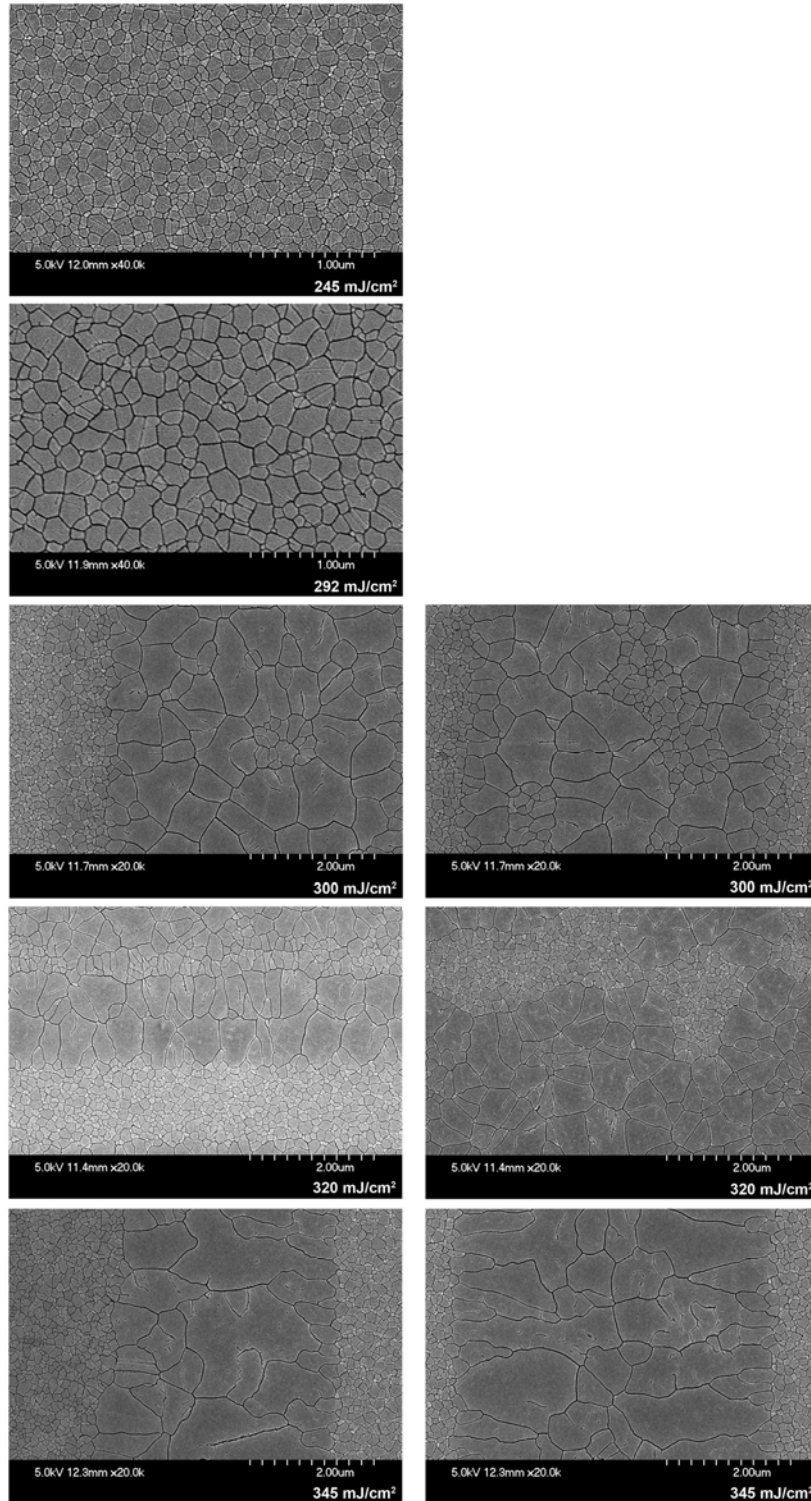


Figure 4-7 SEM photographs of ECTFT structure recrystallized by ELA with energy density ranging from 245 mJ/cm² to 345 mJ/cm²

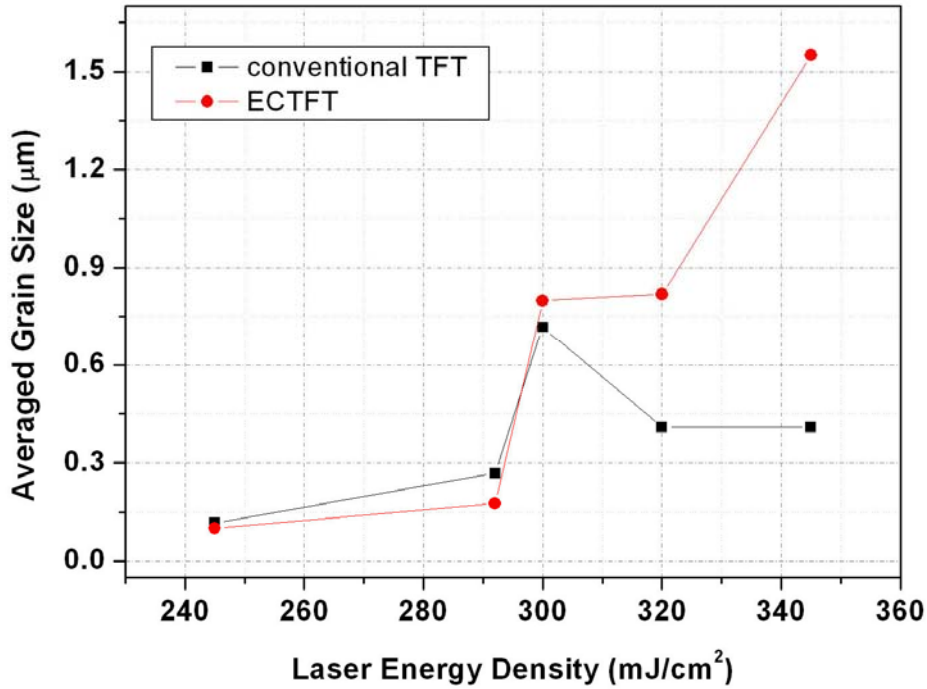


Figure 4-8 The averaged grain size of conventional and elevated channel TFTs versus different laser energy density

Typical $I_{DS} - V_{DS}$ curves of TFTs with different active area thickness are depicted in Fig. 4-9. The conventional TFT with thick channel layer (150 nm) does not exhibit a kink effect, but its ON current was only half compared to the case of ECTFT. Severe kink effect, even at low drain bias, can be observed for the samples with active layer of 100-nm thick. Notably, the ECTFT structure can suppress the kink effect effectively without sacrificing the saturation current.

High drain electric field is a major cause of the kink effect in TFT. The accelerated electrons by lateral electric field induce impact ionization near the drain side. Holes, generated by impact ionization, flow toward the source in the back-channel region and cause a potential barrier lowering at the source junction. Hence, further electrons are injected into the body and contribute to the anomalous increase of the drain current [4.11]. For single crystalline MOSFETs, the maximum channel electric field can be written as [4.39]

$$E_{\max} = (V_{DS} - V_{Dsat}) / l \quad (4.2)$$

where the characteristic length l is given as

$$l = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{ox} x_j} \quad (4.3)$$

and x_j is the drain junction depth. According to the simulation results performed by Anish Kumar K. P. et al., the E_{max} can be reduced by 20% with increasing the junction depth [4.40]. Consequently, for ECTFT, the channel electric field can be relaxed by connecting the thin channel to the thick S/D regions with deep junction depth.

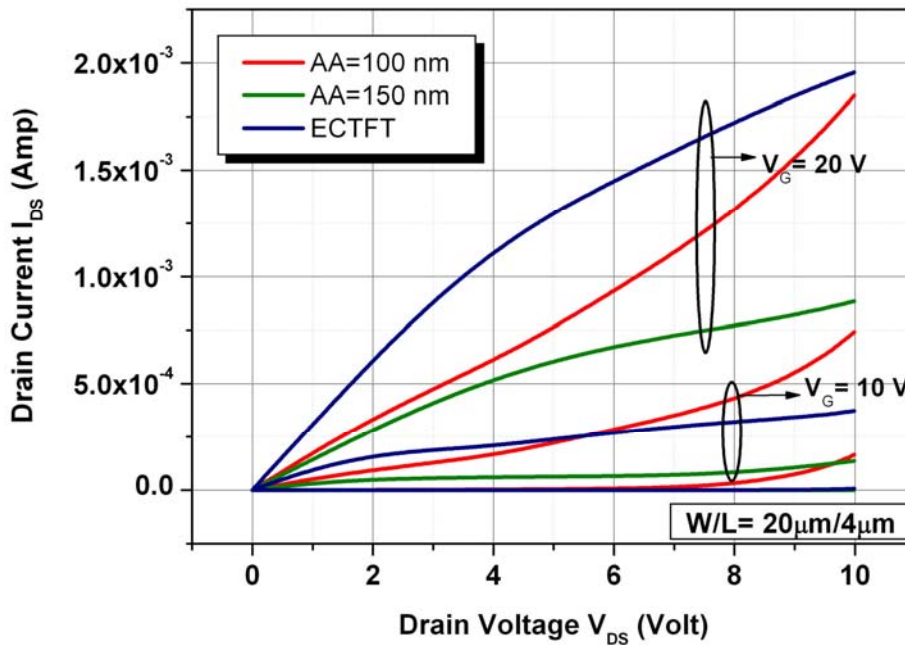


Figure 4-9 $I_{DS} - V_{DS}$ curves of TFTs with different active area thickness; $d = 0 \mu\text{m}$

Figure 4-10 shows the transfer curves and field-effect mobility curves of TFTs with different active layer thickness. Some important device characteristics are also listed in Table 4-2.

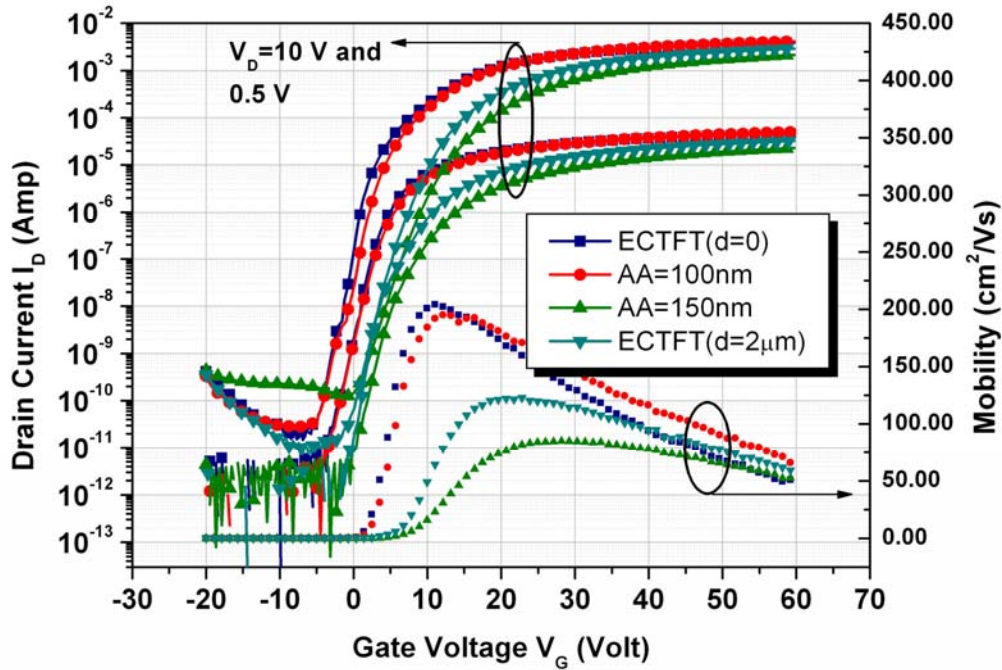


Figure 4-10 Transfer curves and field-effect mobility of TFTs with different active layer thickness

Table 4-2 Device characteristics of conventional TFTs and ECTFT with different gate-overlapped length

	μ_{FE} (cm^2/Vs)	V_{th} (volt)	ON/OFF ratio ($\times 10^7$)	I_{OFF} ($\times 10^{-13}$)* ¹	I_{OFF} ($\times 10^{-10}$)* ²	$R_{S/D}$ ($\text{k}\Omega$)	N_t ($\times 10^{12}$)* ³
AA1000	142	3.6	5.09	8.09	2.64	1.385	1.21
AA1500	81	6.36	1.21	20.5	3.46	2.43	1.59
ECTFT d = 0 μm	153	4.34	6.18	5.58	3.71	0.725	1.18
ECTFT d = 2 μm	121	5.02	6.91	6.83	4.59	1.49	1.33
ECTFT d = 3 μm	99	5.89	3.94	8.98	43	2.62	1.45

*1: the minimum value of $I_D - V_G$ curves as $V_D = 0.1 \text{ V}$

*2: extracted at $V_D = -10 \text{ V}$ and $V_G = -20 \text{ V}$

*3: in cm^{-2} , extracted by the modified Levinson method [4.41], [4.42]

Thanks to the large longitudinal grains in the channel region, ECTFT without gate-overlapped architecture ($d = 0 \mu\text{m}$) exhibit better electrical properties than those of

conventional TFT, such as mobility, ON/OFF ratio, OFF current, subthreshold swing and trap-state density, etc. For GOLDD TFT structure ($d = 2 \mu\text{m}$), a satisfactory ON/OFF current ratio up to 10^7 can be achieved because the GOLDD region would suppress the leakage current at OFF state while maintain the ON current by inducing excess free carriers in the n^- region. In contrast, the electrical properties of conventional TFTs with thick active layer are quite poor, since the channel region cannot be fully recrystallized by laser annealing and contains high density of trap states in the grain boundaries. Moreover, we extracted the S/D series resistance $R_{S/D}$ by measuring R_{ON} of output characteristics of TFTs in the linear region and plotting $R_{ON}W$ as a function of gate length L . $R_{S/D}$ of ECTFT and conventional TFT ($AA = 100 \text{ nm}$) were about $0.725 \text{ k}\Omega$ and $1.385 \text{ k}\Omega$, respectively. Therefore, the ECTFT structure can simultaneously reduce the value of series resistance with thick S/D and maintain good channel crystallizability with a thin active layer. Besides, although the gate and the thin channel regions are not self-aligned, the I-V characteristics are identical by reverse measurement of source and drain electrodes, as shown in Fig. 4-11.

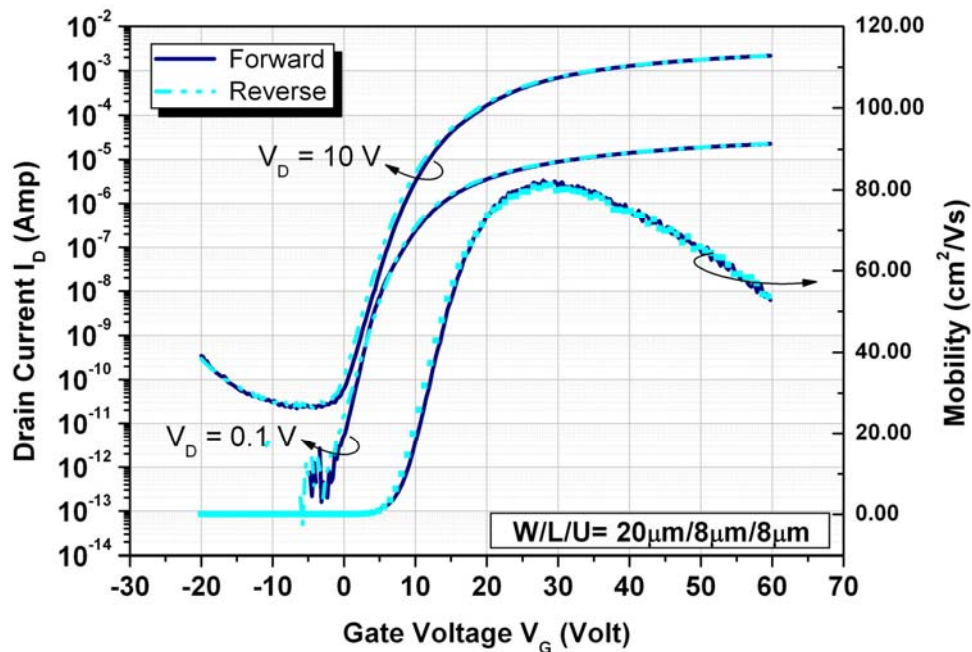
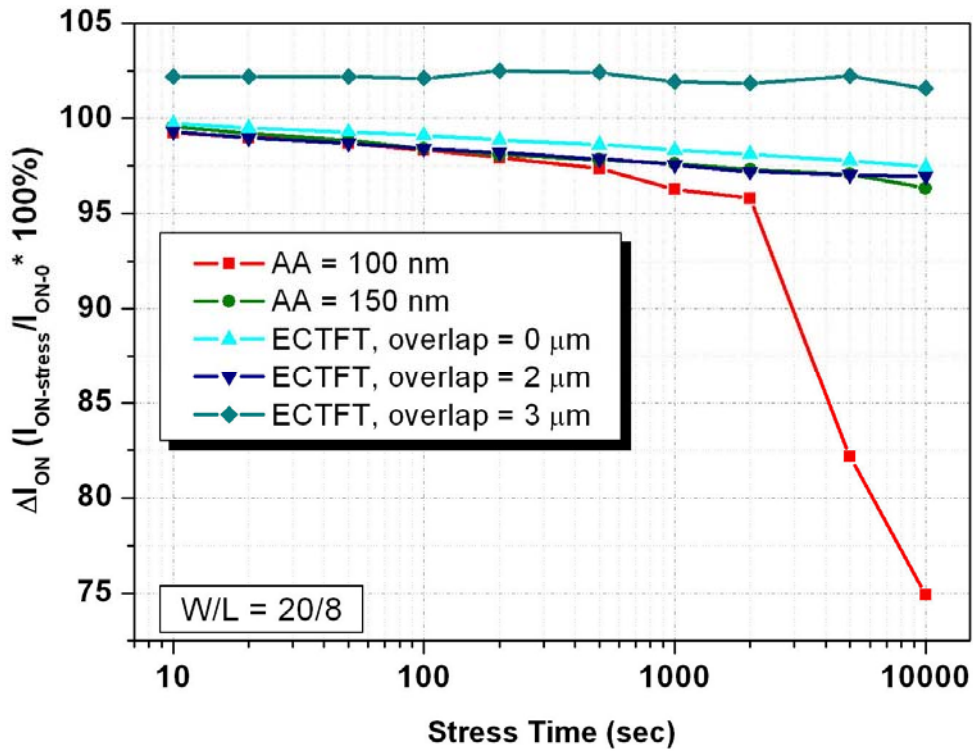
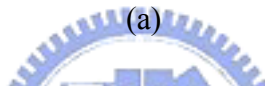
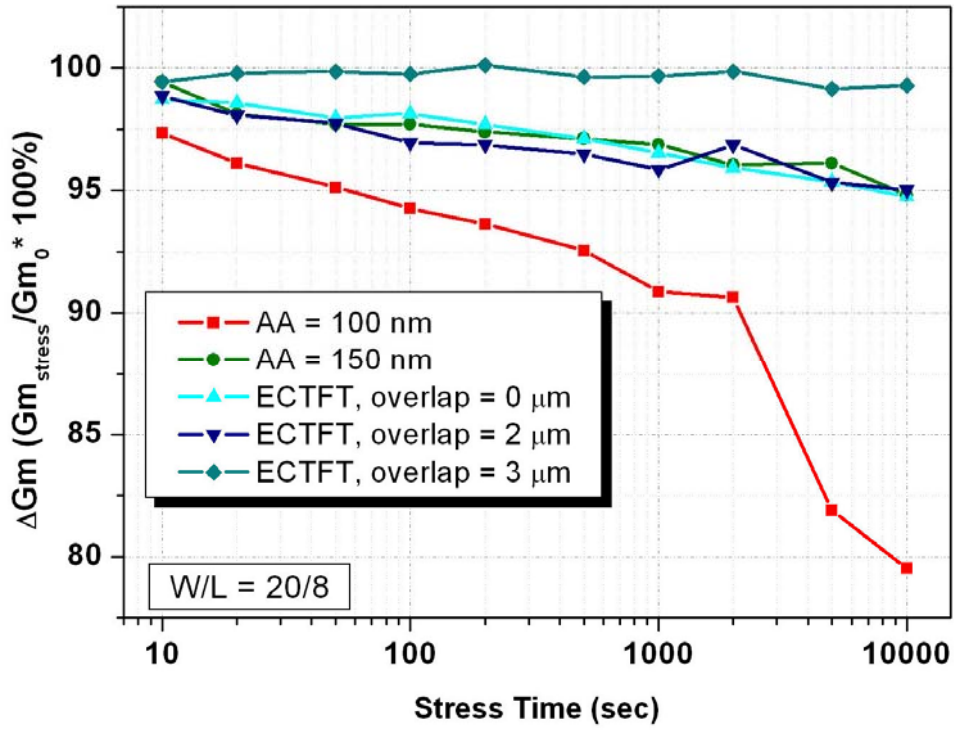


Figure 4-11 Forward and reverse measurement of the transfer curves of an ECTFT with $W/L = 20 \mu\text{m}/8 \mu\text{m}$ and $d = 0$

To evaluate the long-term reliability of TFTs, we performed hot carrier stress with the following conditions: $V_{DS} = 15$ V and $V_{GS} = 7.5$ V. Figure 4-12(a) shows the degradation of transconductance of various TFT structures versus stress time, while Fig. 4-12(b) illustrates the variation of I_{ON} versus stress time. It has been reported that the predominant mechanism for device degradation induced by drain avalanche hot carrier injection is the formation of interface states near the drain [4.43]. Accordingly, the hot carrier immunity can be greatly improved by reducing the electric field and the associated impact ionization rate at the drain junction, which is the case of ECTFT/GOLDD architecture. For proposed structure, however, increasing the length d of gate overlap would deteriorate the device characteristics due to the incorporation of defective thick poly-Si layer, so trade-off between device performance and reliability must be chosen carefully.





(b)

Figure 4-12 The degradation of (a) transconductance and (b) ON-current of various TFT structures versus stress time

4.5 Summary

In this section, we introduced several undesired effects of conventional poly-Si TFTs including large off-state leakage current, kink effect and hot carrier reliability; the corresponding TFT structures for eliminating those effects were also discussed. The proposed ECTFT structure exhibit better device performance than the conventional TFTs. The thick S/D regions can induce super lateral growth in the channel during laser recrystallization, contributing to large longitudinal grain. The lateral electric field can be relaxed with increasing the junction depth near the drain side, so that the kink phenomenon and the hot carrier endurance were improved effectively. The fabrication of ECTFT/GOLDD structure utilized unique selective-LPD technique at room temperature, which is fully compatible with current flat panel display industry.

