Chapter 5

High-Performance Polycrystalline Silicon Thin Film Transistors Crystallized by Excimer Laser Irradiation with a-Si Spacer Structure

---

5.1 Introduction

Low-temperature polycrystalline silicon (LTPS) technology has been the most promising method to manufacture high performance thin film transistors (TFTs) for the past decades [5.1] – [5.3]. The mobility of poly-Si TFTs is generally two orders higher than that of amorphous Si (a-Si) TFTs, so that both n- and p-channel devices with reasonable high drive currents can be achieved in poly-Si [5.4] – [5.5]. The high drive current allows smaller TFTs to be used as the pixel-switching elements, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance [5.6]. In addition, the capability to realize complementary metal-oxide-semiconductor (CMOS) circuits allows low-power driver circuitry to be integrated with the active matrix, for reduced display-module cost and improved reliability [5.7] – [5.11]. As a result, LTPS TFTs has been widely used as a material for mobile applications such as the display of digital cameras and notebook computers. Furthermore, system on panel (SOP) which combines memory and controller with driver circuits on a glass substrate will become the most attractive applications for LTPS TFTs in the near future [5.12]. Thus, there is a great interest in

improving the performance of LTPS TFTs.

Among a variety of crystallization techniques reported to date, excimer laser crystallization (ELC) seems to be the most promising method to meet the requirement of high mobility for high-speed operation [5.13] – [5.16]. Although large grains can be obtained in the super lateral growth (SLG) regime, many small grains still spread between these large grains. According to SLG model [5.17], the lateral grain growth distance is determined by the quenching rate of liquid silicon and the retain-solid Si seed distance. Thus, a little deviation in spatial and/or pulse-to-pulse energy density and a-Si thin film thickness can easily result in partial or full melting of a-Si thin film at local region. Consequently, a very non-uniform grain size distribution is always observed in the SLG regime. The non-uniform grain distribution is the main cause of the enormous performance variation of LTPS TFTs when the laser energy density is controlled in the SLG regime [5.18] – [5.19].

In previous chapters, the fabrications of low-temperature poly-$Si_{1-x}Ge_x$ TFTs by several ELC methods have been demonstrated. In comparison with the ELC poly-Si TFTs, the direct-ELC poly-$Si_{1-x}Ge_x$ TFTs and Si-capped ELC poly-$Si_{1-x}Ge_x$ TFTs both exhibit higher leakage current, larger threshold voltage, lower carrier mobility, and inferior subthreshold swing. It can be attributed to the worse crystallinity as well as the Ge segregation in the ELC poly-$Si_{1-x}Ge_x$ thin film, which result from the different thermal properties of Si and Ge as discussed in chapter 3. On the other hand, for the Ge doped ELC poly-$Si_{1-x}Ge_x$ TFTs with small device dimension, the carrier mobility is greatly improved due to carrier mobility enhancement effect contributed by Ge atoms. It is inferred that the degree of mobility enhancement by Ge incorporation is beyond that of mobility degradation by defect traps generation when TFT size is reduced to 2μm/2μm. Although the Ge doped poly-$Si_{1-x}Ge_x$ TFTs can provide higher field effect mobility, however, they still suffer from the phenomenon of poor device uniformity and the mobility needs to be further enhanced. Thus, novel device fabrication process must be proposed to improve the non-uniform device performance while

still maintain excellent electrical characteristics.

Poly-Si thin films with large grain always result in high-performance poly-Si thin film devices due to the reduction of defect traps of the grain boundaries. Hence, enlarging grain size is the most effective manner for improving the performance of the poly-Si devices. A variety of crystallization methods have been proposed to produce large grains with superior grain size distribution uniformity. They include sequential lateral solidification (SLS) [5.20] - [5.28], grain-filters (or substrate-embedded seeds) method [5.29] - [5.31], phase-modulated ELC using an optical phase-shift mask [5.32] - [5.36], capping reflective or anti-reflective layer [5.37] - [5.42], ELC of selectively floating a-Si thin film [5.43] - [5.47], ELC of pre-patterned a-Si thin film [5.48] - [5.51], dual beam ELA [5.52], and so on. Although all of them provided alternatives to produce large-grain poly-Si thin films, these methods can not readily be implemented using existing ELC equipment.

In this chapter, we describe a novel process for producing high-mobility poly-Si TFTs. In order to induce lateral grain growth, a lateral temperature gradient must be created between the adjacent areas and there must be retained solid Si to act as the seeds for lateral crystallization. By completely melting the a-Si thin film in a certain region and partially melting the one at adjacent area, a large lateral temperature gradient will exist between these two regions, and grains will grow laterally towards the complete melting region from the retained solid Si. In this method, a-Si spacers are formed by dry-etching of the a-Si/Si_3N_4 step structures which then serves as the seeds for lateral grain growth during excimer laser irradiation. Thus, a large-grain poly-Si film is obtained which will lead to improved device performance. In addition, the lateral grain growth starting from the a-Si spacer seed can progress along the opposite direction. Hence, when the channel region is designed to arrange at the spacer region, the boundary perpendicular to the current flow in the channel region is reduced. This improves the disadvantage of the evitable longitudinal boundary at the middle of the channel region in many lateral grain growth methods. Due to the artificial controlling

of the lateral growth and improved periodicity of the polycrystalline microstructure, the uniformity of device characteristic can be further improved.

Besides, another advantage of this proposed crystallization technique is that it can be used to fabricate large dimension TFT, i.e., channel length >10um. Although a variety of methods can achieve artificial lateral grain growth, most of them are restricted to small dimension device (i.e., channel length <10um) owing to the limited lateral growth distance and huge nucleation seed size [5.53]. One of the solutions is to adopt multi-channel structure [5.54]. However, this will increase the total device area, the process complexity, and the layout difficulty. In this method, owing to the tiny width of the a-Si spacer (< 1000Å), the a-Si spacers can be arrange periodically inside the channel region. Consequently, periodic lateral grain growth can be produced at the channel region of large-dimension device. This is also the first time to demonstrate periodic lateral grain growth in the channel region by using existing ELC system until now.

In this chapter, the concept of periodic grain growth by using a-Si spacer structure is first discussed, and the experimental details are then demonstrated. The results of crystallized poly-Si thin films and LTPS TFT performance are presented and analyzed.

5.2. The Concept of Periodic Lateral Grain Growth with a-Si Spacer Structure

For producing the single-crystalline Si (c-Si) TFTs on glass, it is essential not only to ensure formation of the Si grain at a desired position on the substrate, but also to enlarge the average size to larger than the minimum feature size (about 2μm) of the TFTs. Alternatively, it is desired to control the location of the grain boundary, since it enables the realization of the poly-Si TFTs having uniform characteristics by precise control of the number and direction of

grain boundaries in TFTs. Moreover, defects, crystallographic orientation and texture of the large grains are important parameters for the performance of c-Si TFTs. For the formation of Si grain at a desired position, it can be realized by controlling the Si nucleation site at the selected region. The Si grain can be enlarged by increasing Si melt duration time, which can be lengthened by a long pulsed laser irradiation or substrate heating.

In order to induce lateral grain growth, a fluence gradient must be enforced such that the a-Si thin film is melted at the area exposed to higher laser fluence and partially melted at the adjacent area exposed to lower laser fluence. Under this condition, grains grow laterally towards the completely molted region. The lateral grain growth will eventually be arrested by either colliding with lateral grains grown from the other side or by spontaneous nucleation triggered in the severely supercooled molted silicon pool. Evidently, high fluence gradients drive steeper temperature gradients. Since it takes a longer time for the hotter molten silicon region to cool down to the spontaneous nucleation temperature, the lateral grain growth can continuous for a longer distance.

On the other hand, the effect of lateral grain growth by using fluence gradient can also be achieved by adopting the different thicknesses of a-Si thin films in adjacent regions while irradiate with the same laser energy density. By completely melting the a-Si thin film with large thickness and partially melting the one with small thickness, a lateral temperature gradient will exist between the complete melting liquid-phase region and un-melting solid-phase seeds, and grains will grow laterally toward the complete melting region from the retained solid seeds. In this work, an a-Si thin film with two kinds of thickness in a local region is used to produce a local temperature gradient during excimer laser irradiation. The schematic illustration of lateral grain growth mechanism using an a-Si spacer structure is shown in Figure 5.1. As shown in Figure 5.1 (b) and 5.1(c), when excimer laser irradiation is applied on the a-Si thin film, the applied laser energy density is controlled to completely melt the thin region of a-Si thin film but partially melt the thick spacer region. The partial-melted

a-Si spacer serves as the nucleation site for lateral grain growth. As a result, a lateral temperature gradient can be produced between the local thin and thick regions of a-Si film, and grains will grow laterally towards the complete melting region from the retained solid a-Si spacer (i.e., nucleation seeds). On the other hand, according to Figure 5.1(c), the lateral grain growth starting from the a-Si spacer seed can progress along the opposite direction. Hence, when the channel is properly designed to arrange at the spacer region, the boundary perpendicular to the current flow in the channel region is reduced as shown in Figure 5.2. This improves the disadvantage of the evitable longitudinal boundary at the middle of the channel region in many lateral grain growth methods.

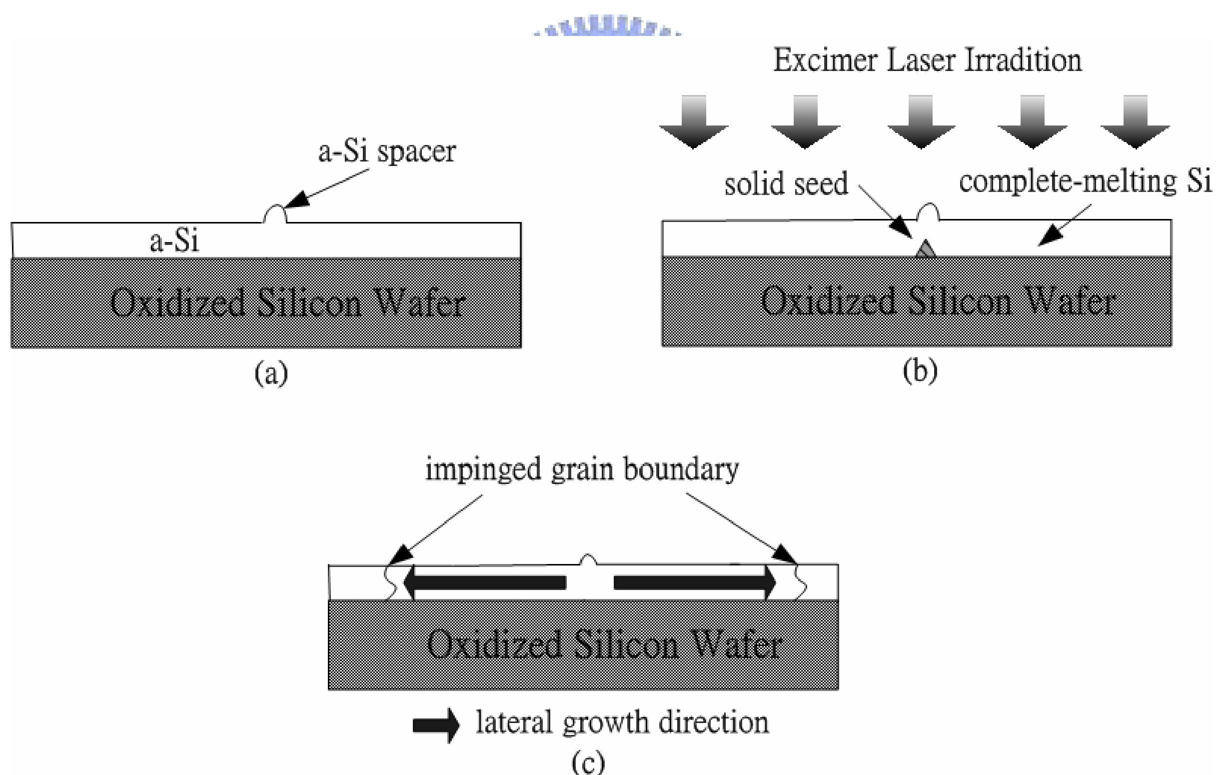

Figure 5.1. The schematic illustration of lateral grain growth mechanism using an a-Si spacer structure.

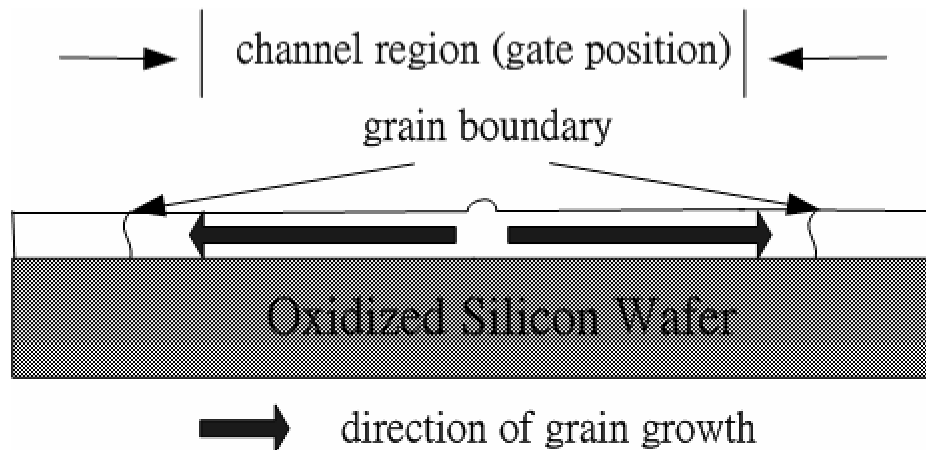

Figure 5.2. The schematic illustration of relative location of the channel region and a-Si spacer seed.

Besides, another advantage of this proposed crystallization technique is that it can be used to produce periodic lateral grain growth on the glass substrate. Figure 5.3 displays the schematic illustration of the periodic grain growth with a-Si spacer structure. The a-Si spacers can be fabricated periodically on the substrate. When proper laser energy intensity is applied on the a-Si thin film, the thin Si region is completely melted and lateral grain growth starts from the a-Si spacer. By suitably arranging the distance between the adjacent a-Si spacers, the lateral grain growth will be arrested until the solid-liquid boundary from opposite side impinges without any spontaneous nucleation. Thus, a periodic grain growth can be observed on the substrate. Although a variety of methods can achieve artificial lateral grain growth, most of them are restricted to produce one lateral longitudinal grain due to the huge nucleation seed size. In this work, owing to the tiny width of the a-Si spacer (< 1000Å), the a-Si spacers can be arrange periodically inside the channel region. Consequently, periodic lateral grain growth can be fabricated at the channel region, which can be used in large dimension TFT. This makes the proposed crystallization technique become useful in the field of System on Panel (SOP) because the circuits on a single panel need a variety of sizes of

TFT devices for different applications.

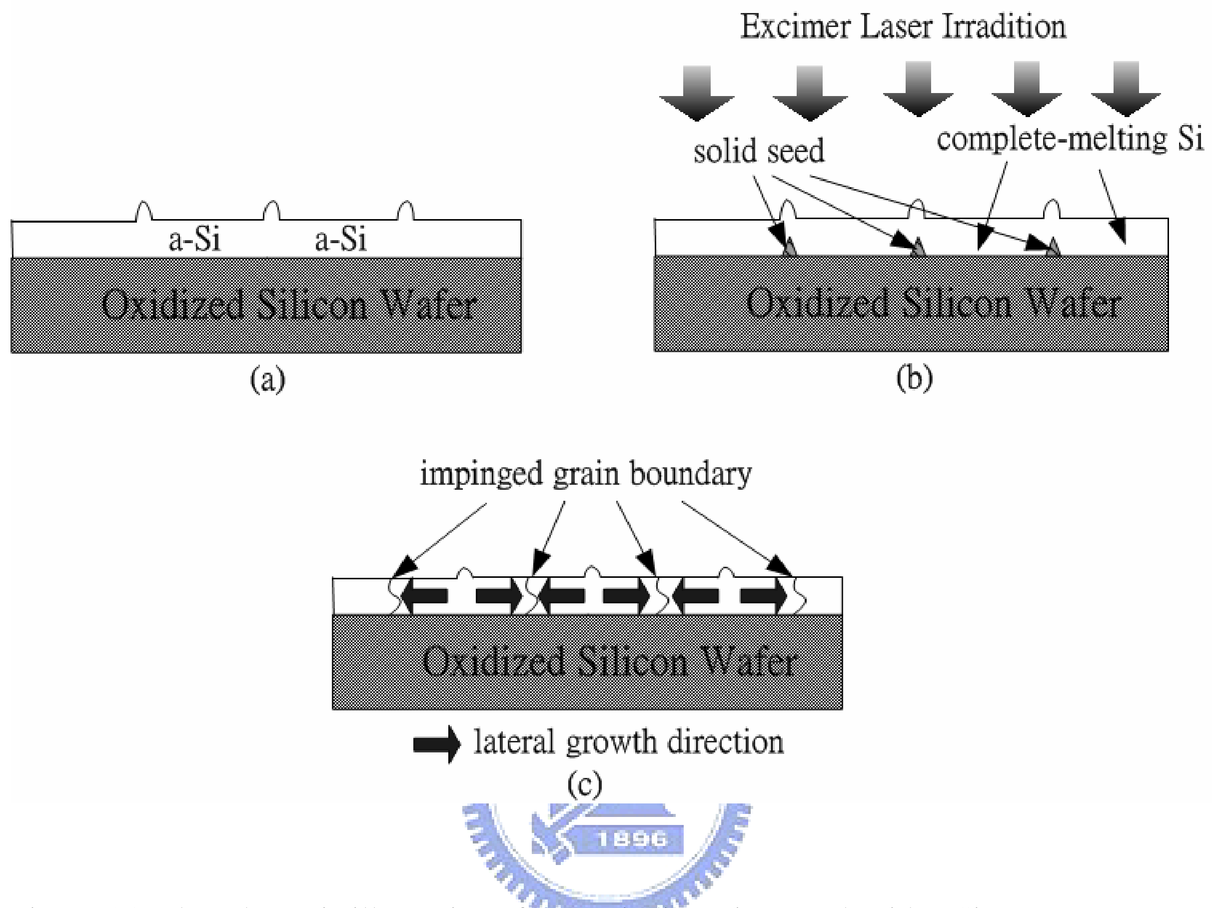

Figure 5.3. The schematic illustration of the periodic grain growth with a-Si spacer structure.

5.3 Experimental Procedure

5.3.1 Sample Preparation for SEM Observation

Figure 5.4 shows the process procedure of preparing samples for SEM analysis. At first, silicon nitride (Si_3N_4) thin films with thickness of 500Å and/or 1000Å were deposited by pyrolysis of pure silane (SiH_4) and ammonia (NH_3) with low-pressure chemical vapor deposition (LPCVD) on oxidized silicon substrates with oxide thickness of 1μm. Then, the Si_3N_4 layer was defined to form individual islands. Next, a 1000Å a-Si layer was deposited

by LPCVD at 550°C with SiH_4 as gas source. The a-Si layer was subjected to reactive ion etching (RIE), so that the a-Si spacers with 500 Å and/or 1000Å heights were formed at the sidewall of the Si_3N_4 islands. After removing the Si_3N_4 layer by phosphoric acid, another 1000Å a-Si layer was deposited by LPCVD at 550°C with SiH_4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-4} Torr and substrate was maintained at 400°C. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. The grain structure of the crystallized poly-Si thin film was analyzed using SEM. In order to facilitate the SEM observation, all the samples were processed by Secco-etch before SEM analysis.

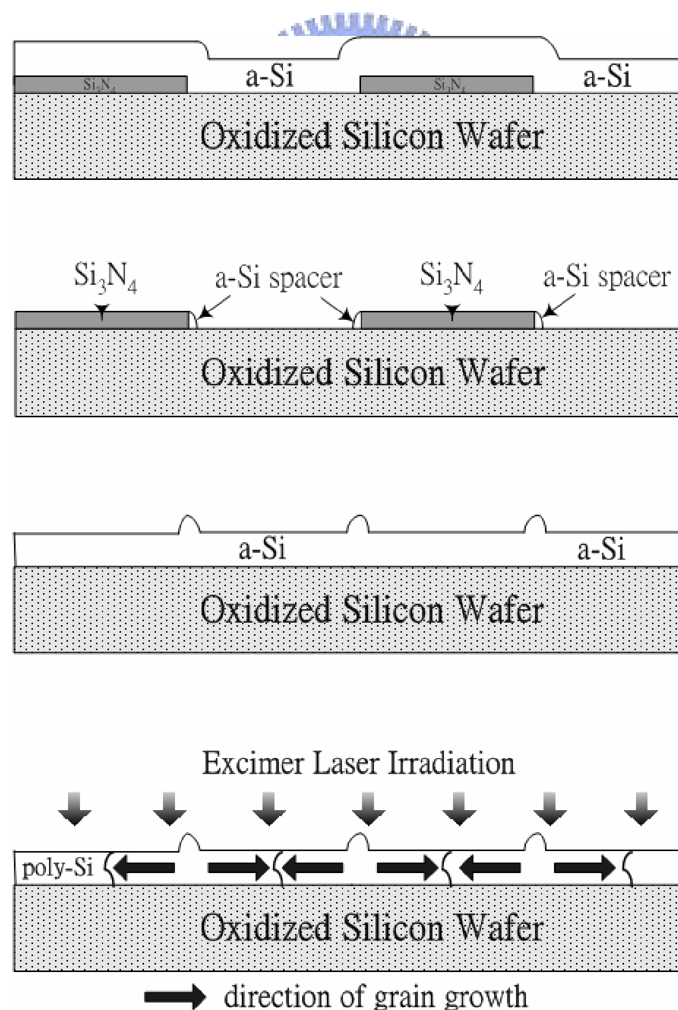

Figure 5.4. The process procedure of producing periodic lateral grain growth.

5.3.2 Fabrication of Small Dimension Poly-Si TFT with a-Si Spacer Structure

Since the lateral grain growth starting from the a-Si spacer seed can progress along the opposite direction, the longitudinal grain boundary at the middle of the channel region can be diminished. Thus, when the a-Si spacer is arranged at the middle of the channel region, no grain boundary perpendicular to the current flow was found inside the channel, which led to the improvement in device performance.

Figure 5.5 illustrates the key processes for fabrication of the poly-Si TFTs crystallized with a-Si spacer structure. At first, Si_3N_4 thin films with thickness of 500Å and/or 1000Å were deposited by pyrolysis of SiH_4 and NH_3 with LPCVD on oxidized silicon substrates with oxide thickness of 1μm. Then, the Si_3N_4 layer was defined to form individual islands. Next, a 1000Å a-Si layer was deposited by LPCVD at 550°C with SiH_4 as gas source. The a-Si layer was subjected RIE, so that the a-Si spacers with 500 Å and/or 1000Å heights were formed at the sidewall of the Si_3N_4 islands. After removing the Si_3N_4 layer by phosphoric acid, another 1000Å a-Si layer was deposited by LPCVD at 550°C with SiH_4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-4} Torr and substrate was maintained at 400°C. The number of laser shots per area was 20 (ie., 95% overlapping) and laser energy density was varied. After laser crystallization, the poly-Si active layers were etched to define the active channel region. Then, 1000 Å-thick tetraethyl orthosilicate (TEOS) gate oxides were deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. 2000Å-thick a-Si thin films were deposited by LPCVD at 550°C for formation of the gate electrode. Then, the a-Si thin films were etched by RIE to form gate electrodes and the gate oxides were removed by buffer oxide etch (BOE) chemical

solution. A self-aligned phosphorous implantation with a dosage of 5 × 10^{15} cm^{-2} was performed to form source and drain regions. 3000 Å-thick TEOS passivation oxide layers were deposited by PECVD and the implanted dopants were activated by thermal annealing at 600°C for 12 hours. After contact opening by RIE, aluminum thin film with a thickness of 5000Å was deposited by thermal evaporation and patterned to complete the fabrication of poly-Si TFTs. A 20-min sintering process was performed at 400°C to reduce the contact series resistance of the source and drain electrodes. No post plasma treatment was carried out on these devices. For comparison, conventional ELC poly-Si TFTs with a thickness of 1000Å were also fabricated.

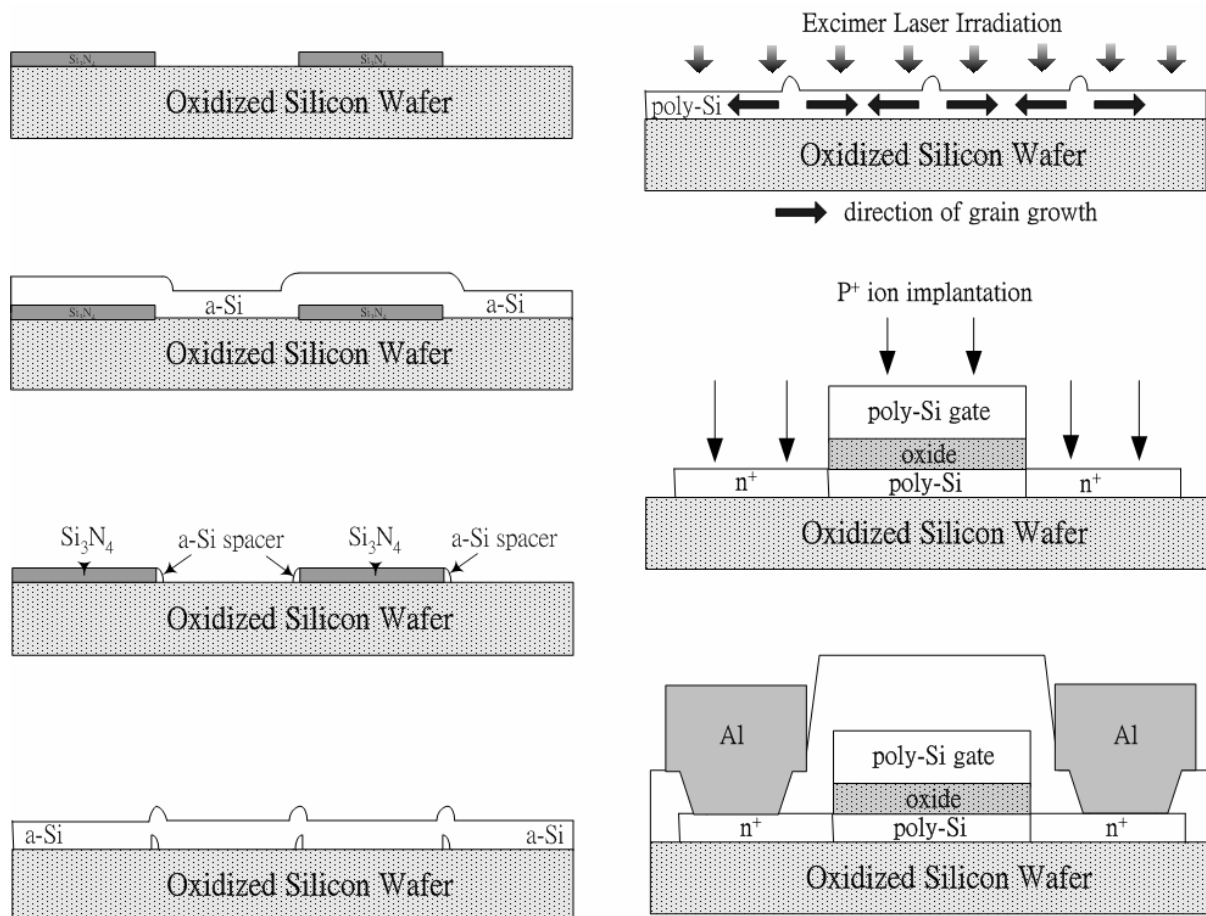

Figure 5.5. The key processes for fabrication of the poly-Si TFTs crystallized with a-Si spacer structure.

5.3.3 Fabrication of Large Dimension Poly-Si TFT with a-Si Spacer Structure

According to previous section, the periodic grain growth could be produced by using a-Si spacer structure. Thus, TFTs with large device dimension, i.e. channel length > 10μm, were fabricated with this crystallization technique. Figure 5.6 displays the schematic illustration of the channel region and the a-Si spacer positions for large-size device. Periodic transverse grains were existed inside the channel and the number of longitudinal grain boundary could be varied by adjusted the distance of adjacent a-Si spacers.

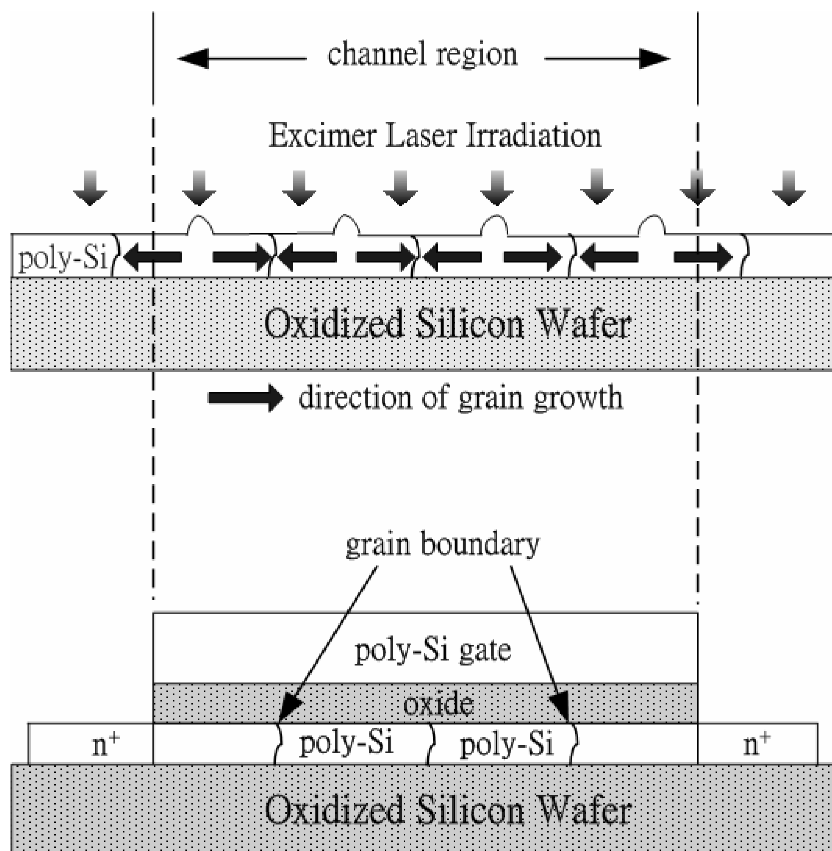

Figure 5.6. The schematic illustration of the relative positions of the channel region and the a-Si spacer location for large-size device.

Figure 5.7 illustrates the key processes for fabrication of the large-dimension poly-Si TFTs crystallized with a-Si spacer structure. At first, Si_3N_4 thin films with thickness of 500Å and/or 1000Å were deposited by pyrolysis of SiH_4 and NH_3 with LPCVD on oxidized silicon substrates with oxide thickness of 1μm. Then, the Si_3N_4 layer was defined to form individual islands. The distances between the adjacent Si_3N_4 islands were varied to investigate the effect of grain boundary on the device characteristics and find out the optimum conditions of the a-Si spacer distance. Next, a 1000Å a-Si layer was deposited by LPCVD at 550°C with SiH_4 as gas source. The a-Si layer was subjected RIE, so that the a-Si spacers with 500 Å and/or 1000Å heights were formed at the sidewall of the Si_3N_4 islands. After removing the Si_3N_4 layer by phosphoric acid, another 1000Å a-Si layer was deposited by LPCVD at 550°C with SiH_4 as gas source. Laser crystallization was performed by KrF excimer laser (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-4} Torr and substrate was maintained at 400°C. The number of laser shots per area was 20 (ie., 95% overlapping) and laser energy density was varied. After defining the active channel region, a 1000 Å-thick TEOS gate oxide was deposited by PECVD at 385°C. A 2000Å-thick a-Si was deposited by LPCVD at 550°C for formation of the gate electrode. Then, the a-Si was etched by RIE to form gate electrodes. A self-aligned phosphorous implantation with a dosage of 5×10^{15} cm^{-2} was performed to form source and drain regions. A passivation oxide layer was deposited and the implanted dopants were activated by thermal annealing at 600°C for 12 hours. Finally, contact opening and metallization were carried out to complete the fabrication of poly-Si TFTs with a-Si spacer structure. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, conventional ELC poly-Si TFTs were also fabricated.

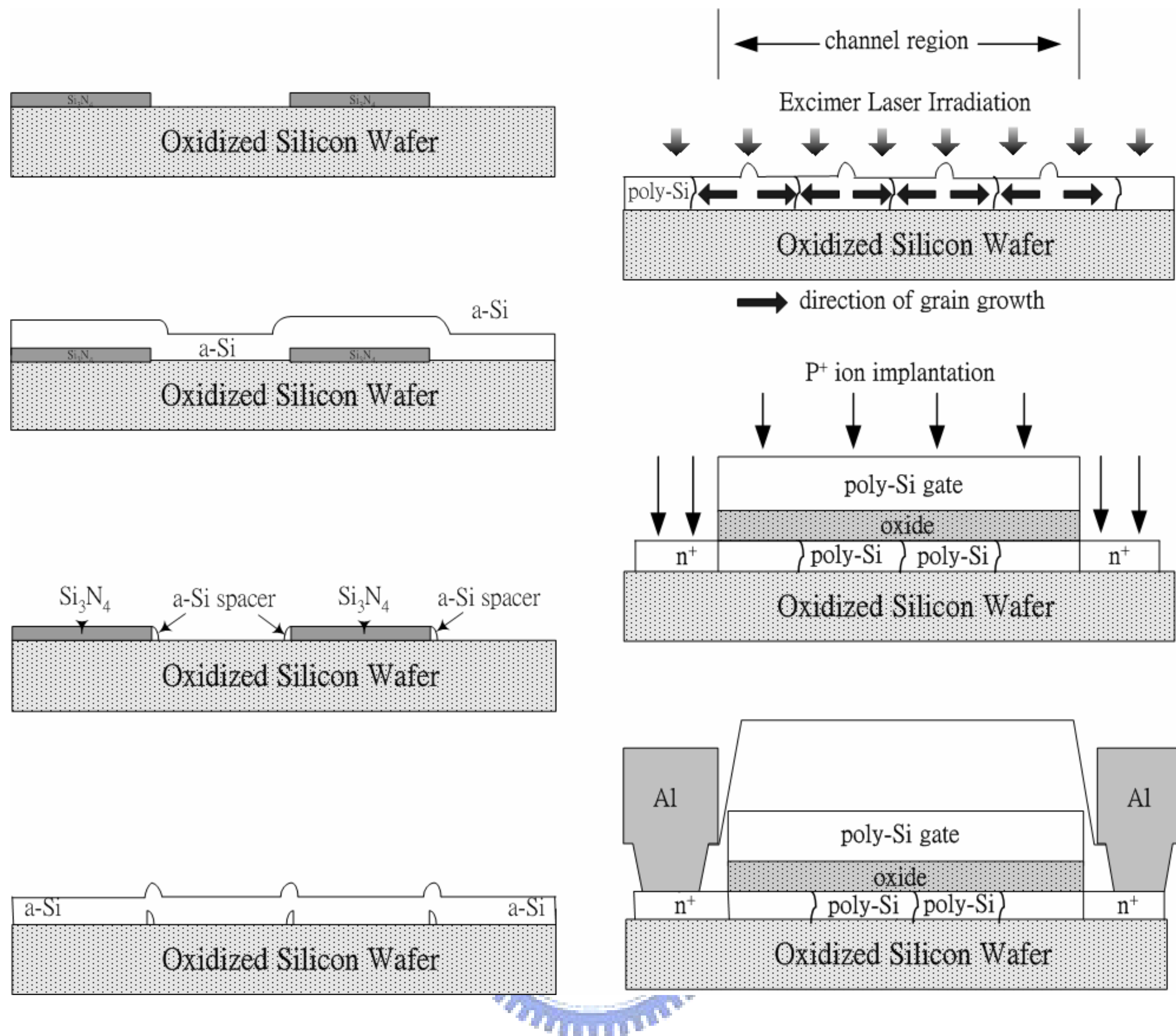

Figure 5.7. The key processes for fabrication of the large-dimension poly-Si TFTs crystallized with a-Si spacer structure.

5.4 Results and Discussion

5.4.1 Material Analysis of Poly-Si Thin Film with Periodic Lateral Grain Growth

Figure 5.8 shows a SEM picture of excimer laser crystallized poly-Si with a-Si spacer

structure after Secco etching. The distance between adjacent a-Si spacers is 1 μm and the locations of a-Si spacer seeds are indicated by the white dash lines. In this case, the thick a-Si spacer region is 1500Å and the other thin region is 1000Å. The laser energy fluence is 435 mJ/cm^2 and the substrate temperature is maintained at 400°C during laser irradiation to reduce the quenching rate of the complete melting Si.

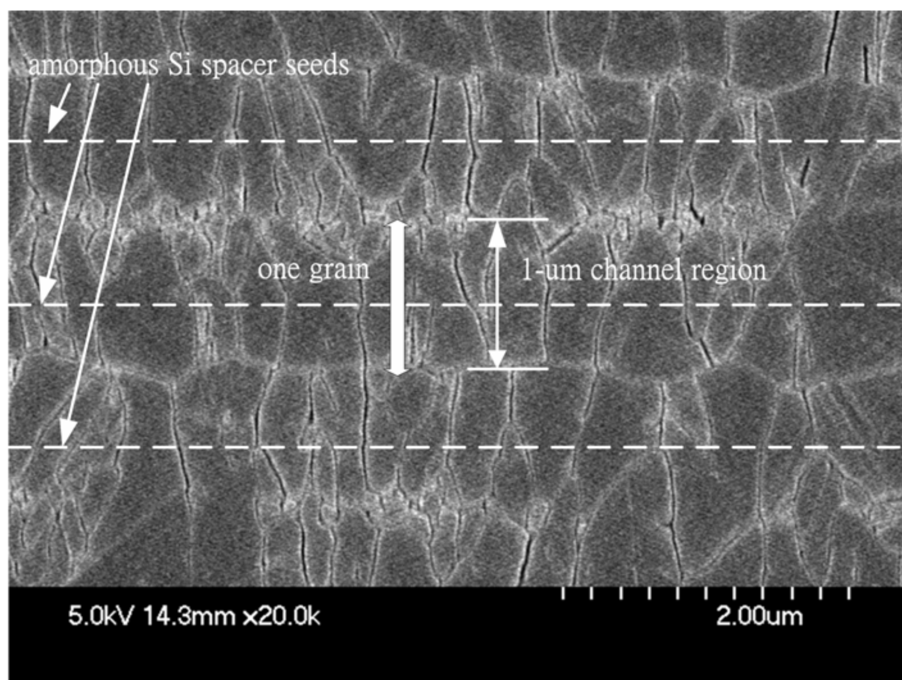

Figure 5.8. SEM picture of excimer laser crystallized poly-Si with 1500Å-thick a-Si spacer structure. The distance between adjacent a-Si spacers is 1 μm

As expected, longitudinal grains with 1 μm in length are formed periodically in the laser crystallized poly-Si thin film. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interface [5.55] - [5.56]. When a proper laser energy density irradiates the silicon thin film containing different thicknesses, the thin region is completely melted while the thick region is only partially melted, leaving behind

islands of solid material. As a result, grains will grow laterally towards the complete melting region from the retained solid seeds. In this work, with laser energy densities between completely melting 1000Å silicon thin film but partially melting the 1500Å a-Si spacer, the lateral growth will start from the still solid a-Si spacer seed, and stretch toward the completely melted region until the solid-melt interface from opposite direction impinge. Furthermore, the lateral growth starting from the a-Si spacer seed can progress along the opposite direction. Hence, when the channel region is suitably designed to arrange at the spacer region, the grain boundaries perpendicular to the current flow in the channel region can be reduced. Thus the field-effect mobility of poly-Si TFTs can be greatly improved with this crystallization technique.

In order to investigate the maximum distance of lateral grain growth, the length of neighboring a-Si spacer seeds is broadened. Figure 5.9 displays the SEM graph of the crystallized poly-Si thin film, in which the length of the adjacent a-Si spacers is 2 μm. The locations of a-Si spacer seeds are indicated by the white dash lines. In this case, the thick a-Si spacer region is 1500Å and the other thin region is 1000Å. The substrate temperature is also maintained at 400°C during laser irradiation to prolong the melting duration of complete melting Si. Evidently, the laser fluence determined the extension of lateral grain growth. When a longer a-Si spacer distance is adopted for crystallization, the laser fluence has to increase high enough to make the longitudinal grains collide with those grown from the other side; otherwise, small grains caused by spontaneous homogeneous nucleation will form between the neighboring a-Si spacer seeds. It is always undesired for device applications. Thus, in this case, the laser fluence has to be raised to enlarge the length of lateral grain growth (~ 460 mJ/cm^2). It is observed that the lateral grain growth can extend to 2 μm. Further detail analysis results reveal that the maximum achievable length of lateral grain growth in this crystallization method is about 2.5 μm.

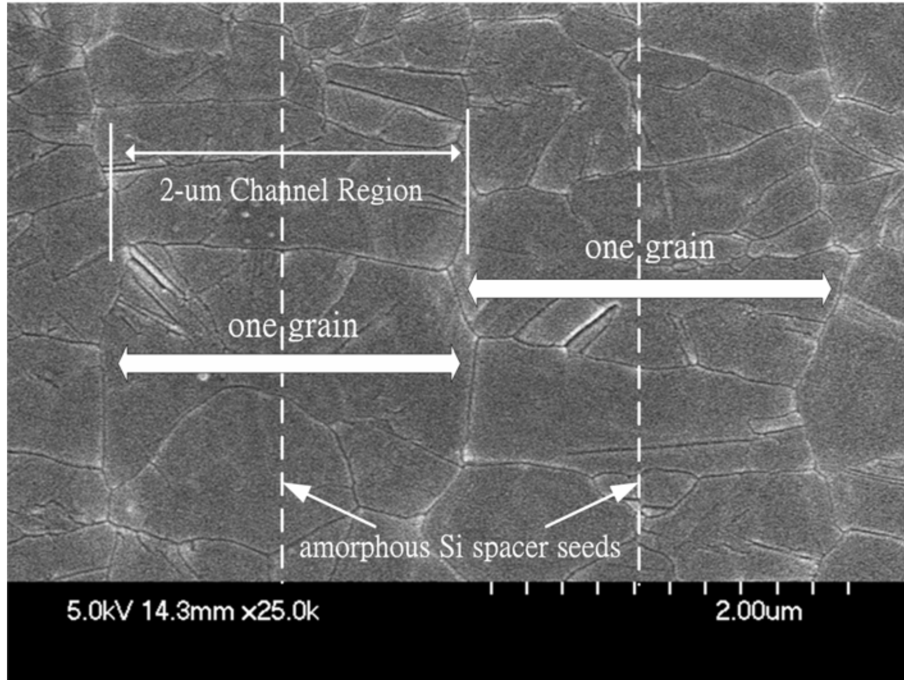

Figure 5.9. SEM graph of the crystallized poly-Si thin film, in which the length of the adjacent a-Si spacers is 2 μm.

The dependence of the lateral grain growth on the applied laser energy fluences was also investigated. Figure 5.10(a) ~ Figure 5.10(d) show the SEM graphs of the crystallized poly-Si thin film. In this case, the applied laser energy densities are 410, 435, 460, and 485 mJ/cm^2, respectively, which are all controlled to fully melt the 1000Å thin region but partially melt the 1500Å a-Si spacer region. The distance of the adjacent a-Si spacers used here is about 2 μm for convenience. Obviously, it can be found that periodic lateral grain growth occurs as the laser energy density exceeds 410 mJ/cm^2. It is evident that lateral growth is limited by spontaneous nucleation in the bulk liquid [5.55]. If spontaneous nucleation can be suppressed or delayed, the lateral growth will continuous to a longer distance, hence producing longer lateral growth. Higher local temperature in the completely molten region which results from high laser fluence implies correspondingly longer time to reach the deep supercoolong required for spontaneous nucleation. As a result, by adopting a suitable length of adjacent

a-Si spacers, periodic lateral grain growth can be acquired in the poly-Si thin film when the laser fluence increases beyond the fully melting threshold of the thin a-Si region.

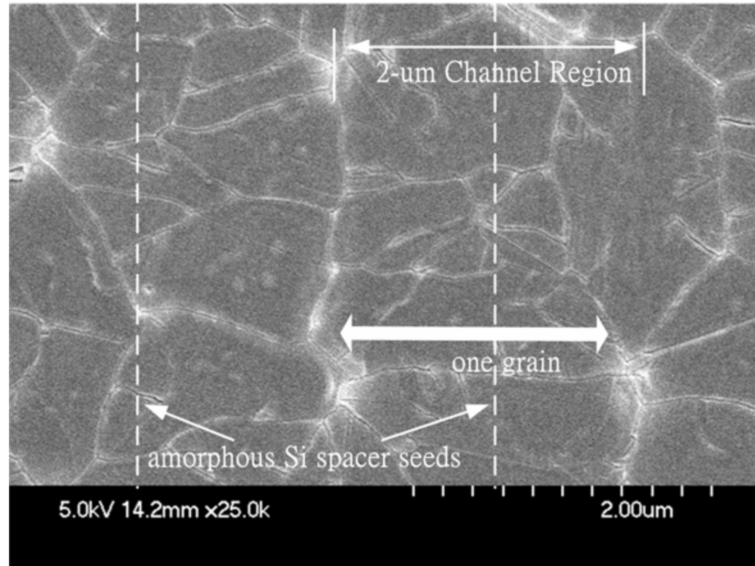

Figure 5.10(a). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 410 mJ/cm^2.

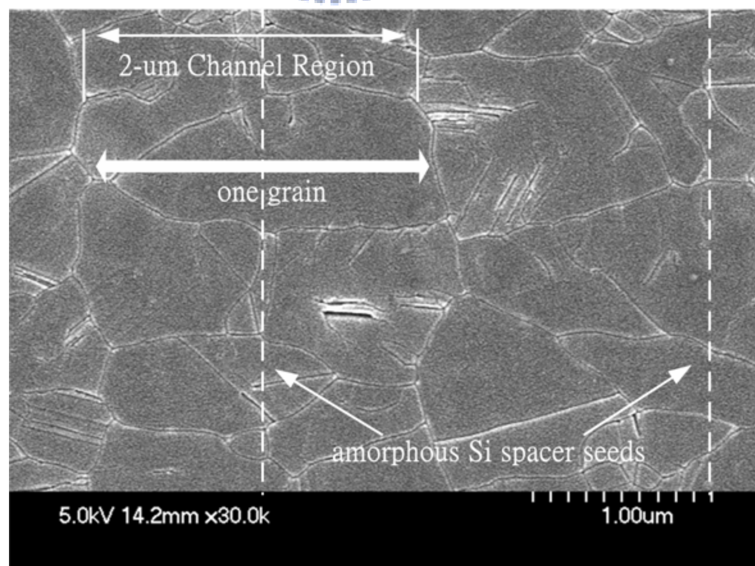

Figure 5.10(b). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 435 mJ/cm^2.

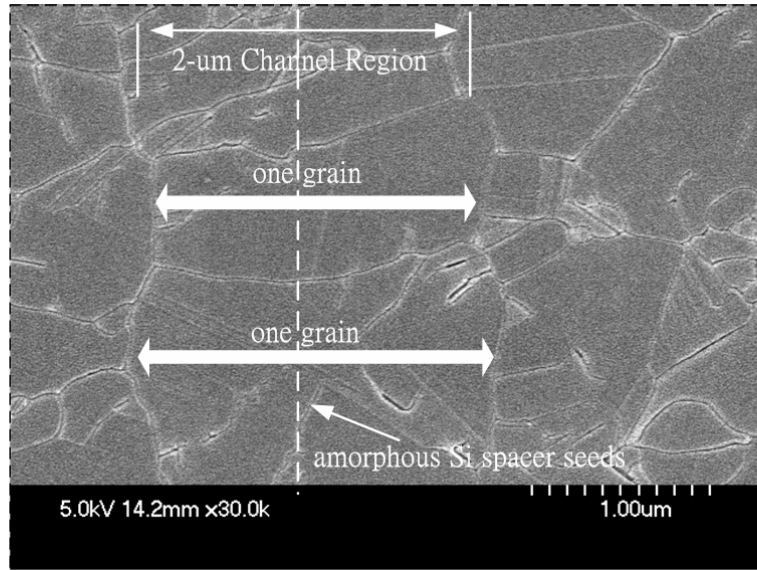

Figure 5.10(c). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 460 mJ/cm^2.

1896

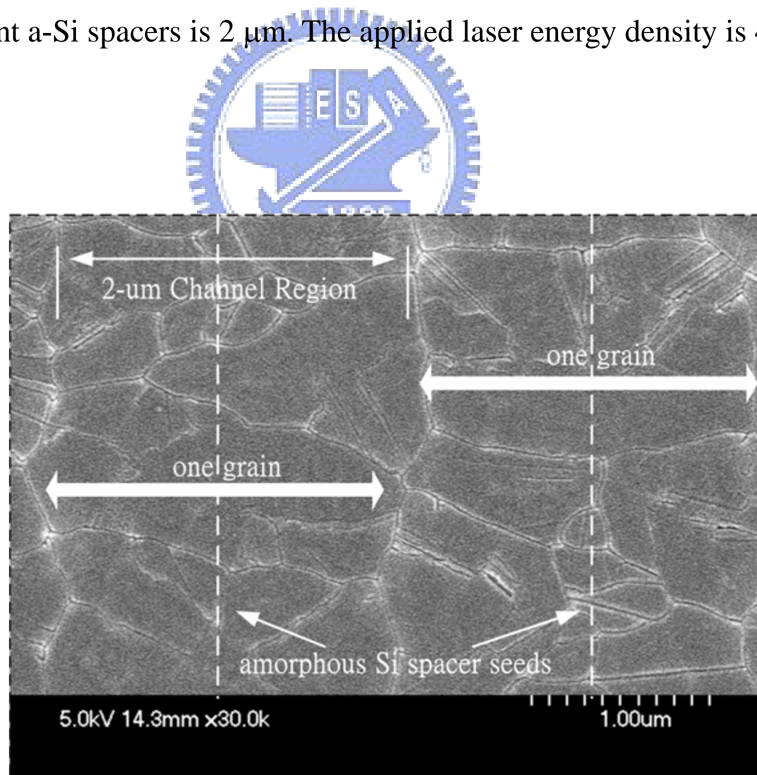

Figure 5.10(d). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 485 mJ/cm^2.

The influence of the a-Si spacer height on the eventual grain structure in the crystallized poly-Si thin film was also demonstrated. Figure 5.11(a) ~ 5.11(b) show the SEM graphs of the crystallized poly-Si thin film where the thick a-Si spacer region is 2000Å and a-Si in the thin region is 1000Å. In this case, the laser energy densities are 510, 535, 560, and 585, respectively, which are all controlled to fully melt the 1000Å thin region but partially melt the 2000Å a-Si spacer region. The substrate temperature is also maintained at 400°C during laser irradiation. Although longitudinal lateral grain growth can be observed as well, fine and small grains are formed in the crystallized poly-Si thin film. The number of the small grain becomes decrease as the applied laser fluence increases. The existence of the small grains in the crystallized poly-Si thin film may be attributed to the vertically grain growth stating from the partially-melted a-Si spacer seed.

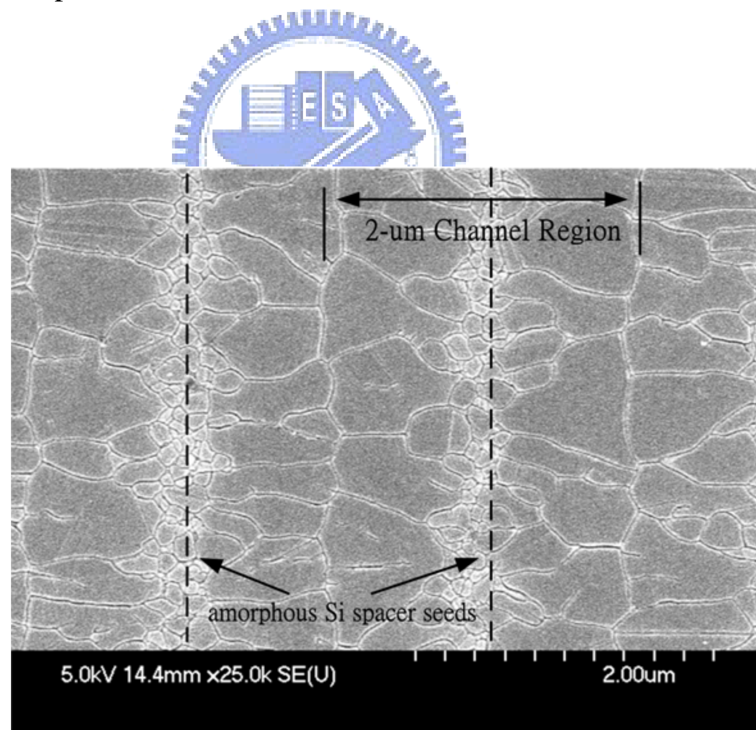

Figure 5.11(a). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 510 mJ/cm^2.

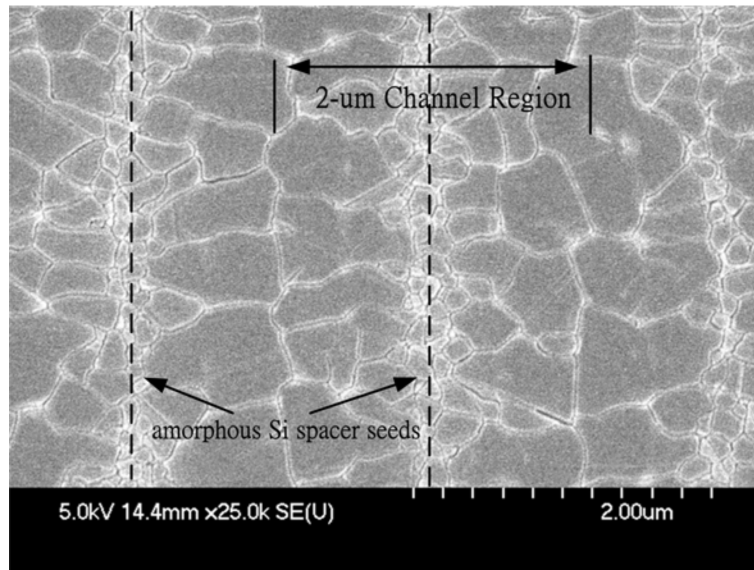

Figure 5.11(b). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 535 mJ/cm^2.

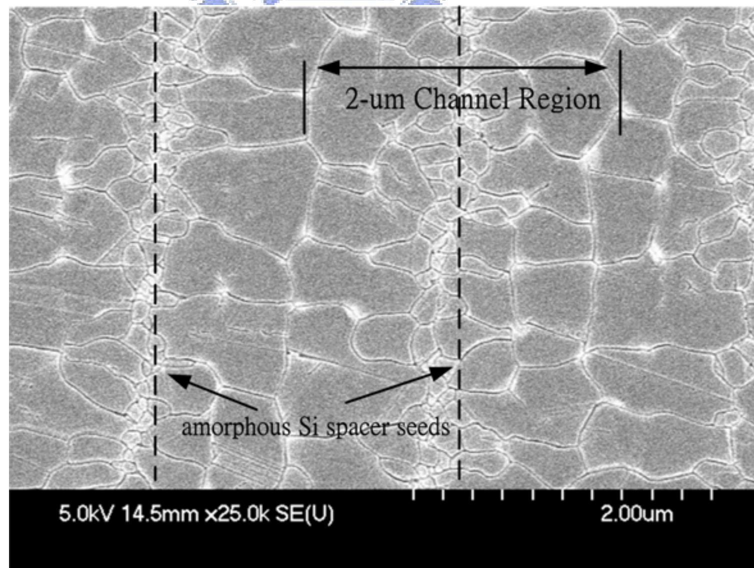

Figure 5.11(c). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 560 mJ/cm^2.

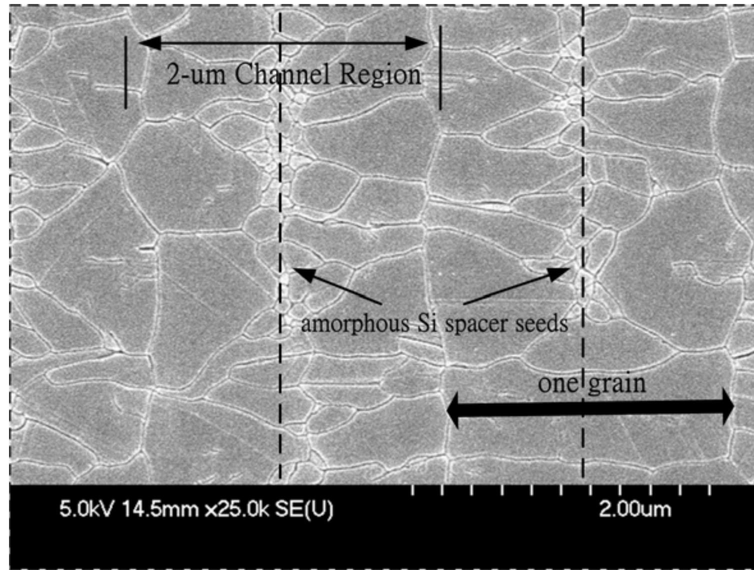

Figure 5.11(d). SEM graph of the crystallized poly-Si thin film. in which the length of the adjacent a-Si spacers is 2 μm. The applied laser energy density is 585 mJ/cm^2.

In chapter 2, it has been discussed that the grain growth in the partially melting regime is characterized by a combination of explosive crystallization, vertical solidification and competitive occlusion of grains. Fine and small grains are acquired in this regime and typical grain sizes on the order of up to twice the film thickness can be achieved. In this case, owing to the insufficient laser fluence and high absorption coefficient of a-Si at 248 nm, the maximum melting depth of the a-Si thin film under laser irradiation is about 1500Å. As a result, there is still retained solid a-Si with a thickness of at least 500Å at the spacer region. Due to the large height of retained solid a-Si, the vertical temperature gradient at the spacer region becomes more apparent. An obvious vertical grain growth will take place at the a-Si spacer region, which results in fine and small grains. This does not appear in the case of 1500Å-thick a-Si spacer because the great part of a-Si at the spacer region can be melted and form nucleation seeds with a tiny height during laser irradiation. Thus, the vertical grain growth is unobvious instead of a lateral grain growth.