Chapter 6

Summary and Conclusions

In this thesis, high-performance low-temperature polycrystalline silicon thin film transistors (LTPS TFTs) have been fabricated according to the viewpoints of channel material or grain re-growth method. Excimer laser crystallization was adopted as the main crystallization technique in this work. The conventional LTPS TFTs produced by excimer laser crystallization have been studied in detail, especially for short-channel devices. The long-term reliability of low-temperature gate oxide has also been investigated. Improvement of the device performance and/or uniformity has been achieved by incorporating of Ge atoms in the channel layer or controlling the location and structure of the poly-Si grains in the active region.

In the chapter 2, conventional LTPS TFTs fabricated by excimer laser crystallization has been investigated in detail. From the material and electrical characteristics analyses, it has been obviously found that the applied laser energy density has a great influence on the performance of LTPS TFTs. Narrow process window and poor device uniformity could be easily observed in LTPS TFTs fabricated with different laser irradiation conditions. The variation of device performance became more and more apparent when the device geometry shrunk. Increase the substrate temperature could enlarge the process window and improve the device uniformity of LTPS TFTs.

High quality low-temperature deposited TEOS oxide thin films have been formed by using large-area plasma enhanced chemical deposition (LA-PECVD) system. Different

short-time plasma treatments, such as O_2, N_2O, and NH_3, were applied to investigate the effects of plasma treatments on the electrical properties and long-term reliability of gate oxide. It was shown that the electrical strength of oxide was improved after N_2O and NH_3 plasma treatments. In addition, NH_3 plasma treatment exhibited the highest enhancement efficiency. O_2 plasma treatment, however, showed some harmful effects on the electrical properties of the TEOS oxide. On the other hand, samples with N_2O plasma treatment showed superior stress endurance under the long-term reliability testing. As a consequence, N_2O plasma treatment might seem to be the best choice to manufacture high quality TEOS oxide films for low-temperature poly-Si TFTs with better long-term stability.

In the chapter 3, the deposition parameters and mechanisms of a-$Si_{1-x}Ge_x$ thin film by low-pressure chemical vapor deposition (LPCVD) have been investigated. To overcome the nucleation problem of the deposition of a-$Si_{1-x}Ge_x$ thin film on SiO_2, a thin seed Si layer must be pre-deposited on SiO_2 surface by exposing the SiO_2 to SiH_4 gas for a short time. A-$Si_{1-x}Ge_x$ alloy demonstrated a lower deposition temperature compared to a-Si thin film. The deposition rate was enhanced as the Ge atomic concentration in the a-$Si_{1-x}Ge_x$ thin film increases, which can be attributed to GeH_4 acted as a catalyst to enhance hydrogen desorption from the film surface. In addition, under a fixed gas flow ratio, the Ge atomic fraction in the $Si_{1-x}Ge_x$ thin film increased as the deposition temperature decreased.

The mechanisms of excimer laser crystallization of LPCVD a-$Si_{1-x}Ge_x$ thin film were also investigated. The effects of Ge atomic concentration and laser irradiation conditions for the ELC poly-$Si_{1-x}Ge_x$ thin films have also been demonstrated. Several material analysis characterization results indicated that a-$Si_{1-x}Ge_x$ thin film could be effectively crystallized by excimer laser irradiation. However, compare to the ELC poly-Si thin film, the ELC poly-$Si_{1-x}Ge_x$ thin film exhibited poor crystallinity. Furthermore, Ge segregation at the grain boundary and film surface occurs in the ELC poly-$Si_{1-x}Ge_x$ thin film. The most possible reason responsible for the Ge segregation was the difference in melting point of these two

atoms, Si and Ge.

Low-temperature poly-$Si_{1-x}Ge_x$ TFTs have been fabricated by excimer laser crystallization. In comparison with the ELC poly-Si TFTs, the ELC poly-$Si_{1-x}Ge_x$ TFTs exhibited higher leakage current, larger threshold voltage, lower carrier mobility, and inferior subthreshold swing. It could be attributed to the worse crystallinity of the ELC poly-$Si_{1-x}Ge_x$ thin film, which resulting from the different thermal properties of Si and Ge.. On the other hand, the segregation of Ge atoms at the grain boundaries and thin film surfaces during ELC was also responsible for the degradation of device performance.

The ELC poly-$Si_{1-x}Ge_x$ TFTs exhibited higher off-state current even though the carrier field–effect mobility was lower. The leakage current was exponentially dependent on the potential barrier height at the drain junction, which was related to the height of bandgap of the active layer. Reduce the energy bandgap of the active layer, which resulting from the adding of Ge atoms in Si, would increase the probability of carrier tunneling through the drain energy barrier to the channel region, leading to high leakage current. In addition, another possible reason responsible for the higher leakage might be the inferior crystallinity of the poly-$Si_{1-x}Ge_x$ thin film.

In the chapter 4, two types of low temperature ELC poly-$Si_{1-x}Ge_x$ TFTs using novel laser and deposition processes were demonstrated. For the ELC poly-$Si_{1-x}Ge_x$ TFTs with a Si capping layer, the poly-$Si_{1-x}Ge_x$ thin film was formed by laser irradiation of a-Si/ poly-$Si_{1-x}Ge_x$ double layer structure. This structure could effectively alleviate the Ge segregation at the film surface during excimer laser irradiation. Due to the reduction of the surface Ge segregation, better device performances were exhibited for the Si-capped ELC poly-$Si_{1-x}Ge_x$ TFTs in comparison with the direct-ELC poly-$Si_{1-x}Ge_x$ TFTs. However, the intrinsic material properties of the ELC poly-$Si_{1-x}Ge_x$ thin films, such as narrow energy bandgap, small grain size, and poor crystallinity, lead to an inferior device performance compared with ELC poly-Si TFTs.

For the Ge-doped poly-$Si_{1-x}Ge_x$ TFT, the poly-$Si_{1-x}Ge_x$ thin films was fabricated by laser irradiation of a-$Si_{1-x}Ge_x$/poly-Si double layer. In view of excellent crystallinity and large grain size, a-Si film was adopted as the underneath starting active layer. During the second laser irradiation, the Ge atoms would diffuse into the underneath poly-Si layer due to the high diffusion coefficient of Ge in melting silicon and the Ge concentration gradient. Then, the solidification process began from the unmelted poly-Si seed layer, yielding epitaxial growth upward to the surface. Therefore, the grain size was almost unchanged after the second laser irradiation. On the other hand, owing to that the grains could vertically re-grow with a high vertical re-growth rate from the unmelted poly-Si, the Ge segregation could be improved remarkably.

Two competing mechanisms, i.e. the defect states induced by Ge segregated at grain boundary and the carrier mobility enhancement by Ge atoms incorporation, were proposed to explain the electrical characteristics of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs with different device dimension. For large device dimension, grain boundaries dominated the carrier transport in the channel, leading to the degradation in device performance. However, when the device dimension was shrunk, carriers suffered from less defect scattering at grain boundaries in the channel region. The carrier mobility of the Ge doped ELC poly-$Si_{1-x}Ge_x$ TFTs was greatly improved due to carrier mobility enhancement effect contributed by Ge atoms. It was inferred that the degree of mobility enhancement by Ge incorporation was beyond that of mobility degradation by defect traps generation when TFT size was reduced to 2μm/2μm. The novel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs exhibited excellent electrical performance in short channel devices that would meet the requirements for the trends of low-temperature polycrystalline TFTs technology developments.

In the chapter 5, high-performance poly-Si TFTs with field-effect mobility exceeding 300 cm^2/V-s have been fabricated with a-Si spacer structure. The poly-Si TFTs with a-Si spacer structure exhibited better electrical characteristics than the conventional ones owing to

the artificially controlled lateral grain growth. Large longitudinal grains were artificially grown measuring about 2.5 μm. Furthermore, the lateral growth starting from the a-Si spacer seed could progress along the opposite direction. Hence, when the channel region was designed to arrange at the spacer region, the grain boundaries perpendicular to the current flow in the channel region could be reduced. In addition to the enhancement of TFT performance, TFTs crystallized with a-Si spacer structure also demonstrated excellent uniformity due to the wide laser process window. This crystallization technique could be also applied to the large-dimension devices because periodic grain growth could be produced in the channel region. Better electrical performances were observed for the poly-Si TFTs crystallized with a-Si spacer structure under W = L = 10 μm and 20 μm design rules. Consequently, this spacer-seeded poly-Si TFTs could be considered for future system-on-panel (SOP) applications.