Chapter 7

Future Prospects

There are some important topics that are valuable for further research about the LTPS TFTs:

In the part of LTPS TFTs device fabrication process:

(a) As described in the chapter 2, short channel effect becomes a serious problem in future LTPS TFTs applications. On of the solution to suppress the short channel effect is to scale down the thickness of gate dielectric. As the thickness of gate oxide is scaled down with device dimension, the quality of deposited oxide can hardly meet the requirements for the insulator. Thus, several approaches have been proposed to produce high-quality thin gate dielectric at low temperature, such as high-density plasma (HDP) oxidation. Although the HDP technique has be studied for several years, further detail researches should be focused on the oxidation mechanism and large-area plasma oxidation with excellent uniformity.

(b) Although excimer laser has been widely used for crystallization of a-Si thin film in the mass production of LTPS TFTs, the poly-Si thin film crystallized by excimer laser annealing has to date suffered from a hard to control random structure. In general, the more grain boundaries there are in the active region, the poor the device performance. Therefore, it is important to control as much as possible the size of the grains, the number of grains and their locations. In this thesis, a novel one-dimensional location-controlled grain growth technique has been proposed to improve the device characteristics and uniformity. The two-dimensional grain controlling process must be developed to further enhance the device performance and

uniformity, especially when the device dimension is comparable with the grain size of the poly-Si thin film.

(c) It is indicated that as the performance of poly-Si TFTs approaches to that of silicon-on-insulator (SOI) MOSFETs, power dissipation in the devices is increased, and therefore, self-heating effect becomes serious because of small thermal conductance of the insulating substrate. The lack of saturation in drain current will be observed when the self-heating effect becomes apparent. Furthermore, self-heating is more significant as the channel length is reduced since the drain current increases. Thus, the self-heating effect may be a problem especially for small-dimension poly-Si TFTs. The approach used to dissipate the heat generating during the device operation must be proposed in the future LTPS TFTs fabrication.

(d) Leakage current is a problem in LTPS TFTs due to presence of grain boundaries in the channel. When the device is off, there are large high electric fields between the drain and the gate edge. When there are grain boundaries in this high field region, high leakage current occurs via field emission through gap states in the grain boundary. Leakage current has been reduced at the expense of process complexity or loss of aperture ratio. A process which minimizes leakage current while minimizing additional process step and maintaining high aperture ratios is desired.

In the part of LTPS TFTs circuit integration:

(a) Poor transistor uniformity is a serious problem for the fully integration of drivers with LTPS TFTs. The LTPS TFTs uniformity is primarily a function of the laser annealing process stability. In order to achieve tight uniformity, laser energy stability must be very accurate. When the uniformity exceeds the design margins, the pixel as well as the peripheral driver circuits will not work correctly. Compensating for the non-uniformity by some novel designs has been attractive in this case.

(b) The inherent low mobility and high threshold voltages of LTPS TFTs over single

crystal silicon pose a power consumption problem. In order to combat these effects, new driver architectures with low power consumption must be proposed.

(c) Perhaps the most serious constraint to the use of integrated drivers is the yield of the denser and larger number of devices. Pixel TFTs are designed to maximize the aperture ratios and are limited in density to the space available within each single pixel. The peripheral circuits are designed to minimize the space and will be densely packed. The additional process steps inherent in LTPS TFT fabrication and the additional mask steps to produce the CMOS driver circuits will also affect the yield.