以準分子雷射結晶法製作高載子移動率

低溫複晶矽與矽鍺薄膜電晶體之研究

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摘要

在本篇論文中，我們以準分子雷射結晶法為基礎，探討準分子雷射結晶法對於低溫複晶矽薄膜電晶體電特性與均勻性的影響，並依據元件通道材料以及結晶結構兩個主題，分別提出改善的方法與技術，進一步的提升低溫複晶矽薄膜電晶體之電特性。此外我們也利用短時間電漿處理法，以期改善低溫閘極氧化層之電特性與可靠度。

首先，我們以準分子雷射結晶法製作低溫複晶矽薄膜電晶體，探討各項雷射製程參數對於元件電特性的影響。根據材料分析的結果，我們發現複晶矽薄膜的晶粒大小及結晶性與雷射能量密度有很大的關連性，只有在某一個很狹小的雷射能量範圍內才能夠得到最大的晶粒。而在此能量範圍內，由於雷射本身的不穩定性，造成晶粒大小的分佈相當不均勻，這也同時導致低溫複晶矽薄膜電晶體之電特性變異性很大，尤其是當元件尺寸微縮至接近晶粒大小的時候，此變異程度更為明顯。在雷射結晶時，適當的提升基板溫度可以有效的降低元件電特性的變異程度。此外，相較於其他結晶技術，準分子雷射結晶法雖然可以得到較佳的薄膜結晶性，但是卻會導致較大的表面粗糙度。這使得當元件尺寸微縮時，為了避免閘極漏電流過大，閘極氧化層的厚度無法隨之縮小，間接地降低元件的驅動能力。因此我們利用短時間的電漿處理法，期待改善薄閘極氧化層的電特

性與可靠度。由實驗的結果發現，以氨氣電漿處理後，閘極氧化層的電特性與可靠度均可以有效的提升。

為了進一步的提升複晶矽薄膜電晶體的驅動能力，我們首先從元件通道材料進行改善。相較於複晶矽薄膜，複晶矽鍺擁有相當高的載子移動率，因此在此論文中我們以複晶矽鍺薄膜做為電晶體主動區的材料。首先我們針對非晶矽鍺薄膜的沉積及以準分子雷射結晶法製作之複晶矽鍺薄膜做深入的探討。由於鍺原子在氧化層薄膜上的成核能力較弱，因此在沈積非晶矽鍺薄膜前，必須將氧化層基板暴露於純矽甲烷氣體中，在其上形成一層薄的非晶矽薄膜，以利於後續之非晶矽鍺薄膜沉積。此外，實驗結果發現，由於鍺原子具有催化的效應，故相較於非晶矽薄膜沉積，利用低壓化學氣相沉積法可於較低的溫度下沉積非晶矽鍺薄膜，且沉積速度隨著隨著鍺甲烷的氣流增加而增加。

根據材料分析的結果顯示，準分子雷射結晶法可有效將非晶矽鍺薄膜轉變成複晶矽鍺薄膜。然而，由於矽跟鍺兩種元素熔點上的差異，在利用準分子雷射結晶的同時，我們會在薄膜表面以及晶粒邊界觀察到很嚴重的鍺偏析現象。此外，相較於傳統利用準分子雷射結晶法所製備的複晶矽薄膜，複晶矽鍺薄膜經準分子雷射結晶後呈現較差的結晶性。因此，利用準分子雷射直接對非晶矽鍺薄膜進行再結晶時，由於製程上所引起的問題 (如:鍺偏析，結晶性差..等)，會導致薄膜電晶體元件有較差的電特性。

為了改善鍺偏析以及結晶性較差的問題，我們提出兩種新型的製程方法來製備高效能的複晶矽鍺薄膜電晶體。在第一種方法中，我們先對非晶矽鍺薄膜進行第一次準分子雷射結晶，而後在其上沉積第二層非晶矽薄膜，接著再進行第二次準分子雷射再結晶。如此一來，下層的鍺原子在第二次雷射結晶時，可以擴散至上層的矽薄膜中形成矽鍺薄膜。而由於第二次雷射結晶時的照射次數少且固化速度較快，可以有效的改善鍺偏析的情形，進而改善元件的特性。然而，受限於複晶矽鍺的本身較差的結晶性，元件的電特性表現仍然不符合需求。

因此，我們進一步提出第二種製程方式來改善上述的缺點。我們將第一個製程方法中的薄膜位置互相調換，此時上層非晶矽鍺薄膜中的鍺原子可以在第二次雷射結晶時向下擴散至複晶矽薄膜中，同時由於複晶矽薄膜擁有較佳的結晶性，因此結晶性與鍺偏析

的問題均可以獲得有效的改善。利用準分子雷射摻雜鍺之複晶矽鍺薄膜電晶體於小尺寸元件上呈現出相當優秀的元件特性。而相較於利用準分子雷射製備的複晶矽薄膜電晶體，利用準分子雷射摻雜鍺之複晶矽鍺薄膜電晶體於載子移動率及驅動電流上分別提升了 41%及 52%。

雖然利用鍺摻雜技術可以有效的提升複晶矽薄膜電晶體的載子移動率，但是對於元件的均勻性卻沒有辦法改善。因此我們提出了一個新穎的側向結晶方式，在想要的區域上控制晶粒的橫向成長，如此一來，除了可以提高元件之載子移動率外，還可以進一步的改善元件的變異性。此一結構為利用傳統間隙壁製程，在局部微小區域產生兩種厚度不同的非晶矽薄膜，當準分子雷射照射在此一結構上使較薄的區域完全熔融時，晶粒便會以這些非晶矽間隙壁為結晶起始點，做橫向成長。由實驗的結果發現，當我們適當的選擇間隙壁的高度，可以形成 2.5 μm長之長型晶粒。此外，由於在此結晶方法中，間隙壁是作為結晶的起始點，因此適當的安排間隙壁與元件通道的相關位置，我們將可以在通道中除去所有垂直於電流方向的晶粒邊界，更進一步的改善元件的驅動能力。以通道長度為 2 μm的元件為例，以此結晶方法做出的元件其載子移動率可以到達 280 $cm^2/V\text{-}s$，而傳統的元件只有 128 $cm^2/V\text{-}s$.

此間隙壁結晶法除了能形成單一的橫向晶粒外，由於其晶粒成核點的尺寸很小，故當我們適當的調整相鄰間隙壁的位置，還可以形成週期性的長型橫向晶粒排列。因此，除了可以應用於小尺寸的元件外，大尺寸的複晶矽薄膜電晶體也可以使用此種結晶方式來提升其驅動能力，如此一來，此結晶技術將非常適用於未來 system-on-panel (SOP)的應用上。

Study on High-Mobility Low-Temperature Polycrystalline Silicon and Silicon-Germanium Thin Film Transistors Fabricated by Excimer Laser Crystallization

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ABSTRACT

In this thesis, based on the excimer laser crystallization (ELC) technique, the influences of laser crystallization parameters on the electrical characteristics and uniformity of the low-temperature polycrystalline silicon thin film transistors (LTPS TFTs) have been investigated. From the two perspectives of channel material and crystallization structure, several approaches have been proposed to further enhance the performance of LTPS TFTs respectively. In addition, the electrical characteristic and long-term reliability of the low-temperature gate oxide have been also improved by using short-time plasma treatments.

First, LTPS TFTs have been fabricated with excimer laser crystallization and the effects of several laser process parameters on the device electrical characteristics are investigated in detail. According to the material analysis results, it is observed that the resulted grain size and crystallinity of the ELC poly-Si thin film are greatly related to the applied laser energy

density. Large grains can only be produced in a narrow laser process window. Meanwhile, in this narrow laser density window, the non-uniform distribution of grain size can be easily found due to the instability of the excimer laser itself. This leads to a large variation in the electrical characteristics of ELC LTPS TFTs, especially when the device dimension is comparable with the grain size of the poly-Si thin film. In addition, although better crystallinity can be produced with ELC, the surface roughness of the ELC poly-Si thin film is more apparent compared to those crystallized with other techniques. The enormous surface roughness makes the thickness of gate oxide unable to decrease with the device dimension. The thicker gate oxide directly reduces the driving ability of the LTPS TFTs. Thus, in this work, short-time plasma treatment is adopted to improve the electrical characteristics and reliability of the thin gate oxide. From the experimental results, the electrical characteristics and reliability of thin gate oxide can be ameliorated effectively after short-time NH_3 plasma treatment.

In order to further enhance the driving ability of the LTPS TFTs, another material is tried to replace the poly-Si thin film in the channel layer. At present, polycrystalline silicon-germanium (poly-$Si_{1-x}Ge_x$) is an excellent candidate as an alternative to poly-Si for the channel active layer due to the high carrier mobility of Ge atom. Thus, poly-$Si_{1-x}Ge_x$ thin film is adopted as the device channel material in this work. The mechanism of amorphous $Si_{1-x}Ge_x$ (a-$Si_{1-x}Ge_x$) thin film deposition and excimer laser crystallization of a-$Si_{1-x}Ge_x$ thin films are investigated in detail. To overcome the nucleation problem of the deposition of a-$Si_{1-x}Ge_x$ thin film on SiO_2, a thin seed Si layer is pre-deposited on SiO_2 surface by exposing the SiO_2 substrate to SiH_4 precursor for a short time. The thin Si film deposition (Si flash technique) on oxide is intended to provide adequate nucleation sites on the oxide surface for subsequent growth of a-$Si_{1-x}Ge_x$ thin film. Besides, the experimental results demonstrate that a-$Si_{1-x}Ge_x$ thin films can be deposited at lower temperature by low-pressure chemical vapor deposition (LPCVD) than a-Si thin films owing to the better catalytic effect of Ge atoms. As

the GeH_4 to SiH_4 gas flow ratio increases, the deposition rate of a-$Si_{1-x}Ge_x$ thin films is enhanced.

According to the material analysis results, a-$Si_{1-x}Ge_x$ thin film can be effectively converted to polycrystalline phase after excimer laser irradiation. However, due to the difference in the melting point of Si and Ge atoms, Ge segregation occurs seriously at film surface and grain boundary during ELC process. Furthermore, ELC poly-$Si_{1-x}Ge_x$ thin films exhibit worse crystallinity in comparison with ELC poly-Si counterparts. As the result, TFTs fabricated by direct laser crystallization of a-$Si_{1-x}Ge_x$ thin film will reveal a degraded performance because of these process related issues, such as worse crystallinity and Ge segregation.

In order to improve the problems of Ge segregation and worse crystallinity, two novel modified processes are proposed to fabrication high-performance poly-$Si_{1-x}Ge_x$ TFTs. In the first approach, a-$Si_{1-x}Ge_x$ thin film of a 500Å thickness is deposited on oxidized silicon wafer and subjected to the first ELC process. After the first laser irradiation, another 500Å-thick a-Si thin film is deposited on top of the ELC poly-$Si_{1-x}Ge_x$ thin film. Next, the second excimer laser irradiation is performed to crystallize the upper a-Si thin film. The Ge atoms diffuse upward into the Si layer during laser irradiation and naturally formed poly-$Si_{1-x}Ge_x$ thin film in the end. Because of the less shot numbers and rapid vertical solidification velocity during the second ELC, the Ge segregation can be suppressed effectively. Although the device performances are improved by introducing a Si capping layer, the worse crystallinity of ELC poly-$Si_{1-x}Ge_x$ active layer still limit the electrical properties of the devices.

Thus, the second modified process is provided to solve the problem of worse crystallinity while still suppress the Ge segregation. In this method, a-Si thin film is used as the starting layer and exposed to the first excimer laser irradiation, in which the laser

parameters are optimized. Next, a thin $Si_{1-x}Ge_x$ layer is deposited on the poly-Si thin film and subjected to the second laser irradiation. The Ge atoms diffuse downward into the poly-Si layer during the second laser crystallization and naturally form poly-$Si_{1-x}Ge_x$ thin film in the end. Because of the better crystallinty of ELC poly-Si thin film, the two issues of crystallinity and Ge segregation for ELC poly-$Si_{1-x}Ge_x$ thin film can be entirely improved. Since the good crystallinity and carrier mobility enhancement by Ge incorporation, Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs exhibit excellent carrier mobility and high driving current in short channel devices. The mobility and drain current of the Ge-doped ELC poly-$Si_{0.91}Ge_{0.09}$ TFTs with W / L = 2 μm / 2μm areenhanced by 41% and 52% than those of the conventional ELC poly-Si counterparts.

Although the field-effect mobility of poly-Si TFTs can be effectively enhanced by incorporation of Ge atoms in the channel region, the uniformity of device performance is still an unsolved problem. A novel lateral crystallization method, in which the large and uniform longitudinal grains can be artificially produced in the desired local region, is proposed to improve the carrier mobility as well as the device uniformity. In this method, a-Si thin film with two kinds of thicknesses in a local region is fabricated by using conventional spacer process. As a proper laser fluence is applied on the a-Si thin film, in which the thin part of a-Si is completely melted, the grains will grow laterally from the un-melting a-Si spacer seeds in the thick part of the a-Si towards the thin region where the Si is completely melted. From the SEM analysis, large longitudinal grains about 2.5 μm long can be acquired when the thickness of a-Si spacer is suitably adjusted. On the other hand, the lateral grain growth starting from the a-Si spacer seed can progress along the opposite direction. Hence, when the channel region is designed to arrange at the spacer region, the boundary perpendicular to the current flow in the channel region is reduced, which further enhance the driving ability of TFT devices. Take the dimension of W = L = 2 μm for example, poly-Si TFT with field effect mobility of about 288 cm^2/V-s can be achieved by using this a-Si spacer method while the

mobility of the conventional counterpart is about 128 cm^2/V-s.

Except for producing single longitudinal grain in the channel region, periodic lateral longitudinal grains can also be fabricated with the a-Si spacer structure. Owing to the tiny width of the a-Si spacer (< 1000Å), the a-Si spacers, i.e. the nucleation seeds, can be arranged periodically inside the channel region. Consequently, under suitable spacer distance and ELC conditions, periodic lateral grain growth can be acquired at the channel region of large-dimension device. This helps to improve the driving ability of the large dimension TFTs. Thus, the proposed crystallization technique become useful in the field of system on panel (SOP) because the circuits on a single panel need varied sizes of TFT devices for different applications.