Chapter 1

Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon thin-Film Transistors (LTPS TFTs) Technology

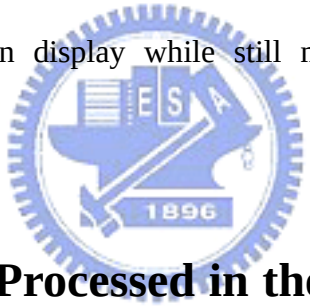
During the last decade, Si–based thin film transistors (TFTs) have been used very successfully for display applications, including flat panel liquid crystal displays (LCDs) [1.1], liquid crystal light valves for projectors [1.2], and organic electro-luminescent displays [1.3]. Currently, in large size active matrix liquid crystal displays (AMLCDs), the pixel switching element are TFTs fabricated in amorphous silicon (a-Si) while the peripheral driving circuitry, for which the very small a-Si TFT mobility is inadequate, is fabricated on single crystal silicon. On the other hand, low-temperature polycrystalline silicon (LTPS) TFTs have been widely studied because of their potential applications in high-performance displays, such as AMLCDs [1.4]-[1.10] and active matrix organic light emitting displays (AMOLEDs) [1.11]-[1.17], and potential for 3-dimension IC's applications [1.18]. Compared to conventional a-Si TFTs, the primary reason for the potential cost and performance advantage of LTPS TFTs is superior mobility performance [1.19]. This fact allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry onto a single glass substrate, thus substantially reducing manufacturing complexity and cost [1.20]. Such panels propose to have all the functions required for display operation. Numerous

display manufacturers now believe that LTPS TFTs will offer a performance and cost advantage over a-Si TFT LCDs at certain panel sizes and pixel formats and a performance advantage only at other display sizes and pixel formats. Therefore, there is great interest in improving the performance of LTPS TFTs.

In order to conform to the requirements imposed by the integrated fabrication of the entire display circuitry (i.e., display drivers and active matrix elements), the poly-Si TFT performance must be optimized, particularly with regard to enhancement of the carrier mobility and reduction of the leakage current. TFT mobility is enhanced by a factor in excess of 100 by switching from amorphous to poly silicon channels [1.21]. Electron and hole mobilities are key parameters in determining the effective conductivity and size of a device. While a-Si TFTs mobilities range from 0.3~1.0 cm^2/V-s, LTPS TFTs mobilities range from 10~500cm^2/V-s. For display applications, many advantages as listed below can be acquired by using high-mobility LTPS TFTs.

- **Reduce the size of the TFT and increase aperture ratios resulting in higher brightness and/or lower power** [1.22]. The higher field-effect mobility allows smaller TFTs to be used as the pixel switching element, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance.
- **Reduce material costs by enabling the integration of driver ICs** [1.23]. Driver ICs account for 11% of the total costs of a 12.1” VGA display for notebook applications and as much as 18% of the total costs for 5” displays for consumer applications. By integrating the driver circuitry, the cost of driver ICs can be saved.
- **Enable the possibility of a complete system on panel (SOP) which could generate a number of innovative new products and markets** [1.24]. LTPS TFT producers could integrate a number of additional circuit types including the panel ASIC, EMI condenser, memory, sound chips, photodiodes, sensors, temperature compensation, distributed processors, etc.

- **Decrease the display module weight and thickness.** Driver integration not only eliminates the weight and thickness of the driver ICs, but also their TAB packages and the PCB they are mounted on.
- **Increase panel reliability** [1.23]. With TAB connection failures accounting for 60% of all notebook returns, eliminating TAB should result in significantly lower returns which should lower support costs.
- **Improve time to market.** By integrating the driver ICs, the time to market will be reduced.
- **Enable panels with higher pixel density resulting in increased information content, reduced jaggies and improved legibility.** The smaller transistors and reduced TFT "on" resistance result in a reduced resistance-capacitance (RC) delay which allows more pixels to be squeezed onto a given display while still meeting settling time, power and brightness requirement.



1.2 Overview of Key Processed in the Fabrication of LTPS TFT

One of the merits of LTPS TFTs compared to high temperature poly-Si (HTPS) TFTs is that it can be processed at temperature low enough to utilize low cost, large area glass substrate rather than area-limited, expensive quartz substrates which requires process temperatures of 900°C. Historically, LTPS TFT array processing has been carried out at temperatures as high as 600°C. Although this is below the strain point of non-alkali glass, processing at over 500°C has required the glass to be pre-annealed to maintain thermal stability at the higher temperatures. Pre-annealing improves thermal stability performance by increasing internal viscosity which results in reduced sag and shrinkage. However,

pre-annealed substrates are twice as expensive as un-annealed ones. Although glass costs are a small portion of total display costs, LTPS manufacturers are looking to minimize glass costs by keeping process temperatures below 450°C. Therefore, there are a number of unique processes to mass produce LTPS TFTs when compared to HTPS TFTs and a-Si TFTs. These include the:

- Deposition of the buffer layer, precursor a-Si, gate dielectric and ILD.
- Crystallization of the a-Si thin films.
- Ion doping to form the source/drain.
- Activation of the dopants.
- Hydrogenation to passivate and repair deep and tail states formed at dangling bonds between and within grain boundaries.
- Array test to measure the integrity of pixels and integrated driver circuits.
- Photolithography equipment to pattern the various films at finer resolutions.

Basically, all the processes in the fabrication of LTPS TFTs would affect the eventual TFT performance. Nevertheless, the LTPS TFT characteristics are profoundly affected by three unique processes mentioned above. They include crystallization of a-Si thin films, low-temperature deposition of gate dielectric, and activation of dopants.

1.2.1 Crystallization of Amorphous Silicon Thin Films

Because crystallization plays a dominant role in determining mobility and uniformity of the polysilicon material, a robust crystallization process is required for LTPS TFTs to become a mainstream technology. In polycrystalline material, grain boundaries cause trap and tail states which exert a negative influence on nearly all aspects of device performance including an increase in Vth, a decrease in subthreshold slope, a decrease in mobility, an increase in

leakage current, and poor device stability [1.25]. The origin of the trapping states at the grain boundaries is though to be associated with the presence of dangling and strained bounds [1.26]. In general, the more grain boundaries there are in active-channel region, the poorer the device performance. Reduction of defect density in polycrystalline material will make it approach the quality of single-crystalline material, which will lead to better performance of polycrystalline device. Therefore, it is important to control as mush as possible the size of the grains, the number of the grains, and the location of the grains.

Poly-Si thin films can be directly deposited on glass substrate by low-pressure chemical vapor deposition (LPCVD) [1.27] and electron cyclotron resonance chemical vapor deposition (ECRCVD). However, due to the high deposition temperature (approximately 625°C) and the poor crystallinity of the as-deposited poly-Si thin film, the direct deposition method has been excluded in the fabrication of LTPS TFTs.

Several crystallization technologies for fabricating high quality poly-Si thin films have been widely studies. In general, we can classify the crystallization technique of poly-Si thin films simply into two groups: solid phase crystallization and liquid phase crystallization. In the solid phase crystallization, nucleation and grain growth are driven by thermal annealing [1.29]. It usually takes a long time to anneal a-Si thin film at low temperature. On the other hand, several kinds of laser equipments are adopted to crystallize the a-Si thin film [1.30]-[1.35]. During laser irradiation, the a-Si thin films are heated to the melting point and intermediately quench to the ambient temperature. Critical parameters for crystallization include grain size, grain size uniformity, number and location of the grains, laser energy stability, process temperature, resulting film thickness uniformity, throughput, and mobility.

In the follow sections, several widely-used recrystallization methods are briefly reviewed. They include solid phase crystallization (SPC), metal-induced crystallization (MIC), and laser crystallization.

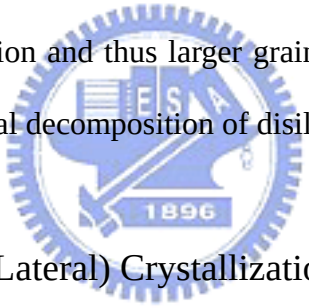
1.2.1.1 Solid Phase Crystallization

1.2.1.1.1 Solid Phase Crystal of Pure Amorphous Silicon

Solid phase crystallization (SPC) of a-Si is a simple and effective method to acquire poly-Si thin film with large grains [1.36]. In the SPC furnace annealing, the a-Si film is annealed in a furnace for as long as 24 hours at temperatures as high as 600°C. SPC of a-Si thin films involves two distinct processes, namely the nucleation of seeds (formation of clusters of crystalline silicon) and their growth to polycrystalline films [1.37]. The transformation in the a-Si annealing proceeds after an apparent incubation period via nucleation and dendritic-like growth of crystal domain within the amorphous matrix [1.38]. The nucleations of the crystals likely occur through the thermal reaction of crystal clusters. The rate-limiting step of the crystallization process is the rate of nucleation of seeds, which has an activation energy of about 5 eV [1.38]. The rate of the crystal growth has an activation energy of about 2.7 eV [1.38], [1.39].

Final grain size is known to be large when the nucleation rate is low and the grain growth rate is high [1.38]. Many alternatives to enlarge grain size of the annealed poly-Si thin film are to modify the structure disorder of the starting a-Si or poly-Si thin film. Previous studies indicated that the grain size was enlarged up to a few micrometers by means of solid-state crystallization of a-Si produced by self-ion bombarded polycrystalline or amorphous films deposited by LPCVD. It is possible that ion-bombardment amorphizes the embryo of crystallines which pre-exist at the interface of the as-deposited amorphous thin films so that the incubation period of nucleation is lengthened [1.40]-[1.42]. On the other hand, it has also been reported that the grain size of the recrystallized films formed from disilane (Si_2H_6) is larger than that formed from silane (SiH_4) [1.43]-[1.46]. The average grain size of the poly-Si thin film resulting from the crystallization of a film deposited in the amorphous phase by

thermal decomposition of disilane, is a increasing function of the deposition rate, while as a function of the deposition temperature it exhibits a maximum at certain temperature (about 470°C) [1.47]. This can be attributed to the minimum nucleation rate resulting from the maximum structural disorder of the Si network. For deposition temperature higher than 470°C, the as-deposited silicon thin films have higher structural order (in the form of crystal-like clusters) which results in higher nucleation rate and thus small grain size; whereas at lower deposition temperature the higher structural disorder of the as-deposited film (or equivalently, the higher free energy) provides a driving force for accelerating the nucleation process. The increase in the grain size can also be obtained by increasing the deposition rate of the film [1.47]. Deposition rate also affects the structural order of the as-deposited film. A-Si thin films deposited at higher rates have higher structural disorder which results in lower nucleation rate during crystallization and thus larger grain size. Therefore, crystallization of a-Si thin films deposited by thermal decomposition of disilane yield very large grain size.



1.2.1.1.2 Metal Induced (Lateral) Crystallization

A number of researchers have examined the introduction of metal impurities during the SPC process. In some case, this has enhanced the crystallization of the a-Si thin films at lower temperature. When a certain metal, for example, Al [1.48], Cu [1.49], Au [1.50], Ag [1.51], Pd [1.52], or Ni [1.53], is deposited on a-Si, the a-Si crystallizes to poly-Si at a lower temperature than its SPC temperature. The reaction between a metal and a-Si occurs at an interlayer by diffusion and its lowers the crystallization temperature. Such enhancement of crystallization is due to an interaction of the free electrons from the metal with covalent Si bonds near the growing interface [1.54]. Considering the metal-Si eutectic temperature, an a-Si thin film can be crystallized at below 500°C. A grain size up to 4-5 um has been achieved, but it is still too small compared to the desirable dimension for high performance TFT with

good controllability.

There are two kinds of crystallization mechanism related with silicide formation: stress-induced and silicide-mediated crystallization (SMC). The a-Si can be crystallized at low temperatures by the stress induced by silicide formation [1.55]. The stress is due to the difference in Si mass density between a-Si and silicide. The SMC requires a formation of silicide with the same lattice structure and a similar lattice constant with silicon. For instance, when nickel is deposited on a-Si, followed by thermal annealing, octahedral precipitates $NiSi_2$ will be formed on a-Si films. The $NiSi_2$ precipitates act as nucleation sites for crystallization. Needlelike crystallites are formed as a result of migration of the $NiSi_2$ precipitates through the a-Si network [1.56].

Among the above metals, self-aligned and bilaterally crystallized metal-induced lateral crystallization (MILC) technology in which nickel is used as the crystallization agent is the simplest one for providing the performance of TFTs. The a-Si under the nickel first undergoes metal-induced crystallization (MIC) and then the nickel migrates to the outside regions leading to the MILC process. Jin et al. [1.56], [1.57] suggested that the MIC process took place in three steps: silicide formation, break-up of the silicide layer into small nodules, and transport of the silicide nodules through the a-Si thin film. In the early stage of the MIC heat treatment, the nickel reacts with the a-Si and converts it into NiSi and $NiSi_2$. Nucleation and growth of the small grains take place at the interface of $NiSi_2$ and a-Si. Eventually, the NiSi and $NiSi_2$ layers break-up into small nodules and start moving laterally into the a-Si thin film. Meanwhile, the activation energy of the a-Si decreases to 1.86 eV from 3.16eV of solid crystallization of the intrinsic silicon in the presence of nickel [1.58], [1.59]. The MILC leads to grain growth in an ellipsoidal shape and its shape is elongated along the crystallization direction to perpendicular to the nickel strip with (110) texture. The grain size reaches a few microns in length but it width remains < 1μm [1.60].

The $NiSi_2$ precipitate acts as a good nucleus of Si, which has the crystalline structure (the

fluorite type) and a small lattice mismatch of 0.4%. The lattice constant of $NiSi_2$, 5.406 Å, is nearly equal to that of Si, 5.430 Å. The formation process of the $NiSi_2$ precipitate strongly depends on the sample condition such as Ni/Si ratio. When a Ni film is deposited on Si and annealed, the inter-reaction follows the sequence: Ni_2Si -> NiSi -> $NiSi_2$. The silicide formation proceeds sequentially, not simultaneously, which means that the metal/silicon diffusion leads to the successive formation of the silicides, starting form the metal-rich to end up to the silicon-rich silicide. Small $NiSi_2$ precipitates aggregate together and become big precipitates and the needles come from the big precipitates, i.e., the crystallization proceeds after reaching a critical size of $NiSi_2$ precipitates. In the initial stage of crystallization, the nucleation occurs randomly at the {111} faces of individual $NiSi_2$ precipitates. The migration of $NiSi_2$ leads to needlelike crystal growth of Si constrained to <111> direction [1.61]. The needlelike crystallization may be catalyzed by solid state diffusion through the migration of Ni, dissolving a-Si at one edge and rejecting crystallized silicon at the opposite edge. Hempel et al. showed the presence of Ni-rich region at the leading edge of needlelike crystallites by using X-ray analysis technique [1.62].

Recently, it was found that MIC and MILC rate was enhanced remarkably in the presence of an electric field [1.63]-[1.65], and the crystallization temperature could be reduced to as below as 380°C [1.66], [1.67]. The explanation for such a phenomenon was the enhanced diffusion of charged nickel through $NiSi_2$ precipitates in an electric field [1.67].

The post-MILC high temperature annealing is a critical step in forming the extremely large grain. At about 800°C, secondary re-crystallization takes place as an extension of MILC annealing. As a result, small grains are consumed by large grains, forming monomodal-distributed grains with large size. The surface anisotropy of the grains is responsible for the further grain enhancement that provides minimum total surface energy in a particular direction [1.68]. The secondary grain growth is further encouraged by the same grain orientation (110) of the small grains in the MILC region. Besides grain size

enhancement, the high temperature annealing also repairs the intragrain defects and enables to achieve single crystal SOI performance.

1.2.1.2 Liquid Phase Crystallization (Laser Crystallization)

The use of pulse-laser processing in fabricating poly-Si TFTs for active-matrix liquid crystal displays is receiving considerable attention [1.69]-[1.70]. The trends toward large displays require the use of low-cost glass substrates with a maximum thermal strain temperature of about 600°C. This restricts any process for fabricating TFTs on such substrates to temperatures of less than 600°C. The basic principle of laser crystallization is the transformation from amorphous to crystalline silicon by melting the silicon for a very short time. The a-Si thin film is actually melted at temperatures approaching 1400°C and grains are formed when the laser pulse turns off. The rapid absorption allows for the adoption of short laser pulses (30ns) which affects only the surface layer. As a result, the glass substrate is kept well below the damage threshold and is unaffected by the laser crystallization process. Impurities from the substrate do not diffuse into the silicon thin film.

The use of high powerful pulsed lasers, working in the nanosecond duration regime allows the deposition of a large amount of energy in very short times into the near surface region. Under suitable conditions, the irradiation leads to the rapid melting of the a-Si layer and its regrowth into poly-Si. The final quality of the device is strongly dependent on the phase transformation mechanisms which must be controlled extremely carefully in order to achieve polycrystals of sufficient quality and size distribution. At a very low laser fluence, a-Si is converted to a stratified system comprising an amorphous layer, a fine-grained poly-Si layer, and a large-grained layer [1.71]. At higher laser energy densities, a small process window allows us to crystallize poly-Si with average grain sizes of more than 10 times the film thickness [1.72]-[1.73].

There are various possible approaches for laser crystallization of a-Si thin film. However, excimer laser crystallization (ELC) appears to be the most promising at the moment [1.69]-[1.70]. ELC of poly-Si TFTs has been studies for a number of years and several important aspects of this process have been well established. The technique yields high-performance, glass substrate poly-Si TFTs with high throughput thanks to the large beam size of the high energy beam used. In addition, because this technique is of extremely short duration (100ns) and an large absorption coefficient for a-Si in the UV light region of excimer laser, it can prevent the introduction of thermal damage to the glass substrate and there also is no need to worry about the thermal compaction problem, which is a serious issue in the solid phase crystallization method. The excimer laser-induced phase and structural modifications of thin Si films involve several melt-mediated and far-from equilibrium transformation processes. In general, the excimer laser-induced crystallization of a-Si thin film can be divided into three crystallization regimes depending on the applied laser fluences [1.74]-[1.75]. The basic features of excimer laser crystallization and the existing models on the transformation process will reviewed in detail in chapter 2.

In recent, a stable diode pumped solid state (DPSS) scanning continuous wave (CW) laser crystallization was also applied to the fabrication of high-performance poly-Si TFTs on non-alkali glass substrate [1.76]-[1.78]. The power instability of DPSS CW laser is less than 1%, which is superior to that of XeCl excimer laser and Ar laser. In this technique, large scanning speed was used to achieve high throughput. The crystallized poly-Si thin film is made up of very large grains (about 3 x 20μm^2). The grain boundaries are generally parallel to one another and to the scan direction of the laser beam. Surface orientation of many grains is nearly (100) direction. Surface of the crystallized poly-Si is smooth and grain boundary does not form ridge. CW lateral crystallization makes it easy to form large grains with high scan speed and wide energy range because of continuous energy supply, directional solidification caused by laser scanning and slow cooling rate of the molten Si. However, this

technique is not well-developed and the crystallization mechanisms and large-area laser annealing equipment are still under investigated.

1.2.2 Gate Dielectric Formation

Although trap states in the bulk of the channel poly-Si thin film tend to dominate TFT electrical behavior, a high-quality gate dielectric is critical for TFT performance and reliability. The integrity of the gate dielectric has been the largest contributor to the yield loss in early LTPS TFTs production. Silicon dioxide (SiO_2) had not typical been used as a gate dielectric in the bottom gate a-Si TFTs production, so a new low temperature gate dielectric process is required for LTPS TFTs. A major problem in gate dielectric films is local breakdown due to the poor interface with the rough silicon surface after excimer laser annealing (ELA) [1.79]. Because of this problem, gate dielectric films have been deposited thicker than necessary to overcome the surface roughness which reduces throughput, increases unit capacitances, reduces TFT drive ability, worsen aperture ratio and reduces power and brightness. Gate dielectric thin films have very serve thickness uniformity requirement of ~8% compared to 15% for SiN_x gate dielectric thin films used in a-Si production to compensate for the roughness of the silicon layer after laser crystallization. A substrate temperature of <400°C is desired while maintaining desired electrical and physical properties such as breakdown voltage, resistivity, interface trap density, fixed charge density, moisture resistance, minimum pinhole, etc.

Oxide thin film can be formed using physical vapor deposition (PVD) or chemical vapor deposition (CVD). For the sake of good step coverage, CVD is preferred. There are a number of different CVD methods and chemistries for forming silicon oxide thin films. High quality silicon oxide thin films have been formed using electron cyclotron resonance chemical vapor

deposition (ECRCVD) [1.80]-[1.82] and microwave-excited plasma chemical vapor deposition [1.83], and others have developed prototypes using remote plasma enhanced chemical vapor deposition (PECVD) [1.19], but these technologies have not been scalable to large substrate sizes. With its production track record in a-Si TFTs, its common use for the a-Si precursor deposition in LTPS TFTs and its capability to process large-area substrates, PECVD has been the universal choice for forming oxides in LTPS applications.

There are two PECVD chemistries being used for forming the gate dielectric – monosilane (SiH_4) with nitrous oxide (N_2O) or tetraethyl orthosilicate (TEOS) with oxygen. The main advantage of forming SiO_x by reacting SiH_4 and N_2O is that the gate oxide layer and the a-Si precursor thin film can be formed in the same process chamber. By means of such process integration, the thin film fabrication equipment can be utilized extremely efficiently as a single substrate multi-chamber cluster tool. Particularly, for bottom-gate device structures, forming the gate dielectric and a-Si precursor thin film in the same chamber prevents exposure to the atmosphere of the critical interface between the gate insulating layer and the polysilicon precursor film, and can optimize throughput and process efficiency. As a result, Silane-based PECVD has been adopted in the fabrication of LTPS TFT.

In recent, however, TEOS-based PECVD gate oxide demonstrates superior physical and electrical characteristics under higher deposition rates. In general, TEOS oxide also provides better step coverage which is an advantage in covering the poly-Si island edges and for interlayer dielectric applications. It continuous to be important to minimize fixed-charge density as well as provide excellent uniformity as these parameters strongly affect the threshold voltage (V_{th}) of LTPS TFTs. To achieve these requirements, relatively low deposition rates have been required, further impacting the throughput of the TFT formation steps. Maximizing the deposition temperature to ~400°C also helps improve gate oxide quality.

1.2.3 Impurity Doping and Low-Thermal-Budge Activation

In the LTPS TFT fabrication process, the ion doping system is used to dope impurities in three device regions: substrate for channel doping, lightly doped drain regions (LDD), and source and drain regions. The purpose for channel doping is to accurately control threshold voltage while the one for form LDD region is to reduce leakage current and enhance reliability. The ion doping system implant impurity elements P (phosphorous), using a PH_3 gaseous source for n-type junctions in n-channel devices and B (boron), using a B2H6 gaseous source, for p-type junctions in p-channel devices. Key parameters for implanting glass substrates include substrate temperature control, accurate dose and specie control, uniformity over a wide range of implant conditions, high throughput. Because display producers tend to use photo-resist masks in the ion implantation process, substrate temperature must be <120°C which creates a significant challenge for ion implantation equipment producers.

The source/drain doping is relatively straightforward, with the primary requirement that the dose level corresponds to a desired source/drain resistance. Little dose control is required. On the other hand, unlike the source/drain implant, the LDD and channel implants are more challenging with more precise dose control requirements. As a result, a wide dynamic range of implant doses, ranging from as wide as 10^{11} to 10^{16} cm^2, is desired. The LDD implantation step is performed between the source/drain and the channel in order to suppress the electric field at the edge of the drain and reduce the leakage current. For the LDD, a relative low dose on the order of 10^{11} cm^2 is required. To carry out this implant, current densities of 0.05 to 15mA/cm^2 are typical needed. In order to control the transistor threshold voltage, an implantation with a dose of about 10^{11} cm^2 is performed. Because precise control of the implantation dose is necessary, actual regulation of the impurity concentration is achieved not

by reducing the implantation time, but rather by using a low current and low gas concentration as is done for the LDD implantation. It is important to be able to maintain a dose control of better than 5% for this application in order to maintain uniformity in device characteristics.

Ion shower system is the most often used impurity doping facility owing to the lowest equipment cost. Ions are extracted and accelerated through a grid and are implanted without mass separation. Ion shower tools typically employ a limited scanning motion of the panel during implant to insure good dose uniformity which can complicate substrate handling. Hydrogen can be coimplanted with the dopant by using PH_3 or B_2H_6 source gasses. The dynamic range of the ion source tends to be limited as the extremely large plasma electrode transparency restricts the range of the gas pressures which can be run in the ion source. In consequence, the V_{th} and LDD low dose implants require extreme dilution of the dopant gas with hydrogen. The amount of dopant actually ionized, and hence the dose rate, depends critically upon the plasma conditions. Thus, the dose control for low dose implants can be limited.

For a transistor to work effectively, the source and drain contacts must have relatively low resistance which requires low sheet resistance in the source and drain regions. In order to achieve low sheet resistance, the source and drain implants must be activated to a high degree. Activation refers to aligning the implanted dopant into the correct lattice sites. The activation step allows the dopant atoms to assume substitutional sites and heal damage to the silicon lattice. Uniformity is very critical so tight control of energy is required. The efficiency of the activation is dependent upon the implant dose, the resistivity, and the conductance. Activation poses a significant challenge to LTPS TFT manufactures due to the temperature limitations. In semiconductor processing, activation is performed by either a furnace anneal or rapid thermal processing (RTP). However, both these steps require temperatures well beyond the strain point of glass. High temperature also drives out the hydrogen incorporated during

implant, necessitating a long post-hydrogenation process.

The activation methods used in LTPS TFT fabrication include excimer laser annealing (ELA), furnace annealing (FA), and rapid thermal annealing (RTA). In ELA, the silicon is heated, melted and reformed without heating the glass, resulting in a very high efficiency approach. Despite the high efficiency, the poly-Si thin film will be peeled off owing to the release of hydrogen which was coimplanted into the poly-Si thin film. In addition, throughput may be another potential bottleneck to the production process.

Another approach is furnace annealing. This process is typically carried out at 500 ~ 600°C for as long as 24 hours. The long process time is necessary in order to keep the substrate temperature below the stress of the glass to prevent substrate warpage or damage. It is less efficient and slower than laser annealing and also presents a bottleneck to the production process.

RTA offers the highest throughput and can achieve better uniformity than ELA. RTA shortens the process time found in furnace annealing by exposing a small portion of the substrate to temperatures beyond the strain point of the glass while using the rest of the substrate as a stable backplane. The substrate is first preheated to 500°C by infrared heaters to reduce the thermal shock of the higher temperatures. It is then passed between high energy Xenon arc lamps where approximately 5% of the substrate is exposed to temperatures beyond the strain point of the glass. The spectral radiation produced by the lamps is transparent to the glass and absorbed only by the silicon thin film [1.84]. The light beam must be uniformly focused to eliminate any possibility of glass warpage due to uneven thermal distribution. The glass substrate is heated by conduction to temperatures just below the film temperatures but only within a small width. The substrate is then processed through a controlled cooling cycle. By processing at high temperatures while minimizing substrate damage, short process times and high throughput can be achieved.

1.3 Electrical Characteristics of LTPS TFTs

An important parameter in determining TFT device performance is the “on” current (I_{on}). A high I_{on} is an indicator of the TFT being able to provide sufficiently high drive current which results in shorter pixel capacitance charging times. This indicates that the high I_{on} device will be able to operate at higher resolutions while maintaining a smaller size and achieving higher aperture ratio than lower I_{on} devices. Currently, the low drive current of LTPS TFTs is a major weakness compared to single crystal silicon devices. The drive current is a function of the carrier field-effect mobility in the device. Improvements in field-effect mobility can improve the drive current. Manufacturers are primarily concerned with higher mobilities at the driver area in order to squeeze in all the required circuitry within the narrow pixel pitch as well as to integrate more circuitry. Field-effect mobility performance is closely tied to the grain size and grain crystallinity. For LTPS TFTs, the nature of the crystallization process typically results in the formation of numerous small grains fewer than 1μm which reduces mobility performance. Therefore, many novel lateral laser crystallization methods have been provided to further enhance the field-effect mobility of the LTPS TFTs [1.85]-[1.90].

Because there are typically numerous grains in the channel, the uniformity of the grain size is also critical. Manufactures typically point to variations in laser energy density as the cause of grain size non-uniformity problems. Today, manufactures appear to be more concerned with uniformity performance and are content to work with small grains. Once uniformity is controlled, they will develop methods to improve grain size while maintaining uniformity and achieve higher mobility levels. Thus, while field-effect mobility performance today is on the lower end of the range for LTPS TFTs, it is expected to improve in the near future if large grain sizes with controlled grain boundaries are implemented which will

narrow the performance gap with single crystal silicon devices.

The anomalous leakage current has traditionally been a significant problem for LTPS TFT displays and manifests itself in the form of image degradation. The leakage current of LTPS TFT has typically be 5~10X that of a-Si TFT and 25~50X worse than single crystal silicon. The dominant leakage current mechanism is the field emission via the traps by high electric field near the drain junction [1.91]-[1.93]. To reduce the leakage current, it is necessary to suppress the electric field in the channel at the edge of the drain. This not only suppresses leakage current when the gate and drain are drain are biased, but prevents degradation of device characteristics over time due to the injection of energetic or “hot” electrons into the gate oxide. On of the most common approaches to reduce the anomalous leakage current is to adopt drain-field-relief structures, such as light doped drain (LDD) or offset gate structure.

Field relief at the drain also helps to avoid non-saturated device output characteristics, i.e. kink effect [1.94]. Thin film devices experience a high electric field at the channel/drain junction region when the device is operated in the saturation region. The high electric field is the major cause of the impact ionization at the channel/drain junction region, which results in the accumulation of the holes in the floating body of the device. The hole accumulation causes a profound kink effect in the current-voltage characteristics of thin-film devices, which in turn deteriorates the output characteristics and reduces the gain of the transistors. In addition, the kink effect also causes the avalanche induced short channel effect which places a limitation on scaling down of the device size. Thus, the kink effect is a serious problem in LTPS TFT for analogue circuit application in large area microelectronics. Recently, a study on the influence of lateral electric field on the anomalous leakage current and kink effect of poly-Si TFT has been reported [1.95]-[1.96]. It was found that the high lateral electric field at the channel/drain junction can be effectively reduced by use of a thick drain but thin channel structure.

1.4 System on Panel (SOP) Issues in LTPS TFT

Presently, the majority of active-matrix-liquid-crystal-displays (AMLCD's) are manufactured on glass substrates using a-Si TFT for the active switching elements. However, there is great interest in using poly-Si TFTs rather than a-Si TFT devices for this application, because of the higher carrier mobility found in the poly-Si material, and because long-term device stability is better. These features of poly-Si TFT have already enabled the integration of row and column drive circuitry, and some additional functionality such as image reversal, aspect ratio control, and level shifting. Furthermore, the carrier field-effect mobility in the poly-Si TFT has steadily been increased over the last 10 years, and recent values have been achieved which are approaching that of single crystal silicon devices. It is expected that the degree of circuit integration will continue to increase as device characteristics improve further, so that entire systems may soon be formed on a single panel. As systems become more complex, they will require other circuit elements in addition to display and circuitry, such as memories, solor cell, touch sensors, and other sensors. Integrated drivers also have the potential for eliminating printed circuit boards, the TAB connectors, and reducing the module assembly labor and equipment costs. However, in order to meet the requirement of System-on-Panel, several drawbacks in the process and/or electrical characteristics of LTPS TFT need to be further improved.

Fully integrated drivers have been slow to develop because of the serious technical challenges.

- LTPS TFTs uniformity – the uniformity of LTPS TFTs devices is primarily a function of the laser annealing process stability. The uniformity variance should be less than 5% across the panel to allow for adequate margins in applying the proper gate and data voltages. When the uniformity exceeds the design margins, the potential for not fully

charging the pixel exists. The result would be uneven brightness for a given gray scale. The LTPS TFTs suffer from poor uniformity of device performance due to the narrow laser process window for producing large-grained poly-Si thin film. The fluctuation of pulse-to-pulse laser energy and non-uniform laser beam profile make laser energy density hard to hit the super lateral growth regime everywhere. Increasing shot density per area may improve the crystallization uniformity and promote the secondary grain growth. However, the process throughput will decrease thereof, which is not desirable for mass production.

- LTPS TFTs power consumption – the inherent low mobility and higher threshold voltages of LTPS TFTs over single crystal silicon devices pose a power consumption problem. It is reported that compared to single crystal silicon transistors, LTPS TFTs have higher supply voltage, larger threshold voltage, and lower transconductance. These result in a higher power consumption when use a LTPS TFT driver. The properties of high supply voltage, larger threshold voltage, and lower transconsuctance are also related to the crystallinity of the poly-Si thin films. The disadvantages mentioned above can be solved by improving the crystallinity of the poly-Si thin films.
- LTPS TFTs mobility – Manufactures have reported mobilities of 80 to over 200 cm^2/V-s. The higher the mobility, the smaller the LTPS TFT and the less space taken by the driver. Since the defect traps place a profound influence on electrical characteristics of LTPS TFTs, the most effective approach to improve the mobility of LTPS TFTs is to reduce the defect traps by promoting the quality of the poly-Si thin films.
- LTPS TFTs reliability – the stability of device characteristics under long-term operation is indispensable for circuit applications. As a result, the reliability of LTPS TFTs must be taken into consideration when they are applied to advanced circuitry. The special processes used in the fabrication of LTPS TFTs and nature properties of the crystallized poly-Si make the reliability issues in LTPS TFTs different from those in the conventional

MOSFETs. The crystallized poly-Si is generally full of weak strain Si-Si bonds and dangling bonds. Besides, the hydrogenation process also creates a large amount of weak Si-H bonds in poly-Si. These weak bonds can easily be broken during device operation, which will result in the variation of device characteristics.

- Yield – the introduction of integrated driver circuits will have a yield impact on the entire panel. Pixel TFTs are designed to maximize the aperture ratios and are limited in density to the space available within each single pixel. The peripheral circuits are designed to minimize the space and will be densely packed. The additional process steps inherent in LTPS TFT and the additional mask steps to fabricate the CMOS driver circuits will also affect the yield. With redundant design, the yield losses associated with the higher device density can be reduced to between a 2% and 15% differential compared to designs without integrated drivers.

1.5 Motivation

Considering the issues of System on Panel (SOP) mentioned in former section, the enhancement of field-effect mobility and uniformity of LTPS TFTs become the most important topic in future applications. In this thesis, we start to improve the field-effect mobility and/or uniformity of LTPS TFT in two aspects. From the perspective of channel material, owing to the carrier mobility enhancement of germanium atom, polycrystalline silicon germanium (poly-$Si_{1-x}Ge_x$) thin film is adopted to replace the poly-Si active layer in LTPS TFT. On the other hand, from the perspective of crystallization structure, a novel spacer-aided crystallization method is proposed to artificially control lateral grain growth in the channel region by using excimer laser irradiation.

1.5.1 From the Perspective of Channel Material – Enhance the Field-Effect Mobility by Adding Germanium Atoms into the Poly-Si Active Layer

Although pulsed excimer laser crystallization (ELC) is an effective technique in improving the crystallinity of polysilicon thin films, the grain size is always smaller than 1um for conventional excimer laser crystallization method. This will result in an upper limitation of the field-effect mobility of ELC LTPS TFTs. Therefore, a novel approach has to be found out to further enhance the field-effect mobility of the ELC LTPS TFTs. In the case of single crystal technology, it is well known that Ge shows much higher mobility than Si. The mobility of single crystal device can be improved by adopting $Si_{1-x}Ge_x$ thin film instead of Si thin film. On the other hand, for the poly-$Si_{1-x}Ge_x$ TFT, it is reported that there are two remarkable effects when some Ge atoms were incorporated into poly-Si thin film. One is to lower the crystallization temperature of poly-Si thin film [1.97]. The other is to enhance the effective hole mobility [1.98]-[1.99]. Thus, poly-$Si_{1-x}Ge_x$ thin film seems to be a promising candidate to replace poly-Si thin film as the active layer. However, most of the poly-$Si_{1-x}Ge_x$ thin films were crystallized by using conventional solid-phase crystallization [1.100]-[1.102]. Very few researches have been done about the recrystallization mechanism of ELC poly-$Si_{1-x}Ge_x$ thin film until now. In this thesis, poly- $Si_{1-x}Ge_x$ thin film was fabricated by excimer laser crystallization of a-$Si_{1-x}Ge_x$ thin film. Various analysis methods were adopted to investigate the mechanisms of ELC poly- $Si_{1-x}Ge_x$ thin film in detail. A precise laser crystallization model was established to explain the phenomena of ELC poly- $Si_{1-x}Ge_x$ thin film.

In addition, poly-$Si_{1-x}Ge_x$ TFTs fabricated by excimer laser irradiation were demonstrated. The electrical characteristics of the poly-$Si_{1-x}Ge_x$ TFTs were compared to

those of the poly-Si TFTs. Although the device fabrication process of poly-$Si_{1-x}Ge_x$ TFTs is almost compatible with that of conventional poly-Si TFTs, some unexpected process-related issues arise from the different intrinsic properties of Si and Ge. Therefore, the fabrication process of poly-$Si_{1-x}Ge_x$ TFTs needs to be modified to avoid degrading the device performance. In this thesis, two different process flows were proposed to accomplish high performance low-temperature ELC poly-$Si_{1-x}Ge_x$ TFTs.

1.5.2 From the Perspective of Crystallization Structure – Enhance the Field-Effect Mobility and Improve the Device Uniformity by Using A-Si-Sapcer-Aided Location-Controlled Lateral Laser Crystallization

Although the excimer laser crystallization have been shown the capability of fabricating good-performance LTPS TFTs, the quality of poly-Si thin film produced by the technique is still not sufficient to be applied to ultra high-performance LTPS TFTs. Narrow process window and the uniformity of the crystallized poly-Si thin film are noteworthy issues. As many prior literatures have shown, the grain size of the ELC poly-Si thin film is significantly dependent on energy density of laser irradiation so that the energy for producing super lateral growth is too critical to hit it right. Fluctuation of energy profile, pulse-to-pulse energy variation and unevenness of initial a-Si thin films will also crucially affect grain growth after solidification. As a result, a variety of crystallization methods have been proposed to solve the above problems, such as sequential lateral solidification (SLS), phase-modulated ELC using an optical phase-shift mask, and dual beam ELC. However, these methods can not readily be implemented using existing ELC equipment. In this thesis,

we propose a novel crystallization structure, which is called a-Si spacer structure, to control large lateral grain growth in the channel region. In this method, a-Si spacers were formed by dry-etching of the a-Si/Si_3N_4 step structures which then served as the seeds for lateral grain growth during excimer laser irradiation. Consequently, a large-grain poly-Si film is obtained which will lead to improved device performance. In addition, due to the artificial controlling of the lateral growth and improved periodicity of the polycrystalline microstructure, the uniformity of device characteristic can be further improved.

1.6 Thesis Organization

In chapter 2, two main fabrication processes, i.e. excimer laser crystallization and low-temperature gate dielectric deposition, of LTPS TFT were investigated. The experimental results and crystallization mechanism of ELC poly-Si thin film were studied. The influences of several ELC parameters on the electric characteristics of LTPS TFTs were also discussed. In addition, high quality TEOS oxide films were prepared by large-area plasma-enhanced chemical vapor deposition (LA-PECVD). The characteristics of the large area plasma enhanced chemical vapor deposited TEOS oxide after various short-time plasma treatments were investigated as a function of annealing ambient and time. The long-term reliabilities of the plasma-treated oxides were also analyzed.

In chapter 3, the deposition parameters of the a-$Si_{1-x}Ge_x$ thin film and excimer laser crystallization of poly-$Si_{1-x}Ge_x$ thin film were investigated. A variety of material analysis methods, such as X-Ray diffraction (XRD), Rutherford backscattering spectroscopy (RBS), and Raman spectroscopy, were used to characterize the deposition and crystallization mechanisms. Several physical characterizations were performed to appraise the composition, crystallinity and grain structure of the ELC poly-$Si_{1-x}Ge_x$ thin film prepared by various

process parameters, including laser energy density, shot number per unit area, and substrate temperature. The crystallization mechanism of ELC poly-$Si_{1-x}Ge_x$ thin film was proposed to explain the phenomenon observed from the experiment results. The crystallinity of ELC poly-$Si_{1-x}Ge_x$ thin film was also compared with conventional ELC poly-Si thin film. In addition, the low-temperature poly-$Si_{1-x}Ge_x$ TFTs fabricated by direct excimer laser crystallization of a-$Si_{1-x}Ge_x$ thin film were fabricated. The electrical properties of ELC poly-$Si_{1-x}Ge_x$ TFTs, including field-effect mobility, subthreshold swing, threshold voltage, and on/off current ratio, were reviewed. The process-related issues of ELC poly-$Si_{1-x}Ge_x$ TFTs were also discussed in this chapter.

In chapter 4, two modified fabrication processes of low-temperature ELC poly-$Si_{1-x}Ge_x$ TFTs were proposed to improve the crystallinity of the poly-$Si_{1-x}Ge_x$ thin film and avoid the process-related issues described in chapter 4. ELC poly-$Si_{1-x}Ge_x$ TFTs with Si-capped layer was provided to lower the Ge atomic concentration at the thin film surface. Although the device performance was improved, however, it still does not meet the requirement due to the poor crystallinity of the poly-$Si_{1-x}Ge_x$ thin film. Thus, another approach, which was called Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs, was provided to further improve the device characteristics. The Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs exhibited excellent electrical characteristics for small dimension devices in comparison with conventional ELC poly-Si. The detail mechanisms of the process-modified ELC poly-$Si_{1-x}Ge_x$ TFTs were investigated in this chapter.

In chapter 5, a novel and simple crystallization method to control lateral grain growth in the device channel region using excimer laser irradiation was proposed. The results of crystallized poly-Si thin films were analyzed. In addition to small dimension LTPS TFTs, large dimension LTPS TFTs fabricated by this crystallization method were also presented and the relation between the numbers of grain boundaries in the channel region and the electrical characteristics of LTPS TFTs were investigated.

Finally, summary and conclusions as well as recommendation for further research are given in chapter 6 and chapter 7, respectively.