Chapter 2

Process and Device Characterizations of Low-Temperature Polycrystalline Silicon Thin Film Transistors

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2.1 Introduction

Active matrix liquid crystal displays (AMLCDs) have been used for portable personal computer, airplane television broadcasting systems, and a range of other applications. It is expected that in the near future, the demand of flat panel displays will continuous to grow with the rapid development of wireless communications and high definition television. To keep AMLCDs cost competitive among different types of flat panel displays, it will be beneficial to integrate peripheral driver circuits onto the display backplate, and reduce the fabrication complexity of the thin film transistors (TFTs) used in the display array. The amorphous Si (a-Si) TFTs technology is not suitable for the requirement of integration peripheral driver circuits due to the low filed-effect carrier mobility. Thus, new technique has to be developed. Since the demonstration of the first compact color TV liquid crystal displays in 1983 [2.1], polycrystalline silicon (p-Si) TFT LCD technology has been actively pursued. One obvious and well known benefit of p-Si TFT is, as compared to the conventional a-Si TFT technology, higher field-effect carrier mobility. In recent years, many studies on poly-Si TFTs have focused either on reducing the process time or on lowering the process temperature while keeping the advantages of the good properties of poly-Si [2.2]. The latter is more importance since it enables the use of inexpensive glass as starting substrate. One of the

common methods of preparing poly-Si thin films is solid phase crystallization (SPC) of a-Si thin films at 600°C for 20 – 48 hours [2.3]. However, the temperature for SPC is too high to use glass substrate for large-area TFT-LCDs. Recently, many methods are reported to lower the process temperature, such as metal adsorption on a-Si thin films [2.4], multilayer with metals [2.5], and alloying Si with Ge [2.6]. But these methods leave the Si thin films in high impurity levels and provide worse electrical properties of the devices. On the other hand, many researches are developed to increase the poly-Si TFTs performance, either by improving the polysilicon layer quality, with a laser annealing for instance, or by using post-process treatments such as TFT hydrogenation.

The development of low temperature poly-Si by laser crystallization has brought attention to integration of large-area electronics with peripheral drivers. The trends toward large displays require the use of low-cost glass substrates with a maximum thermal strain temperature of about 600°C. This restricts any process for fabricating TFTs on such substrates to temperatures of less than 600°C. The basic principle of laser crystallization is the transformation from amorphous to crystalline silicon by melting the silicon for a very short time. The a-Si thin film is actually melted at temperatures approaching 1400°C and grains are formed when the laser pulse turns off. The rapid absorption allows for the adoption of short laser pulses (30ns) which affects only the surface layer. As a result, the glass substrate is kept well below the damage threshold and is unaffected by the laser crystallization process. Impurities from the substrate do not diffuse into the silicon thin film.

There are various possible approaches for laser crystallization of a-Si thin film. However, excimer laser crystallization (ELC) appears to be the most promising at the moment [2.7]-[2.8]. ELC of poly-Si TFTs has been studies for a number of years and several important aspects of this process have been well established. The technique yields high-performance, glass substrate poly-Si TFTs with high throughput thanks to the large beam size of the high energy beam used. In addition, because this technique is of extremely

short duration (100ns) and an large absorption coefficient for a-Si in the UV light region of excimer laser, it can prevent the introduction of thermal damage to the glass substrate and there also is no need to worry about the thermal compaction problem, which is a serious issue in the solid phase crystallization method. The excimer laser-induced phase and structural modifications of thin Si films involve several melt-mediated and far-from equilibrium transformation processes. In general, the excimer laser-induced crystallization of a-Si thin film can be divided into three crystallization regimes depending on the applied laser fluences [2.9]-[2.10]. The basic features of excimer laser crystallization and the existing models on the transformation process will reviewed in detail in the following sections.

The threshold voltage of TFT device depends on the fixed charge in the gate dielectric thin film, the defect density and the doping level in the Si active layer, and the work function of the gate electrode. High quality gate dielectric thin film is one of the most important issues for fabricating high performance TFTs. A-Si TFTs with silicon nitride (SiN) gate insulator shows superior performance over those with silicon dioxide (SiO_2). According to the defect pool model [2.11], the superior performance of a-Si TFTs with a SiN gate insulator is attributed to the positive fixed charge in the nitride dielectric. The positive charges in the gate insulator result in, through equilibration equations, lower defect densities located above the midgap of the a-Si band gap. Therefore, the threshold voltage is small and positive. However, the threshold voltage of poly-Si TFTs with a SiN gate insulator is negative. One of the approaches to obtain small and positive threshold voltages for poly-Si TFTs is to use SiO_2 for the gate insulator.

The plasma enhanced chemical vapor deposited TEOS oxide has been widely used in large-area electronics applications. However, as-deposited TEOS oxide usually can hardly attain this requirement, especially for oxide electrical strength and long-term reliability issue. As a result, post annealing or other post treatments may be necessary to further enhance the oxide quality. Post gate oxide densification with conventional furnace annealing (CFA) has

been widely applied in high-performance LTPS TFTs [2.12]-[2.13]. Although the benefits of simplicity and low cost could be acquired, it requires a long process time (>2 hr.) and a high process temperature (~600°C), which maybe result in shrinkage of glass substrate. Recently, rapid thermal processing (RTP) has attracted large attention due to the short process time involved [2.14]-[2.15]. However, the thermal stress is the limiting factor. Plasma passivation has been used to improve the performance of LPTS TFTs [2.16]. When plasma treatment is applied to enhance oxide quality, it shows the benefits of low thermal budget.

In this chapter, a systematic study is made on excimer laser crystallized poly-Si thin films and LTPS TFTs fabricated on the resulting poly-Si thin film. The relationship between laser annealing condition and LTPS TFT performance is investigated. In addition, the electrical characteristics of the TEOS oxide, which was prepared by large area plasma enhanced chemical vapor deposition (LA-PECVD), after various short-time plasma treatments are investigated as a function of plasma ambient and process time. The reliability tests including charge to breakdown (Q_{bd}) and bias temperature stress (BTS) are also analyzed in these samples.

2.2 Excimer Laser Crystallization of a-Si Thin Film

2.2.1 Heat Transport and Grain Growth Mechanism of Excimer-Laser-Annealed Poly-Si Thin Films.

Excimer laser crystallization (ELC) of a-Si thin film is presently widely used method for preparing poly-Si thin film on foreign substrates. Excimer lasers emit in the UV region (output wavelengths 193, 248, and 308nm for ArF, KrF and XeCl gas mixtures, respectively) with a short pulse duration (10-30ns). The combination of strong optical absorption of the UV light in silicon ($\alpha > 10^6$ cm^{-1}) and small heat diffusion length during the laser pulse (~ 100

nm) implies that high temperature can be produced in the silicon surface region, causing melting, without appreciable heating of the substrate. This makes the ELC process compatible with glass or plastic substrate, one of the major advantages of this technique.

There are many discussions in the literature of the absorption mechanism of intense laser radiation in solids. Among them, four absorption mechanisms in semiconductors seem to be important. They are:

(1) Direct excitation of lattice vibrations by absorption of light with photon energy ($h\nu$) well below the band-gap energy (E_g).

(2) Excitation free or nearly free carriers by absorption of light with $h\nu < E_g$; such carriers will always be present as a result of finite temperatures and/or doping.

(3) An induced metallic mechanism due to free carriers generated by the laser light itself.

(4) Electron-hole excitation by light with $h\nu < E_g$.

Kuriyama et al. used thermal analysis to calculate the recrystallization process during ELC [2.17], [2.18]. The solidification velocity of molten Si during laser annealing can be controlled by three factors: laser pulse width, laser energy density, and substrate temperature during ELC. According to their papers, the substrate temperature is most effective among the three factors. The melting duration increases with substrate temperature. The solidification velocity can be reduced to about one-third by substrate heating.

It is becoming increasing clear that the excimer laser-induced phase and structural modifications of thin Si films involve several melt-mediated and far-from equilibrium transformation process. J. S. Im et al. identified that excimer laser crystallization of a-Si thin film on foreign substrates can divide into three transformation regimes with respect to the applied laser energy densities [2-19], [2-20]. They are partial melting regime, fully melting regime, and near complete melting regime as shown in Fig. 2.1 ~ Fig. 2.3 respectively.

Partial-melting regime (low energy density regime)

In the partial melting regime, the energy density of incident laser pulse is above the surface melting threshold but below the complete melt-through energy density (i.e., melting depth < film thickness). The a-Si thin film can be partially melted and subsequently can be crystallized. Explosive crystallization of a-Si thin film occurs at the onset of the transformation and follows by vertical regrowth. The early trigger of explosive crystallization may be attributed either to the presence of microcrystalline clusters – which was confirmed by analyzing the solid phase crystallization behavior and is absent in high-dose ion irradiated a-Si thin films – and/or to the possible presence of impurities such as hydrogen.

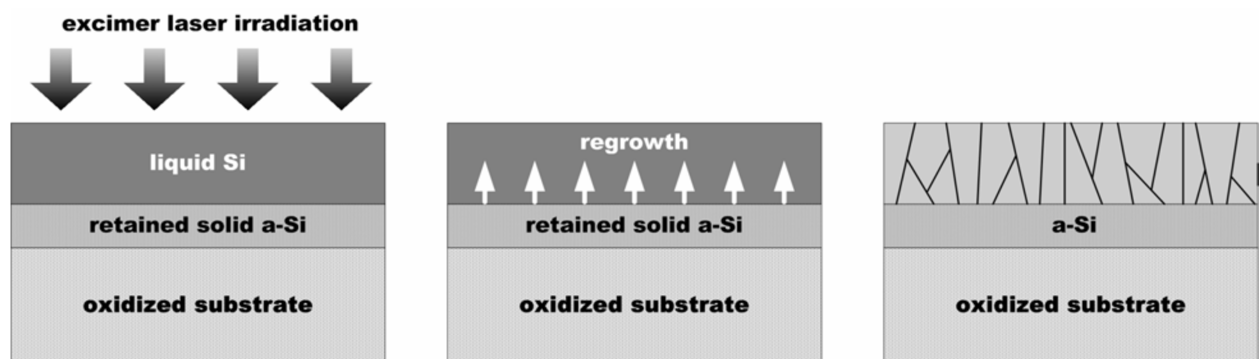

Figure 2.1. The schematic view of the recrystallization mechanism in the partial melting regime.

In this regime, there is an increase in the grain size with increases in the laser energy density. This occurs up to the point at which the average grain radius is approximately equal to the film thickness.

Complete melting regime (high energy density regime)

In the complete melting regime, the energy density of incident laser pulse is sufficient high to lead to a complete melting of the a-Si thin film and no unmelted Si remains. A sudden

increase in the melt duration, which is observed at the transition from the low to high energy density regime, is strong indicative of the transition from partial melting and regrowth to complete melting. The complete-melting Si thin film is then followed by significant supercooling of the liquid before the occurrence of the transformation to the solid phase. In this regime, the final microstructure is insensitive to large variations in laser energy densities. For low substrate temperature, fine-grained and small-grained poly-Si thin films are observed. In addition, amorphization of the poly-Si thin film is found for thinner film thickness.

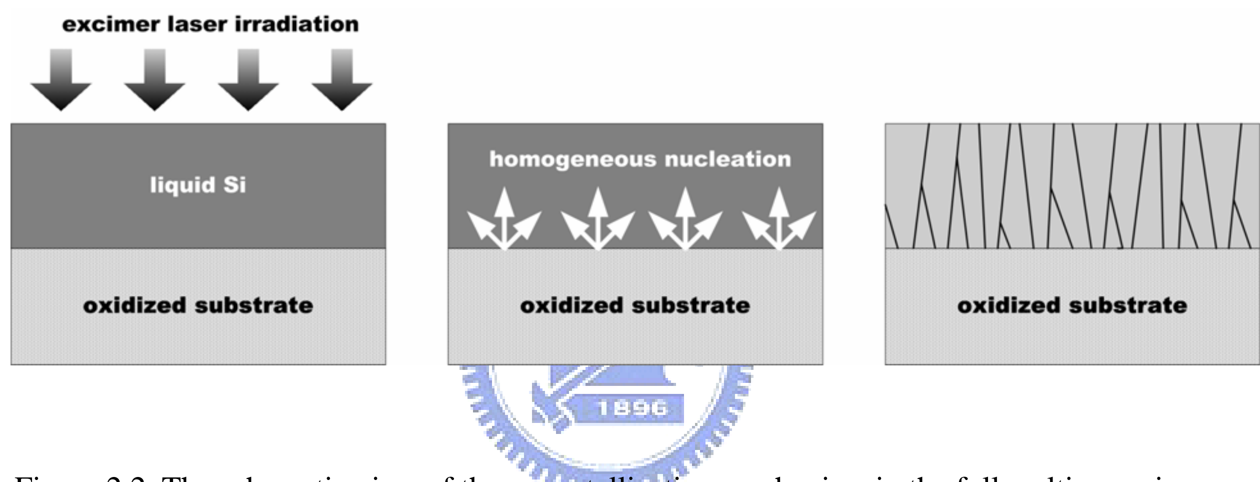

Figure 2.2. The schematic view of the recrystallization mechanism in the full melting regime.

Near complete melting regime (super lateral growth regime)

In the near complete melting regime, the energy density of the incident laser pulse leads to a unmelted a-Si thin film composed of discrete islands (i.e. melting depth ≅ film thickness). At this point, with a small increase in the energy density, an extremely sharp increase in the grain size occurs. Due to the technological significance of large-grained poly-Si thin film and its dramatic nature, this regime is also referred as the super lateral growth (SLG) regime. With further slight increases in laser energy density, a dramatic reversal in the microstructural trend is observed in that fine-grained poly-Si thin film is obtained. This transition marks the end of the low energy density regime and the beginning of the high energy density regime.

In view of the above interpretations imposed on the low and high energy density regimes, it can be argued that the large-grained poly-Si thin film obtained in the SLG regime is a consequence of the liquid phase regrowth from the discontinuous and small solid seeds, which are never fully melted. In other word, the SLG regime corresponds to the condition at which point near-complete melting of the film occurs to the extent that the unmelted a-Si thin film no longer forms a continuous layer; instead, the residual Si is composed of discrete island. Hence, as the temperature begins to drop, growth from these clusters can proceed. Depending on the separation distance between these seeds, it is possible for significant lateral growth to take place before the impingement of the grain occurs. However, there is a limit to the maximum lateral growth distance, which can be achieved as continuous cooling of the liquid layer via conduction to the substrate eventually would lead to copious nucleation of solids in bulk liquid ahead of the interface. High substrate temperature lead to lower quenching rates, which in turn provides more time for lateral growth to take place before bulk nucleation intervenes. In addition, the SLG distance will also increase with increasing film thickness, decreasing thermal conductive of the substrate, and increasing the laser pulse duration [2.20].

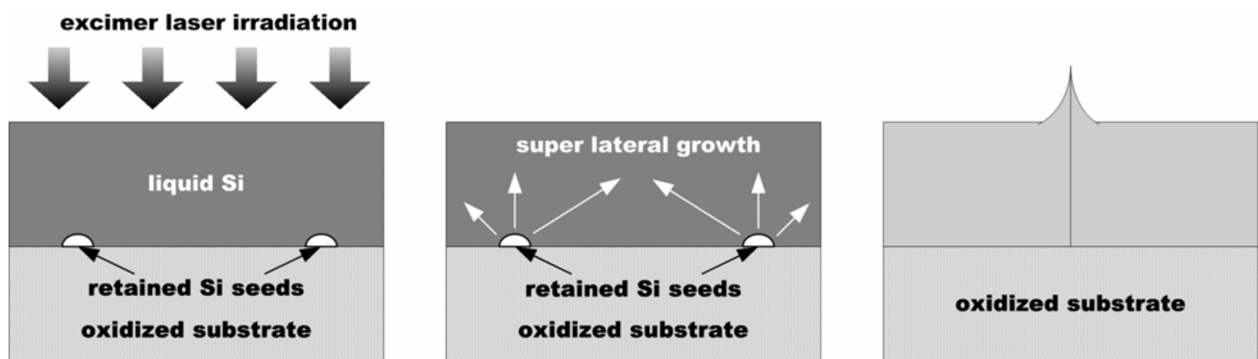

Figure 2.3. The schematic illustration of the recrystallization mechanism in the super lateral growth (SLG) regime.

2.2.2 Experimental Procedure

2.2.2.1 The Excimer Laser Crystallization System

Figure 2.4 illustrates the brief schematic of excimer laser crystallization system. The light source of this system is KrF excimer laser, which wavelength is 248nm (Lambda Physik LPX 210i series). The maximum output power is about 600mJ and the maximum frequency is 100Hz. In this work, the pulse laser is operated at a frequency of 10 Hz and the peak energy density at the substrate stage is below 600 mJ/cm^2. The output laser light is passed through a series of mirrors and long-axis homogenizer which splits the beam by the number of its elements and converts the original beam to a spatial uniform top hat profile in the long-axis direction and a semi-Gaussian profile in the short-axis direction. The length and width of the laser beam at the working stage is adjusted to 22.5 mm x 1.1 mm.

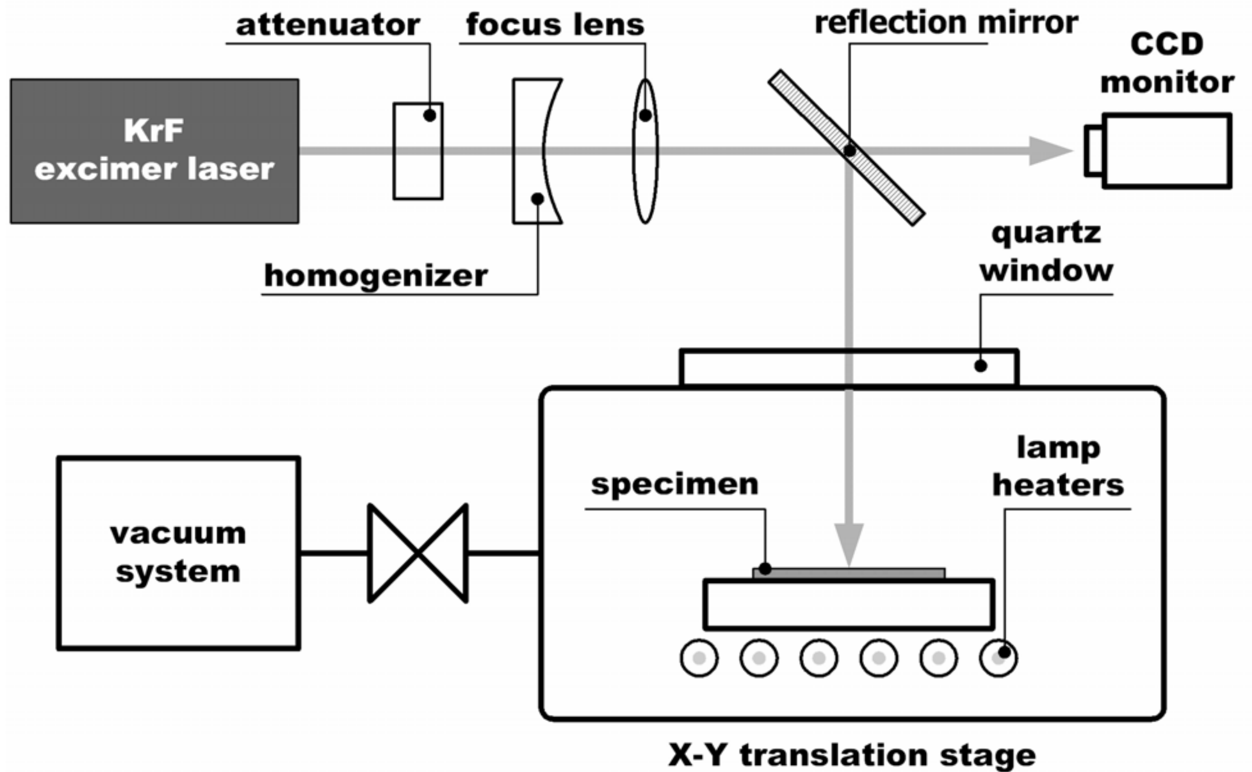

Figure 2.4. The brief schematic of excimer laser crystallization system.

The sample is scanned with overlapping pulses in a vacuum chamber. The overlap helps to reduce the non-uniformities resulting from each pulse as the middle of the pulse tends to result in better crystallinity than the edges. The non-uniformities resulting from pulse to pulse and spatial deviation of the irradiation energy are also reduced. The movement of the sample is controlled by the x-y translation stage. The velocity of the x-y translation stage during crystallization process depends on the shot numbers per unit area under certain laser frequency. The scanning direction is parallel to the short axis of the laser beam. In addition, the crystallization process can be performed at either room temperature or 400°C in order to control the solidification velocity.

2.2.2.2 Sample Preparation for Material Analysis

In order to prepare the sample for material analysis, silicon dioxide (SiO_2) with a thickness of 1 μm was thermally growth on bare silicon wafers by furnace. These oxidized silicon wafers were used as the starting substrate in order to imitate the real glass substrate. And then, a-Si thin films with thickness of 500Å and 1000Å were deposited on the oxidized Si wafers by low-pressure chemical vapor deposition (LPCVD) at 550°C. The a-Si thin films were prepared by decomposition of pure silane (SiH_4). After a device-grade clean process, the a-Si thin films were crystallized by a KrF excimer laser irradiation (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-4} Torr and substrate was maintained at room temperature or 400°C. The shot numbers per unit area were 100 (i.e. overlap = 99%). Several laser energy densities were adopted in this work.

The relationship between the final crystallized poly-Si thin films and laser irradiation conditions was investigated by using several material analysis techniques. Scanning electron microscopy (SEM) analysis was utilized to analysis the grain size and grain structure under different laser process conditions. In order to facilitate the SEM analysis, some samples were processed by Secco-etch [2.21] before observation. Secco-etch preferably etches the grain boundaries in poly-Si thin films. Atomic force microscopy (AFM) was used to analyze to surface morphology as well as the grain size of the crystallized poly-Si thin films.

2.2.2.3 Fabrication of ELC LTPS TFTs

Figure 2.5 illustrates the key processes for fabrication of the ELC LTPS TFTs. The maximum process temperature of these LTPS TFTs is 550 °C. At first, a-Si thin films with thicknesses of 500 Å or 1000Å were deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C with SiH_4 as gas source. After a device-grade clean, the a-Si thin films

were crystallized by a KrF excimer laser irradiation (λ=248nm). During the laser irradiation, the samples were located on a substrate in a vacuum chamber pumped down to 10^{-4} Torr and substrate was maintained at room temperature or 400°C. The excimer laser annealing was performed in the scanning mode with various energy densities to investigate the effects of laser annealing conditions on the performance of the fabricated LTPS TFTs. The shot numbers per unit area were 100 (i.e. overlap = 99%). After laser crystallization, the poly-Si active layers were etched to define the active channel region. Then, 1000 Å-thick tetraethyl orthosilicate (TEOS) gate oxides were deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. 2000Å-thick a-Si thin films were deposited by LPCVD at 550°C for formation of the gate electrode. Then, the a-Si thin films were etched by reactive ion etching (RIE) to form gate electrodes and the gate oxides were removed by buffer oxide etch (BOE) chemical solution. A self-aligned phosphorous implantation with a dosage of 5×10^{15} cm^{-2} was performed to form source and drain regions. 3000Å-thick TEOS passivation oxide layers were deposited by PECVD and the implanted dopants were activated by thermal annealing at 600°C for 12 hours. After contact opening by RIE, aluminum thin film with a thickness of 5000Å was deposited by thermal evaporation and patterned to complete the fabrication of poly-Si TFTs. A 20-min sintering process was performed at 400°C to reduce the contact series resistance of the source and drain electrodes. No post plasma treatment was carried out on these devices.

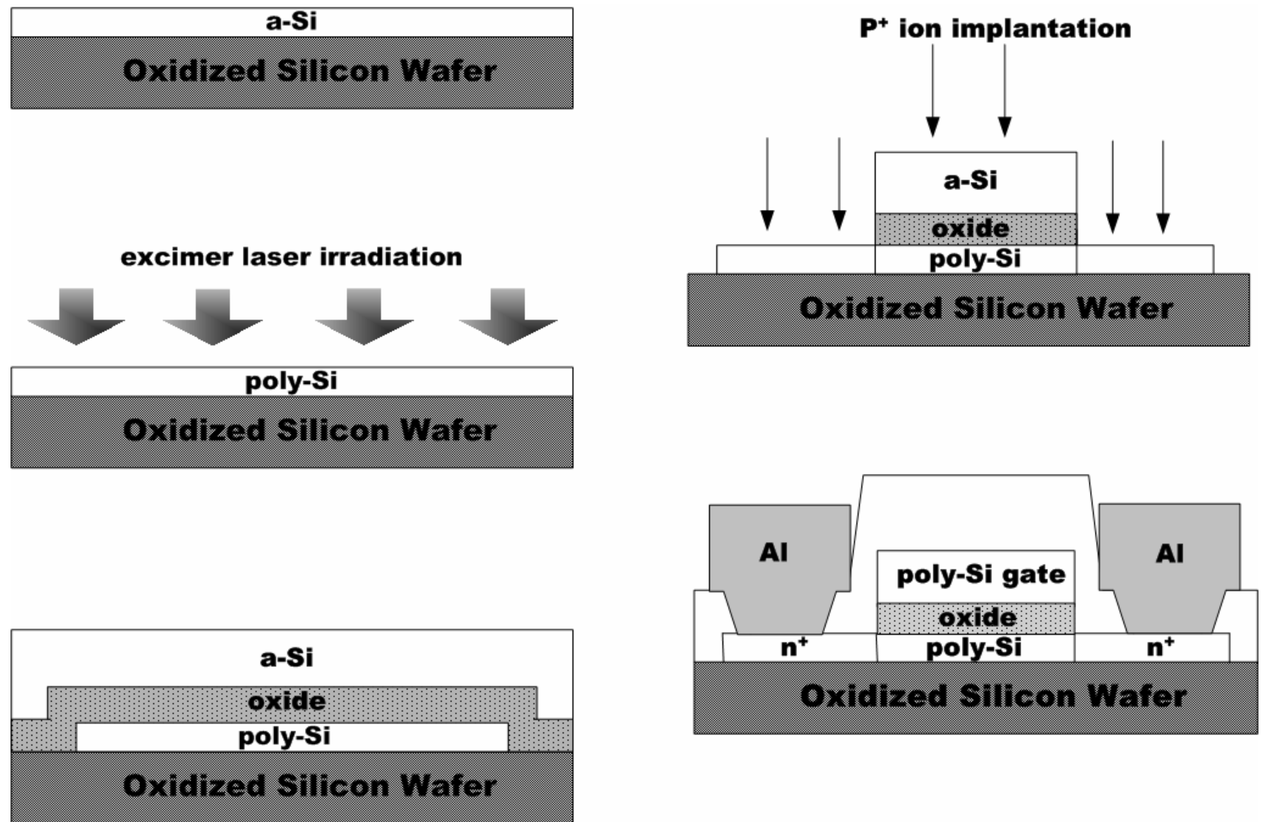

Figure 2.5. The key processes for fabrication of the ELC LTPS TFTs.

2.2.3 Results and Discussion

2.2.3.1 Material Characterization of ELC Poly-Si Thin Films

2.2.3.1.1 Scanning Electron Microscopy (SEM) Analysis

Figure 2.6(a) ~ 2.6(c) shows the SEM graphs of the 500Å-thick poly-Si thin film crystallized in the three different recrystallization regimes. The substrate temperature during laser irradiation is maintained at 400°C and the shot number per unit area is 100 (i.e. 99% overlap). Fig. 2.6(a) and 2.6(c) are the images of the poly-Si thin films crystallized in the

partial melting regime and full melting regime, respectively. Fig. 2.6(b) is the micrograph of the poly-Si thin film crystallized in the SLG regime. Obviously, large grains with 0.5 μm ~ 0.7 μm in size can be acquired in the SLG regime. On the other hand, the grains crystallized in the partial melting and full melting regimes are smaller than 0.1 μm, fairly lower than those fabricated in the SLG regime. This will result in degraded electrical characteristics of LTPS TFT when the applied laser energy is controlled in the partial melting regime or full melting regime.

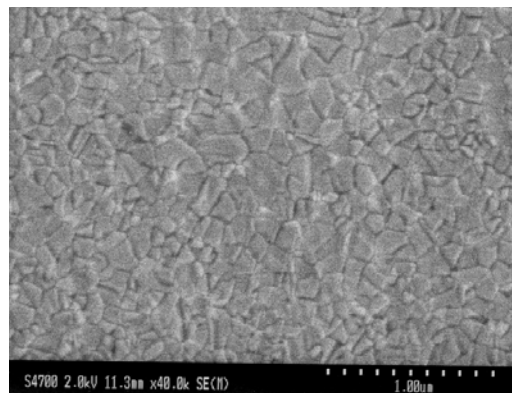

Figure 2.6(a). SEM graph of the 500Å poly-Si thin film crystallized in the partial melting regime

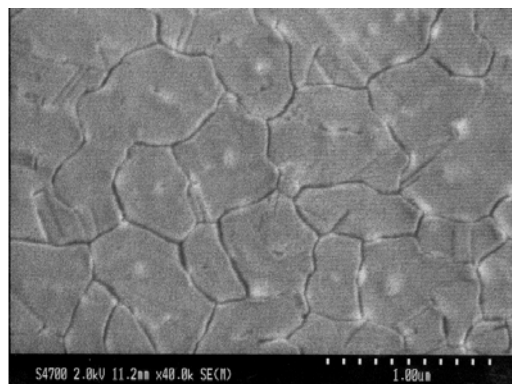

Figure 2.6(b). SEM graph of the 500Å poly-Si thin film crystallized in the SLG regime.

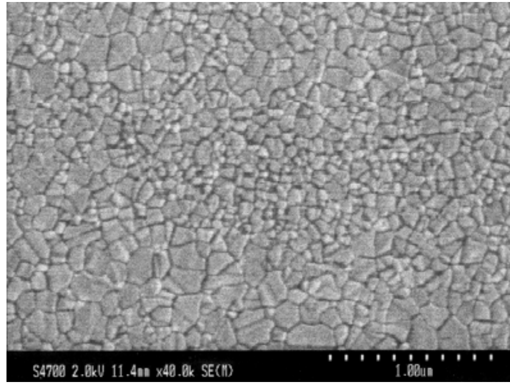

Figure 2.6(c). SEM graph of the 500Å poly-Si thin film crystallized in the full melting regime.

Fig. 2.7 (a) ~ 2.7(c) display the SEM graph of the 1000Å-thick poly-Si thin films crystallized in the three different recrystallization regimes. The substrate temperature during laser irradiation is maintained at 400°C and the shot number per unit area is 100 (i.e. 99% overlap). Fig. 2.7(b) is the micrograph of the poly-Si thin film crystallized in the SLG regime and Fig. 2.7(a) and 2.7(c) are the micrographs of the poly-Si thin film crystallized in the partial melting regime and full melting regime, respectively. Similar to the case of 500Å-thick poly-Si thin film, huge grains measuring above 1 μm can be found in the SLG regime. The grain sizes in either partial or full melting regime are also much smaller than those in the SLG regime.

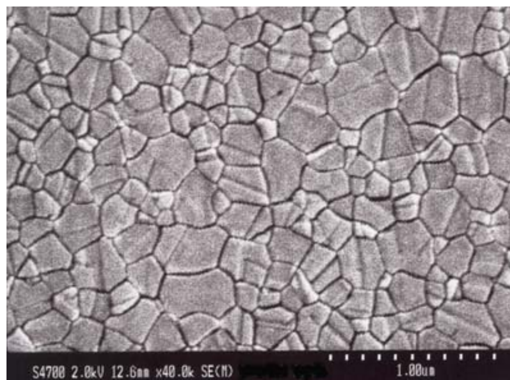

Figure 2.7(a). SEM graph of the 1000Å poly-Si thin film crystallized in the partial melting regime.

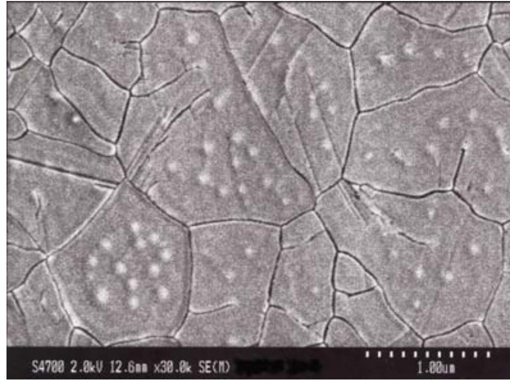

Figure 2.7(b). SEM graph of the 1000Å poly-Si thin film crystallized in the SLG regime.

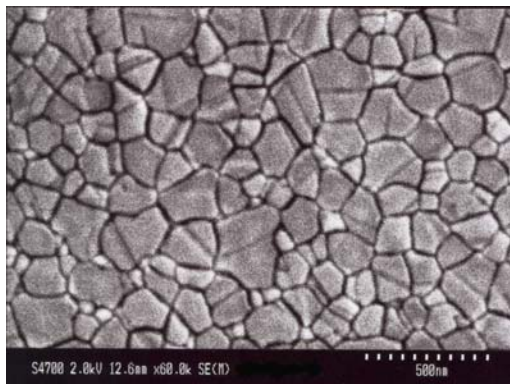

Figure 2.7(c). SEM graph of the 1000Å poly-Si thin film crystallized in the full melting regime.

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Figure 2.8 (a) and 2.8(b) show the 500Å- and 1000Å-thick poly-Si thin film crystallized in the SLG regime. Although large grains can be obtained in this regime, many small grains still spread between these large grains. This represents that the grain size distribution is fairly non-uniform in the SLG regime. The large deviation in grain size is resulted from the recrystallization mechanism of the SLG regime. According to SLG model, the lateral grain growth distance is determined by the quenching rate of liquid silicon and the retain-solid Si seed distance. Thus, a little deviation in spatial and/or pulse-to-pulse energy density and a-Si thin film thickness can easily result in partial or full melting of a-Si thin film at local region. Consequently, a very non-uniform grain size distribution is always observed in the SLG regime. The non-uniform grain distribution is the main cause of the enormous performance

variation of LTPS TFTs when the laser energy density is controlled in the SLG regime. The relationship between the grain size uniformity and the TFT performance variation will be investigated in the following section.

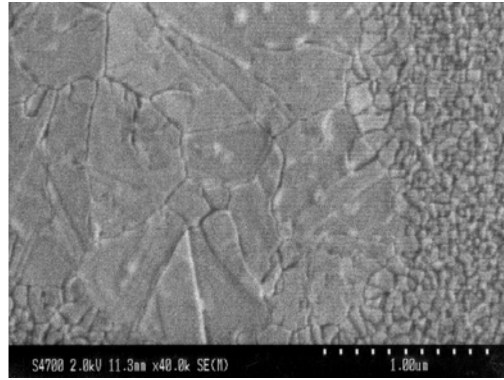


Figure 2.8(a). SEM graph of the 500Å poly-Si thin film crystallized in the SLG regime.

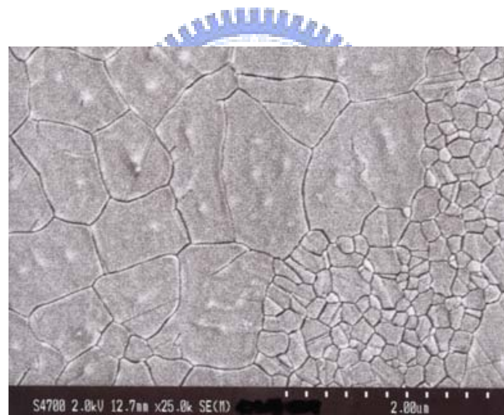


Figure 2.8(b). SEM graph of the 1000Å poly-Si thin film crystallized in the SLG regime.

2.2.3.1.2 Atomic Force Microscopy (AFM) Analysis

Figure 2.9(a) ~ 2.9(c) are the AFM images the 1000Å-thick poly-Si thin film crystallized in the three different recrystallization regimes. In this case, for the sake of simplicity, only 1000Å-thick poly-Si thin film crystallized at room temperature is used. The results are universal for the other cases. Fig. 2.9(b) is the image of the poly-Si thin film crystallized in the SLG regime and Fig. 2.9(a) and 2.9(c) are the image of the poly-Si thin film crystallized

in the partial melting regime and full melting regime, respectively. The surface roughness of the poly-Si thin film becomes obvious after laser irradiation. For the partial melting case, the surface roughness should be ascribed to the positive feedback of optical interference effect [2.22]. The roughness is determined by the total number of pulses incident on the surface. There is a positive feedback effect occurring in this situation with interference between the incident wave and a surface diffracted wave leading to a long range periodic surface roughness pattern which progressively enhances the interference effect with each subsequent pulse. For the full melting case, the surface roughness can also be attributed to the same mechanism.

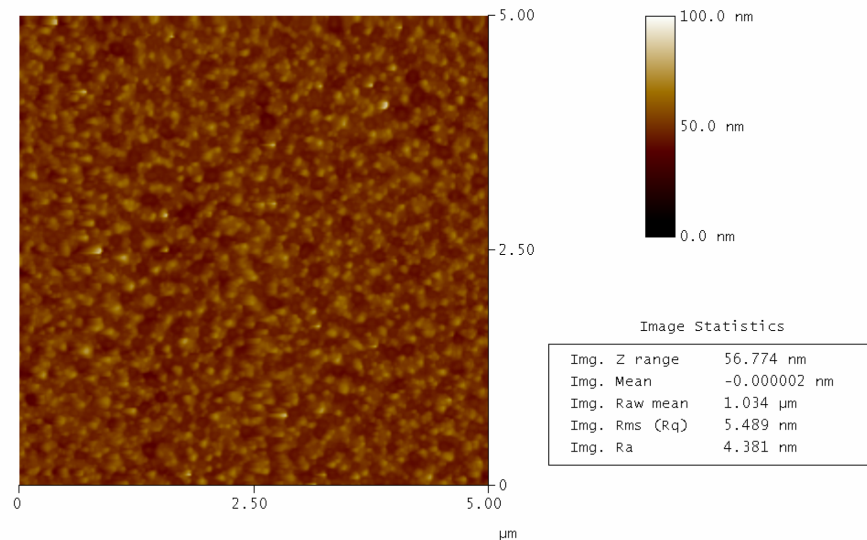


Figure 2.9(a). AFM image of the 1000Å poly-Si thin film crystallized in the partial melting regime.

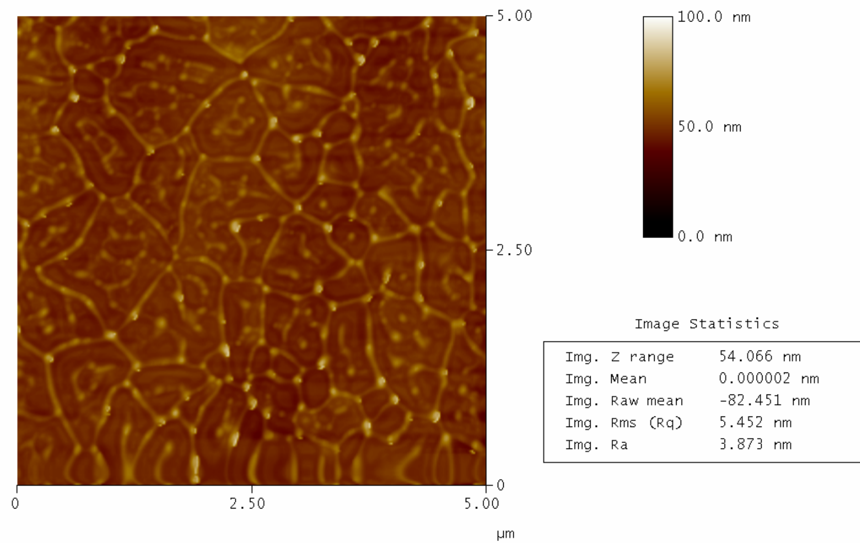


Figure 2.9(b). AFM image of the 1000Å poly-Si thin film crystallized in the SLG regime.

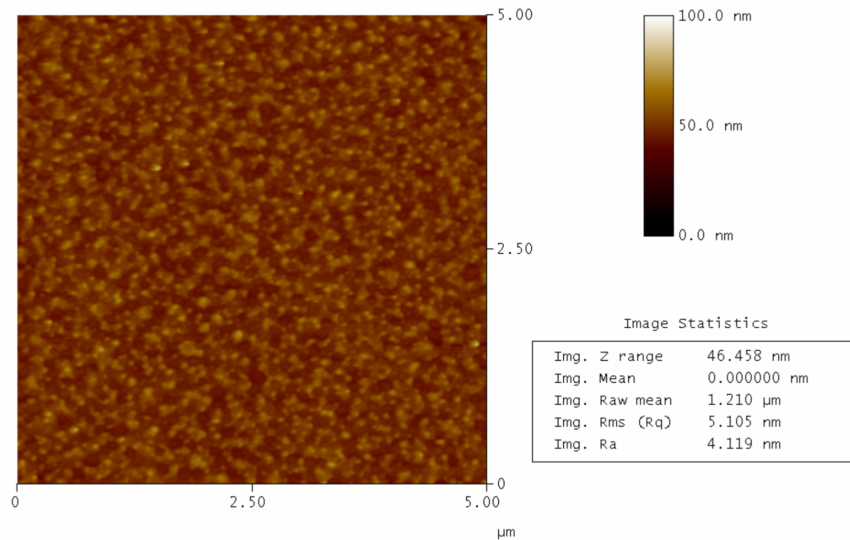


Figure 2.9(c). AFM image of the 1000Å poly-Si thin film crystallized in the full melting regime.

As shown is Fig. 2.9(b), for the SLG regime, the grains can be distinguished apparently

due to the huge hillock formation at the grain boundaries. The hillock is resulted from the freezing of capillary waves excited in the melting silicon during laser crystallization [2.23]. Grain boundaries and vertices, which typically are the last to freeze during lateral grain growth, have accumulated silicon due to the action of the expanded solid material on the remaining (denser) liquid material. When the laser crystallization begins, nucleated grains advance laterally through the denser liquid at first. As the solid regions grow, they fill a larger volume than the melt they consume. Eventually, the remaining liquid extends above the surrounding film. Where two grains meet to form a grain boundary, a ridge develops. Where three or more grains meet to form a vertex, a hillock may develop. From the view point of device operation, the roughness has a profound influence on the gate dielectric interface and the long-term reliability of poly-Si TFT.

2.2.3.2 Electrical Characterization of ELC LTPS TFT

Figure 2.10(a) ~ 2.10(d) show the dependence of field-effect mobility and threshold voltage of the ELC LTPS TFTs with 500Å-thick active layer on the applied laser energy density and substrate temperature during laser irradiation. The current-voltage characteristics were measured by using HP4156 precise semiconductor parameter analyzer. Twenty LTPS TFTs were measured for each laser process condition to provide an inspection on the uniformity of LTPS TFTs. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_d = (W/L) \times 10^{-8}$ A at $V_{ds} = 0.1$V. The maximum field effect mobility was extracted from the transconductance in the linear region at $V_d = 0.1$V. The solid squares in the figures are the average characteristic values at specific laser energy density and the vertical bars indicate the maximum and minimum characteristic values.

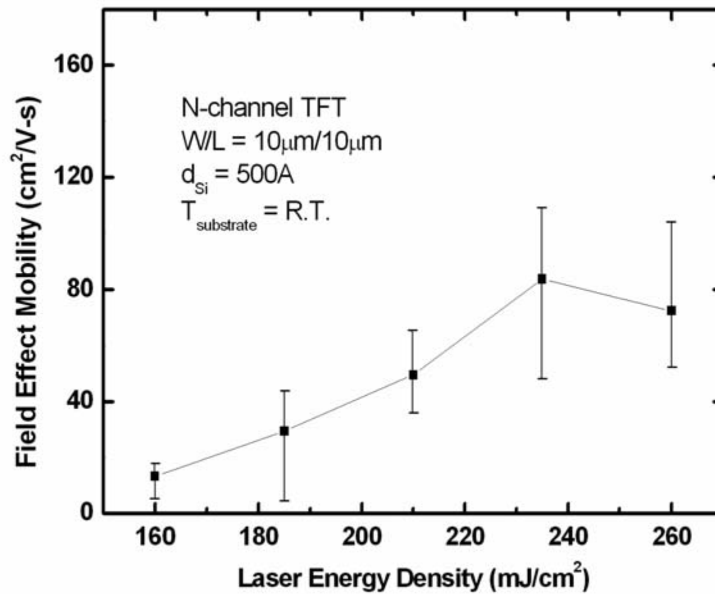


Figure 2.10(a). The dependence of field-effect mobility of LTPS TFTs with 500Å-thick active layer on the applied laser energy density for ELC performing at room temperature.

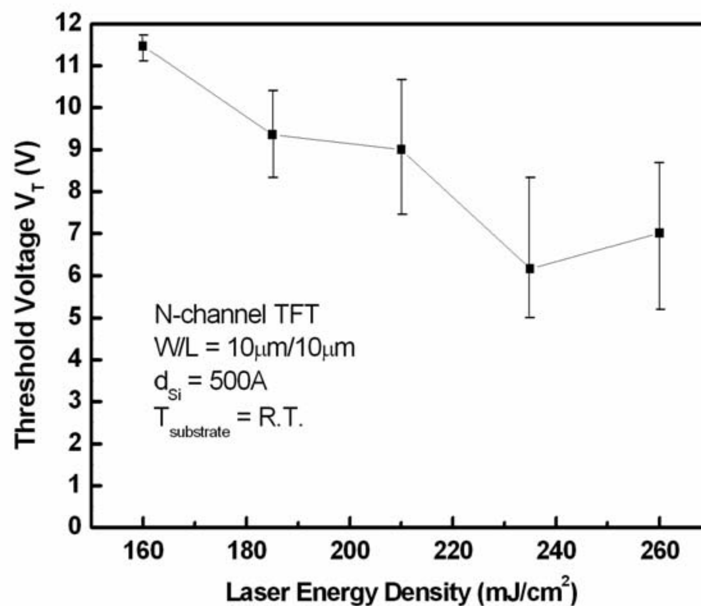


Figure 2.10(b). The dependence of threshold voltage of LTPS TFTs with 500Å-thick active layer

on the applied laser energy density for ELC performing at room temperature.

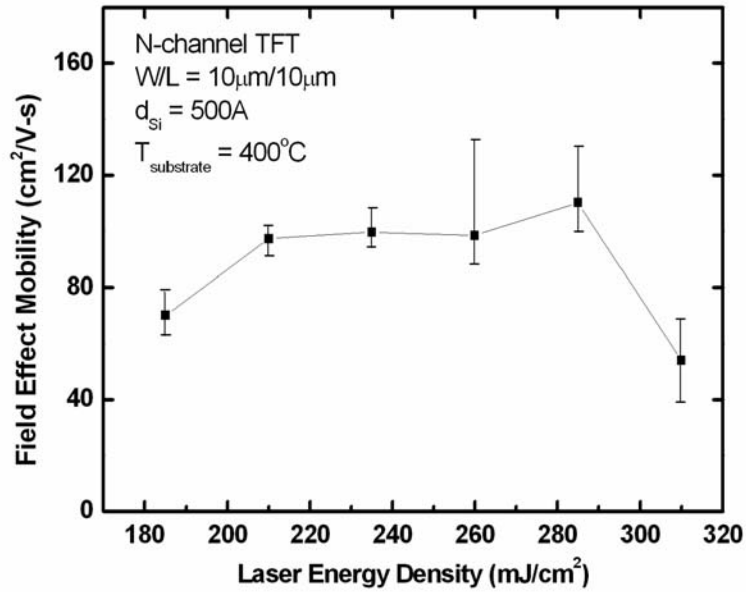


Figure 2.10(c). The dependence of field-effect mobility of LTPS TFTs with 500Å-thick active layer on the applied laser energy density for ELC performing at 400˚C.

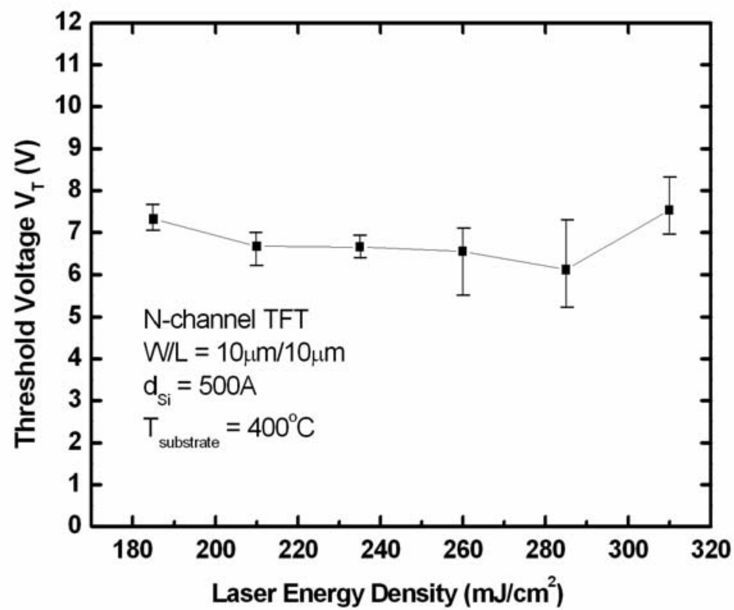


Figure 2.10(d). The dependence of threshold voltage of LTPS TFTs with 500Å-thick active layer

on the applied laser energy density for ELC performing at 400˚C.

Owing to the dependence of the grain size and the crystallinity of the poly-Si thin film

on the laser energy density, the applied laser energy density plays an important role in the eventual electrical characteristics of ELC LTPS TFTs. With increasing laser energy density, the field-effect mobility and threshold voltage of LTPS TFTs are ameliorated gradually as a result of the improvement in grain size and crystallinity. The reduction of the threshold voltage with increasing fluence indicates the change in the quality of poly-Si thin film. Devices whose channels have more defects simply require large gate voltage in order to fill the great number of traps before device can turn on. Thus, the threshold voltage is reduced as the grain size increased with increasing laser fluence. In addition, sudden increase in field-effect mobility and decrease in threshold voltage are observed within a narrow energy density range, accompanying a larger variation of TFT performance. Increase the substrate temperature during laser irradiation can broaden the narrow process window.

As discussed in former section, in the super lateral growth (SLG) regime, a little pulse-to-pulse and spatial deviation of the irradiation energy can easily cause partially or full melting of a-Si thin film, which means departure from the narrow SLG regime. Consequently, a non-uniform grain size distribution is always observed in the SLG regime. This non-uniform grain size distribution results in a large variation in the electrical characteristics of LTPS TFTs.

Besides, compare Fig. 2.10(a) ~ 2.10(d), increase the substrate temperature can not only increase the grain size but also improve the poor uniformity of grain size distribution [2.17], [2.24]. In this work, the a-Si surface was irradiated with an excimer laser beam having a trapezoidal intensity profile. As a result, in the laser irradiation edge region, where the laser energy density gradually decreases from maximum to zero, a region mixed of a-Si and small-grain poly-Si is created. When excimer laser irradiation is performed at room temperature substrate temperature on the first edge of the laser irradiation region (containing a mixture of a-Si and small-grain poly-Si), the surface temperature of this region should exceed the melting temperature of a-Si during exposure to a second equivalent overlapping

laser beam. However, the surface temperature should not exceed the melting temperature of the poly-Si. This is probably the main reason for the poor uniformity of the poly-Si in the laser irradiation overlap region in the case of laser annealing at room substrate temperature. For the 400°C substrate temperature, in the second-laser-recrystallized poly-Si region, the surface temperatures should exceed both a-Si and poly-Si melting temperature in the case of 400°C substrate temperature during laser irradiation. This suggests that the crystallinity of poly-Si thin film in the laser irradiation overlap region can be improved.

Figure 2.11(a) ~ 2.11(d) show the dependence of field-effect mobility and threshold voltage of the ELC LTPS TFTs with 1000Å-thick active layer on the applied laser energy density and substrate temperature during laser irradiation.

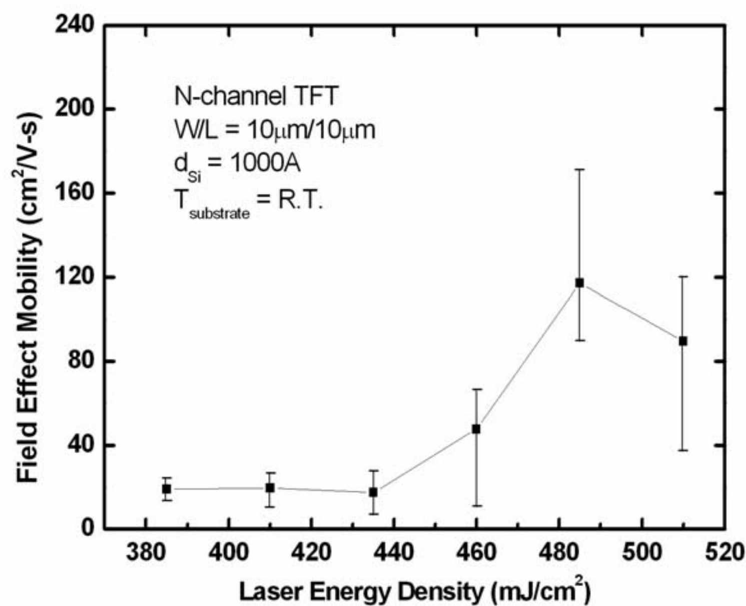


Figure 2.11(a). The dependence of field-effect mobility of LTPS TFTs with 1000Å-thick active

layer on the applied laser energy density for ELC performing at room temperature.

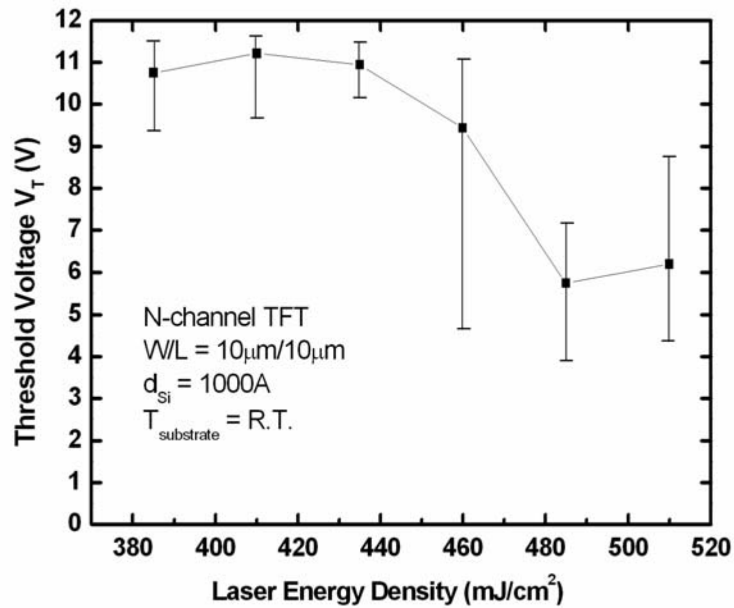
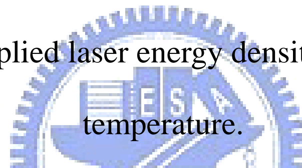


Figure 2.11(b). The dependence of threshold voltage of LTPS TFTs with 1000Å-thick active layer on the applied laser energy density for ELC performing at room temperature.



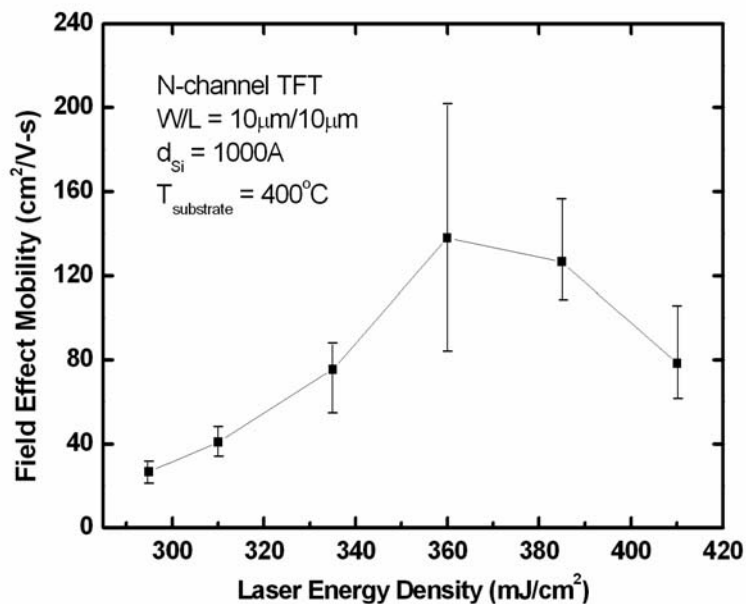


Figure 2.11(c). The dependence of field-effect mobility of LTPS TFTs with 1000Å-thick active

layer on the applied laser energy density for ELC performing at 400°C.

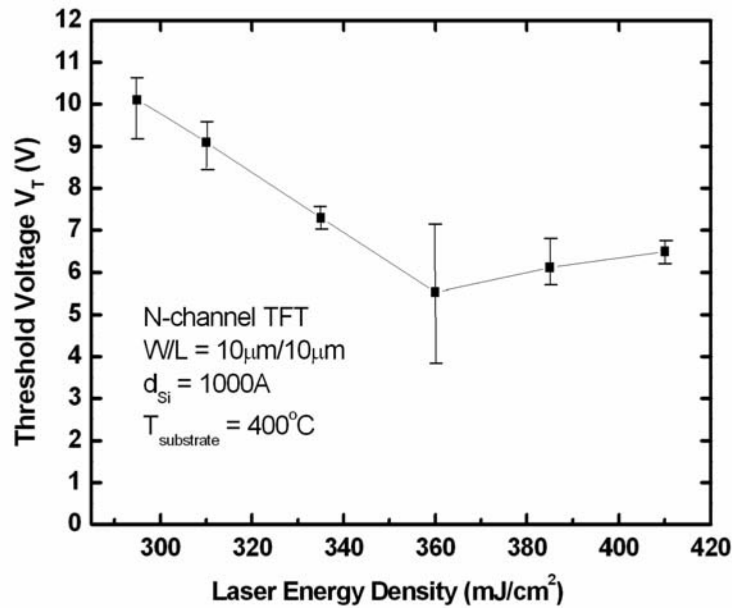


Figure 2.11(d). The dependence of threshold voltage of LTPS TFTs with 1000Å-thick active layer on the applied laser energy density for ELC performing at 400°C.

Similar to the 500Å-thick ELC LTPS TFTs, the field-effect mobility and threshold voltage of the 1000Å-thick ELC LTPS TFTs are improved gradually with increasing laser energy density. In addition, the narrow process window and non-uniform TFT electrical characteristics can also be observed in this case of 1000 Å-thick TFT devices. Increase the substrate temperature during laser irradiation enhances the device uniformity and enlarges the process window as well.

2.2.3.3 Short Channel Effect of ELC LTPS TFTs

Figure 2.12(a) ~ 2.12(d) show the dependence of field-effect mobility and threshold voltage of the ELC LTPS TFTs with 500Å-thick active layer on the device dimension and substrate temperature during laser irradiation. The applied laser energy density was controlled at optimum condition, i.e. super lateral growth (SLG) regime. Twenty LTPS TFTs were

measured for each laser process condition to provide an inspection on the uniformity of LTPS TFTs. The solid squares in the figures are the average characteristic values at specific device dimension and the vertical bars indicate the maximum and minimum characteristic values. Obviously, the field-effect mobility of LTPS TFTs is enhanced as the device dimension decreases. This can be attributed to the less grain boundaries and intra-grain traps existing inside the device active region. Grain boundaries and intra-grain defects cause deep and tail states which exert a profound influence on device characteristics and degrade carrier transport. Reduction of these trap state density can diminish the degraded effect in field-effect mobility.

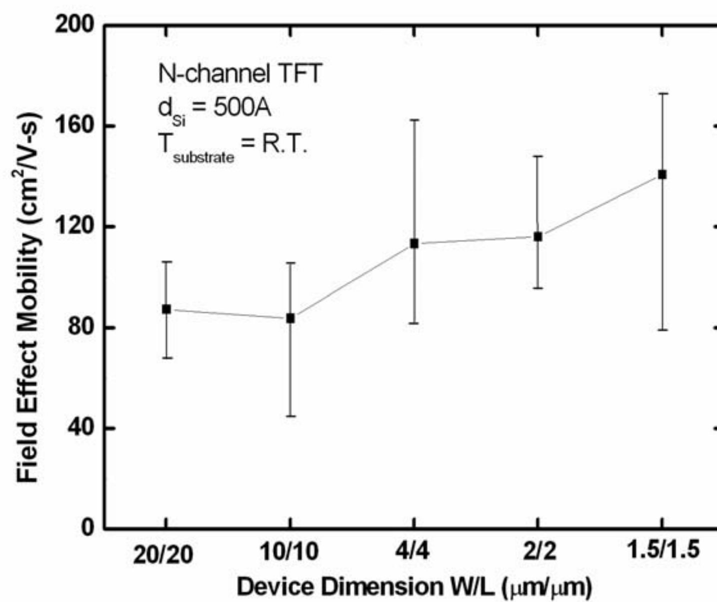


Figure 2.12(a). The dependence of field-effect mobility of LTPS TFTs with 500Å-thick active layer on the device dimension for ELC performed at room temperature.

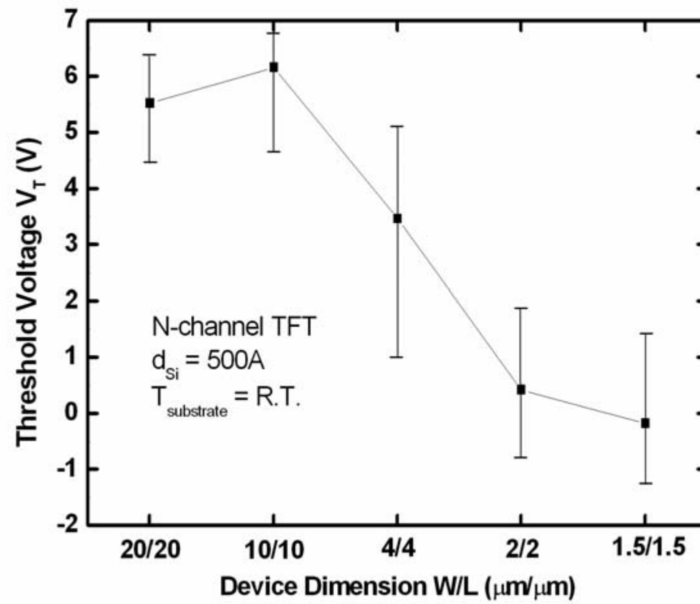


Figure 2.12(b). The dependence of threshold voltage of LTPS TFTs with 500Å-thick active layer on the device dimension for ELC performed at room temperature.

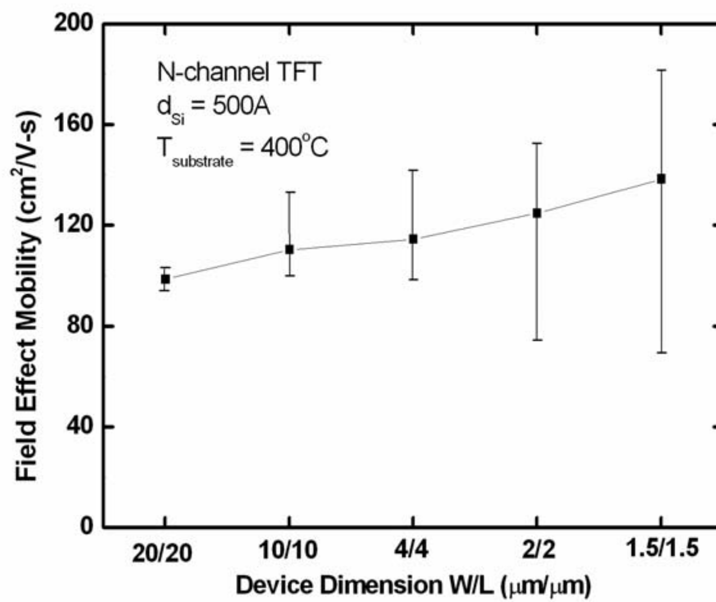


Figure 2.12(c). The dependence of field-effect mobility of LTPS TFTs with 500Å-thick active layer on the device dimension for ELC performed at 400°C.

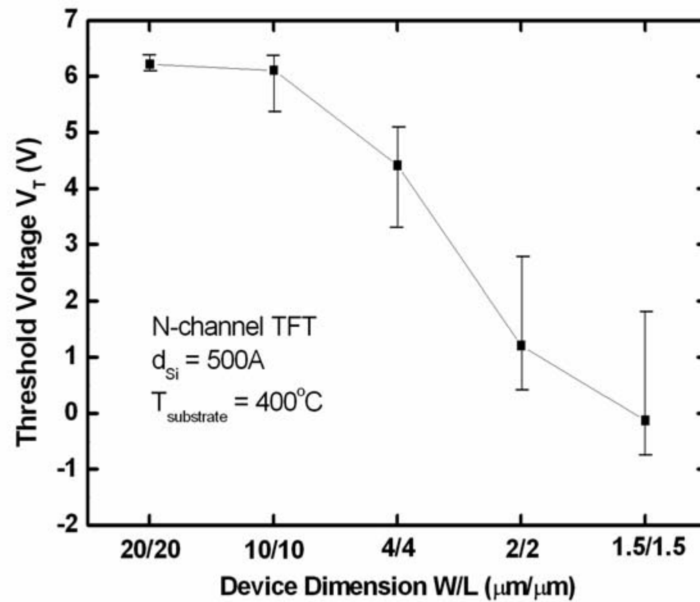


Figure 2.12(d). The dependence of threshold voltage of LTPS TFTs with 500Å-thick active layer on the device dimension for ELC performed at 400°C.

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On the other hand, the threshold voltage of LTPS TFTs dramatically decreases with the device dimension. The threshold voltages in this work are defined at a fixed drain current scaled by the device geometry, that is at a drain current of W/L x I_{DN} where I_{DN} is the same for all devices. This definition corresponds to approximately the same surface band bends for all devices. One of the possible reasons responsible for the decreasing threshold voltage is less trap state density existing inside the device region. Devices whose channels have more defects simply require large gate voltage in order to fill the great number of traps before device can turn on. Thus, the threshold voltage is reduced as the device dimension decreases. On the other hand, it has been shown that LTPS TFTs display very severe short-channel threshold shifts which may limit the extent to which gate lengths can be shrunk [2.25]-[2.26]. At low drain bias, the channel charge is partially supported by the source and drain, i.e. charge sharing model [2.27]. As the device geometry decrease, the total proportion of the

channel charge supported by the source and drain become more significant. Thus, the applied gate voltage needing to induce the same amount of channel free carrier is reduced.

In order to allow for adequate margins in applying the proper gate and data voltage, the uniformity of the device performance across the panel is very important. From Fig. 2.12(a) ~ 2.12(d), it can be obviously found that the device-to-device variation becomes more apparent as the device geometry shrinks gradually. This phenomenon is attributed to the laser annealing process. In general, the grain size of poly-Si thin film after excimer laser crystallization is approximate to 0.5μm ~ 1.5μm depending on the annealing condition and the grain distribution is fairly random. Under large device geometry, for example W/L = 10μm/10μm, there are at least 9 ~10 grains existing inside the channel region. Thus, the device characteristics are almost unchanged when the total number of grain inside the device region increases or decreases slightly. When the device geometry is shrunk closely to the grain size (<2μm), however, there may be only 2~3 grains distributing inside the device active region. Serious device-to-device performance variation occurs owing to the tiny change in the total number of grain inside the device channel region. Consequently, in addition to the short-channel effect, the phenomenon of poor device uniformity also puts huge limitation in the device dimension shrinkage of LTPS TFTs. This will restrict the technology development and product applications of LTPS TFTs in the future. One of the solutions is to form large uniform grains where the locations of the grain boundaries are artificially controlled and the grains are oriented in the same direction.

Figure 2.13(a) ~ 2.13(d) show the dependence of field-effect mobility and threshold voltage of the ELC LTPS TFTs with 1000Å-thick active layer on the device dimension and substrate temperature during laser irradiation. The phenomena discussed in the case of LTPS TFTs with 500Å-thick active layer are also observed apparently.

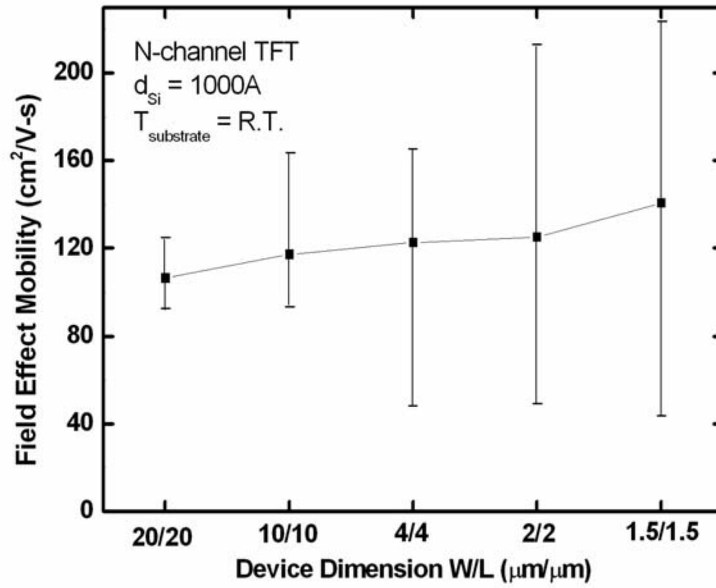

Figure 2.13(a). The dependence of field-effect mobility of LTPS TFTs with 1000Å-thick active layer on the device dimension for ELC performed at room temperature.

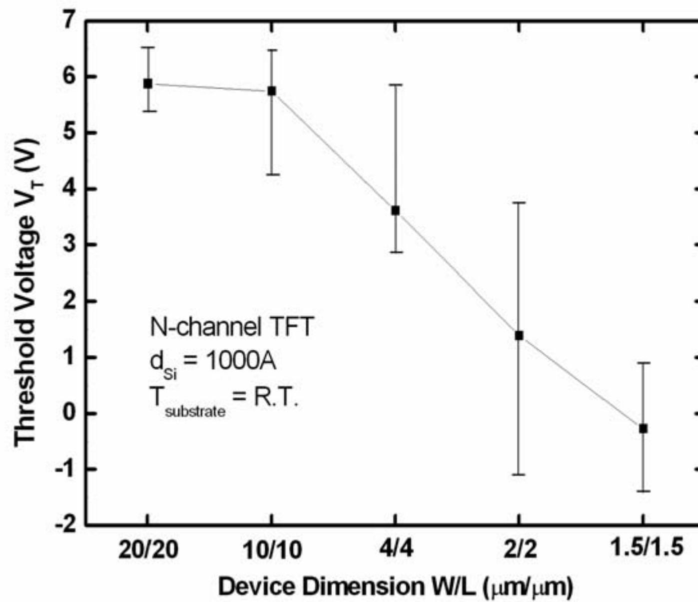

Figure 2.13(b). The dependence of threshold voltage of LTPS TFTs with 1000Å-thick active

layer on the device dimension for ELC performed at room temperature.

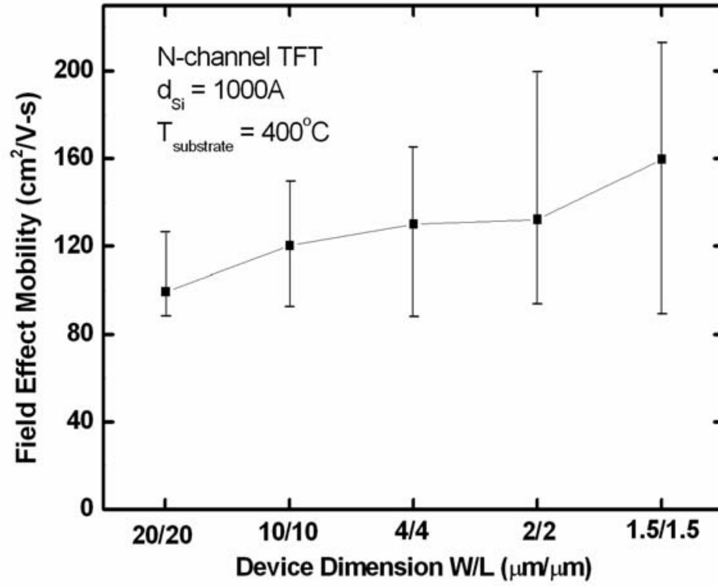

Figure 2.13(c). The dependence of field-effect mobility of LTPS TFTs with 1000Å-thick active layer on the device dimension for ELC performed at 400°C.

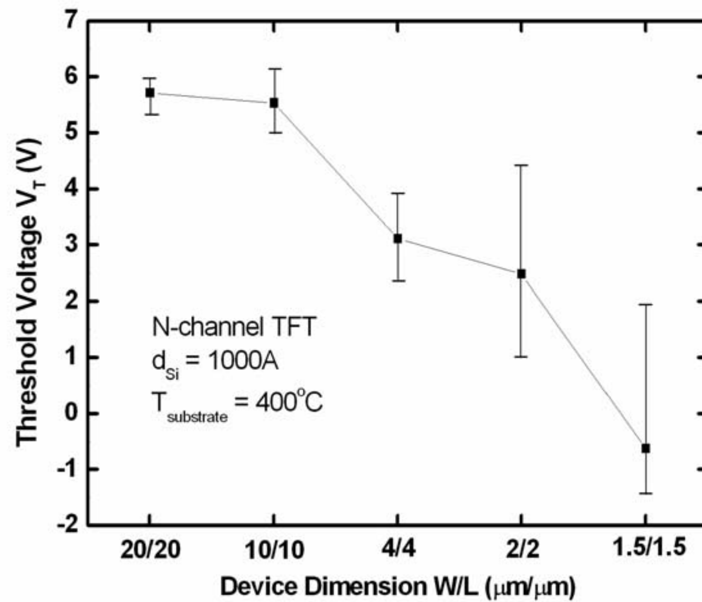

Figure 2.13(d). The dependence of threshold voltage of LTPS TFTs with 1000Å-thick

active

layer on the device dimension for ELC performed at 400°C.

2.3 Deposition and Reliability Analysis of Low-Temperature Gate Dielectric

2.3.1 Low-Temperature Deposition of SiO_2 Thin Film

The plasma enhanced chemical vapor deposited tetraethylorthosilicate (TEOS) oxide has been widely used in large-area electronics applications. Among these applications, high quality gate dielectric is one of the most important issues for fabricating high performance low-temperature polysilicon thin film transistors (LTPS TFTs). However, as-deposited TEOS gate oxide usually can hardly attain this requirement, especially for oxide electrical strength and long-term reliability issue, due to the poor interface with the rough silicon surface after laser crystallization. Thus, TEOS gate oxide have to be deposited thicker than necessary to overcome the surface roughness which reduces throughput, increases unit capacitance, reduces TFT drivability, worsens aperture ratio, and reduces power and brightness. On the other hand, post annealing or other post treatments have been used to further enhance the oxide quality. Post gate oxide densification with conventional furnace annealing (CFA) has been widely applied in high-performance LTPS TFTs [2.12] - [2.23]. Although the benefits of simplicity and low cost could be acquired, it requires a long process time (>2 hr.) and a high process temperature (~600°C), which maybe result in shrinkage of glass substrate. Recently, rapid thermal processing (RTP) has attracted large attention due to the short process time involved [2.14] – [2.15]. However, the thermal stress is the limiting factor. Plasma passivation has been used to improve the performance of LPTS TFTs [2.16]. When plasma treatment is applied to enhance oxide quality, it shows the benefits of low thermal budget. In this work, high quality TEOS oxide films were prepared by large-area plasma- enhanced chemical vapor deposition (LA-PECVD) system. The electrical characteristics of the

LA-PECVD TEOS oxide after various short-time plasma treatments were investigated as a function of plasma ambient and process time. The reliability tests including charge to breakdown (Q_{bd}) and bias temperature stress (BTS) were also analyzed in these samples.

2.3.2 Experimental Procedure

2.3.2.1 Low-Temperature SiO_2 Thin Film Deposition

In order to analysis the electrical characteristics of the as-deposited TEOS oxide, standard metal-oxide-semiconductor (MOS) capacitors were fabricated. After the complete RCA clean, gate oxide with a thickness of 620 Å was deposited on single crystal p-type <100> Si substrate by large-area plasma- enhanced chemical vapor deposition (LA-PECVD) system using TEOS- O_2 base chemistry. The substrate temperature during deposition was maintained at 400 °C and the gas flow rates of TEOS and O_2 were 20sccm and 1000sccm. After deposition of TEOS oxide, aluminum gate electrodes were deposited by thermal evaporation and patterned with lithography to isolate individual MOS capacitors. The area of the top aluminum electrode was $0.55mm^2$. The sintering step was performance at 400°C for 20min. Figure 2.14 displays the fabrication process of the MOS capacitors.

Cross-section transmission electron microscope (TEM) analysis was used to precisely investigate the thickness and uniformity of the TEOS oxide. The breakdown field and leakage current were measured by using HP4156A precise semiconductor parameter analyzer. The capacitance-voltage electrical characteristics such as interface state density (D_{it}) and flatband voltage (V_{fb}) were measured by using and Keithley quasi- & high-frequency system.

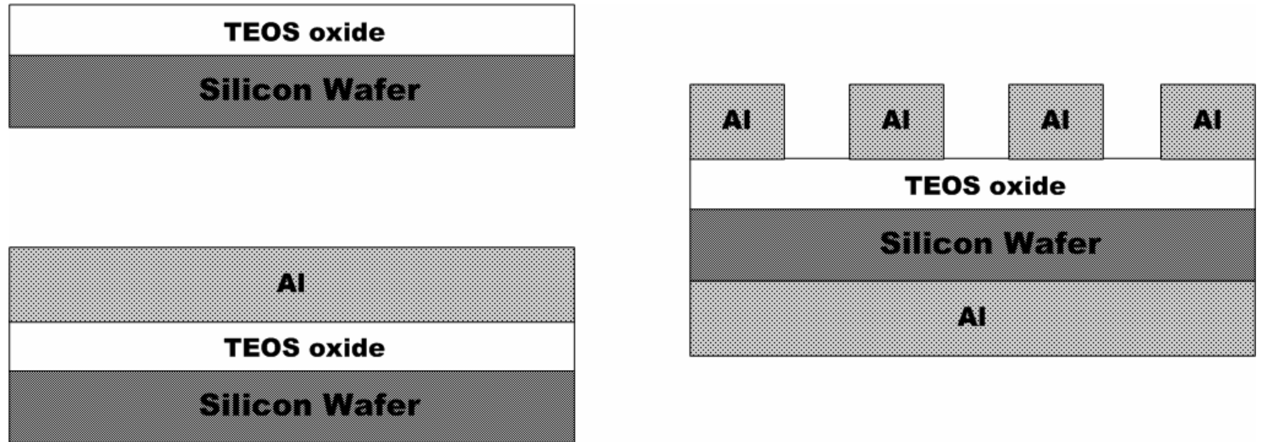

Figure 2.14. The key fabrication process of the MOS capacitors.

2.3.2.2 Post Plasma Treatment of SiO_2 Thin Film

Owing to the poor as-deposited electrical characteristics of the TEOS oxide, the post plasma treatment was adopted to further enhance the performance of the TEOS oxide. The key process flows was shown in Fig. 2.15. MOS capacitors were made on single crystal p-type <100> Si substrate. After the standard RCA clean, a 620 Å-thick gate oxide was deposited by LA-PECVD using TEOS- O_2 base chemistry. The substrate temperature during oxide deposition was kept at 400 °C and the gas flow rates of TEOS and O_2 were 20sccm and 1000sccm. After the deposition of TEOS oxide, the samples were subjected to various plasma treatments with different periods of time by using conventional parallel-plate PECVD. The plasma treatment parameters in this work were listed in Table 2-1. After the plasma treatment, aluminum gate electrodes were deposited by thermal evaporation and patterned with lithography to isolate individual MOS capacitors. The area of the top electrode was $0.55mm^2$. The aluminum sintering step was performed at 400°C for 20min.

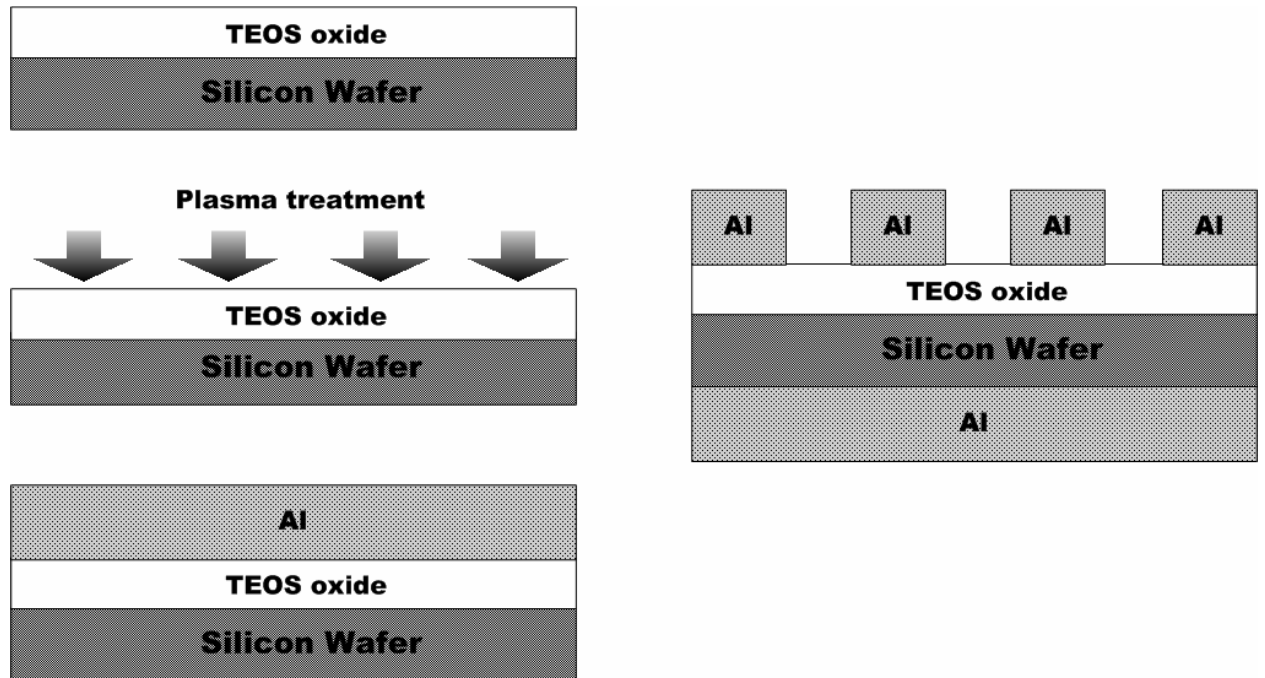

Figure 2.15. The key fabrication process of the plasma-treated MOS capacitors.

The electrical characteristics such as interface state density (D_{it}), flatband voltage (V_{fb}), breakdown voltage, and leakage current were measured by using HP4156A precise semiconductor parameter analyzer and Keithley quasi- & high-frequency system to investigate the effect of post plasma treatment. The electrical strength such as charge to breakdown (Q_{bd}) test and bias temperature stress (BTS) were also performed to analysis the long-term reliability of the plasma-treated TEOS oxide.

Table 2.1 Plasma treatment parameters

Plasma Conditions	
Gas	O_2, N_2O, NH_3
Flow Rate (sccm)	100
Power (W)	50
Pressure (mtorr)	500
Substrate Temperature (°C)	350

Time (min.)	5, 10, 20

2.3.3 Results and Discussion

2.3.3.1 Low-temperature SiO_2 Thin Film

Figure 2.16(a) and 2.16(b) are the cross-section TEM graphs of as-deposited TEOS oxide. From these two graphs, it can be seen that the TEOS oxide deposited by LA-PECVD has a smooth interface with Si substrate, and the variation of thickness is smaller than 2.5%. The capacitance-voltage (C-V) curve is illustrated in Fig. 2.17. The electrical characteristics of the as-deposited oxide are summarized in Table 2-2. According to these results, the TEOS oxide thin films prepared by the LA-PECVD process have good electrical properties.

Table 2-2. Electrical characteristics of the TEOS oxide deposited by LA-PECVD

Electrical Characteristics	
Breakdown Field (MV/cm) at Jg = 1.8 A/cm^2	10.54
Leakage Current Density (A/cm^2) at E=4MV/cm	3.02×10^{-9}
Flatband Voltage (V_{fb})	-1.672
Interface State (1/cm^2)	2×10^{10}

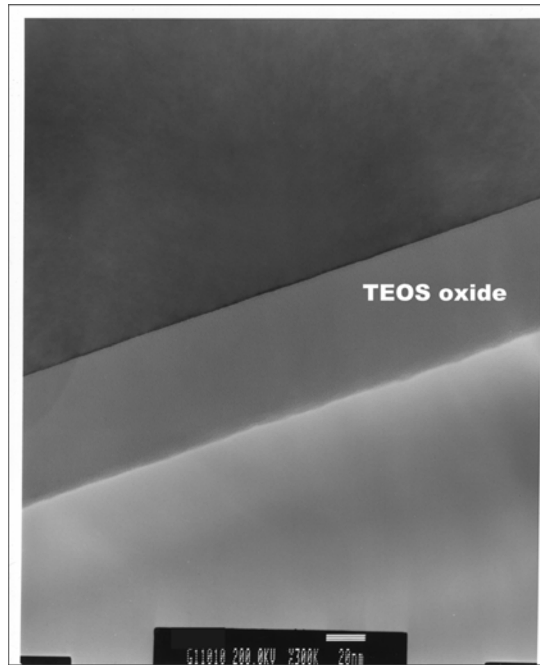

Figure 2.16(a). The cross-section TEM graphs of as-deposited TEOS oxide (X300K).

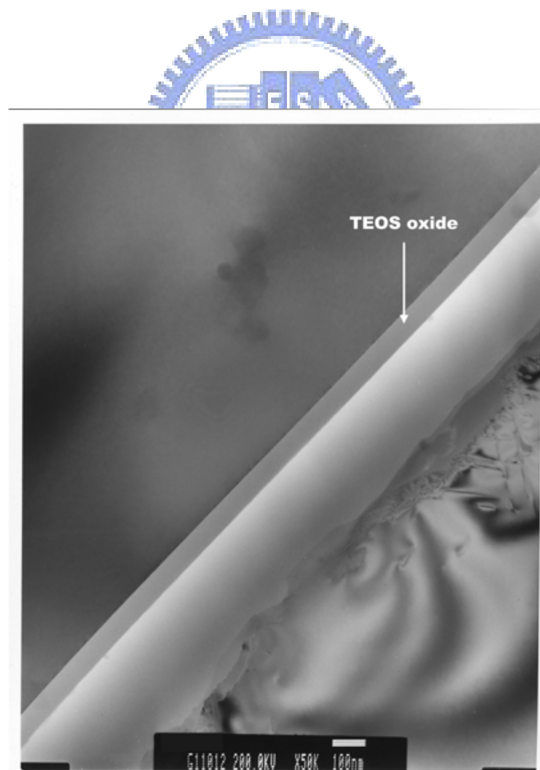

Figure 2.16(b). The cross-section TEM graphs of as-deposited TEOS oxide (X50K).

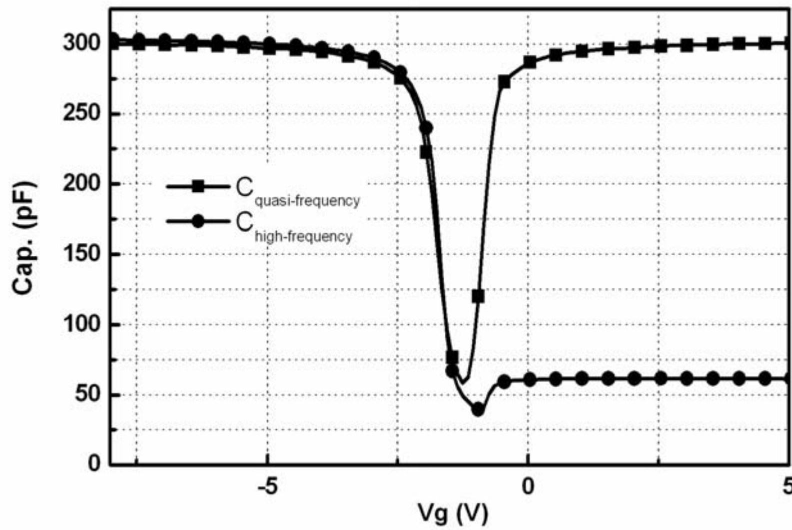

Figure 2.17. The capacitance-voltage (C-V) characteristic of the as-deposited TEOS oxide.

2.3.3.2 Long-Term Reliability of Post-Plasma-Treated SiO_2 Thin Film

To further improve the performance of the as-deposited TEOS oxide, different short-time plasma treatments were applied. Figure 2.18 shows the effects of different short-time plasma treatments on time-zero dielectric breakdown (TZBD). The breakdown field was defined as the electrical field across the TEOS oxide when the leakage current density was 1.8 A/cm^2 and the influence of flatband voltage was also excluded. The TZDB field starts increasing after 5-min treatment for NH_3 and N_2O plasma. Furthermore, NH_3 plasma exhibited higher enhancement efficiency than N_2O plasma. This might due to the high dissolution efficiency of nitrogen atoms in NH_3 plasma. The improved characteristics after nitrous ambient treatment are believed to be due to various reasons such as reduced interface stress, stronger Si-N bonds and the oxynitride layer acting as a barrier for hydrogen diffusion [2.28]. Hydrogen and nitrogen atoms passivate the dangling bonds as well as the strained bonds at the Si/SiO_2 interface and in the bulk oxide. However the TZDB field was degraded

after 20-min NH_3 plasma treatment. This can be attributed to more hydrogen atoms incorporating into the oxide thin film after further increasing NH_3-plasma treatment time. The incorporated hydrogen atoms might react with Si-O bonds and then formed Si-OH and Si-H bonds [2.29]. The more the Si-OH and Si-H bonds, the lower the breakdown field.

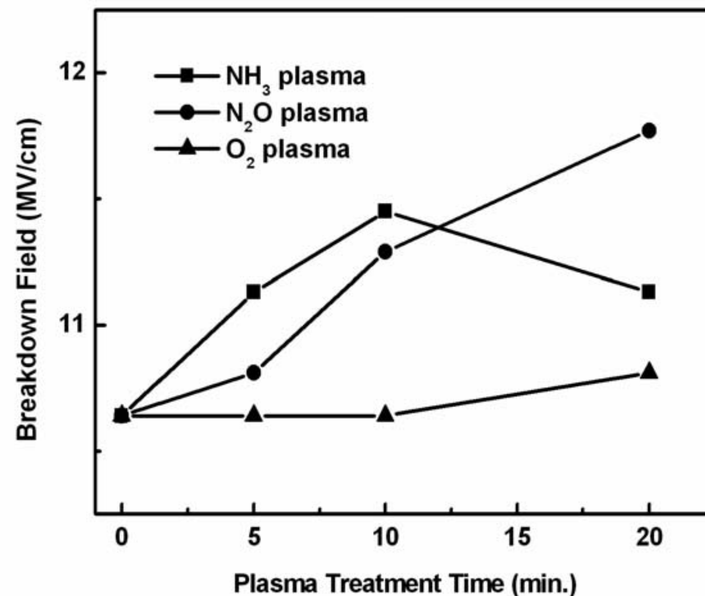

Figure 2.18. Time-zero dielectric breakdown Characteristics of TEOS oxide as a function of treatment time under different plasma ambient

For O_2 plasma treatment, there was no encouraged effect on the breakdown field. Instead, the breakdown field is degraded after 5-minute and 10-minute treatments. One reason might be attributed to the fact that the generated oxygen radicals impinged on the Si-O bonds in the TEOS oxide thin films and reacted with the oxygen atom to form the oxygen molecule, which diffused out of the films eventually [2.30]. The decrease of oxygen content caused by O_2-plasma treatment has been proven by Chen *et al.* using SIMS [2.31]. This phenomenon caused the composition of the TEOS oxide be far from stoichiometric SiO_2 and became more porous than the original. The breakdown field and leakage current density (not shown here), therefore, were deteriorated.

The charge-to-breakdown (Q_{bd}) characteristics of these plasma-treated TEOS oxide are shown in Figure 2.19. The stress was done at room temperature with a constant current density of –90.22 mA/cm^2.

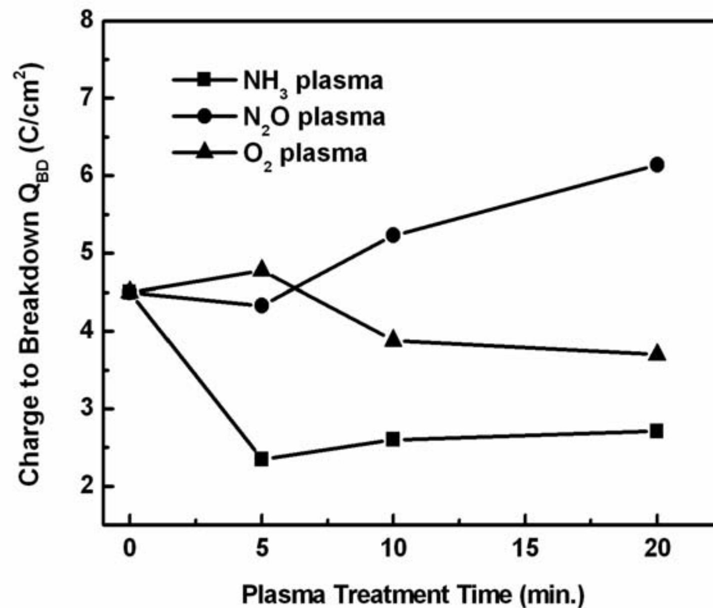

Figure 2.19. Charge-to-breakdown characteristics of TEOS oxide as a function of treatment time

under different plasma ambient.

It could be found that a significant improvement in Q_{bd} after 10-minute treatment in N_2O plasma. On the contrary, the O_{bd} was degraded in both NH_3- and O_2-treated TEOS oxide. The difference between N_2O and NH_3 plasma treatment can be explained by the incorporation of hydrogen atoms. In NH_3 plasma ambient, hydrogen atoms were incorporated in the oxide and passivated the dangling and strained bonds. When the negative constant current stress is applied, i.e. gate injection, the interface between SiO_2 and Si substrate is the primary damage site [2.31]. During the gate injection, the energetic electrons were emitted to the substrate interface and impinge on the weak Si-H bonds. Then the weak Si-H bonds were broken and some dangling bonds were created. The dangling bonds acted as the trapping centers of

electrons and holes and thus resulted in the degradation of Q_{bd}. With N_2O plasma treatment, the strong Si-N bonds were formed in the oxide thin films, which resulted in an improvement of Q_{bd}.

The decrease of Q_{bd} of O_2-plasma treated oxide thin films could be attributed to the decrease of oxygen content in TEOS oxide thin films as mentioned above, which could create more defects in the oxide. Therefore, O_2-plasma treatment did not seem to be a good method to improve the quality of TEOS oxide thin films.

The dependence of the bias temperature instability on the TEOS oxide thin films with NH_3 and N_2O plasma treatments was investigated. The change in interface state density after stress is shown in Figure 2.20. The bias temperature stress was done at 140°C for 10 minutes with an applied voltage of –25V. It can be seen that the N_2O-plasma treated oxide thin films show superior stability than the NH_3-plasma treated ones for 5- and 10-minutes annealing. The hydrogen atoms existing in the oxide also acted as a primary instability factor. N. Bhat *et al* have shown that the bias temperature instability is caused by hydrogen induced trap creation [2.32]. More hydrogen atoms existing in the oxide after NH_3 plasma treatment, more weak Si-H bonds were easily broken by the impingement of electrons at elevated temperature even when the electric field was low. Therefore the interface state density was deteriorated more significantly for NH_3-plasma treated oxide thin films than N_2O-plasma treated ones.

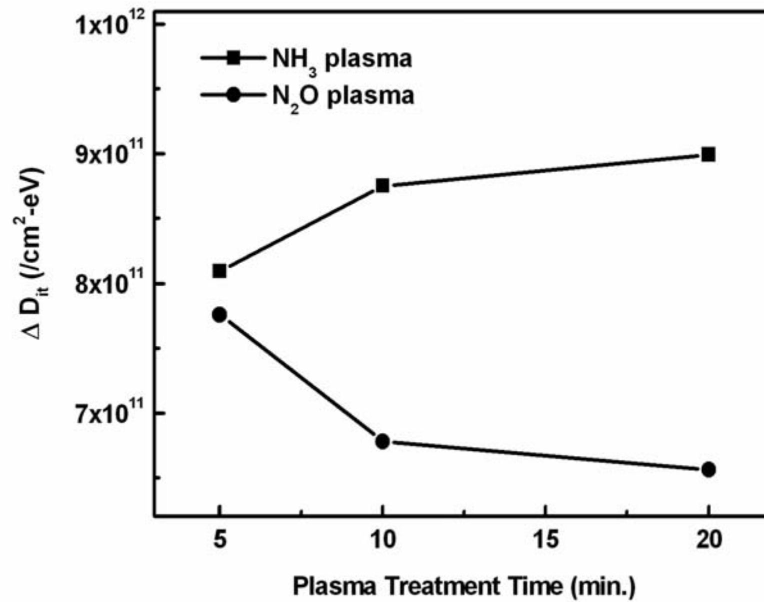

Figure 2.20. Bias temperature instability characteristics of TEOS oxide as a function of

treatment time with NH_3 & N_2O plasma ambient.

2.4 Summary

Conventional LTPS TFTs fabricated by excimer laser crystallization has been investigated in detail in this work. From the material and electrical characteristics analyses, it has been obviously found that the applied laser energy density has a great influence on the performance of LTPS TFTs. Narrow process window and poor device uniformity can easily observed in LTPS TFT fabricated with different kinds of laser irradiation conditions. The variation of device performance became more and more apparent when the device geometry shrunk. Increase the substrate temperature could enlarge the process window and improve the device uniformity of LTPS TFTs.

High quality low-temperature deposited TEOS oxide thin films have been formed by

using LA-PECVD system. Different short-time plasma treatments, such as O_2, N_2O, and NH_3, were applied in our experiments. The electrical properties, such as TZDB, Q_{bd}, and BTS, were used to explain the effects of plasma treatments. It was shown that the electrical strength of oxide was improved after N_2O and NH_3 plasma treatments. In addition, NH_3 plasma treatment exhibited the highest enhancement efficiency. O_2 plasma treatment, however, showed some harmful effects on the electrical properties of the TEOS oxide. On the other hand, samples with N_2O plasma treatment showed superior stress endurance in the Q_{bd} test and BTS. As a consequence, N_2O plasma treatment might seem to be the best choice to manufacture high quality TEOS oxide films for low-temperature poly-Si TFTs with better long-term stability.