Chapter 4

Fabrication of Low-Temperature Polycrystalline Silicon-Germanium Thin Film Transistors by Using Novel Germanium Excimer Doping Method

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4.1 Introduction

In recent, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) become more noticeable owing to their attractive applications in active matrix displays, such as LCDs and OLEDs [4.1] - [4.14]. Active matrix displays with integrated circuits on a single glass substrate can be implemented by high-mobility LTPS TFTs [4.15]. Since the device driving capability will crucially influence the performance of the integrated circuits, the mobility of the device becomes a significant problem. To achieve high mobility for high-speed operation, excimer laser crystallization (ELC) has been widely used to fabricate LTPS TFTs [4.16] - [4.17]. According to the previous reports, the mobility would be limited to a saturation value due to other unfavorable effects, such as large surface roughness [4.18] – [4.19], restricted grain size, and poor low-temperature gate dielectric quality. Even though the mobility of ELC poly-Si TFT can meet the requirements for many circuit applications, further enhancement of mobility is necessary for high-level system integration. Essentially, Ge

incorporated in Si (i.e. $Si_{1-x}Ge_x$) can not only lower the process thermal budget, but also promote the carrier mobility; hence, $Si_{1-x}Ge_x$ seems to be a potential material for the active layer of a TFT [4.20] – [4.22]. According to the results reported by Julie A. Tsai *et al.*, poly-$Si_{1-x}Ge_x$ TFTs have been found to have higher mobility than similarly processed poly-Si TFTs [4.22]. However, most of the poly-$Si_{1-x}Ge_x$ TFTs were fabricated by using conventional solid-phase crystallization [4.23] - [4.24]. Only a few studies have been conducted for the ELC poly-$Si_{1-x}Ge_x$ TFT [4.25].

In the previous chapter, it has been found that direct laser annealing of amorphous $Si_{1-x}Ge_x$ (a-$Si_{1-x}Ge_x$) thin film would result in a serious Ge segregation at film surface and grain boundaries. This would lead to the degraded electrical characteristics of poly-$Si_{1-x}Ge_x$ TFTs. The phenomenon of Ge segregation might be resulted from the 478°C different in melting point between Ge and Si atoms. Due to the higher melting point of Si compared to Ge, the Si atoms in the melting $Si_{1-x}Ge_x$ thin film would be expected to solidify first. At the end of solidification, numerous Ge atoms would aggregate at the grain boundary and film surface, where were the last solidification region during ELC process. By the way, according to the results of our work, directly laser annealing of a-$Si_{1-x}Ge_x$ thin film would also result in small grain size due to the high nucleation rate of low-melting-point $Si_{1-x}Ge_x$ thin film. On the other hand, the atomic concentration of Ge in the active layer should be kept in the moderate low level due to the apparent alloy scattering at high Ge concentration. As a result, two kinds of modified processes for fabricating the ELC poly-$Si_{1-x}Ge_x$ TFTs are demonstrated in this work. The feature of the two proposed processes is to reduce the above-mentioned phenomena during ELC process, such as serious Ge segregation, poor $Si_{1-x}Ge_x$ thin film, and high Ge concentration in the surface channel.

In the first part of this work, ELC poly-$Si_{1-x}Ge_x$ TFTs with a-Si/ a-$Si_{1-x}Ge_x$ double layers are demonstrated to minimize the Ge segregation effect during ELC process. In this process, two excimer laser irradiations with two different laser energy densities and laser shot

numbers are performed. The first laser irradiation is used to crystallize the a-$Si_{1-x}Ge_x$ thin film and the second laser irradiation is carried out to introduce the Ge diffusion upward into the above Si layer. The surface segregated Ge resulted from the first laser annealing of a-$Si_{1-x}Ge_x$ thin film acts as the Ge diffusion source for the Si capping layer during the second excimer laser irradiation. Although the device performances are improved by introducing a Si capping layer, the crystallinity of the active layer is still worse owing to the recrystallization of a-$Si_{1-x}Ge_x$ thin film. Thus, another modified fabrication process is proposed to further improve the poor crystallinity of the poly-$Si_{1-x}Ge_x$ thin film based on the first modified process flow.

In the second part of this work, a Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs with lower Ge concentration and better crystallinity in the active layer is proposed. A-$Si_{1-x}Ge_x$/poly-Si double-layers structure is adopted to fabricate high quality ELC poly-$Si_{1-x}Ge_x$ thin film. Similarly, two excimer laser irradiations with two different laser energy densities and laser shot numbers are used. The first laser irradiation is used to crystallize the a-Si thin film and the applied laser energy density is controlled in the super-laser-growth regime. Thus, large grain size and excellent crystallinity can be observed in the ELC poly-Si thin film. During the second laser irradiation, the Ge will diffuse naturally into the underneath poly-Si layer due to the high diffusion coefficient of Ge in melting silicon and the Ge concentration gradient. When the second laser irradiation is performed, laser energy density must be carefully controlled so that the poly-Si is partially melted. These grains can vertically regrow with a high vertical regrowth rate from the unmelted poly-Si. Therefore, the Ge segregation can be improved remarkably and the large grain size will not be significantly changed [4.26]. The novel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs demonstrates excellent carrier mobility and driving current under small device dimension due to better crystallinity and mobility enhancement by Ge atom incorporation.

4.2 Experimental Procedure

4.2.1 Fabrication of ELC Poly-$Si_{1-x}Ge_x$ TFTs with Si capping Layer

The self-aligned p-channel poly-$Si_{1-x}Ge_x$ TFTs with Si acpping layer were fabricated on oxidized silicon wafer. All processes were conducted at temperature below 450˚C, except for a-Si layer deposited by low-temperature chemical vapor deposition (LPCVD) at 550˚C.

The p-channel poly-$Si_{1-x}Ge_x$ TFTs with a Si capping layer were fabricated by the following sequence of processes, and the key processes are illustrated in Figure 4.1. Before deposition of a-$Si_{1-x}Ge_x$ thin film, the oxidized silicon wafer was exposed to the pure silane (SiH_4) precursor for 10 minutes at 450˚C by LPCVD to improve the nucleation of a-$Si_{1-x}Ge_x$ on SiO_2. This killed the long incubation time found for a-$Si_{1-x}Ge_x$ thin film deposition on an oxide surface [4.27]. Next, a-$Si_{1-x}Ge_x$ thin film of a 500Å thickness was deposited on oxidized silicon wafer by decomposition of silane (SiH_4) and germane (GeH_4) with LPCVD at 450°C. Different GeH_4 to SiH_4 gas flow ratios were adopted to deposit a-$Si_{1-x}Ge_x$ thin film with various Ge atomic concentrations. And then, the a-$Si_{1-x}Ge_x$ thin film was irradiated by a semi-gaussian shaped KrF excimer laser at room temperature in a vacuum ambient pumped down to 10^{-3} torr. The shot numbers per unit area were 100 and the laser energy density was controlled in the super-lateral-growth regime to acquire the largest grain size. After the first laser irradiation, another 500Å-thick a-Si thin film was deposited on top of the ELC poly-$Si_{1-x}Ge_x$ thin film by LPCVD at 550℃. Next, the second excimer laser irradiation was performed to crystallize the upper a-Si thin film at room temperature. The shot numbers per

unit area are 100. Laser energy density was carefully controlled so that the a-Si thin film was fully melted and the original poly-$Si_{1-x}Ge_x$ thin film was in partially melting region. The Ge atoms diffused upward into the Si layer during laser irradiation and naturally formed poly-$Si_{1-x}Ge_x$ thin film in the end. The Ge concentration in the eventual poly poly-$Si_{1-x}Ge_x$ thin film was adjusted by the initial Ge concentration of the a-$Si_{1-x}Ge_x$ thin film. After defining the active layer, a 1000Å-thick TEOS gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. A 3000Å-thick Al thin film was deposited by thermal evaporation. Then, the Al thin film was etched by reactive ion etching (RIE) to form gate electrodes, and the gate oxide was also removed by RIE in sequence. After the gate electrodes were patterned, a self-aligned B^+ ion implantation with the dose concentration of 5×10^{15} cm^{-2} was carried out to form the source and drain regions. A 3000Å TEOS oxide was deposited by PECVD at 350°C as passivation layers. Then, excimer laser annealing was performed to activate the implanted dopants and recrystallize the source and drain region at room temperature. The shot numbers per unit area used for dopant activation were 20 and the laser energy density was controlled in the partial melting regime. After contact holes opening, Al was deposited by thermal evaporation and patterned to form the electrical connecting pads. Finally, the devices were treated with NH_3 plasma by PECVD for four hours. Conventional ELC poly-Si TFTs were also fabricated for comparison.

The typical transfer and output characteristics of the ELC poly-$Si_{1-x}Ge_x$ TFTs were measured by HP4156 precise emiconductor parameter analyzer. The device parameters including field-effect mobility, threshold voltage, subthreshold swing and ON/OFF current ratio were extracted from the measured characteristics. The electrical performances of the ELC poly-Si controlling samples were also estimated to compare with the ELC poly-$Si_{1-x}Ge_x$ counterparts.

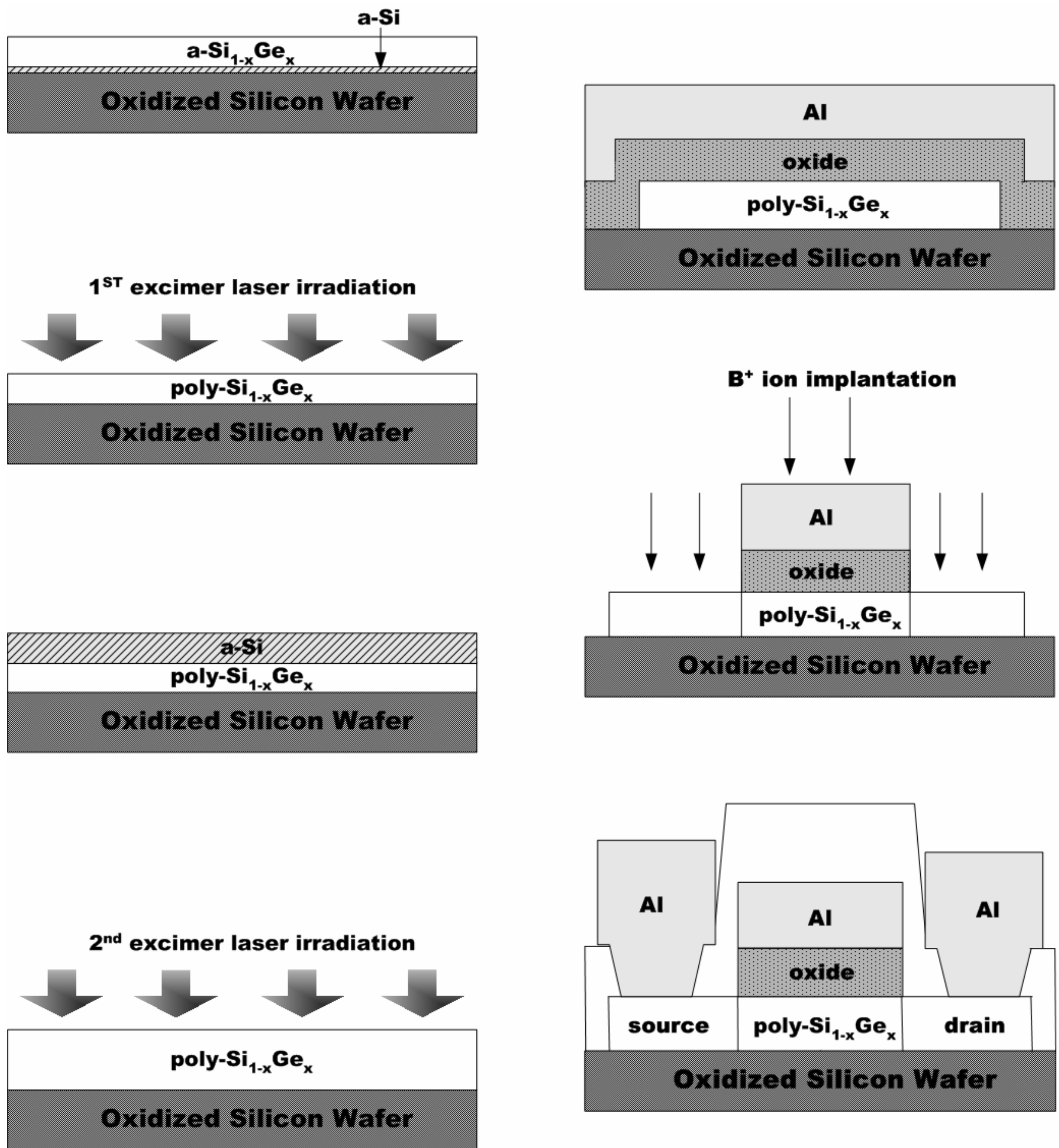


Figure 4.1. The key fabrication process of ELC poly-$Si_{1-x}Ge_x$ TFTs with Si capping layer.

4.2.2 Fabrication of Ge-Doped ELC Poly-$Si_{1-x}Ge_x$ TFTs.

In order to further improve the device performance of poly-$Si_{1-x}Ge_x$ TFTs, another novel fabrication process was proposed. All processes were also conducted at temperature below 450°C, except for a-Si layer deposited by low-temperature chemical vapor deposition (LPCVD) at 550°C.

Figure 4.2 illustrates the key processes for fabrication of the n- and p-channel poly-$Si_{1-x}Ge_x$ TFTs. At first, a-Si thin film with a 500Å thickness was deposited on oxidized Si wafers by LPCVD at 550°C. Then, the a-Si thin film was crystallized by a semi-gaussian shaped KrF excimer laser irradiation at room temperature in a vacuum ambient pumped down to 10^{-3} torr with optimal laser conditions, i.e. a shot density of 100 shots per area (99% overlapped) and energy density lying in the super-lateral-growth regime. After first laser irradiation, a-$Si_{1-x}Ge_x$ thin film of a 100Å thickness was deposited on the ELC poly-Si thin film by decomposition of silane (SiH_4) and germane (GeH_4) with LPCVD at 450°C. Different GeH_4 to SiH_4 gas flow ratios were adopted to deposit a-$Si_{1-x}Ge_x$ thin film with various Ge atomic concentrations. To obtain poly-$Si_{1-x}Ge_x$ thin film, the a-$Si_{1-x}Ge_x$ thin film was then subjected to the second excimer laser irradiation at room temperature in a vacuum ambient pumped down to 10^{-3} torr with a shot density of 10 shots per area (90% overlapped). Laser energy density was carefully controlled so that the a- $Si_{1-x}Ge_x$ thin film was fully melted and the original poly-Si_1 thin film was in partially melting region. The Ge atoms diffused downward into the poly-Si layer during laser irradiation and naturally formed poly-$Si_{1-x}Ge_x$ thin film in the end. The Ge concentration in the eventual poly poly-$Si_{1-x}Ge_x$ thin film was adjusted by the initial Ge concentration of the a-$Si_{1-x}Ge_x$ thin film. The RBS analysis revealed that the Ge atomic concentrations in the eventual poly-$Si_{1-x}Ge_x$ thin film were 5% and 9%. In

addition, according to the AES analysis results, the atomic concentration of Ge atom was a little higher at the film surface than in the bulk of the poly-$Si_{1-x}Ge_x$ thin film after the second laser irradiation. And then, the poly-$Si_{1-x}Ge_x$ thin films were tailored in to active islands. Next, a 1000Å-thick TEOS gate oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 385°C. A 3000Å-thick Al thin film was deposited by thermal evaporation. Then, the Al thin film was etched by reactive ion etching (RIE) to form gate electrodes, and the gate oxide was also removed by RIE in sequence. After the gate electrodes were patterned, self-aligned P^+ or B^+ ions implantations with the dose concentration of 5×10^{15} cm^{-2} were carried out to form the source and drain regions of n- and p-channel devices, respectively. A 3000Å TEOS oxide was deposited by PECVD at 350°C as passivation layers. Then, excimer laser annealing was performed to activate the implanted dopants and recrystallize the source and drain region at room temperature. The shot numbers per unit area used for dopant activation were 20 and the laser energy density was controlled in the partial melting regime. After contact holes opening, Al was deposited by thermal evaporation and patterned to form the electrical connecting pads. Finally, the devices were treated with NH_3 plasma by PECVD for four hours. Conventional ELC poly-Si TFTs were also fabricated for comparison.

The transfer and output characteristics of the Ge-doped poly-$Si_{1-x}Ge_x$ TFTs were measured by HP4156 semiconductor parameter analyzer. The device parameters including field-effect mobility, threshold voltage, subthreshold swing and on/off current ratio were extracted from the measured characteristics. The electrical properties of the ELC poly-Si controlling samples were also estimated to compare with the ELC Ge-doped poly-$Si_{1-x}Ge_x$ TFTs.

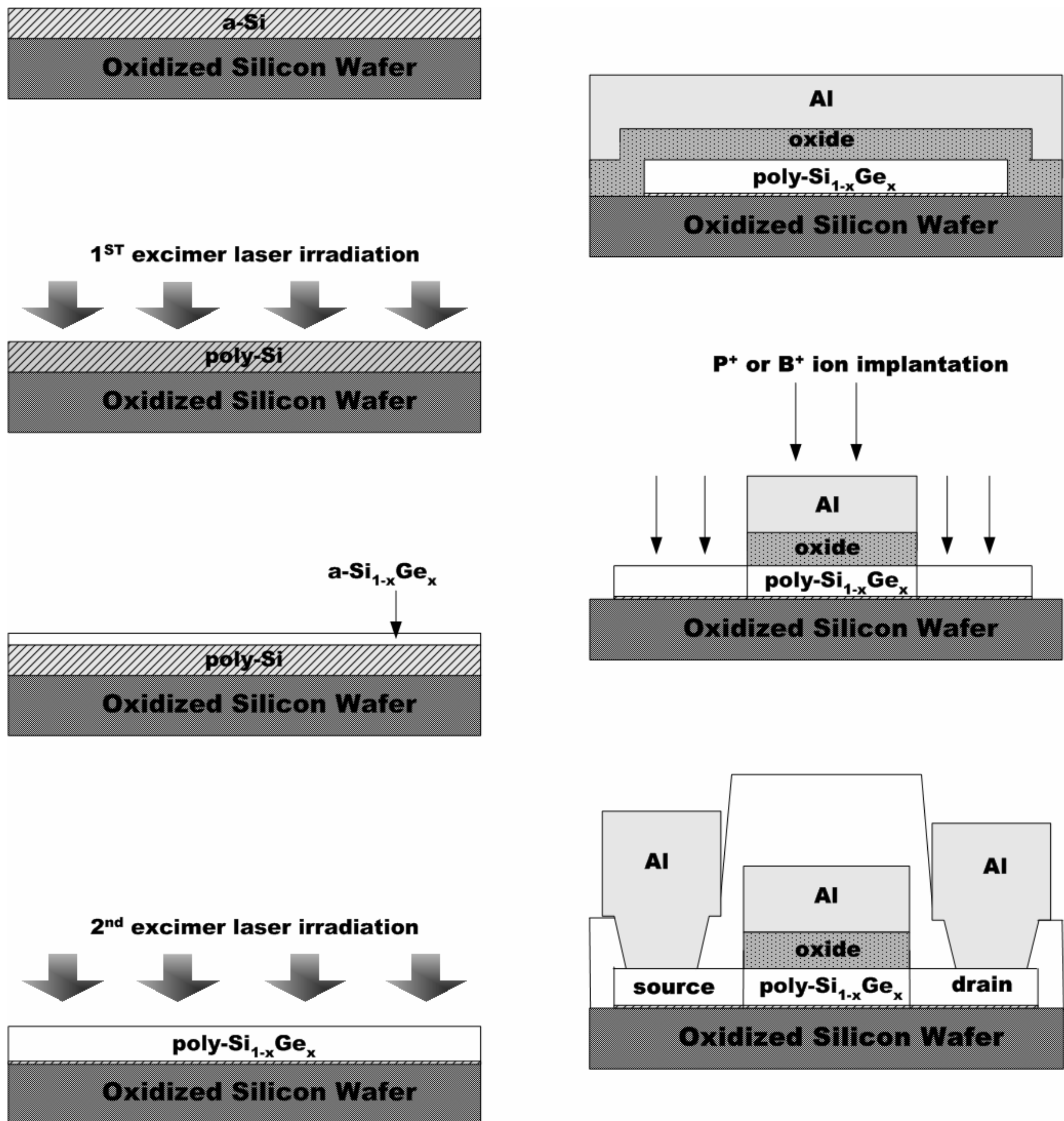


Figure 4.2. The key fabrication process of Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs.

4.3 Results and Discussion

4.3.1 Characterizations of ELC poly- $Si_{1-x}Ge_x$ TFTs with Si capping layer

4.3.1.1 The Principle of Controlled Ge Segregation

In the previous work, it has be shown that directly laser annealing of a-$Si_{1-x}Ge_x$ thin film would result in a serious Ge segregation at film surface and grain boundaries. The device performance is dramatically degraded by the surface Ge-rich layer because of large amounts of defects existing inside this layer. The phenomenon of Ge segregation is resulted from the different melting point between Ge and Si. Due to the higher melting point of Si compared to Ge, the Si atoms in the melting $Si_{1-x}Ge_x$ thin film is expected to solidify first. At the end of solidification, numerous Ge atoms will aggregate at the grain boundary and film surface, where are the last solidification region during ELC process.

In order to reduce the unacceptable phenomenon of Ge segregation occurring during ELC process, a-Si capping layer structure is provided to suppress the Ge segregation in the surface active layer. The key process for the proposing structure is to introduce Ge atom into the above Si thin film without causing Ge segregation again. The segregated Ge atoms at the poly-$Si_{1-x}Ge_x$ thin film surface after the first ELC act as a solid diffusion source for the a-Si capping layer during the second laser irradiation. The object of reducing Ge segregation can be achieved by decreasing the total melting period and/or accelerate the solidification speed of the crystallized thin film during the second excimer laser irradiation. According to previous reports [4.28] – [4.29], the solidification period will be substantially decreased if the nucleation sites have been already existed in the thin film. In other words, the solidification

speed of the crystallized thin film is enhanced as the applied laser energy density is in partial melting regime. In addition, the total melting period can also be acquired by decreasing the laser shot numbers per unit area.

In this work, the first laser annealing is used to acquire poly-$Si_{1-x}Ge_x$ thin film with excellent crystallinity. Thus, the laser energy density is controlled in the super-lateral-growth regime and the laser shot numbers per unit area are 100, which will enhance the secondary grain growth. The second laser annealing is adopted to let Ge atoms distribute in the whole thin film. As the second laser irradiation is performed, the Ge atoms aggregated at the poly-$Si_{1-x}Ge_x$ thin film surface diffuse into the upper Si thin film naturally. The second laser energy density must be carefully controlled so that the underneath poly-$Si_{1-x}Ge_x$ thin film is in partially melting regime. Therefore, all original nucleation sites survive during the second laser irradiation. The grains can be regrown vertically from the under poly-$Si_{1-x}Ge_x$ thin film upward to the upper Si layer with a very high solidification speed. On the other hand, the shot numbers adopted in the second laser irradiation is fewer than those in the first ELC. The total melting period can be diminished by combining these two methods mentioned above. As a result, the Ge segregation is expected to alleviate in this proposed process when the laser energy density and laser shot number per unit area are well-controlled in accordance with the designing recipes.

4.3.1.2 Electrical Characterization of ELC Poly-$Si_{1-x}Ge_x$ TFTs with Si Capping Layer

Figure 4.3 and Figure 4.4 show the typical transfer characteristics of p-channel ELC poly-$Si_{1-x}Ge_x$ TFTs with a Si capping layer. The device dimensions are W/L = 10μm/10μm and 5μm/5μm, respectively. The Ge atom concentration of the initial underneath $Si_{1-x}Ge_x$ thin film is 23%. According to RBS analysis, the Ge concentration of the eventual poly-$Si_{1-x}Ge_x$

thin film is about 12%. The electrical parameters including field-effect mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold swing, and on/off current ratio are extracted from the transfer characteristics. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of I_d = - (W/L) x 10^{-8} A at $|V_{ds}|$ = 0.1V. The field effect mobility is extracted from the maximum transconductance in the linear region of I_d-V_g characteristics at $|V_d|$ = 0.1V. The on/off current ratio is specified by the maximum drain current at $|V_{ds}|$ = 5V and $|V_{gs}|$ = 30V over the minimum drain current at $|V_{ds}|$ = 5V.

Compared with the direct-ELC poly-$Si_{1-x}Ge_x$ TFTs mentioned in previous chapter, the electrical device performances are improved by adopting the Si capping layer structure. Higher mobility, lower threshold voltage, and better subthreshold swing are acquired for the ELC poly-$Si_{1-x}Ge_x$ TFTs with Si capping structure. This represents that the capping a-Si thin layer can effectively alleviate the Ge segregation induced by the ELC process as expected. The reduction of Ge atoms at the film surface leads to a decrease of Ge-related defects. Thus, the performance of the poly-$Si_{1-x}Ge_x$ TFTs is ameliorated. In addition, it is also found that the field-effect mobility increases as the device dimension shrinks. Since the numbers of the grain boundary in the active layer decrease with device dimension, higher carrier mobility is observed under small device dimension. However, when the device dimension decrease further to smaller size such as W/L = 2μm/2μm, the device characteristics become to fail. This may be attributed to the poor crystallinity of the initial underneath ELC poly-$Si_{1-x}Ge_x$ thin film. In chapter 3, it has been shown the lower melting point of Ge atom will result in faster nucleation rate and/or more nucleation sites during excimer laser crystallization. The density of homogeneous nucleation site increased with the Ge atomic concentration [4.30]. Therefore, poor crystallinity and smaller grain are found for the ELC poly-$Si_{1-x}Ge_x$ thin film. The poor crystallinity will have a profound effect on the device performance especially when the device dimension shrinks, which are responsible for the degraded characteristics of the small-dimension ELC poly-$Si_{1-x}Ge_x$ TFTs with Si capping layer.

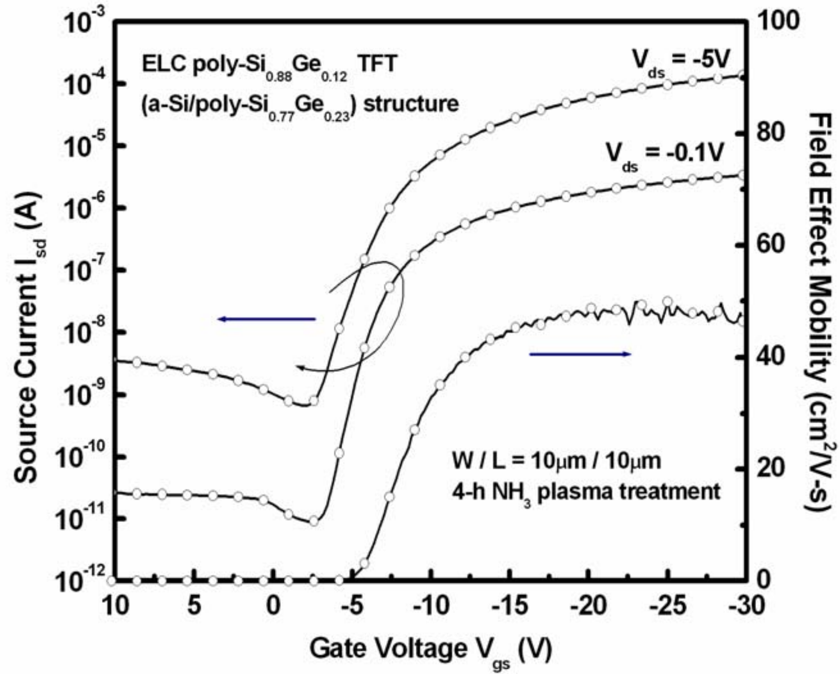
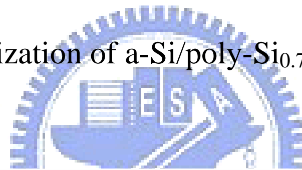


Figure 4.3. Typical transfer characteristics of p-channel poly-$Si_{0.88}Ge_{0.12}$ TFTs fabricated by excimer laser crystallization of a-Si/poly-$Si_{0.77}Ge_{0.23}$ structure. W = L = 10μm.



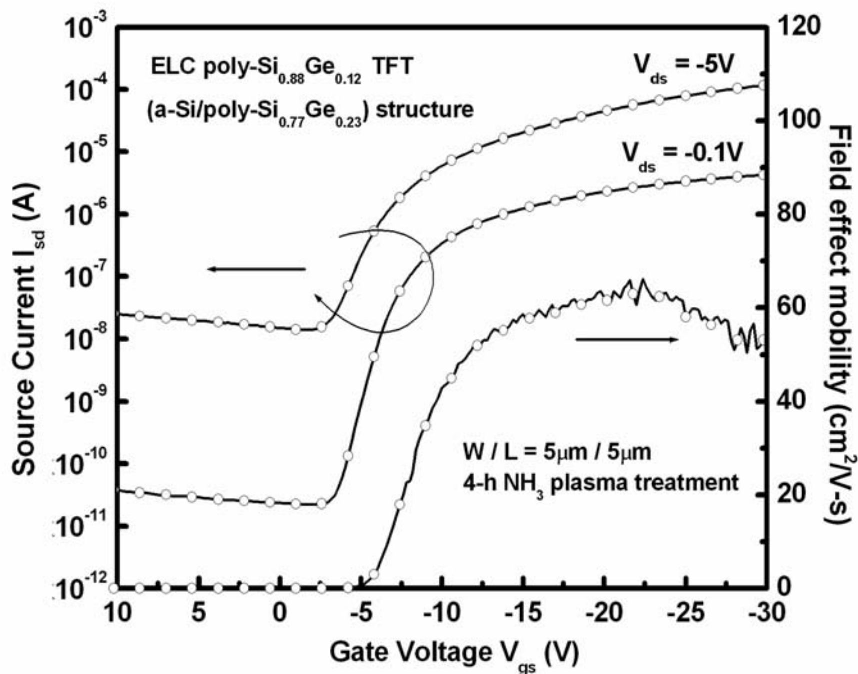


Figure 4.4. Typical transfer characteristics of p-channel poly-$Si_{0.88}Ge_{0.12}$ TFTs fabricated by excimer laser crystallization of a-Si/poly-$Si_{0.77}Ge_{0.23}$ structure. W = L = 5μm.

Figure 4.5 and Figure 4.6 display the transfer characteristics of the ELC Si-capped poly-$Si_{1-x}Ge_x$ TFTs with a 33% Ge atomic concentration in the initial underlying poly-$Si_{1-x}Ge_x$ layer. The Ge concentration in the final poly-$Si_{1-x}Ge_x$ thin film is 16%. The detail electrical characteristics of poly-$Si_{1-x}Ge_x$ TFTs with a Si capped layer are summarized in Table 4-1. It is observed that the carrier mobility increases with the increasing Ge atomic concentration in the underneath poly-$Si_{1-x}Ge_x$ thin film. The enhancement of carrier mobility can be attributed to the intrinsic property of higher carrier mobility for Ge atoms. Similarly, as the device dimension shrinks, the mobility increases further. No acceptable electrical characteristics are acquired for smaller device dimension (W = L = 2μm) owing to the poor crystallinity of poly-$Si_{1-x}Ge_x$ thin film. Figure 4.7 and Figure 4.8 show the output characteristics of the ELC Si-capped poly-$Si_{0.84}Ge_{0.16}$ TFTs. From these figures, it also demonstrates that ELC Si-capped poly-$Si_{0.84}Ge_{0.16}$ TFTs can provide high turn-on current under reasonable bias condition.

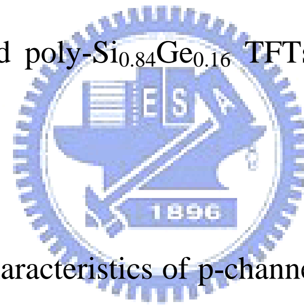


Table 4.1. Measured electrical characteristics of p-channel ELC poly-Si TFTs and Si-capped poly-$Si_{1-x}Ge_x$ TFTs after 4-h NH_3 plasma treatment.

W / L (μm/μm)	Structure	Mobility (cm^2/V-s)	Threshold Voltage (V)	Subthreshold Swing (V/dec)	I_{on}/I_{off} @ V_{ds} = -5V
10/10	Poly-Si	102	-2.36	240	$2.4x10^8$
	$Si/Si_{0.77}Ge_{0.23}$	50	-6.12	812	$2.1x10^5$
	$Si/Si_{0.67}Ge_{0.33}$	70	-4.76	982	$3.4x10^4$
5/5	Poly-Si	121	-3.24	352	$6.8x10^8$
	$Si/Si_{0.77}Ge_{0.23}$	60	-6.16	950	$8.4x10^3$
	$Si/Si_{0.67}Ge_{0.23}$	82	-5.33	935	$3.4x10^4$

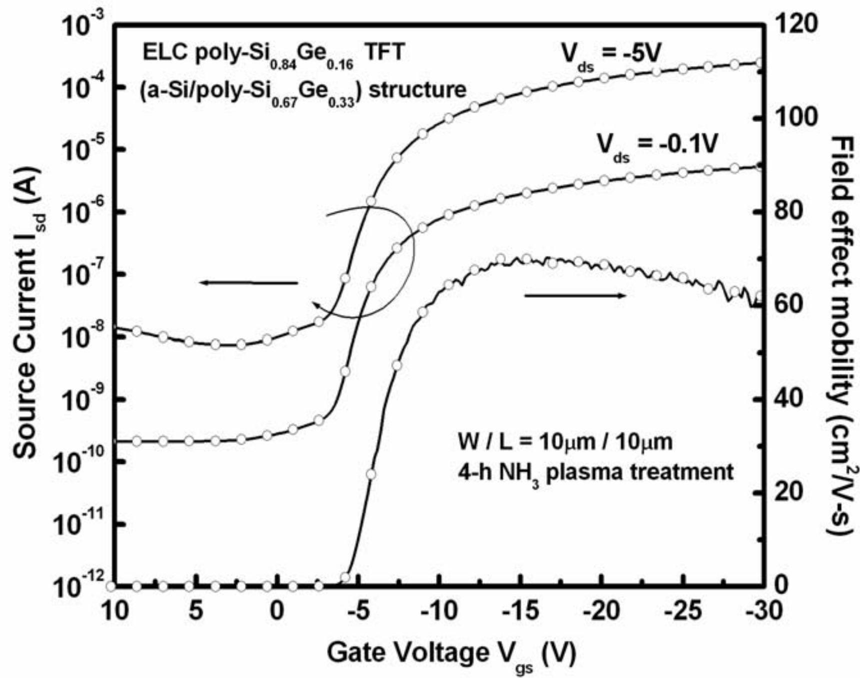


Figure 4.5. Typical transfer characteristics of p-channel poly-$Si_{0.84}Ge_{0.16}$ TFTs fabricated by excimer laser crystallization of a-Si/poly-$Si_{0.67}Ge_{0.33}$ structure. W = L = 10μm.

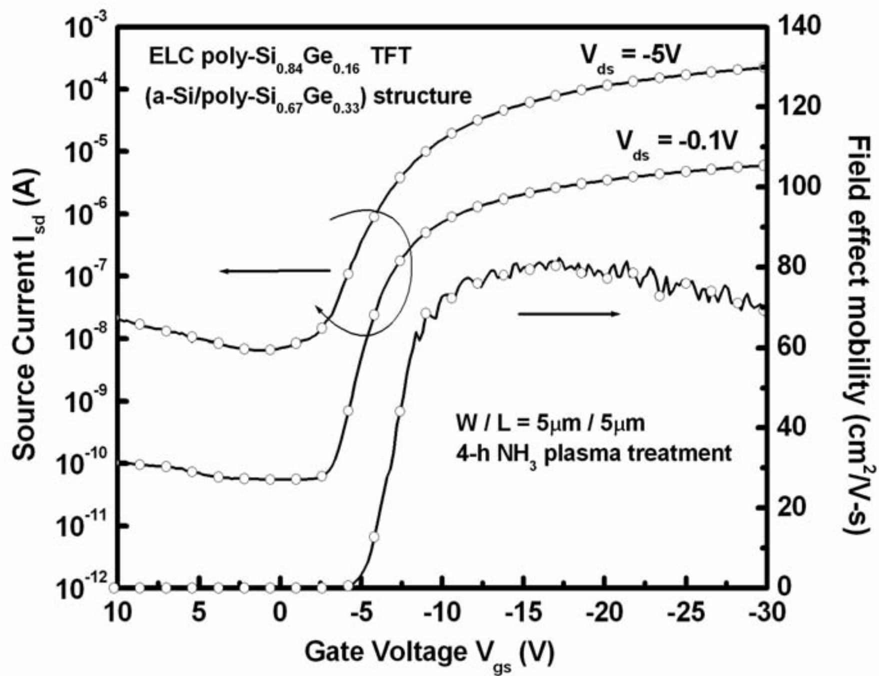


Figure 4.6. Typical transfer characteristics of p-channel poly-$Si_{0.84}Ge_{0.16}$ TFTs fabricated by excimer laser crystallization of a-Si/poly-$Si_{0.67}Ge_{0.33}$ structure. W = L = 5μm.

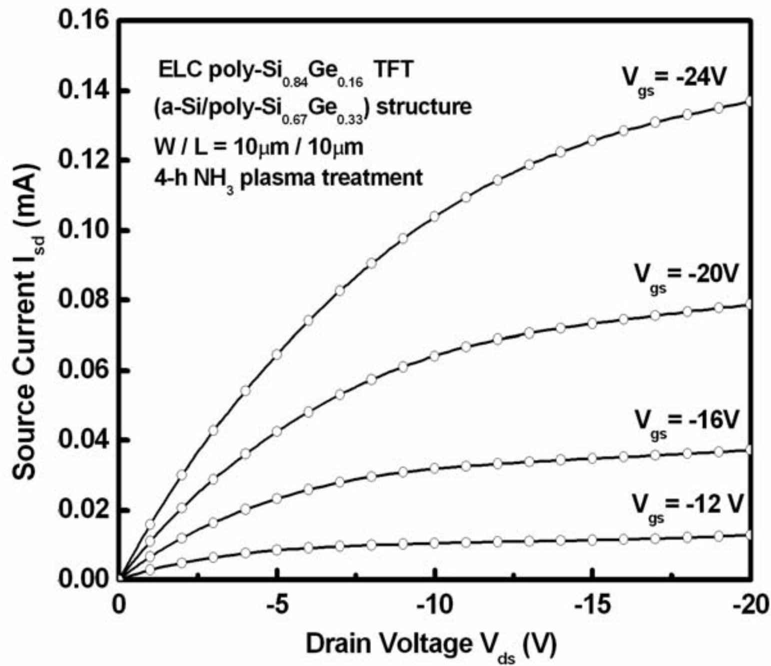


Figure 4.7. Typical output characteristics of p-channel poly-$Si_{0.84}Ge_{0.16}$ TFTs fabricated by excimer laser crystallization of a-Si/poly-$Si_{0.67}Ge_{0.33}$ structure. W = L = 10μm.

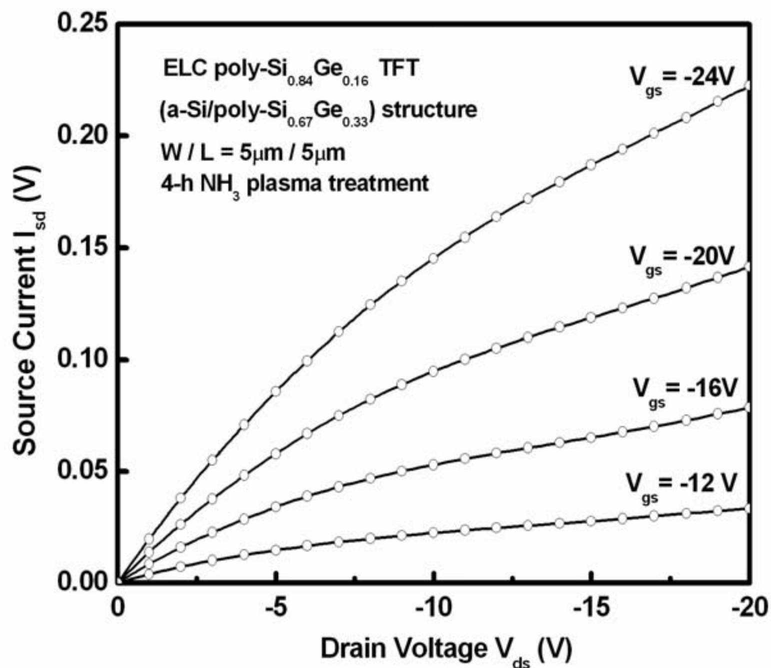


Figure 4.8. Typical output characteristics of p-channel poly-$Si_{0.84}Ge_{0.16}$ TFTs fabricated by excimer laser crystallization of a-Si/poly-$Si_{0.67}Ge_{0.33}$ structure. W = L = 5μm.

Although the electrical characteristics are improved for the ELC poly-$Si_{1-x}Ge_x$ TFTs with Si capping layer, however, the performances are still inferior to those of the conventional ELC poly-Si TFTs. Lower field-effect mobility, higher threshold voltage, smaller on/off current ratio, and poorer subthreshold swing are observed for the ELC Si-capped poly-$Si_{1-x}Ge_x$ TFTs compared to the ELC poly-Si TFTs. This can ascribed to the smaller grain size and poor crystallinity of the ELC poly-$Si_{1-x}Ge_x$ thin film in comparison with the ELC poly-Si thin film even though the applied laser annealing conditions are both in optimum for these two cases. Among this modified process, the first ELC is still applied on the a-$Si_{1-x}Ge_x$ thin film. Consequently, the poor crystallinity is improved not yet even with the upper Si capping layer. The overall electrical characteristics of the ELC Si-capped poly-$Si_{1-x}Ge_x$ TFTs are inferior to those of the conventional ELC poly-Si TFTs.

In addition, expect for the poor crystallinity of ELC poly-$Si_{1-x}Ge_x$ thin film, another possible reason responsible for the larger leakage current of the ELC poly-$Si_{1-x}Ge_x$ TFTs is the narrower energy bandgap at drain junction. Increase the Ge atomic concentration in the poly-$Si_{1-x}Ge_x$ thin film will further reduce the energy bandgap of $Si_{1-x}Ge_x$ thin film, leading to higher leakage current of TFTs as discussed in chapter 3.

As a result, in the next section, a Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs is proposed to improve the crystallinity while still maintain the high mobility property of Ge atoms.

4.3.2 Characterization of Ge-Doped ELC Poly- $Si_{1-x}Ge_x$ TFTs

4.3.2.1 The Improvement of Thin Film Crystallinity and Controlled Ge Segregation

In previous section, the ELC poly-$Si_{1-x}Ge_x$ TFTs with Si capping layer have been

demonstrated. Although the overall electrical characteristics are still unacceptable for the ELC Si-capped poly-$Si_{1-x}Ge_x$ TFTs due to the relatively poor crystallinity in the active layer, it has been displayed that the field-effect mobility can be effectively enhanced by suitably controlling the Ge atomic concentration and carefully adjusting the device process flow. To take the advantage of carrier enhancement for $Si_{1-x}Ge_x$ thin films and avoid device performance degradation associated with poor crystallinity and Ge segregation in the active layer, a novel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFT is proposed in this section.

The key process for fabricating the proposed poly-$Si_{1-x}Ge_x$ TFTs is to let Ge atoms distribute uniformly in the whole thin film and maintain better crystallinity of the active layer after ELC. Thus, a-$Si_{1-x}Ge_x$/poly-Si double layer structure is used to fabricate high quality ELC poly-$Si_{1-x}Ge_x$ thin film. In view of the excellent crystallinity and large grain size of ELC poly-Si thin film, the a-$Si_{1-x}Ge_x$ thin film in the former structure is replaced by the a-Si thin film as the underneath starting layer. The grain size and crystallinity of the poly-Si thin film are determined when the first laser irradiation is applied for crystallization, in which the process conditions are optimized. Thin a-$Si_{1-x}Ge_x$ layers with different Ge atomic fractions are deposited upon the poly-Si film and act as the solid diffusion source as the second excimer laser irradiation is carried out. When the second laser irradiation is performed, laser energy density must be carefully controlled to fully melt the upper a-$Si_{1-x}Ge_x$ thin layer but allow the underneath poly-Si layer lie in the partially melting regime. During the second laser irradiation, the Ge atoms will diffuse into the underneath poly-Si layer due to the high diffusion coefficient of Ge in melting silicon and the Ge concentration gradient. Then, the solidification process begins from the unmelted poly-Si seed layer, yielding epitaxial growth upward to the surface. Therefore, the grain size is almost unchanged after the second laser irradiation. On the other hand, owing to that the grains can vertically re-grow with a high vertical re-growth rate from the unmelted poly-Si, the Ge segregation can be improved remarkably. As a result, poly-$Si_{1-x}Ge_x$ thin film with better crystallinity and suppressed Ge

segregation can be acquired by this novel laser doping technique.

In order to confirm the Ge atomic concentration of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ thin film, RBS analysis was performed. Figure 4.9 displays the RBS analysis results of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ thin films capped with a-$Si_{0.77}Ge_{0.23}$ and a-$Si_{0.67}Ge_{0.33}$ upper layers, respectively. The Ge atomic concentrations in the eventual poly-$Si_{1-x}Ge_x$ thin film are 5% and 9%, respectively. As a result, the poly-$Si_{1-x}Ge_x$ thin film with low Ge concentration can be obtained by using the novel Ge-doped ELC poly-$Si_{1-x}Ge_x$ process in comparison with the as-deposited $Si_{1-x}Ge_x$ thin film.

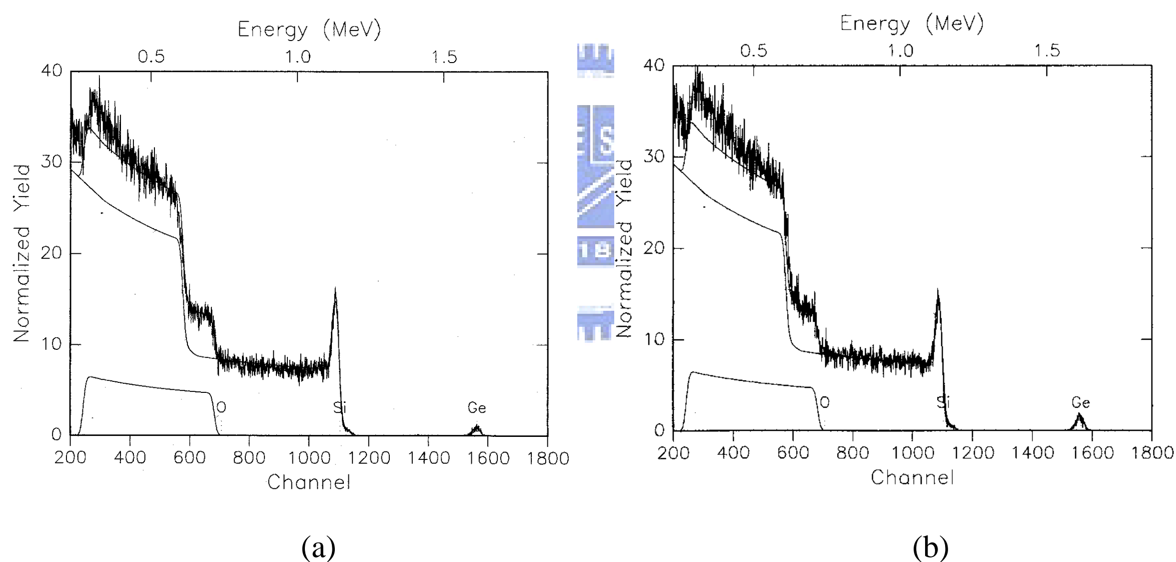


Figure 4.9. The RBS analysis results of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ thin films capped with (a) a-$Si_{0.77}Ge_{0.23}$ and (b) a-$Si_{0.67}Ge_{0.33}$ upper layers. The final Ge atomic concentration is equivalent to (a) 5% and (b) 9%, respectively.

4.3.2.2 Electrical Characterization of Ge-Doped ELC poly-$Si_{1-x}Ge_x$ TFTs

Figure 4.10 and Figure 4.11 show the typical transfer characteristics of the conventional ELC n-channel poly-Si TFTs and the Ge-doped n-channel poly-$Si_{1-x}Ge_x$ TFTs with larger device dimension (W/L = 10μm/10μm, and 5μm/5μm). The electrical parameters including field-effect mobility (μ_{FE}), threshold voltage (V_{th}), subthreshold swing, and on/off current ratio are extracted from the transfer characteristics. The threshold voltage is defined as the gate voltage required to achieve a normalized drain current of I_d = - (W/L) x 10^{-8} A at $|V_{ds}|$ = 0.1V. The field effect mobility is extracted from the maximum transconductance in the linear region of I_d-V_g characteristics at $|V_d|$ = 0.1V. The on/off current ratio is specified by the maximum drain current at $|V_{ds}|$ = 5V and $|V_{gs}|$ = 30V over the minimum drain current at $|V_{ds}|$ = 5V.

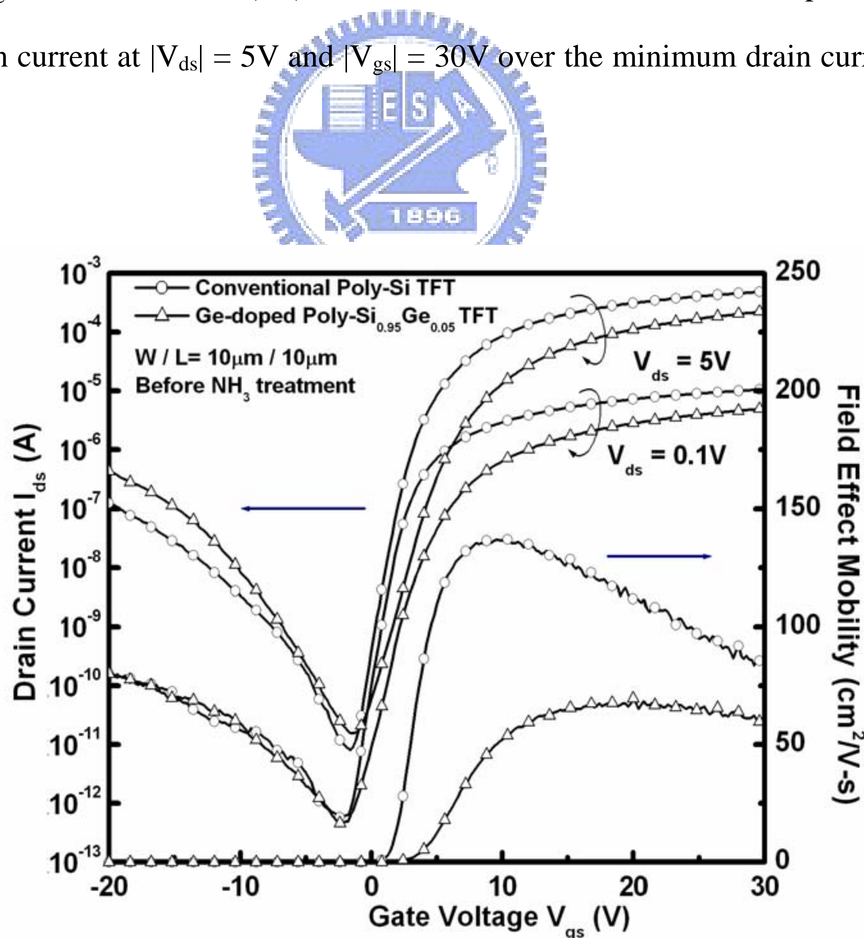


Figure 4.10. The typical transfer characteristics of the conventional ELC n-channel poly-Si TFTs and the Ge-doped n-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 10μm/10μm.

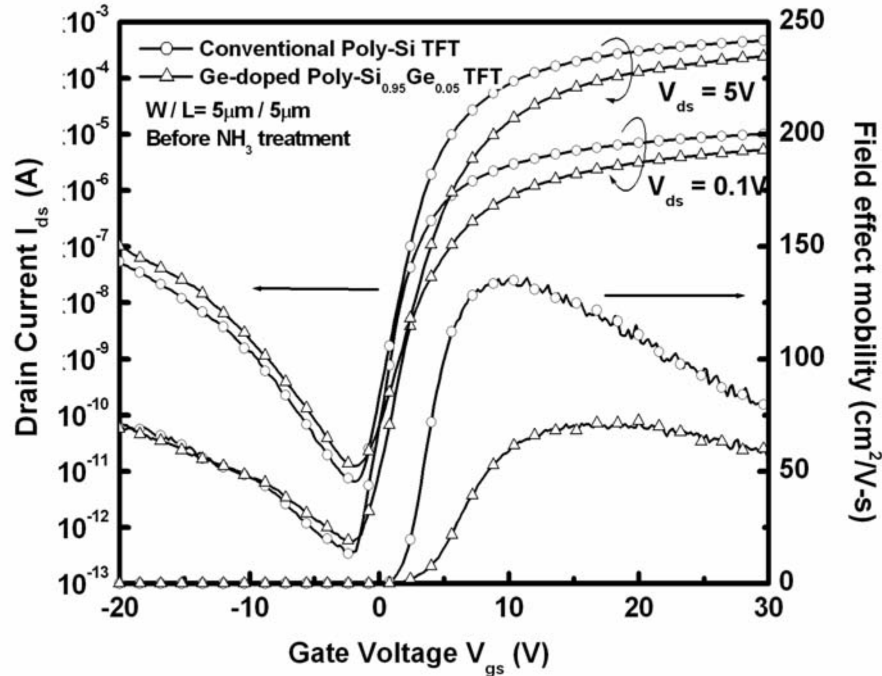


Figure 4.11. The typical transfer characteristics of the conventional ELC n-channel poly-Si TFTs and the Ge-doped n-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 5μm/5μm.

According to these figures, for large dimension TFT devices, it is observed that the conventional ELC poly-Si TFTs exhibit better device electrical performance than the Ge-doped poly-$Si_{1-x}Ge_x$ TFTs. The lower carrier mobility of the Ge-doped poly-$Si_{1-x}Ge_x$ TFTs can be attributed to the large amounts of grain boundaries existing within the long channel devices. Although the grains can regrow with a high vertical regrowth rate for the second laser irradiation, a portion of Ge atoms will segregate to grain boundaries due to the lower melting point of Ge compared to Si. Thus, the segregated Ge atoms piled up the grain boundary will become carrier scattering centers, which build potential barriers during carrier transport from drain to source. The larger dimensions of the device, the more grain boundaries are involved in the channel region, which will degrade the carrier transport in the channel. In other words, it is inferred that the degree of mobility degradation by defect trap generation is beyond that of mobility enhancement by Ge incorporation.

Figure 4.12 ~ Figure 4.15 show the typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{1-x}Ge_x$ TFTs with larger device dimension (W/L = 10μm/10μm, and 5μm/5μm) and different Ge atom concentrations in the channel. Similarly, the unacceptable effect in the conducting channel is also observed for the large dimension p-channel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs. In addition, it can be found that as the Ge atomic concentration in the active layer increases, the filed effect mobility of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs is gradually approaching that of conventional ELC poly-Si TFTs. This means that the mobility enhancement resulted from Ge incorporation becomes more obvious as the Ge concentration increases.

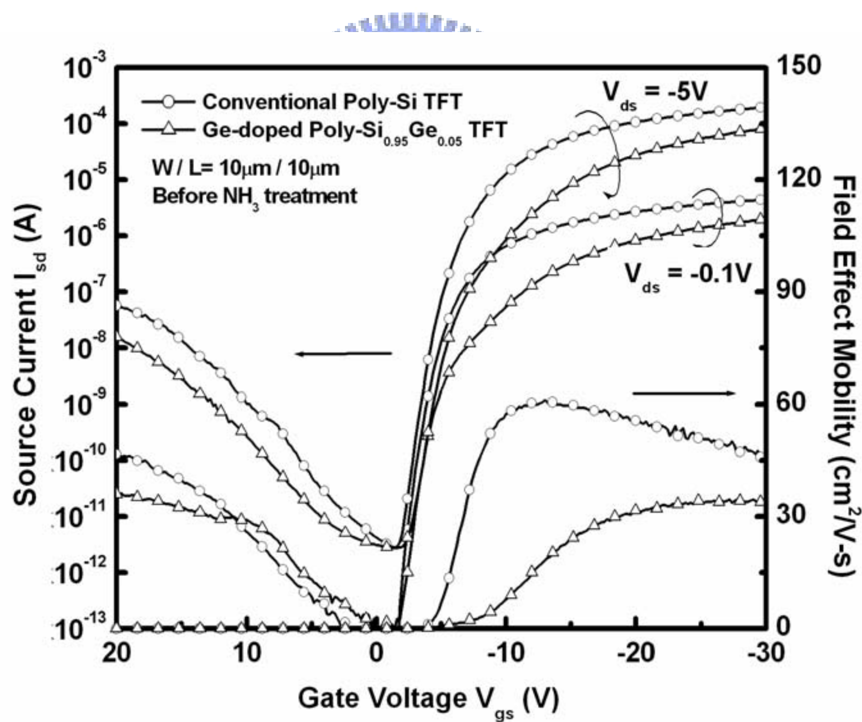


Figure 4.12. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 10μm/10μm.

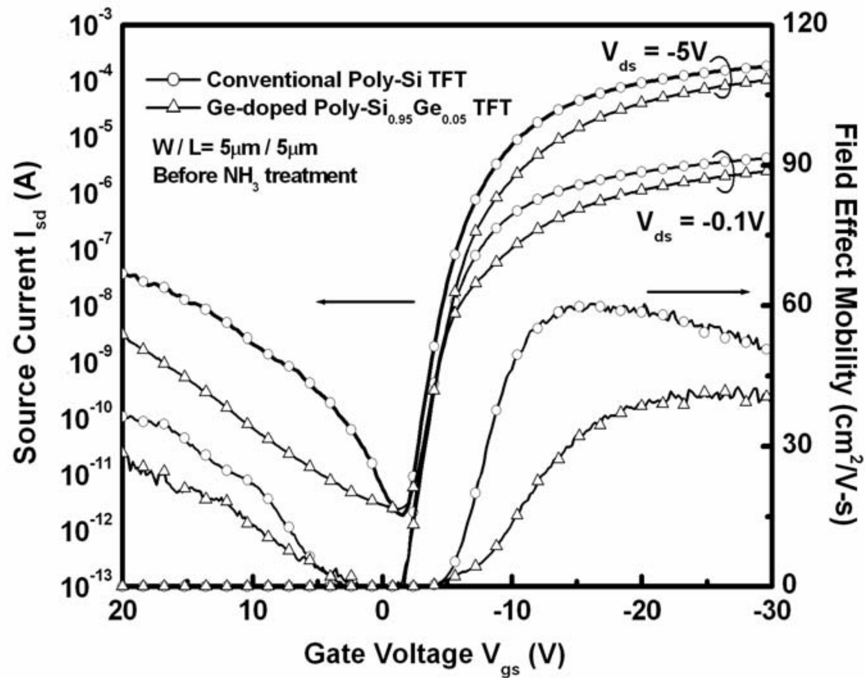


Figure 4.13. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 5μm/5μm.

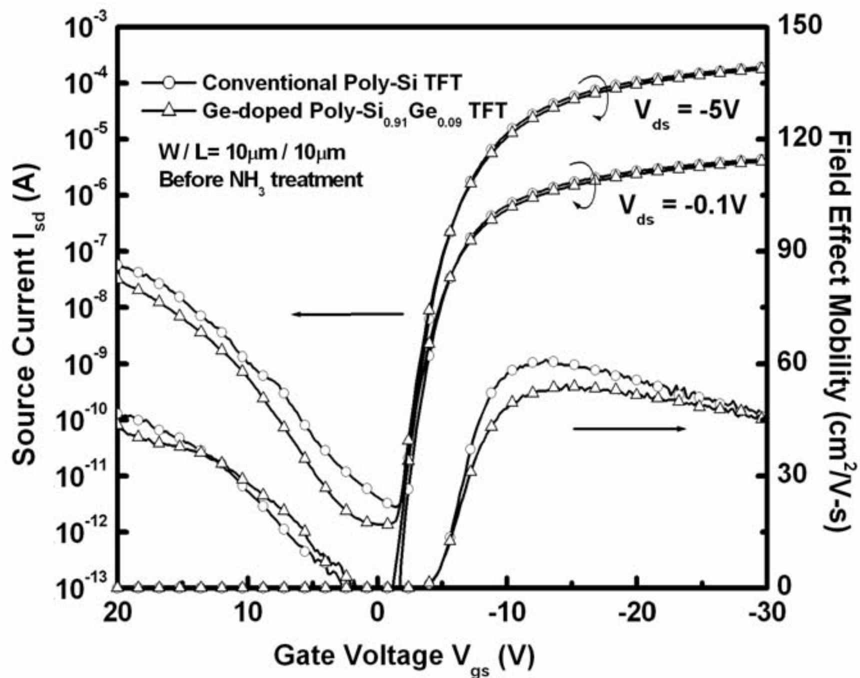


Figure 4.14. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.91}Ge_{0.09}$ TFTs. W/L = 10μm/10μm.

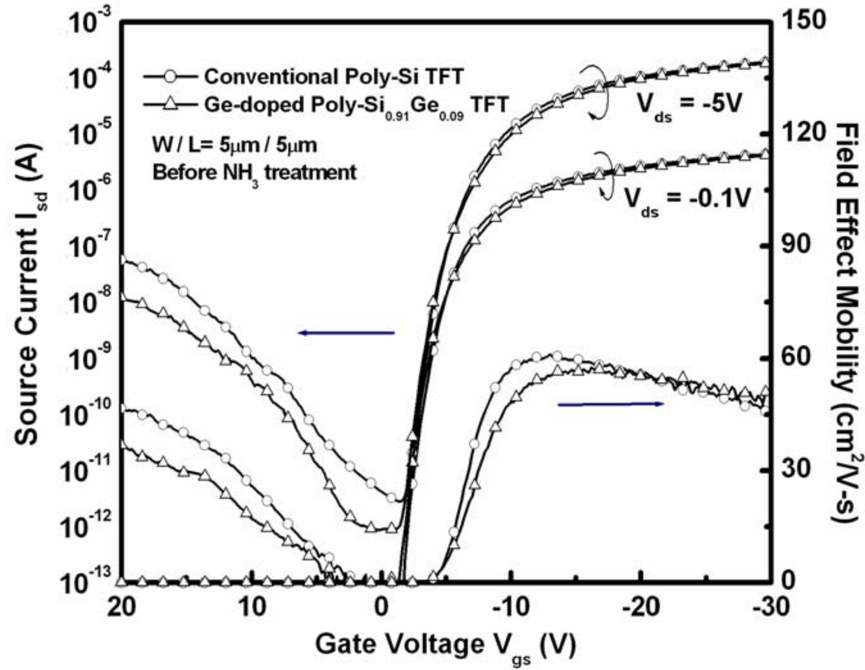


Figure 4.15. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.91}Ge_{0.09}$ TFTs. W/L = 5μm/5μm.

As the device dimension shrinks, the performance of the Ge-doped poly-$Si_{1-x}Ge_x$ TFTs reveals a significant different trend, which is unlike those of the Si-capped poly-$Si_{1-x}Ge_x$ TFTs. Figure 4.16 and Figure 4.17 display typical transfer characteristics of conventional n-channel ELC poly-Si and Ge-doped n-channel poly-$Si_{1-x}Ge_x$ TFTs with small device dimensions (W/L = 2μm/2μm, and 1.5μm/1.5μm), respectively. For small-dimension TFT devices, the Ge-doped poly-$Si_{1-x}Ge_x$ TFTs exhibits better device performance than those of larger device dimension. This result can be ascribed to the successful reduction of grain boundaries and defect density in the channel region. As discussed in previous section, for the ELC poly-$Si_{1-x}Ge_x$ TFTs with Si capping layer, the electrical characteristics become degraded owing to the poor crystallinity of ELC poly-$Si_{1-x}Ge_x$ thin film in spite of the reduction of grain boundaries. However, for the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs, the starting substrate is poly-Si, which possesses better crystallinity. Thus, the phenomenon occurred in the Si-capped ELC poly-$Si_{1-x}Ge_x$ TFTs will not take place for the Ge-doped counterparts. The

mobility continuous to improve as the dimension shrinks for the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs.

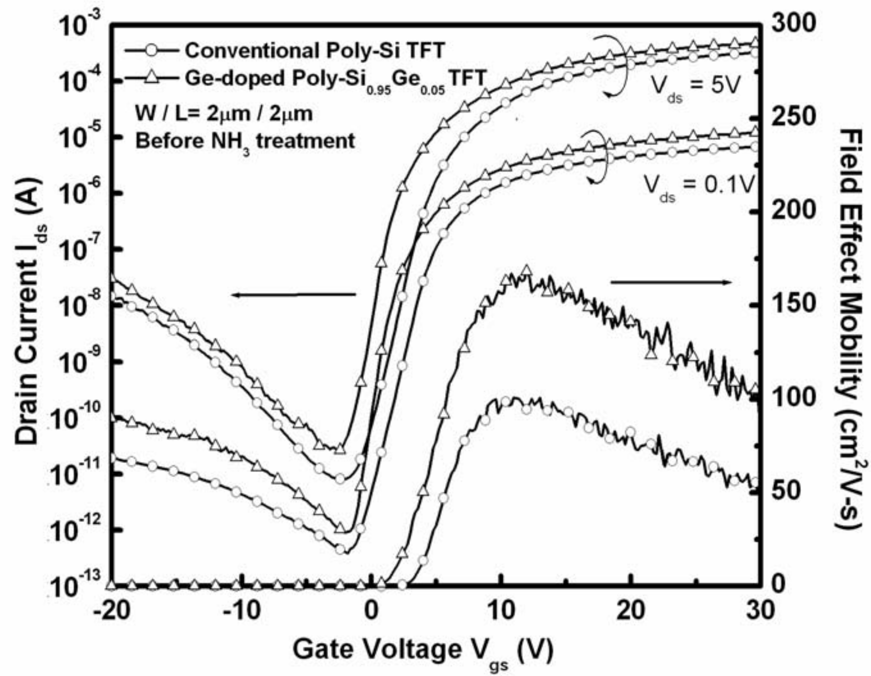


Figure 4.16. The typical transfer characteristics of the conventional ELC n-channel poly-Si TFTs and the Ge-doped n-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 2μm/2μm.

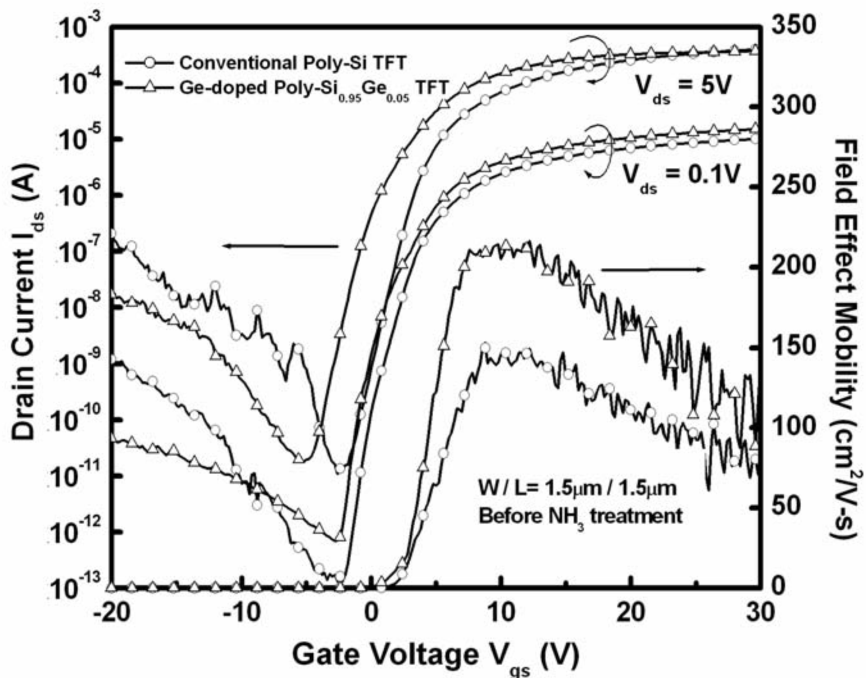


Figure 4.17. The typical transfer characteristics of the conventional ELC n-channel poly-Si TFTs and the Ge-doped n-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 1.5μm/1.5μm.

Furthermore, it is shown that Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs reveal higher drain current than conventional ELC poly-Si TFTs when the device dimension is shrunk to W/L = 2μ/2μm. The same phenomena of device performance enhancement can also be observed for small dimension p-channel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs as shown in Figure 4.18 - Figure 4.21. The mobility of the n- and p-channel Ge-doped ELC poly-$Si_{0.95}Ge_{0.05}$ TFTs devices with W/L = 2μm/2μm are increased by 47% and 24% respectively compared to that in the conventional ELC poly-Si TFTs. The detail electrical parameters of both conventional ELC poly-Si and Ge-doped poly-$Si_{1-x}Ge_x$ TFTs before plasma treatment are summarized in Table 4-2 and Table 4-3.

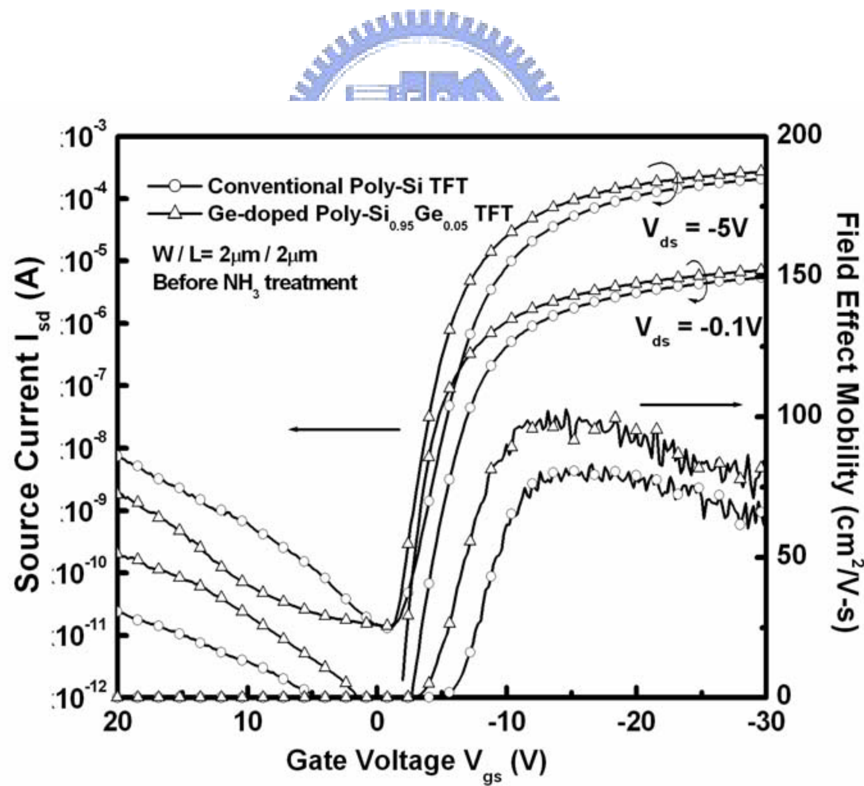


Figure 4.18. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 2μm/2μm.

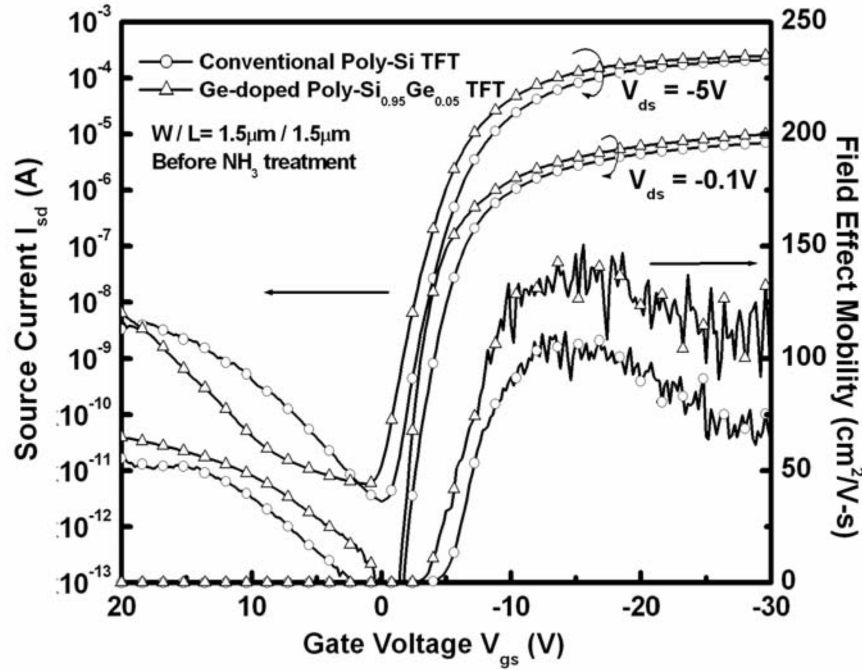


Figure 4.19. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs. W/L = 1.5μm/1.5μm.

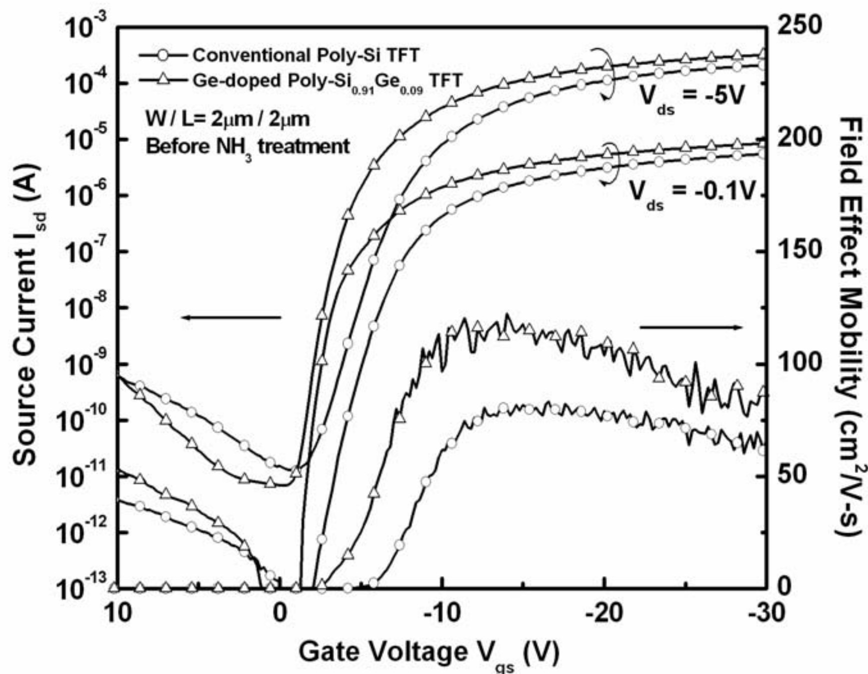


Figure 4.20. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.91}Ge_{0.09}$ TFTs. W/L = 2μm/2μm.

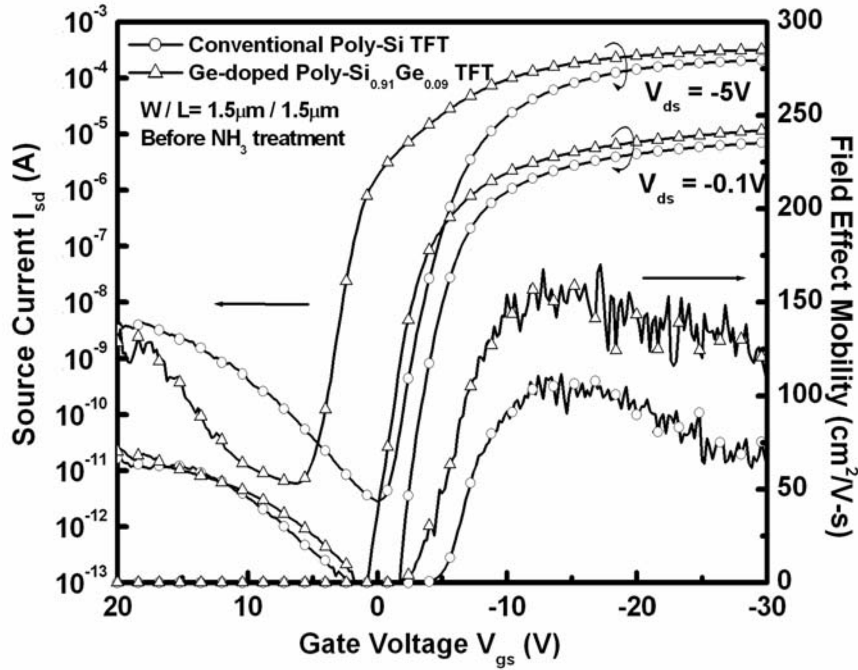


Figure 4.21. The typical transfer characteristics of the conventional ELC p-channel poly-Si TFTs and the Ge-doped p-channel poly-$Si_{0.91}Ge_{0.09}$ TFTs. W/L = 1.5μm/1.5μm.

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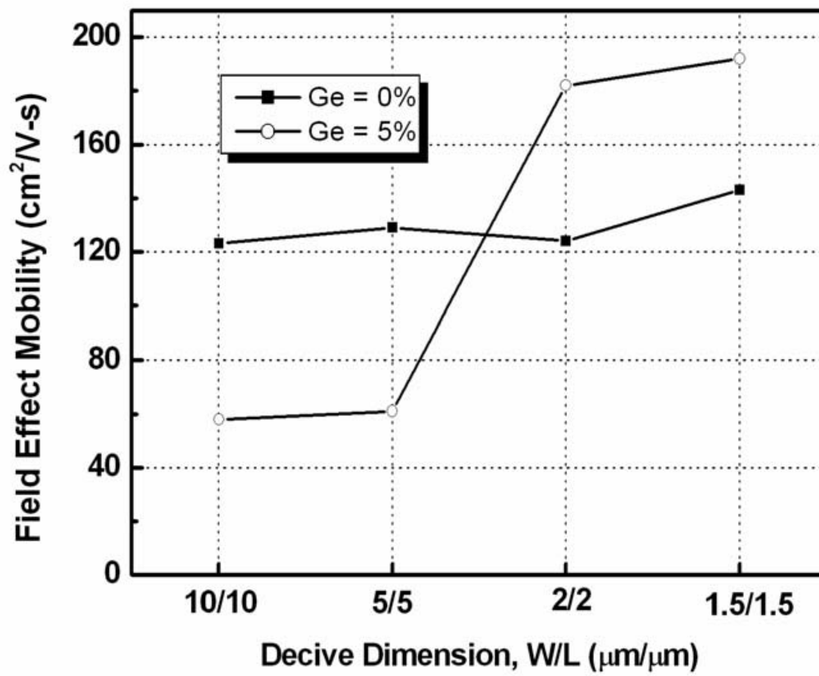
Table 4.2. Measured electrical characteristics of n-channel ELC poly-Si TFTs and Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs before NH_3 plasma treatment.

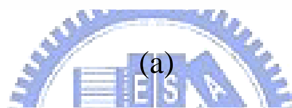
W / L (μm/μm)	Structure	Mobility (cm^2/V-s)	Threshold Voltage (V)	Subthreshold Swing (V/dec)	I_{on}/I_{off} @ V_{ds} = -5V
10/10	Poly-Si	123	1.80	707	$6.1x10^7$
	Poly-$Si_{0.95}Ge_{0.05}$	58	4.09	976	$1.5x10^7$
5/5	Poly-Si	129	1.92	717	$7.1x10^7$
	Poly-$Si_{0.95}Ge_{0.05}$	61	3.16	815	$2.0x10^7$
2/2	Poly-Si	124	3.33	754	$4.0x10^7$
	Poly-$Si_{0.95}Ge_{0.05}$	182	1.68	703	$1.7x10^7$
1.5/1.5	Poly-Si	143	2.91	561	$3.7x10^7$
	Poly-$Si_{0.95}Ge_{0.05}$	192	1.25	576	$2.1x10^7$

Table 4.3. Measured electrical characteristics of p-channel ELC poly-Si TFTs and Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs before NH_3 plasma treatment.

W / L (μm/μm)	Structure	Mobility (cm^2/V-s)	Threshold Voltage (V)	Subthreshold Swing (V/dec)	I_{on}/I_{off} @ V_{ds} = -5V
10/10	Poly-Si	59	-4.81	323	6.9×10^7
	Poly-$Si_{0.95}Ge_{0.05}$	28	-7.29	327	1.5×10^7
	Poly-$Si_{0.91}Ge_{0.09}$	44	-5.39	274	1.3×10^8
5/5	Poly-Si	61	-5.18	326	9.8×10^7
	Poly-$Si_{0.95}Ge_{0.05}$	39	-6.7	285	4.4×10^7
	Poly-$Si_{0.91}Ge_{0.09}$	58	-5.00	501	2.1×10^8
2/2	Poly-Si	79	-6.24	597	1.7×10^7
	Poly-$Si_{0.95}Ge_{0.05}$	98	-4.75	450	2.0×10^7
	Poly-$Si_{0.91}Ge_{0.09}$	112	-4.12	461	4.6×10^7
1.5/1.5	Poly-Si	118	-4.20	362	7.5×10^7
	Poly-$Si_{0.95}Ge_{0.05}$	151	-3.77	429	4.4×10^7
	Poly-$Si_{0.91}Ge_{0.09}$	167	-4.12	399	5.4×10^7

Figure 4.22 displays the dependence of field-effect mobility on device dimension and Ge atomic concentration for n-channel and p-channel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs. For the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs, the mobility is still inferior to that of ELC poly-Si TFT under large device dimension, i.e. W/L > 5μm/5μm. However, the mobility becomes superior to that of poly-Si TFTs when the device dimension shrinks to equal to 2μm. Furthermore, the mobility also enlarges as the Ge atom concentration increases.

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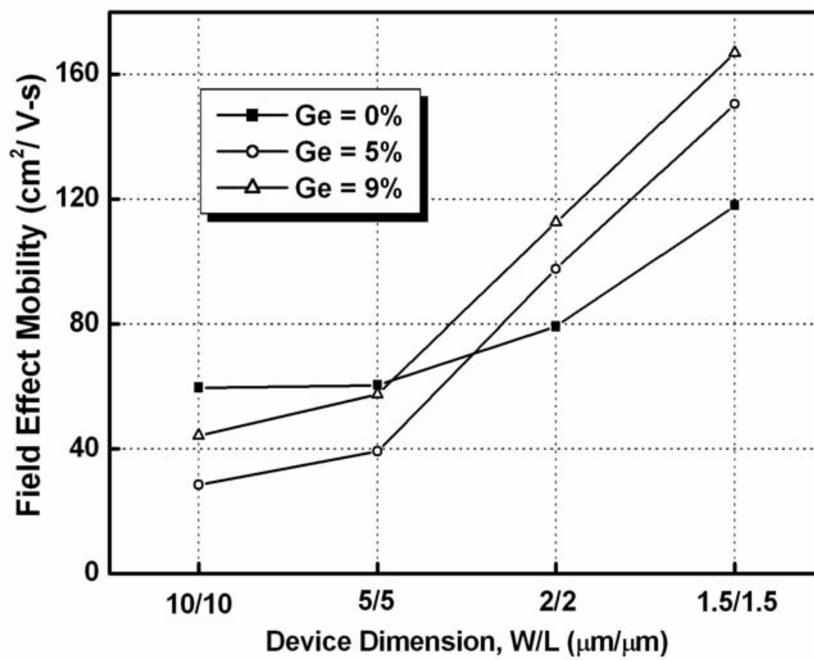
(a)



(b)

Figure 4.22. The dependence of mobility on device dimension and Ge atomic concentration for (a) n-channel and (b) p-channel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs.

These phenomena can be attributed to two different mechanisms, which compete with each other and dominate under different device dimension. One is the numbers of grain boundary existed in the channel. The segregated Ge atoms piled up the grain boundary become carrier scattering centers and build potential barriers during carrier transport from drain to source, which degrade the device performance and limit the carrier mobility. The other is the carrier mobility enhancement resulted from Ge atoms incorporation in the surface channel. For long channel devices, there are numerous numbers of grain boundaries inside the channel. The grain boundaries put a profound negative influence on the device characteristics, which suppresses the carrier enhancement effect by Ge incorporation. Thus, for large device dimension, the mechanism that dominates the electrical characteristics is the grain boundary effect. On the other hand, under small device dimension, there are few grain boundaries inside the active region. The improvement in the electrical characteristics can be ascribed to that the degree of mobility enhancement by Ge incorporation is beyond that of mobility degradation by defect trap at grain boundaries. This assumption can be further proven in the case of Ge-doped ELC poly-$Si_{0.91}Ge_{0.09}$ TFTs. A more noticeable enhancement in the field-effect mobility is achieved by moderately increasing the Ge concentration within the poly-$Si_{1-x}Ge_x$ film. The mobility and drain current of the Ge-doped ELC poly-$Si_{0.91}Ge_{0.09}$ TFTs with W/L = 2μm/2μm are enhanced by 41% and 52% than those of the conventional ELC poly-Si counterparts.

Although the field-effect mobility still remarkably improves, the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs demonstrate a more serious short channel effect than conventional ELC poly-Si TFTs as the device dimension shrink to W/L = 1.5μm/1.5μm. This can be ascribed to the narrower energy bandgap of the poly-$Si_{1-x}Ge_x$ in comparison with poly-Si. According to previous reports [4.31], two mechanisms may account for the short channel effects in polycrystalline TFTs. At low drain bias, the channel charge is partially supported by the source and drain diffusions. At moderate or high drain bias, channel avalanche multiplication

and the associated charging of the device island by carriers generated by impact ionization near the drain are dominant. These effects will be expected to become more remarkable for poly-$Si_{1-x}Ge_x$ due to smaller energy bandgap. The avalanche generation rate will increase as the energy bandgap of the channel layer at drain junction become narrower. As a result, Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs exhibit more serious short channel effect.

On the other hand, the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs with W/L = 2μm/2μm exhibit higher off-state current at $|V_{ds}| = 0.1V$ but almost the same amount at $|V_{ds}| = 5V$. The higher leakage current at low drain bias for the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs can be also attributed the smaller bandgap of the poly-$Si_{1-x}Ge_x$ thin film. According to the poly-Si TFTs leakage current mechanism [4.32] – [4.33], the leakage current is derived from the energetic carriers tunneling through the energy bandgap at the drain junction. At low drain bias (V_d ~ 0.1V), the activation energy of a carrier emitted from the trap to contribute to conduction process is about the half of the bandgap of the poly-Si. Thus, thermal emission is the dominant leakage mechanism in the low field. Reducing the energy bandgap of the active layer will increase the probability of carrier tunneling through the drain energy barrier to the channel region, leading to high leakage current. With the adding of Ge atom in Si, the energy bandgap become narrower. Thus, the leakage current is higher for the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs. Besides, as the applied drain bias increases, the carriers become more energetic and can get into the channel by trap-assisted tunneling or direct tunneling. At this moment, the dominant factor will not only be the energy bandgap entirely. Other factors including defect density, trap distribution, and channel conductivity are possibly responsible for the leakage current. Therefore, the higher leakage current of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs is only observed under low drain voltage. Nevertheless, the off-state behavior can be alleviated by introducing the device structures of lightly doped drain (LDD) [4.34] – [4.35] or gate-overlapped lightly doped drain (GOLDD) [4.36] – [4.41] during the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs fabrication.

Figure 4.23 and Figure 4.24 display the output characteristics of the conventional p-channel ELC poly-Si TFTs and the Ge-dope p-channel poly-$Si_{1-x}Ge_x$ TFTs. It is demonstrated that ELC Ge-doped poly-$Si_{1-x}Ge_x$ TFTs provide higher driving current than conventional ELC poly-Si TFTs under the same bias condition. The improved driving current can be attributed to the carrier mobility enhancement. In addition, it should be noted that the lack of saturation in drain current is observed for the Ge-doped ELC poly-$Si_{0.91}Ge_{0.09}$ TFTs. The non-saturated drain current is resulted from impact ionization occurring in the high electric field region at the drain end of the channel [4.42] – [4.43]. Holes are injected into the floating body forcing further electron injection from the source, and then collected by the drain. This added drain current augments impact ionization which, in turn, forward biases the floating body harder, thereby causing a regenerative action which leads to a premature breakdown. This avalanche phenomenon is related to the carrier tunneling through the bandgap. Therefore, this non-saturated effect becomes more obvious for Ge-doped ELC poly-$Si_{0.91}Ge_{0.09}$ TFTs due to the narrower bandgap of poly-$Si_{0.91}Ge_{0.09}$ thin films.

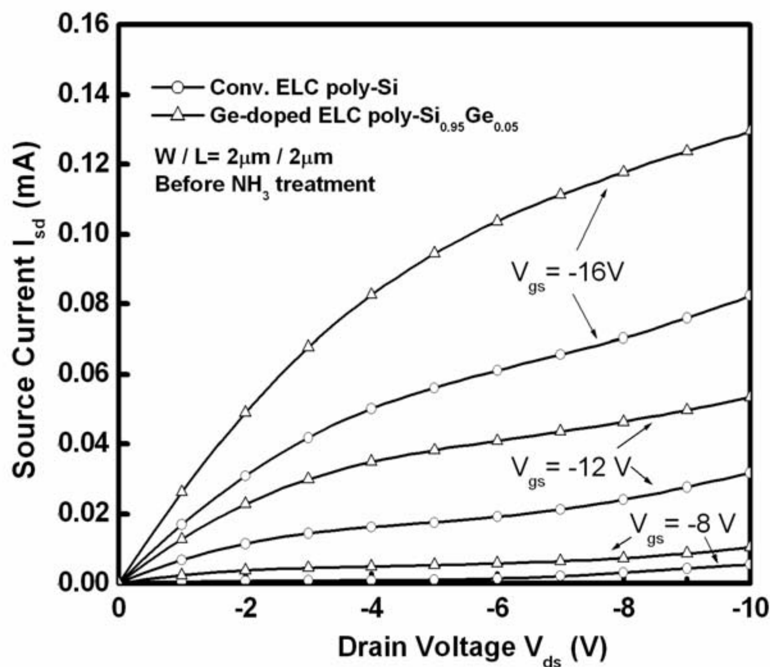


Figure 4.23. The output characteristics of the conventional p-channel ELC poly-Si TFTs and the Ge-dope p-channel poly-$Si_{0.95}Ge_{0.05}$ TFTs.

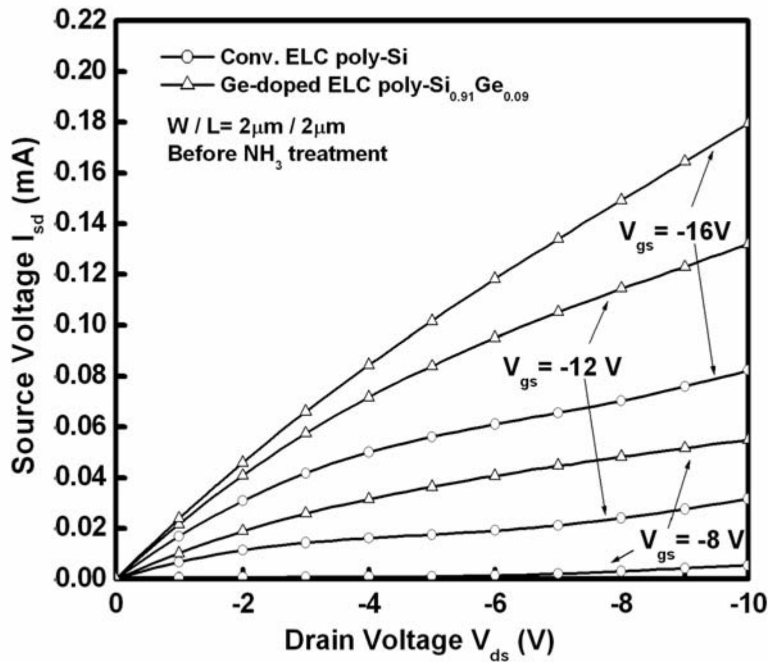


Figure 4.24. The output characteristics of the conventional p-channel ELC poly-Si TFTs and the Ge-dope p-channel poly-$Si_{0.91}Ge_{0.09}$ TFTs.

Figure 4.25 and Figure 4.26 show the n-channel and p-channel transfer characteristics of the conventional ELC poly-Si TFTs and the Ge-dope poly-$Si_{0.95}Ge_{0.05}$ TFTs after 4-h NH_3 plasma treatment, respectively. The device dimension is W = L = 2μm. The electrical characteristics after plasma treatment are summarized in Table 4-4 and Table 4-5. An improvement of field-effect mobility can be found in both kinds of TFTs after plasma passivation due to the reduction of defects states [4.44] – [4.45]. On the contrary, some electrical characteristics slightly degraded after NH_3 plasma passivation. The degradation may be ascribed to the plasma damage during plasma treatment [4.46]. In addition, it can be also found that the passivation efficiency of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs is lower than that of ELC poly-Si TFTs. The hydrogen passivation behavior of the poly-$Si_{1-x}Ge_x$ thin film is more complex than that of poly-Si thin film due to the additions of the Ge-related and $Si_{1-x}Ge_x$-related defects, which may result in the different passivation mechanisms compared

to Si-related defects. According to the paper repoted by T.J. King *et al*, hydrogenation of poly-$Si_{1-x}Ge_x$ TFTs by H^+ ion implantation needed more implant doses than the hydrogenation of poly-Si TFTs [4.47]. The poor hydrogenation efficiency of poly-$Si_{1-x}Ge_x$ TFTs might be explained as that the hydrogen radicals preferentially attached to Si atoms rather than Ge atoms [4.48]. However, most of the defects residing in the poly-$Si_{1-x}Ge_x$ thin film were related to the Ge atoms. Therefore, the defects in poly-$Si_{1-x}Ge_x$ TFTs might not be fully passivated after the 4 hours plasma treatment, which resulted in a poor passivation efficiency of the poly-$Si_{1-x}Ge_x$ TFTs.

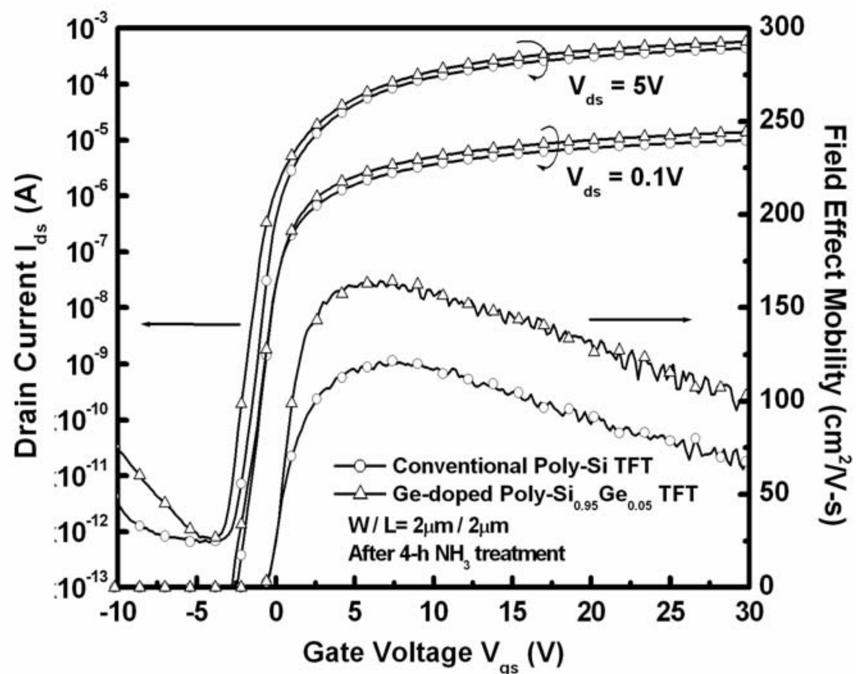


Figure 4.25. The n-channel transfer characteristics of the conventional ELC poly-Si TFTs and the Ge-dope poly-$Si_{0.95}Ge_{0.05}$ TFTs after 4-h NH_3 plasma treatment. W = L = 2μm.

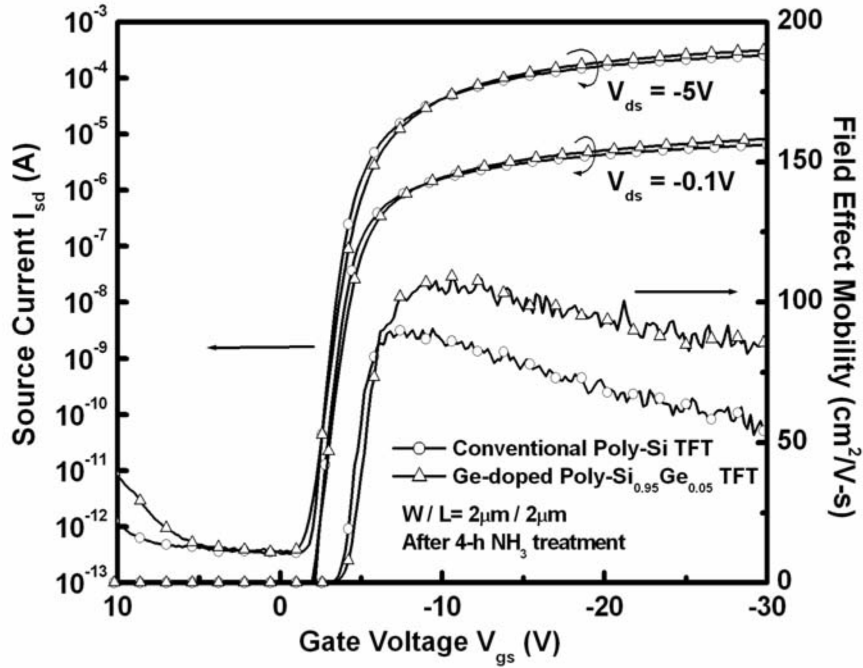


Figure 4.26. The p-channel transfer characteristics of the conventional ELC poly-Si TFTs and the Ge-dope poly-$Si_{0.95}Ge_{0.05}$ TFTs after 4-h NH_3 plasma treatment. W=L = 2μm.

Table 4.4. Measured electrical characteristics of n-channel ELC poly-Si TFTs and Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs after 4-h NH_3 plasma treatment.

W / L (μm/μm)	Structure	Mobility (cm^2/V-s)	Threshold Voltage (V)	Subthreshold Swing (V/dec)	I_{on}/I_{off} @ V_{ds} = -5V
10/10	Poly-Si	160	0.31	372	$1.2x10^9$
	Poly-$Si_{0.95}Ge_{0.05}$	81	1.30	784	$5.2x10^7$
5/5	Poly-Si	164	0.25	331	$1.1x10^9$
	Poly-$Si_{0.95}Ge_{0.05}$	95	1.20	664	$1.4x10^8$
2/2	Poly-Si	122	-0.23	647	$7.0x10^8$
	Poly-$Si_{0.95}Ge_{0.05}$	164	2.57	422	$8.3x10^8$
1.5/1.5	Poly-Si	216	-1.09	396	$9.6x10^8$
	Poly-$Si_{0.95}Ge_{0.05}$	219	-0.65	532	$2.7x10^8$

Table 4.5. Measured electrical characteristics of p-channel ELC poly-Si TFTs and Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs after 4-h NH_3 plasma treatment.

W / L (μm/μm)	Structure	Mobility (cm^2/V-s)	Threshold Voltage (V)	Subthreshold Swing (V/dec)	I_{on}/I_{off} @ V_{ds} = -5V
10/10	Poly-Si	80	-3.71	263	4.4×10^8
	Poly-$Si_{0.95}Ge_{0.05}$	49	-3.78	245	1.9×10^8
	Poly-$Si_{0.91}Ge_{0.09}$	63	-2.17	259	3.5×10^7
5/5	Poly-Si	95	-3.24	265	7.4×10^8
	Poly-$Si_{0.95}Ge_{0.05}$	51	-3.72	323	4.7×10^8
	Poly-$Si_{0.91}Ge_{0.09}$	71	-2.36	275	4.7×10^7
2/2	Poly-Si	91	-3.39	284	7.7×10^8
	Poly-$Si_{0.95}Ge_{0.05}$	109	-4.29	237	6.7×10^8
	Poly-$Si_{0.91}Ge_{0.09}$	116	-4.02	220	6.7×10^7
1.5/1.5	Poly-Si	156	-4.11	205	8.9×10^8
	Poly-$Si_{0.95}Ge_{0.05}$	180	-4.46	265	6.7×10^8
	Poly-$Si_{0.91}Ge_{0.09}$	190	-2.91	245	7.0×10^7

4.4 Summary

Two types of low temperature ELC poly-$Si_{1-x}Ge_x$ TFTs using novel laser and deposition processes were demonstrated in this chapter.

For the ELC poly-$Si_{1-x}Ge_x$ TFTs with a Si capping layer, the poly-$Si_{1-x}Ge_x$ thin film was formed by laser irradiation of a-Si/ poly-$Si_{1-x}Ge_x$ double layer structure. This structure could effectively alleviate the Ge segregation at the film surface during excimer laser irradiation.

Due to the reduction of the surface Ge segregation, better device performances were exhibited for the Si-capped ELC poly-$Si_{1-x}Ge_x$ TFTs in comparison with the direct-ELC poly-$Si_{1-x}Ge_x$ TFTs. However, the intrinsic material properties of the ELC poly-$Si_{1-x}Ge_x$ thin films, such as narrow energy bandgap, small grain size, and poor crystallinity, lead to an inferior device performance compared with ELC poly-Si TFTs.

For the Ge-doped poly-$Si_{1-x}Ge_x$ TFT, the poly-$Si_{1-x}Ge_x$ thin films was fabricated by laser irradiation of a-$Si_{1-x}Ge_x$/poly-Si double layer. In view of excellent crystallinity and large grain size, a-Si film was adopted as the underneath starting active layer. During the second laser irradiation, the Ge atoms would diffuse into the underneath poly-Si layer due to the high diffusion coefficient of Ge in melting silicon and the Ge concentration gradient. Then, the solidification process began from the unmelted poly-Si seed layer, yielding epitaxial growth upward to the surface. Therefore, the grain size was almost unchanged after the second laser irradiation. On the other hand, owing to that the grains could vertically re-grow with a high vertical re-growth rate from the unmelted poly-Si, the Ge segregation could be improved remarkably.

Two competing mechanisms, i.e. the defect states induced by Ge segregated at grain boundary and the carrier mobility enhancement by Ge atoms incorporation, were proposed to explain the electrical characteristics of the Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs with different device dimension. For large device dimension, grain boundaries dominated the carrier transport in the channel, leading to the degradation in device performance. However, when the device dimension was shrunk, carriers suffered from less defect scattering at grain boundaries in the channel region. The carrier mobility of the Ge doped ELC poly-$Si_{1-x}Ge_x$ TFTs was greatly improved due to carrier mobility enhancement effect contributed by Ge atoms. It was inferred that the degree of mobility enhancement by Ge incorporation was beyond that of mobility degradation by defect traps generation when TFT size was reduced to 2μm/2μm. The novel Ge-doped ELC poly-$Si_{1-x}Ge_x$ TFTs exhibited excellent electrical

performance in short channel devices that would meet the requirements for the trends of low-temperature polycrystalline TFTs technology developments.