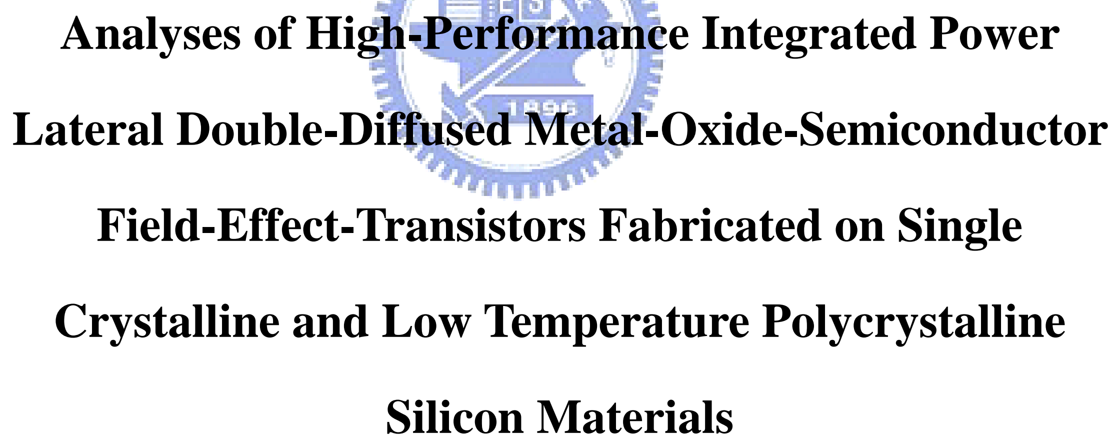
國 立 交 通 大 學
電子工程學系電子研究所

博 士 論 文

製作於單晶矽與低溫多晶矽基材之高性能整合型功率橫向雙擴散金氧半場效電晶體之分析



Analyses of High-Performance Integrated Power Lateral Double-Diffused Metal-Oxide-Semiconductor Field-Effect-Transistors Fabricated on Single Crystalline and Low Temperature Polycrystalline Silicon Materials

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中華民國九十三年七月

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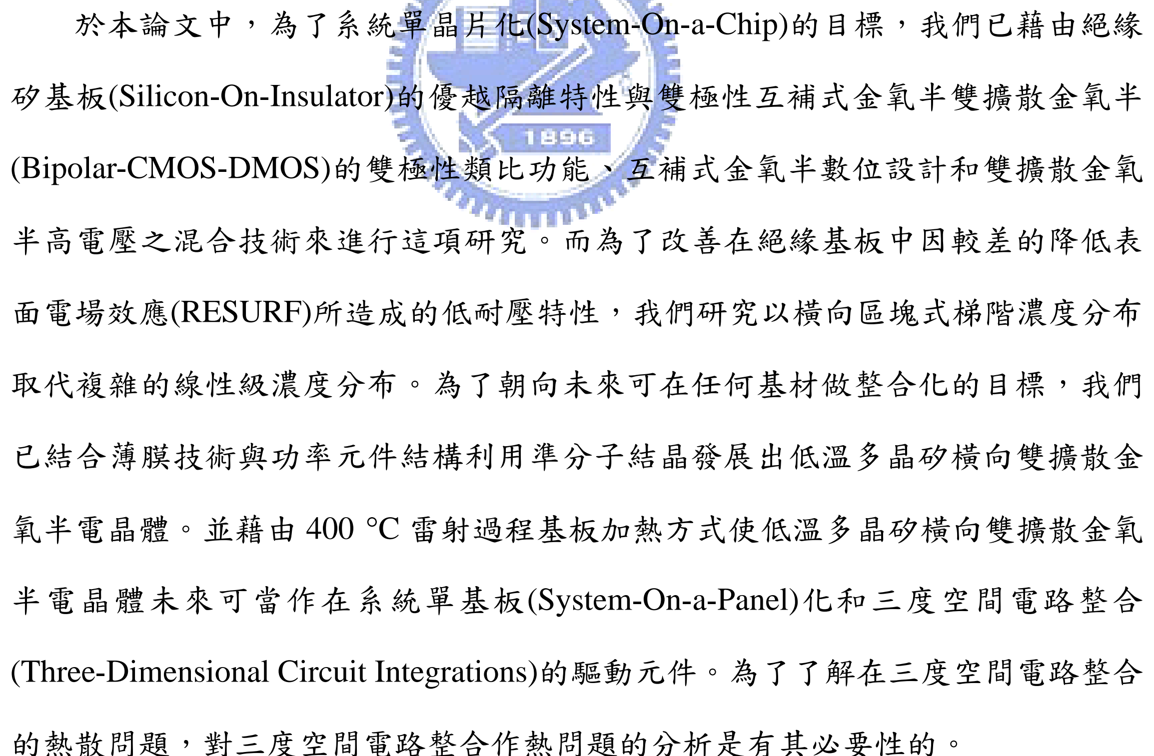
摘要



於本論文中，為了系統單晶片化(System-On-a-Chip)的目標，我們已藉由絕緣矽基板(Silicon-On-Insulator)的優越隔離特性與雙極性互補式金氧半雙擴散金氧半(Bipolar-CMOS-DMOS)的雙極性類比功能、互補式金氧半數位設計和雙擴散金氧半高電壓之混合技術來進行這項研究。而為了改善在絕緣基板中因較差的降低表面電場效應(RESURF)所造成的低耐壓特性，我們研究以橫向區塊式梯階濃度分布取代複雜的線性級濃度分布。為了朝向未來可在任何基材做整合化的目標，我們已結合薄膜技術與功率元件結構利用準分子結晶發展出低溫多晶矽橫向雙擴散金氧半電晶體。並藉由 400 °C 雷射過程基板加熱方式使低溫多晶矽橫向雙擴散金氧半電晶體未來可當作在系統單基板(System-On-a-Panel)化和三度空間電路整合(Three-Dimensional Circuit Integrations)的驅動元件。為了了解在三度空間電路整合的熱散問題，對三度空間電路整合作熱問題的分析是有其必要性的。

首先，我們成功的在不更動任何測試性參數下把十二伏特開基極崩潰和二十五伏特開射極崩潰電壓雙極性、1.2 伏特起始電壓的互補式金氧半和四十伏特崩潰電壓擴散金氧半之雙極性互補式金氧半雙擴散金氧半技術直接用在絕緣矽基板橫

向雙擴散金氧半元件的製作。而為了同時表現出其高功率、高速度和高頻率的特性，其輸出特性、切換與微波性能將以中道方式取代個別特性的最佳化。最後，根據實驗結果，被證實矽基材型的雙極性互補式金氧半雙擴散金氧半技術(Bulk Bipolar-CMOS-DMOS)可藉由絕緣矽基板材料來達到高速度、高頻率和高耐壓的應用，像是高電壓整合型電路開關(10^{-9}秒範圍)與射頻功率放大器(從 10^{6}赫茲到 10^{9}赫茲)。

在階梯濃度的研究中，我們提出區域劃分方法去分析高電壓階梯濃度型絕緣矽基板橫向絕緣閘極雙載子電晶體的結構。發現在導通狀態電特性梯階濃度與線性級濃度元件有相同的順向電壓降。藉由區域劃分中點方式可以推導出崩潰電壓並且可以指出在漂移區中的相關崩潰電場值。再者，為了減少不必要的光罩數，我們發展出衰減因數(Degraded Factor)去求得在最少分區數(Frames)下得到較好的性能。最後，用 660 伏特的梯階濃度結果為例去跟模擬器(MEDICI Simulation)的 606.6 伏特結果比較發現非常的吻合。

在系統單基板化和三度空間電路整合的研究中，我首次提出一新奇的利用準分子雷射長晶技術製作的低溫多晶矽高電壓橫向雙擴散金氧半電晶體(LTPS LDMOS)。然而，為了提升此元件的特性，將從兩個著眼點出發：一是整合功率元件與薄膜技術，另一是說明準分子雷射處理對製造低溫元件的必要性。根據結果得到，在漂移區長度 15-μm和二十五伏特汲極電壓下，經過雷射處理過後的開關電流比(ON/OFF Current Ratio)較處理前的大了 10^{6}倍之多。且經過雷射處理過後的低溫多晶矽高電壓橫向金氧半電晶體在特性導通阻抗和崩潰電壓下也展現出比以前像是半絕緣(Semi-Insulating)、金屬場效平板(Metal-Field-Plate)和移位汲極(Offset-Drain)等高電壓薄膜電晶體(High-Voltage Thin Film Transistors)較好的交換特性(Trade-Off)。

為了進一步提高多晶矽薄膜的結晶性質與低溫多晶矽高電壓橫向雙擴散金氧半電晶體的性能，我們將首次利用準分子雷射結晶時 400 °C基板加熱來達到低溫多晶矽高電壓橫向雙擴散金氧半電晶體的高電壓與極低導通電阻的特性。其開關

電流比在 0.1 伏特和 10 伏特汲極電壓各自展現出 2.96×10^5和 6.72×10^6的特性。最大電流上限值提高到 10mA最大功率上限提升到 1 瓦特以上在 90 伏特汲極電壓和 20 伏特閘極電壓時。相較於傳統的移位汲極(Offset-Drain)薄膜電晶體，其尺寸在通道寬長比(W/L_{ch})600-μm/12-μm下的特性導通阻抗可減少 667 倍。

本論文的最後，我們將討論熱散問題因為有許多有潛力的應用都需要在較高溫度下操作。功率的浪費造成元件額外的溫度上身使得其在高溫環境下發生的效應更為嚴重。而且就功率元件而言常常會比一般元件溫度來的高些，但如果過高的溫度發生在有問題的元件上常常會造成重大的損毀。對於單一顆功率元件的損壞可能會使一台電腦當機、終止汽車的驅動系統或使得一正在運行的車輛停止前進。這問題在三維電路整合會比二維晶片來的嚴重因為在相同的功率下因三維晶片比二維晶片面積要小，導致功率密度極劇上升。所以，確實的了解功率電晶體的熱性質對於使用這些元件的系統可靠度來說是很重要的。為了了解這問題，我們將研究當環境溫度在 300 K 到 400K 時在單晶矽與多晶矽高壓元件間的不同電特性與討論室溫和 400 °C 雷射長晶技術之低溫多晶矽高電壓橫向雙擴散金氧半電晶體的熱穩定度特性。結果發現在 400 °C 雷射長晶技術的低溫多晶矽高電壓橫向雙擴散金氧半電晶體展現出比雷射長晶技術前和室溫雷射長晶技術的低溫多晶矽高電壓橫向雙擴散金氧半電晶體(LTPS LDMOS)低的熱敏感度。因此，400 °C 雷射長晶技術的低溫多晶矽高電壓橫向雙擴散金氧半電晶體非常適合用在未來高熱可靠度的系統單基板化應用。

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ABSTRACT

In this dissertation, for the sake of system-on-a-chip (SOC), silicon-on-insulator (SOI) and Bipolar-CMOS-DMOS (BCD) technology have been studied because of its superior isolation characteristics and mixture of the analog functions of bipolar, digital design of CMOS and high-voltage elements of DMOS on the same chip. In order to improve breakdown voltage from less reduced-surface-field (RESURF) effect of SOI devices, the step doping profile are investigated instead of complicated linearly graded doping profile by the distinct doping region along lateral direction. In order to stride forward the future integrations on any substrates, the LTPS LDMOS using excimer laser crystallization has been demonstrated by combination of the thin film technology and power device architecture. The LTPS LDMOS at 400 °C substrate heating during excimer laser annealing will be used to expect to be a future driver device in system-on-a-panel (SOP) and three-dimensional (3-D) circuit integrations. Additionally, in order to comprehend heat dissipation in 3-D integration circuits, analyses of thermal problems in 3-D circuits are necessary.

First, traditional Bipolar-CMOS-DMOS (BCD) technology, which is designed for

only lateral bipolar (Bipolar, 12 V BV_{CEO} and 25 V BV_{CBO}), complementary metal oxide semiconductor (CMOS, 1.2 V threshold voltage) and double diffused metal oxide semiconductor (DMOS, 40 V breakdown voltage) transistors on the bulk silicon wafer, has been successfully utilized directly to fabricate silicon-on-insulator lateral-double -diffused-metal-oxide-semiconductor (SOI LDMOS) for the first time without changing any trial parameters. To simultaneously display the characteristics of high-power, high-speed and high-frequency, the results of output characteristics, switch and microwave performance must be moderate instead of individual optimum. Finally, according to the experimental results, it is proved that Bulk-BCD technology simultaneously enables high speed, high frequency and high blocking voltage applications—such as those in high-voltage integrated circuit switches (ns-range) and RF power amplifiers (MHz range to GHz range)—using a SOI wafer.

In the study of step doping profile, a partition method is proposed to analyze the high-voltage step-doping silicon on insulator lateral insulated gate bipolar transistor (Step-Doping SOI-LIGBT) structure. The on-state characteristics will be present with the similar forward voltage drop (Vce) value between the step doping and linearly graded doping devices. The breakdown voltage can be deduced by the partition mid-point method and the corresponding breakdown electric field will also be fingered out in the step drift region. Furthermore, in order to reduce the undesirable additional masks, the degraded factor (D) is developed to evaluate the minimum number of frames with the better performance. Eventually, a 660 V step analytical results will be exemplified to compare with a 606.6 V MEDICI simulation, which shows very good agreement by this proposed method.

In the study of future SOP and 3-D integrations, a new low-temperature polycrystalline silicon high-voltage LDMOS (LTPS HVLDMOS) using excimer laser crystallization has been proposed for the first time. However, in order to enhance LTPS

HVLDMOS characteristics, there are two starting points: 1) integrate the thin film technology with the power device, 2) clarify the requirement of excimer laser treatment for low temperature power devices. As a result, the ON/OFF current ratio after laser treatment is improved over 10^6 times than that before laser treatment at L_{drift}=15-μm and Vds=25 V. The LTPS HVLDMOS after laser treatment also demonstrates the better trade-off between the specific on resistance and breakdown voltage against the previous HVTFTs by solid phase crystallization—such as semi-insulating (SI), metal-field-plated (MFP), and offset-drain (OD) HVTFTs.

In order to further improve the quality of crystallized poly-Si thin films and the performance of LTPS LDMOS, low-temperature poly-Si lateral double diffused metal oxide semiconductor (LTPS LDMOS) with high voltage and very low on-resistance has been achieved using excimer laser crystallization at 400 °C substrate heating for the first time. The ON/OFF current ratios were exhibited with 2.96×10^5 and 6.72×10^6 while operating at Vds=0.1 V and 10 V, respectively. The maximum current limit was up to 10 mA and maximum power limit could be enhanced over 1 Watt at Vds=90 V and Vgs=20 V. The Ron,sp with dimensions of W/L_{ch}=600-μm/12-μm could be significantly decreased 6.67×10^2 times in the magnitude as compared with the traditional offset drain (OD) TFTs.

At last part of this thesis, the issue of heat dissipation will be discussed because many potential applications require operation at elevated temperatures. The effects of a high temperature ambient are exacerbated by power dissipation which causes additional temperature rise within the device. Power devices are often expected to run hotter than other component, but the excessive temperature rise of an inherently problem device will often lead to catastrophic failure. Failure of a single power device can shut down a computer, bring to halt a motor-driven system, or stop a vehicle dead in its tracks. This problem is anticipated to be exacerbated in 3-D circuit integration because the same

power generated in a 2-D chip will now be generated in a smaller 3-D chip size resulting in a sharp increase in the power density. Therefore, accurate characterization of the thermal properties of power transistors is critical to the reliability of the systems using these devices. In order to understand this problem, the different electrical characteristics between crystalline and polycrystalline high voltage devices will be studied and the thermal stability of the LTPS LDMOS between the room temperature and 400 °C irradiation will also be discussed over the ambient temperatures of 300 K–400 K. The results of ambient temperature variation in LTPS LDMOS at 400 °C irradiation are demonstrated the less sensitivity than the LTPS LDMOS before laser irradiation and at room temperature irradiation. Hence, the LTPS LDMOS at 400 °C irradiation is very suitable for future system-on-a-panel (SOP) applications with higher temperature reliability.

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