Chapter 1

Introduction

Power devices have been developed with smart power technology and widely applied in industrial segment—such as home automation network nodes, motors power supply bridge, in automotive field—such as dense engine control units, smart sensors, and single-chip smart switches, in consumer segment—such as single chip camera controls, in computer market—such as hard disk drives, motherboards, and graphics cards, and in car-radio field—such as audio amplifiers [1.1]-[1.6]. There also have a wider range of applications through the use of SOI wafers with high speed, high frequency and high blocking voltage capabilities for radio frequency (RF) power amplifiers, plasma display panel (PDP) scan driver IC, and RF power supply [1.7]-[1.9]. Recently, there is a great interest to study the power integrated circuits (PICs) and high voltage thin film transistors (HVTFTs) in order to achieve the goals of system-on-a-chip (SOC) and system-on-a-panel (SOP) [1.10]-[1.12]. In this chapter, the design concept will be introduced firstly and then the current status of power devices will be illustrated with the subsections of power MOSFETs, isolated gate bipolar transistors (IGBTs), application examples, and reliability issues. Finally, the motivation in this dissertation will be clarified with detailed description from the integration requirement to the future reliability consideration.

1.1 Brief of Power Device Design

An ideal power device is difficult to be fabricated because it is usually limited in

the current conducting of the on state and voltage blocking of the off state in a number of ways. For example in switch application, it actually requires enough time to finish the completed transition during the change between the on and off state. Furthermore, while operating in the destructive modes, the damage not only destroys the device performance but also affects the surrounding circuit elements and makes an overall system failure. Additionally, the cost and complexity will significantly determine the device performance in the overall circuit and focus a particular application aspect like device types, control, and protective circuitry function. Thus, designers will only depend their need to design the device, and frequently the cost and physical size restrict the device usefulness.

In the recent year, the determination from cost and physical size is more and more evident in power electronics. The power devices will be designed with the limited performance and only can work in some fields of function. It is not surprising that no single device can support and cover all capability in power device applications because there have wide requirements in the blocking voltage, driving current, and switching speed. Since 1995, the designers start to breakthrough this limitation and seek the adequate balance between cost and performance. They try to enhance the blocking voltages by modified junction arrangement and develop new devices to overcome some limitation in previous device types—such as using novel structures or materials. Recently, the advent material is silicon-carbon (SiC), which can bring the high voltage, high frequency, and high temperature robustness for power devices [1.13]-[1.17]. But, these days, the power devices are still widely fabricated with the material of silicon (Si) because silicon can achieve the excellent compromise among the semiconductor properties, material cost, and easy fabrication in nowadays foundry.

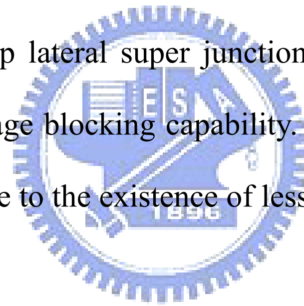
1.2 Current Status of Power Semiconductor Devices

1.2.1 Power MOSFETs

Faster switching characteristics for low-medium power levels can be obtained using bipolar junction transistors (BJTs) or metal oxide semiconductor field effect transistors (MOSFETs). The BJTs for p-n-p junction have fast switching capability than thyristors with p-n-p-n structure, but suffer from losses in the control electrode. Power MOSFETs are evolved from MOS integrated circuit technology and have potential to replace BJTs for low voltage, low power and high-frequency applications. The high input impedance of the MOS gate allows the easy integration of the control circuit and eliminates power loss from gate terminal. The ultra low specific on resistance has led to replace the rectifiers with low voltage and low power MOSFETs used as synchronous rectifier [1.18], increasing the efficiency of low voltage switch mode power supplies (SMPs). The other advantages are the fast switching capability and improvement in forward biased safe operating area (FBSOA). In order to make efforts towards optimizing the structure, design, and process, the v-shaped groove MOS (VMOS), double diffused MOS (DMOS), u-shaped groove (UMOS), and trench structures with improved specific on-resistance have been developed.

Although the MOSFET structures have a lot of merits, they are not suitable for high voltage designs. The reason is that the power MOSFETs suffers from the rapid increase in specific on-resistance of the drift region in order to increase the breakdown voltage. Until 1998, Siemens corporation has successfully fabricated the COOLMOS™ device by superjunction concept to attain a shrink factor of 5 in cell size and reduce specific on-resistance against the actual state-of-the-art in power MOSFETs [1.19],

[1.20]. The COOLMOS™ is evolved from a conventional DMOS structure but it breaks the square law dependence in the case of standard DMOS with the linear voltage relationship in specific on resistance. In a conventional DMOS, the high blocking voltage requirements is obtained by reducing the doping concentration and increasing the thickness of the epitaxial layer, which is relative to increase the on-resistance. However, in COOLMOS™ device, by extending the body region of a DMOS with a vertical strip in the epitaxial layer, the high blocking voltage capability can be obtained in both horizontal and vertical directions by reduced surface field (RESURF) effect and the junction voltage drop can be avoided. Moreover, while the donor and acceptor charge reach the balance state in their depletion regions, the superior breakdown voltage can be achieved well than any state-of-the-art power MOSFETs. Additionally, it also can be attempted to develop lateral super junction structures into silicon-on-insulator (SOI) to increase their voltage blocking capability. But, this idea is merely suitable for short drift length devices due to the existence of less-RESURF effect in long drift length ones.



1.2.2 Insulated Gate Bipolar Transistors (IGBTs)

In order to obtain a better performance, the combined benefits of fundamental devices are study to devote in developing hybrid semiconductor devices—such as driving a BJT with a power MOSFET in the conjunct configuration. Insulated gate bipolar transistor (IGBT) is one of the efficient combinations with a BJT and MOSFET device. The function of MOSFET is to provide the base current to drive the connected BJT. This structure requires a high voltage MOSFET of equal size to drive the low current gain high voltage BJT, which has a wide base region. While the different kind of carriers are injected from the collector into the base region of BJT, the IGBT device will

conduct in the high-level injection regime, which can possess a very low forward voltage drop at high current levels. Additionally, the MOSFET gate oxide insulates the gate electrode so that there is no power dissipation in the control gate. Unfortunately, although the IGBT structure has the above advantages, the switching speed will be limited by the stored charge in the base region, which is generated from carrier injection, and this minority carrier lifetime will determine the turn off time during the transient characteristics. Thus, the non-punch-through (NPT) IGBT has been developed with the lifetime reduction techniques to shorten the turn off time but increase the forward voltage drop from a long base region.

As the voltage rating is raised over 1200 V, the very large thickness of base region will make the thick epitaxial growth, which is more expensive [1.21]. Punch-through (PT) IGBT is a well-known structure to support the same forward blocking voltage with a smaller thickness of the base region. Although the PT IGBT structure seems to be widely used, the two kinds of structures have their individual supporters and so far there have not a final conclusion which is the best one. In respect of IGBT functions, it can offer a wide safe operating area (SOA) with a forward drop comparable to a diode, but also show the bad turn-off performance [1.22], [1.23]. The IGBT has replaced the role of BJT for medium voltage and medium power applications and also replaced the thyristor in many high power applications. In next stage, the main development goals of IGBT is to increase the current driving capability, blocking voltage capability, switching speed, device ruggedness, and to decrease the saturation voltage and manufacturing costs. Additionally, in order to improve the forward voltage drop, the IGBTs have led to the emergence of the trench gate structure to increase the cell densities. The optimum cell structure and further development in trench technology will allow a significant reduction in saturation voltage [1.24].

1.2.3 Examples of Power Devices Applications

In order to further understand its functions, there are some examples described as follows for power devices applications. The hard disk drive (HDD) is composed by several chips—such as microprocessor, “combo” chip, and pre-amplifier. The complex microprocessor integrating non-volatile memory for software is dedicated to data read-write and head positioning. A “combo” chip, including power, analog and digital stages, takes care of spindle rotation control plus voice coil actuation for head moving and positioning. The read-write pre-amplifier has to perform very high bandwidth and extra low noise. The power MOSFETs are used in the spindle rotation and voice coil motor (VCM) controls as spindle drives and DC-to-DC converters. Recently, a double actuator has been introduced to improve precision in head positioning on the disk [1.25]. There are two different families called milli-actuators and micro-actuators. The first one based on a piezoceramic material placed on the voice coil suspension, are electrically similar to a capacitor driven at high voltage. The others are implemented by micro machining directly integrated on the same silicon of their driver and controller.

In recent years, color plasma display panel (PDP) has begun to attract a great deal of attention as the next generation of large-screen flat panel display because the products of the PDP over 40 inches in diagonal have been announced by several PDP manufacturers since 1996. It is one of the most promising flat panel devices for full color wall hanging digital high definition television (HDTVs). The PDP driver ICs fall into two categories data driver ICs and scan driver ICs. As the PDPs have been developed toward the large screen and high resolution, the number of the high voltage driving circuits in one PDP has been increasing. Therefore, PDP driver ICs are required highly to possess multiple output circuits and, in the contrast, the chip size should be reduced by another technique. These ICs are also required high voltage driving

capability ranging from 60 V to 200 V [1.26]. A scan driver IC requires both high blocking between 150 V and 250 V and high current capability from 200 mA to 400 mA, which will bring a large chip size by conventional Bulk technology. Therefore, for reducing the chip size of the IC/power dissipation and increasing the switching speed, the SOI technology should be utilized to fabricate a scan driver IC by its superior isolation characteristics.

Power integrated circuits (PIC) have been developed in the recent advances for circuit integration technology. This technology has improved the significant reliability and reduced the size, weight, and cost as important motivations. Power electronics is used to process and control the electric energy flow by combining the knowledge of power systems, solid-state electronics, electrical machines, signal processing, and electromagnetics. The main building block of a power electronic system is a converter, which uses power semiconductor devices to increase the conversion efficiency. The circuit integration can extend the use of power converters for portable and automotive applications.

The present revolution of power electronics, which is mainly due to fast evolution of power semiconductor devices, has resulted in cost reduction, performance improvement, and widespread application of power electronics systems. The energy conservation through more efficient use of electrical energy and its effect on environment is the other important role of power electronics [1.27]. The use of power converters for variable speed drives results in the energy savings and recovers the additional converter cost in a short period. The wide range variable speed AC drives are being widely applied in industrial applications and home applications. The power electronics plays a dominant role in pollution control by permitting the use of electronic and trains, and generation of power form environmentally clean sources.

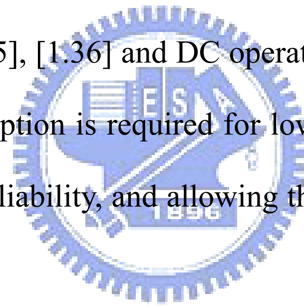
1.2.4 Power Device Reliability

The switching power devices are subjected to a large number of stresses as the switching frequency, voltage, and current levels in the power converters. These stresses led to inferior performance, short-term, or long-term reliability concerns like power losses and electromagnetic interface (EMI), short circuit and unclamped inductive switching, or field failure [1.28]. Hard switching of power device involves the intervals of high current and voltage stress, which lead to power loss and reliability concerns. Soft switching can minimize the overlapping portions of current and voltage transients, which reduces the switching power loss and improves the efficiency [1.29]. In a power device, the silicon chip is mounted on a carrier and sealed for access to the external circuit elements. This package must be able to efficiently dissipate the heat generation within the device. In addition, the electrical connections by use of wire bonds will introduce the parasitic resistance and inductance. It also will experience the serious electrical and thermal cycles even under normal operation.

The most common stresses suffer in the switching devices include high dV/dt across as follows: 1) the device terminals, 2) unclamped inductive stress, which forces the device to operate in the avalanche operational mode, and 3) stressful reverse recovery of the freewheeling diode, which is connected anti-parallel to the main device. Firstly, the inductive turn-off under high-load conditions is the most common cause of high dV/dt across the device. This turn-off dV/dt can induce the parasitic bipolar transistor turn on in a power MOSFET or cause the parasitic thryristor latch up in the IGBT. Secondly, the unclamped inductive stress makes the device operate at its breakdown voltage under high current conditions. The resulting high power dissipation can cause the device failure if the rise of temperature is beyond the limits. Thirdly, the reverse recovery of the anti-parallel diode brings a high dV/dt across the device, which

it may not be able to sustain. In power MOSFETs, the internal body diode is usually used as the anti-parallel diode. Therefore, reverse recovery suffers much more stress than with an external diode.

The SOI technology is based on the use of a buried oxide layer (BOX), which provides the better electrical isolation and significant reduction of parasitic capacitance [1.30]-[1.34]. In spite of the best electrical performance and operating frequency of SOI LDMOS devices, the low thermal conductivity of the BOX layer does not allow a fast and efficient heat extraction from the active silicon layer to the substrate becoming critical in high power devices due to the large delivered current levels. As a consequence, severe self-heating effects can eventually degrade the device electrical characteristics under prolonged high-temperature operation—i.e. long pulse overloads with high power losses [1.35], [1.36] and DC operation [1.37]. Thus, it is important that the very low power consumption is required for low operating temperature of the chip, increasing overall system reliability, and allowing the use of more power devices on the same board.



1.3 Evolution of Power Semiconductor Technology

1.3.1 High Voltage Integrated Circuit (HVIC)

Various technological advances in VLSI and high voltage devices have made possible the development of high voltage integrated circuits (HVICs), which typically combine one or more high voltage transistors on the same chip with low voltage analog or digital control circuitry. In applications, the HVICs are very attractive and cost effective solution for power control systems, such as motor drive, electronic, and

switched mode power supplies [1.38]. The use of HVICs can also significantly reduced the total parts count, thus resulting in smaller system size as well as the improvement of reliability. The HVIC is composed of two parts: low voltage section for low side power switch driving and digital control of application, and the high voltage section integrating the stages required for high side power switching driving and level shifting of the digital signal from ground to the floating source of the high side power switch. In order to turn on high side switch, it needs higher gate voltage than source voltage because of the source of high side switch is floated from ground to rectified mains high voltage. Therefore, high side gate drive part must be carefully designed to sustain the high voltage and be isolated from low voltage control part [1.39], [1.40]. In order to transfer the signal, a specialized gate-driver is required in the LDMOS to ensure the fastest switching time. The stray impedances associated with package bond wires and circuit board tracks limit the charging current and increase the switching time. Thus, by integrating the gate-discharge transistors, the turn off time can be reduced but the turn on still affected by the stray impedances. Low impedance paths, in the form of wide metal or tracks, are provided to carry the large LDMOS gate charging currents. The output of the gate-driver is applied to many points along the winding LDMOS structure to minimize gate signal propagation delays.

1.3.2 System-on-a-Chip (SOC) and Three-Dimensional Integration

System-on-a-chip (SOC) is a broad concept that refers to the integration of nearly all aspects of a system design on a single chip [1.41], [1.42]. These chips are often mixed signal and/or mixed technology designs, including such diverse combinations as embedded DRAM, high performance and low power logic, analog, radio frequency (RF), and programmable platforms. SOC designs are often driven by the ever-growing

demand for increased system functionally and compactness at minimum cost, power consumption, and time to market. These designs form the basis for numerous novel electronic applications in the near future in areas such as wired and wireless multimedia communications including high-speed internet applications, aircraft/automobile control and safety, and home security. Three-dimensional (3-D) integration to create multiplayer Si ICs is a concept that can significantly improve deep-submicrometer interconnect performance, increase transistor packing density, and reduce the chip area and power dissipation [1.43]. Additionally, 3-D ICs can be very effective vehicles for large-scale on-chip integration of different systems. The 3-D architecture offers extra flexibility in system design, placement, and routing.

For instance, logic gates on a critical path can be placed very close to each other using multiple active layers. Furthermore, the 3-D chip design technology can be exploited to build SOCs by placing circuits with different voltage and performance requirement in different layers. The 3-D integration would significantly alleviate many of the problems for SOC fabrication on a single Si layer. The 3-D integration can reduce the wiring, thereby reducing the capacitance, power dissipation, and chip area and therefore improve the chip performance. Additionally, the digital and analog components in the mixed-signal systems can be placed on different Si layers thereby achieving better noise performance due to lower electromagnetic interference between such circuit blocks. From an integration point of view, mixed-technology assimilation could be made less complex and more cost-effective by fabricating such technologies on separate substrates followed by physical bonding.

1.3.3 Technology Options

In order to realize the future silicon-on-a-panel and three-dimensional circuit

integration, the growth of low temperature polycrystalline silicon (LTPS) appears to the most promising technology to fabricate the multiple active layers on the separated dielectric interlayer for compatibility with the relevant two-dimensional process. The best way of forming the high quality polysilicon films is obtained by crystallization of precursor amorphous silicon films [1.44], [1.45]—i.e. solid phase crystallization (SPC) [1.46], metal induced later crystallization (MILC) [1.47], [1.48], and excimer laser crystallization (ELC) [1.49], [1.50]. Solid phase crystallization can process with high uniform polyslicon grains and high throughput. It is an effective method but the grains tend to include many intra-grain defects like twins and stacking faults. These large-scale crystalline defects will cause the decrease in the field effect mobility and the increase in the threshold voltage of the devices [1.51]. Another method bases on the nickel (Ni) seed to induce simultaneous lateral crystallization due to an interaction of the free electrons from the metal with covalent Si bonds near the growing interface [1.52]. It offers even lower thermal budget (<500 °C) and large grain size than the method of solid phase crystallization. However, in spite of the above merits, it is not suitable for the future integration technology due to the metal contamination, which leads to a large leakage current and unstable electricity especially in high voltage operation (>100 V).

Excimer laser crystallization (ELC) is a technique for using UV region emission to grow relative large grains from the molten phase during the short pulse duration (10-30 ns) [1.53]. As the energy is increased to reach the maximum grain size, the Si film is almost totally melted and only few unmelted crystalline clusters, sparsely distributed. When this condition occurs, the grains grow laterally around the crystalline clusters until they impinge on each other and the excess of 1-μm grain size can be reached. This particular condition is often referred to as super lateral growth (SLG) [1.54]. The excellent performance can be obtained with high electron-field mobilities in the range of 300-400 cm^2 V s^{-1}, less in-grain defects, low subthreshold swing, low threshold

voltage, and no metal contamination against the methods of SPC and MILC [1.55]-[1.57]. Furthermore, ELC allows the use of the inexpensive glass substrates instead of expensive quartz ones because of the shallow heat-affected damage and below 600°C fabrication at the nano-second process time [1.58]. According the above reasons, the excimer laser crystallization (ELC) seems to the better technology to form high-quality polysilicon at low temperatures (< 600 °C) for future system-on-a-panel and three-dimensional integration [1.59].

1.4 Motivation

In order to realize the circuit integration, silicon-on-insulator (SOI) seems to be a promising technology because of its superior isolation characteristics than the junction isolated (JI) devices, reducing the minor carriers effect in LIGBT by a thin SOI layer, and increasing the blocking voltage under well-RESURF design. In recent years, Bipolar-CMOS-DMOS (BCD) technology becomes a good candidate to achieve the aim of System-on-a-chip (SOC) because it can mix with the analog functions of bipolar, digital design of CMOS and high-voltage elements of DMOS on the same chip toward high-voltage, high-power and high-density developments. The “high-voltage BCD” is changing from junction to dielectric isolation adopting the SOI approach to attain a large dense chip, a low parasitic capacitance and high power efficiency, to improve RF thermal degradation characteristics, and to satisfy requirements such as reduced parasitic capacitance, suppression of bipolar parasitic effects and substrate leakage. The “high density” BCD, so called “VLSI BCD”, is following the CMOS roadmap converging to the same process platforms with the challenge to maximize power device performances maintaining full compatibility. Nevertheless, previous BCD technologies

are interested in analyzing low-voltage (~100V) and thin-silicon-layer characteristics with several cycles of SOI generations. Therefore, in chapter 2, the bulk BCD technology for lateral Bipolar (12 V BV_{CEO} and 25 V BV_{CBO}), CMOS (1.2 V threshold voltage) and DMOS (40 V breakdown voltage) transistors will be attempted to directly fabricate the SOI-LDMOS devices without modifying any process for economy in system integration process.

Unfortunately, although the silicon-on-insulator (SOI) have many advantages for integration circuits, there still have two significant problems in the SOI devices—such as self-heating effect and lower breakdown than JI devices. The lower breakdown voltage is due to less RESURF effect with strong vertical electric field from buried oxide layer [1.60]. Thus, in order to get the high breakdown voltage devices, a linearly graded doping profile in the drift region is necessary to provide a more uniform electric filed distribution along the drift region and so to optimize the RESURF condition [1.61]. Nevertheless, in practice, it is impossible to obtain a perfectly linear variation doping in the drift region from the drain to the source side. Moreover, the linearly graded doping profile requires the precise designs in sequence of slit openings for mask of the impurity implantation and the subsequent drive-in process for 1200 °C at 580 min [1.62]. In chapter 3, when replacing the linear profile by the distinct doping region along lateral direction, the separated uniform doping can be easily realized by different implant dosages. Nevertheless, the additional mask of the step doping case is a serious problem in the cost aspect. Hence, this chapter is to offer a partition method and degraded factor to derive the electrical characteristics and reduce the undesirable additional masks with the better performances.

In order to stride forward the system-on-panel (SOP) applications and three dimensional (3-D) circuit integrations, low-temperature polysilicon high-voltage thin film transistors (LTPS HVTFTs) have been widely studied and discussed in liquid

crystal displays, field emission displays, plasma displays, and high speed printers. These HVTFTs include the offset drain (OD), lightly doped-drain (LDD), metal field plated (MFP), Multi gate (MG), and semi insulating (SI) HVTFTs. Although these devices provide the high blocking or current capability, they still exist a lot of issues—such as on-state degradation, gate dielectric reliability, circuit/operation complexity, and surface contamination—resulting in the unsuitable implementation of the integration electronic systems. In chapter 4, the LTPS LDMOS using excimer laser crystallization has been demonstrated by combination of the thin film technology and power device architecture for the first time. The excimer laser crystallization (ELC) is a promising technology to obtain the high current capability due to the large grains, less defects, and compatible glass substrate against the solid phase crystallization (SPC) of HVTFTs [1.63]. The LDMOS architecture is a promising design to obtain high blocking capability due to the reduced-surface-field (RESURF) against the only offset drain (drift) region of HVTFTs [1.64]. Additionally, in order to reveal the necessity of laser technology in future 3-D integration system, the influence of excimer laser crystallization for improving the current capability in LTPS LDMOS will also be estimated in this chapter.

Although the LTPS LDMOS using excimer laser crystallization has been developed to accomplish the initial scope in SOP and 3-D integration in chapter 4, its current capability is not enough to act as a driver device for future system integration. Thus, in order to improve its performance, the new grain growth technology is necessary to obtain the high quality of polysilicon thin film and expected close to the characteristics of single crystalline silicon (c-Si) LDMOS. In the previous studies, we know that the poly-Si films obtained with smaller grain sizes is due to the extremely fast solidification velocity during excimer laser annealing—i.e. the duration in the order of nano-seconds. Therefore, in order to enhance the current driving capability, the solidification velocity of molten Si must be controlled with the three factors: laser pulse

width, energy density, and substrate temperature during excimer laser annealing. However, among the three factors, the substrate temperature during excimer laser annealing is the most effective to control the solidification velocity without thermal damage to the glass substrate. This means that a low cost glass substrate can be used for suppressing the SiO_2 interface temperature below 600 °C. Additionally, the temperature of 400 °C substrate heating is the most appropriate because the extension of solidification velocity will tend to saturate when the substrate is heated over 400 °C. Therefore, in chapter 5, the 400 °C substrate heating during excimer laser annealing will be used to fabricate the high current driving LTPS LDMOS for future driver devices in SOP and 3-D integration.

In two dimensional integration circuits (2-D ICs), heat dissipation has been a serious problem to degrade the device performances and impact the interconnect/device reliability due to increased junction leakage, electromigration failures, and accelerated other failure mechanism [1.65]. This problem is anticipated to be exacerbated in 3-D integration because the same power generated in a 2-D chip will now be generated in a smaller 3-D chip size resulting in a sharp increase in the power density [1.66], [1.67]. Additionally, in recent years, many potential applications are gradually required to operate at elevated temperatures. In power devices, they are often expected to run hotter than other component, but the excessive temperature rise of an inherently problem device will often lead to catastrophic failure and an increase in on-resistance. In active matrix liquid crystal display (AMLCD), the back illumination will increase the operating temperature of the hydrogenated amorphous silicon (a-Si:H) TFTs to over 70 °C. Thus, before implementing the 3-D integration, analyses of thermal problems in 3-D circuits are necessary to comprehend the limitations of this technology and also evaluate the thermal robustness of different designs. In chapter 6, the different electrical characteristics between crystalline and polycrystalline high voltage devices will be

studied and the thermal stability of the LTPS LDMOS between the room temperature (in chapter 4) and 400 °C irradiation (in chapter 5) will also be discussed over the ambient temperatures of 300 K–400 K.

Chapter 2

Investigation of Conventional Single-Crystalline Silicon -On-Insulator Lateral-Double-Diffused-Metal-Oxide -Semiconductor (SOI Lateral-DMOS) Fabrication by Bipolar-Complementary MOS-DMOS Process on Bulk Silicon Substrate

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In this chapter, traditional Bipolar-CMOS-DMOS (BCD) technology, which is designed for only lateral bipolar (Bipolar, 12 V BV_{CEO} and 25 V BV_{CBO}), complementary metal oxide semiconductor (CMOS, 1.2 V threshold voltage) and double diffused metal oxide semiconductor (DMOS, 40 V breakdown voltage) transistors on the bulk silicon wafer, has been successfully utilized directly to fabricate silicon-on-insulator lateral-double-diffused-metal-oxide-semiconductor (SOI LDMOS) for the first time without changing any trial parameters. To simultaneously display the characteristics of high-power, high-speed and high-frequency, the results of output characteristics, switch and microwave performance must be moderate instead of individual optimum. Finally, according to the experimental results, it is proved that Bulk-BCD technology simultaneously enables high speed, high frequency and high blocking voltage applications—such as those in high-voltage integrated circuit switches (ns-range) and RF power amplifiers (MHz range to GHz range)—using a SOI wafer.

2.1 Introduction for BCD and SOI BCD

In a time of fast technology advancement, smart power technologies represent an answer to the every increasing market demand of system-on-silicon where both the signal processing part (analog and/or digital) and true power actuators can be combined. This is not only an economical requirement because the integration brings several advantages in term of reliability improvement, electromagnetic interference (EMI) reduction, and last but not least, space and weight reduction. Several mixed technologies have been generated to properly address specific application needs. In this light, concepts like technologies portability are gaining strong importance since allow synergy between power discrete advancements and signal part evolution due to scaled horizontal and vertical dimensions. At the beginning of the smart power era a new process technology category, called BCD, is introduced mixing on the same chip [2.1]. After that time the progress has evolved not only towards the reduction of the minimum lithography but also looking at the needs of different application fields in terms of type and variety of integrable components and maximum voltage capability. A wide process family is today available from 16-V and 700-V.

Since a few years, a splitting in the roadmap in three major technology directions is happening with different evolving criteria: 1) the "high-voltage BCD" are changing from junction to dielectric isolation adopting the SOI approach to satisfy requirements such as reduced parasitic capacitance, suppression of bipolar parasitic effects and substrate leakage. Plasma display panel drivers are products which take advantage of this new approach in the high voltage BCD field. 2) "high power BCD" are being pursued for those applications, especially in the automotive field, in which high current and only a moderate control circuit integration is needed and the reduction of the power

device areas is limited by the capability to dissipate the power. 3) in the “high density” direction, the so called “VLSI BCD”, are following the CMOS roadmap converging to the same process platforms with the challenge to maximize power device performances maintaining full compatibility with advanced CMOS and non-volatile-memories (NVM) of equivalent lithography generation.

Bipolar-CMOS-DMOS (BCD) technology, which can mix with the analog functions of bipolar, digital design of CMOS and high-voltage elements of DMOS on the same chip, has been widely applied in commerce toward high-voltage, high-power and high-density developments. It can be used in the automotive field to make very dense engine control units, sophisticated smart sensors and single-chip smart switches for multiplex wiring circuitry [2.2]-[2.4]. In the computer market it can be employed to integrate hard disk drivers [2.5]. In car-radio filed to realize complex and powerful audio amplifiers [2.6], [2.7]. In consumer segment, single chip camera controls and in general single chip solutions for portable equipments can become typical applications [2.8]. Other promising applications in industrial segment are home automation network nodes, motors power supply bridges.

Most recently, silicon on insulator BCD (SOI BCD) has been improved to integrate BCD with SOI technology to attain a large dense chip, a low parasitic capacitance and high power efficiency and to improve RF thermal degradation characteristics with respect to the display and RF applications among others [2.9], [2.10]. Silicon on insulator (SOI) process has many advantages over a conventional junction isolated process. Latch-up is eliminated, parasitic capacitances are much smaller (reducing cross talk and increasing speed) and oxide isolation increasing packing package density. Various applications of BCD-SOI technology, such as automotive and class-D audio, benefit from the total suppression of DC parasitic currents, latch-up, and low capacitances. The advantages in reduction of mask count,

elimination of epitaxy and smaller device areas compensate for the disadvantage of the higher cost of the direct wafer-bonded substrate. Nevertheless, previous researchers were interested in analyzing low-voltage (~100V) and thin-silicon-layer characteristics by several cycles of generation of SOI reduced surface field (RESURF) BCD technology.

In this chapter, traditional Bulk-BCD technology is first attempted in the direct fabrication and analysis of a high-voltage-rating SOI LDMOS on a thick SOI without modifying any processes for economy. The process flow will be described as the following compatible Bulk-BCD technology step by step. The electricity discussion is divided into three major parts: First, the safe-operating-area (SOA) is investigated to show that its operation region is sufficiently large in many field manipulations. Second, the transient character is analyzed to illustrate that a thicker silicon layer will not affect the SOI LDMOS speed more seriously for the high-voltage integrated circuit (HVIC) switch. Finally, microwave performance is simulated to verify that this technology can be used in a radio-frequency (RF) amplifier.

2.2 Device Fabrication

The compatible LDMOS structure was fabricated using a bonded SOI wafer ($\rho \approx 1$ to $100\ \Omega$-cm) with a 4-μm buried oxide and a 5-μm silicon film layer ($\rho \approx 3$ to $5\ \Omega$-cm) using 0.5 μm BCD technology in Fig. 1. The traditional 12/25/5/40 V Bulk-BCD process and 450 V SOI-LDMOS process flows were both listed for comparison in Table 1. First, a BCD N-type bipolar sinker was used to increase the curvature radius against a high electric field at its drain terminal. Then, a p-body was generated by masking the BCD NMOS p-well with 50 KeV boron dose of 4×10^{13} cm^{-2} and driving-in of about

3-μm depth at 1150 ˚C. Next, a 5000-Å-thick BCD LOCOS isolator without an n-channel field implant was formed as its field oxide to reduce the surface electric field. In addition, the unused BCD bipolar p-base was suitable for low-voltage and low-thermal-budget design, such as very large scale integration (VLSI) technology. Furthermore, its 515-Å-thick gate oxide was realized to attain power MOSFET conditions by merging BCD high-voltage active area and CMOS gate oxide thickness.

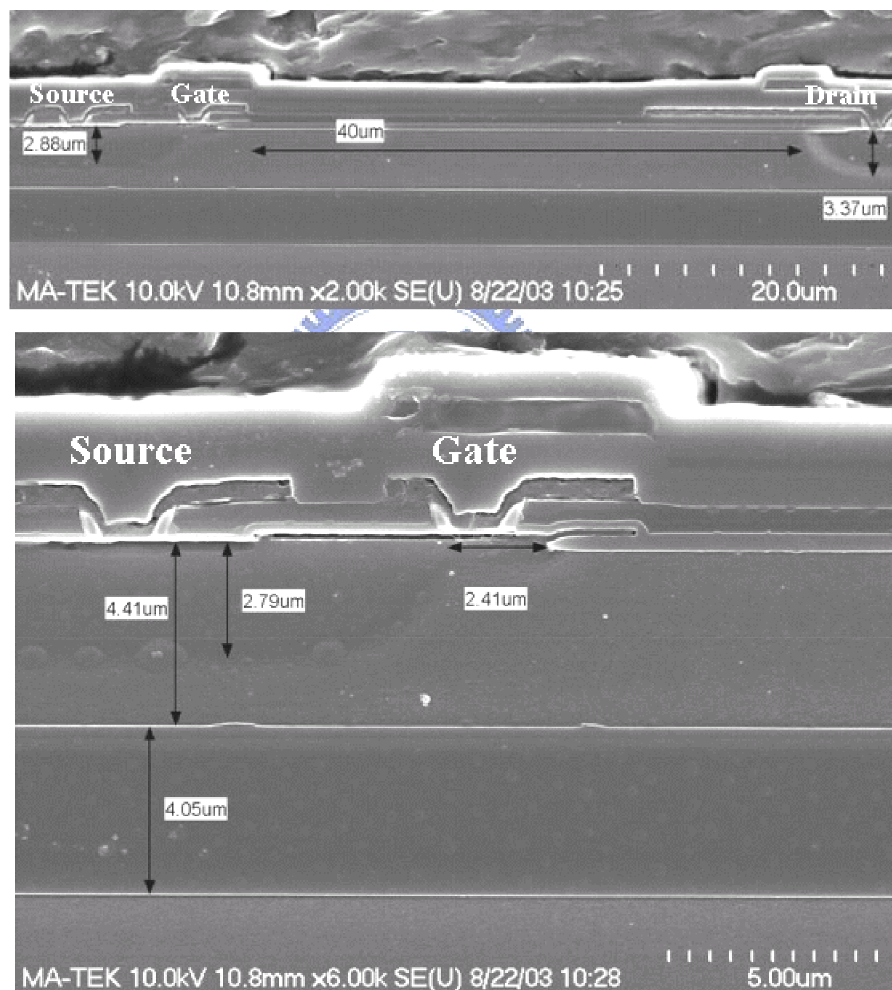

Fig. 2-1. SEM cross-sectional view of the compatible SOI-LDMOS with 4-μm buried oxide, 5-μm silicon film layer, 40-μm drift length, 2.88-μm p-well depth and 3.37-μm n-buffer depth.

Table 2-1. Comparison of 12/25/5/40V Bulk-BCD

and 450V SOI-LDMOS process flows.

12/25/5/40V BCD Process Flow	450V SOI-LDMOS Process Flow
1. Wafer Start—**Silicon Wafer**	1. **SOI Wafer** (5um silicon, 4um BOX)
2. NBL MASK	
3. PBL MASK	
4. N-Epitaxial	
5. Sinker MASK **Bipolar Sinker Formation**	2. Sinker MASK **N-Buffer Layer Formation**
6. NW MASK **PMOS N-Well formation**	
7. PW MASK **NMOS P-Well formation**	3. PW MASK **Boron/ 4e13/ 50 KeV**
8. Active Area MASK **LOCOS (Local Oxidation of Silicon) define**	4. Active Area MASK **FOX (Field Oxide) and LOCOS define**
9. Nch FLD MASK	
10. P-base MASK	
11. HV Gate Oxide MASK and LV Etch **High-Voltage and CMOS Oxide Define**	5. HV Gate Oxide MASK and LV Etch **High-Voltage Oxide Define**
12. Poly MASK **Gate formation and Emitter Define**	6. Poly MASK **Gate formation**
13. Nch S/D MASK	7. Nch S/D MASK
14. Pch S/D MASK	8. Pch S/D MASK
15. Contact MASK	9. Contact MASK
16. Metal MASK	10. Metal MASK

Then, the BCD bipolar poly emitter and CMOS gate-poly were defined as its gate layer. Subsequently, the BF_2^+ and As^+ implantations with a dose of 3.5×10^{15} cm^{-2} were carried out to form drain/source/butting regions. Finally, its contact opening and metallization were performed to complete this fabrication.

2.3 Results and Discussion

2.3.1 Thickness Consideration of SOI Active Layer

The relationship between breakdown voltage and the thickness of a silicon film layer on SOI was shown in Fig. 2-2 with the function of the parabolic curve [2.11]. The relationship could be divided into two catalogs—bulk silicon like regime and SOI specific characteristics regime. While the thickness of the silicon film layer decreased progressively in bulk silicon like regime, the breakdown voltage was also reduced due to the decrease in the sustain voltage capability of the silicon film layer. However, while it was decreased below about 2-μm thickness for the 4-μm-thick buried oxide, breakdown voltage would increase because the carriers in the vertical ionization path were not sufficient in the SOI specific characteristics regime [2.12]. Although, from the numerical analysis, the thin silicon film layer below approximately 2-μm thickness seemed to possess a higher breakdown voltage than the thick ones, practical fabrication was difficult to achieve since the small thickness would induce a higher electrical field on the silicon film layer [2.13]. Moreover, as shown in Fig. 2-3, the on-resistance of the thin devices would be raised abruptly when the thickness was lower than 1-μm [2.14]. Thus, in this experiment, the silicon film layer of 5-μm thickness, which was not too thick for easy isolation, was selected in order to obtain a wider process window, a higher breakdown voltage and a lower on-resistance at a suitable RF operation frequency (MHz range to GHz range) than those of the thin films.

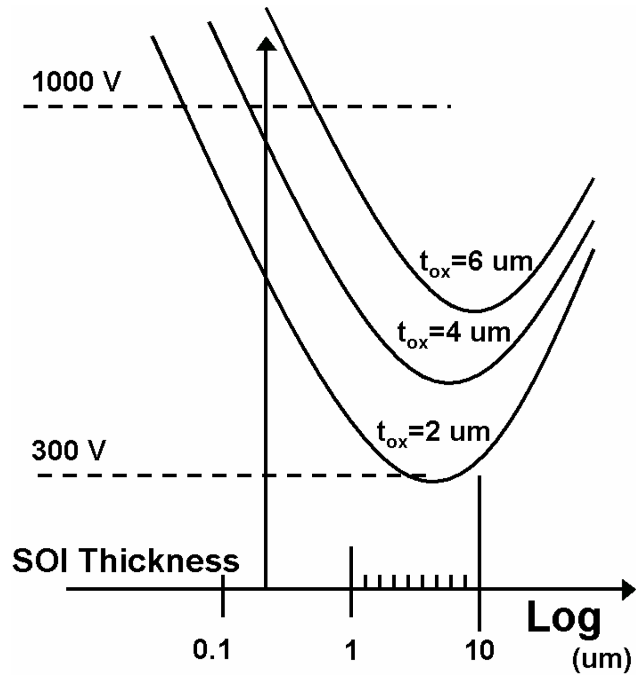

Fig. 2-2. Breakdown voltage as a function of SOI thickness with buried oxide thickness as a parameter from t_{ox}=2-μm to t_{ox}=4-μm.

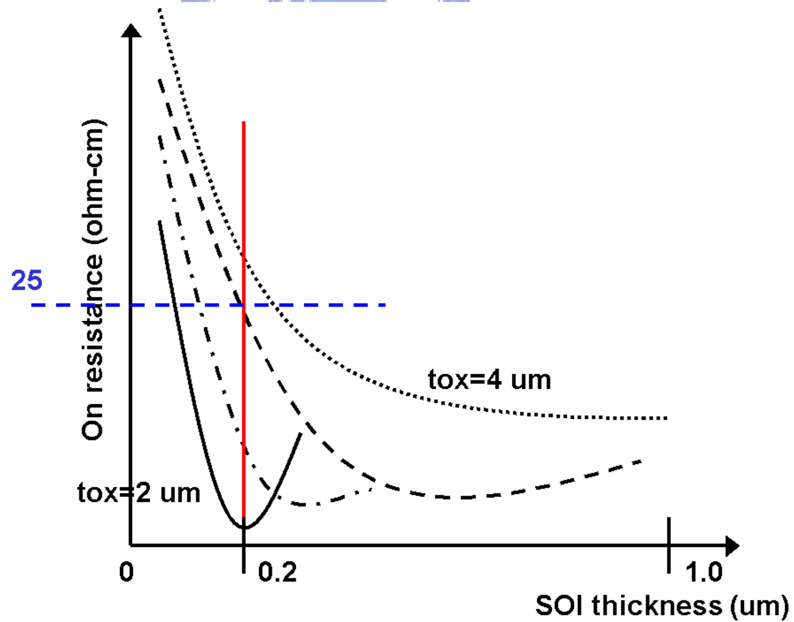

Fig. 2-3. Calculated on-resistance as a function of SOI and buried oxide (BOX) thickness from t_{ox}=2-μm to t_{ox}=4-μm.

2.3.2 Dependence of Breakdown Voltage on Drift Length and Drain Metal Extension

Figure 2-4 exhibited the dependence of breakdown voltage and forward voltage drop (Vce) on its drift length extension. The drift length of 40-μm in this compatible device would be set as an initial point of drift length extension. The drift length extensions were varied in a step of 5-μm from 0 to 30-μm. The forward voltage drop was defined at a gate voltage of 12-V and a drain current density of 50 A/cm^2. Although the extended drift length was expected to obtain a higher blocking capability, the breakdown voltage was still sustained at a constant value of 461.5 V as the drift length increased. It was attributed that the vertical breakdown voltage limited the maximum breakdown voltage above 40-μm drift length in this SOI structure [2.15]-[3-17]. Moreover, the forward voltage drop was increased stably from 0 to 20-μm and abruptly above 20-μm as the drift length increased.

Figure 2-5 showed another relationship of breakdown voltage and forward voltage drop for drain metal extension. The drain metal length of 10-μm in this compatible device would be set as an initial point of drain metal extension. The drain metal extensions were varied from -6 to 6-μm relative to the initial 10-μm drain metal length. According to the results, the breakdown voltage could be improved from 451-V to 481-V as the metal length increase from -6-μm to 6-μm. The reason was that the drain metal extension, which was overlapped at passive layer, could split the N-drift/n+-drain junction electric field. Moreover, it was desired that the enhancement of blocking capability didn't accompany with the increase of forward voltage drop. However, it was worth to mention that the metal extension in blocking voltage enhancement still had a limit until affecting the electric field distribution in the drift region and would increase the drain capacitance (Cd) so as to decay the operation speed.

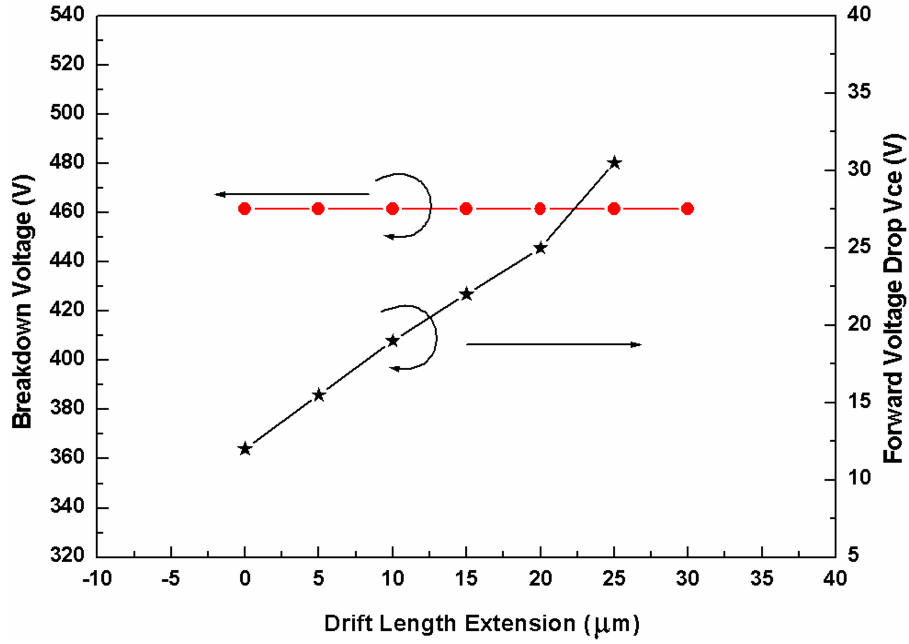

Fig. 2-4. Dependence of breakdown voltage and forward voltage drop (Vce) on drift length extension of additional 25-μm length.

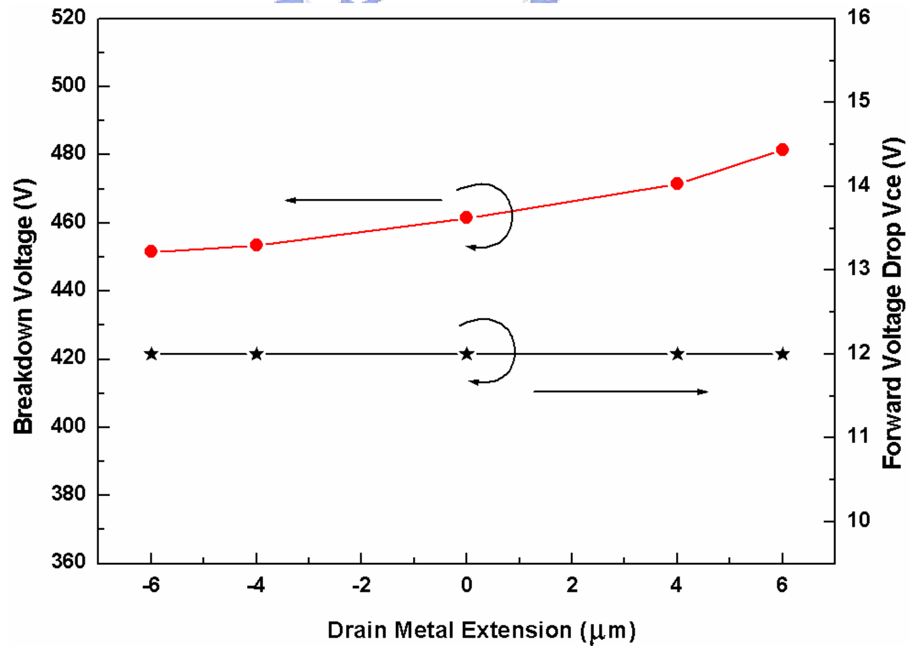

Fig. 2-5. Relationship of breakdown voltage and forward voltage drop at 10-μm length drain metal with the variation from –5-μm to 5-μm.

2.3.3 Safe Operating Area for Compatible BCD SOI-LDMOS

The famous norm of safe operating area (SOA), which was defined by logarithmic scale I-V characteristics, indicated that the devices could operate inside this area without suffering damage. It was bounded by $R_{DS,on}$, maximum rated power P_T, maximum current I_{DS}, and maximum sustainable voltage. The $R_{DS,on}$ current limited was determined by the on-state resistance. The maximum P_T limit would be attained while the thermal dissipation ($V_{DS} \times I_{DS}= P$) was not well. It could be improved by heat sink design or short gate pulse time. The maximum current I_{DS} was allowed by metal connections until the electron migration (EM) happened. The maximum sustainable voltage was limited by avalanche breakdown phenomena in the p/n junction. The SOA of the power MOSFET and bipolar transistor are different in a number important ways.

Firstly, in the definition, the bipolar transistor has two distinctions of forward-bias SOA (FBSOA) and reverse-bias SOA (RBSOA), which refer to the bias condition of the base-emitter junction. During a cycle switching, the negative bias is applied to the base to affect turn-off characteristics and both FBSOA/RBSOA come into play. However, the operation of power MOSFET only considers a single SOA curve for all bias conditions. Secondly, the SOA of bipolar transistor has a second breakdown voltage limit but the power MOSFET does not. It is because the power MOSFET is a major-carrier device and free of the thermal runaway and current-focusing phenomena responsible for second breakdown in the bipolar transistor. In addition, the limit of SOA of power MOSFET was also decided by hot-electron-injection phenomenon which appears to be more serious when used in a high current and high voltage applications because it results in device degradation and destruction by snapback due to kirk-effect [2.18]-[2.22].

To operate more stably under high-speed and high-frequency conditions, it should

be ensured whether the device remained in a safe-operating-area (SOA) without destructive failure at all times. High-power measurement was performed using the KEITHLEY model 2361 and a complete I-V curve was extracted using the simulator of Taurus [2.23]. As shown in Fig. 2-6 (a), the on-state resistance A-B and the maximum voltage limit C-D were located at 248.82 mΩ-cm^2 and 461.5 V, respectively.

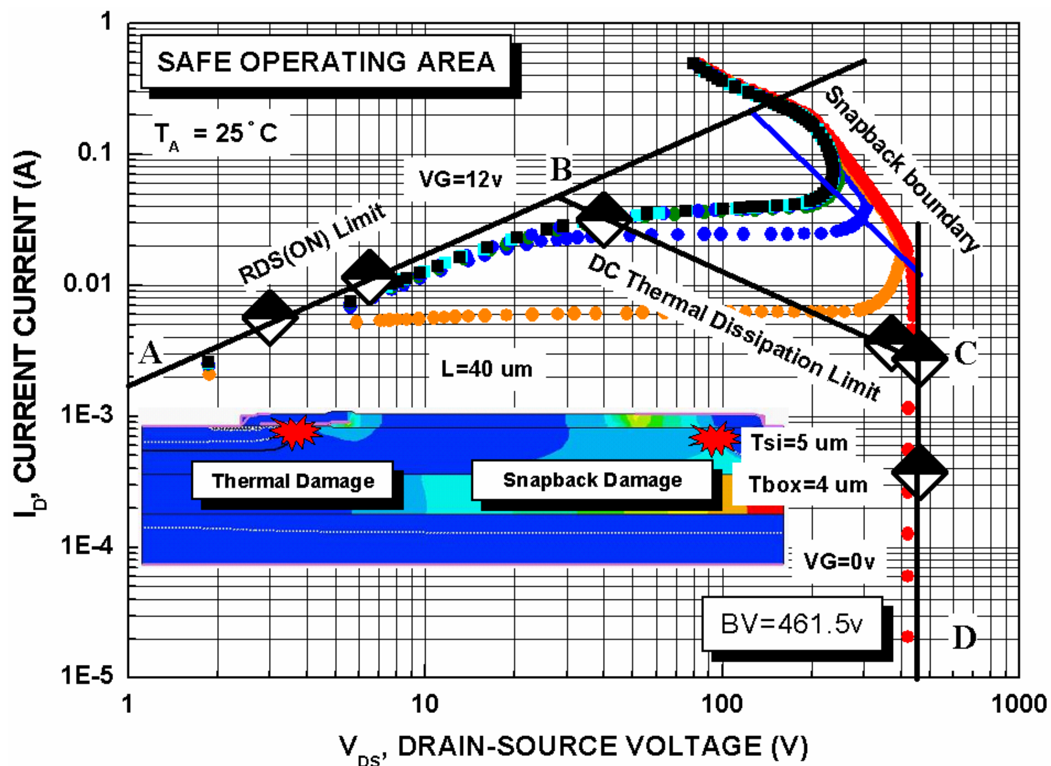

Fig. 2-6. (a) Investigation of the SOA with the measured (DC thermal dissipation limit) and simulated (snapback boundary) maximum rated power limitations at room temperature.

In general, the maximum rated power limit was mostly defined on the set of a snapback boundary, particularly where thermal effects had less influence [2.24]. But, in this case, the power limit line was moved from a snapback boundary to the maximum DC thermal dissipation B-C due to its small area as well as its large power density (1.27

W, 2636.3 W/cm^2). On the other hand, Figure 2-6 (b) showed the various I-V electrical characteristics after exceeding the maximum DC thermal dissipation limit. It was demonstrated that the isolated gate oxide was changed into an oxide with p-n diode characteristics (n-type poly-gate/p-type well). The reason for this was that its local thinning and bad dissipation behavior could not suffer such thermal strike. Moreover, the gate to the source was unlike the drain to the source or the gate with an n-drift resistor protection.

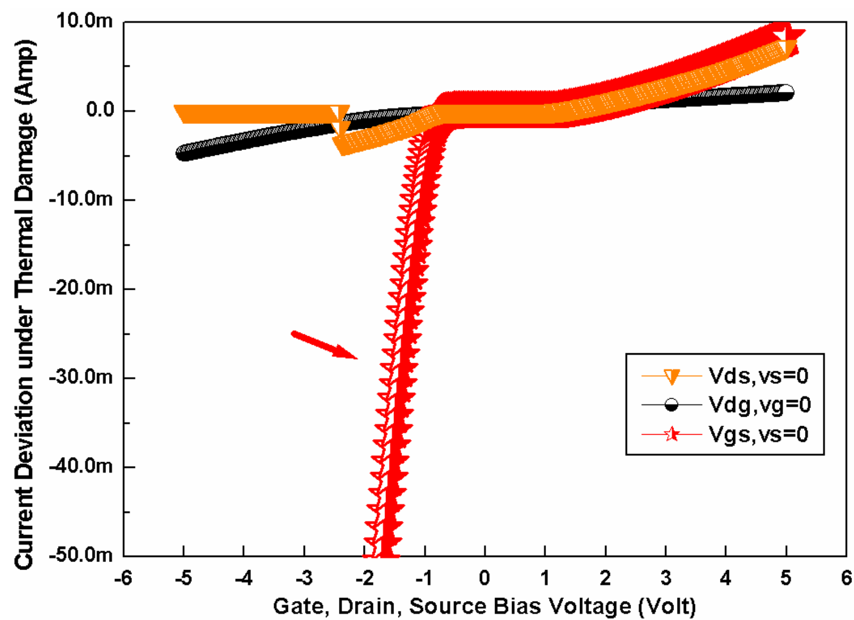

Fig. 2-6. (b) Current variation after thermal damage as a function of terminal biases of drain-to-source, drain-to-gate, and gate-to-source.

2.3.4 Transient Characteristics of Compatible BCD SOI-LDMOS

Dielectric isolation (DI) technology using silicon on insulator (SOI) substrates has attracted attention in smart power devices and HVIC applications because of superior isolation. Recent publications have shown that SOI power devices can achieve high

breakdown voltages over 700-V on thin SOI layer, which also allows easier isolation processes [2.11]. Considering high-speed applications, power devices have traditionally been used as power switches. LDMOS was a technology choice due to its simpler gate drive circuitry compared to bipolar devices. The availability of LIGBT, which combines the benefits of gate-controlled device with high current handling capability of bipolar device, has posed a serious competition to LDMOS devices. Nevertheless, LIGBT has two inherent drawbacks to LDMOS devices. First, the device has a 0.7-V forward on-set voltage, thus excluding its use in application that requires a low forward voltage drop of less than 0.7-V. Second, there exits a bipolar current tail during turn-off, which lasts about an order of magnitude longer than that of LDMOS devices.

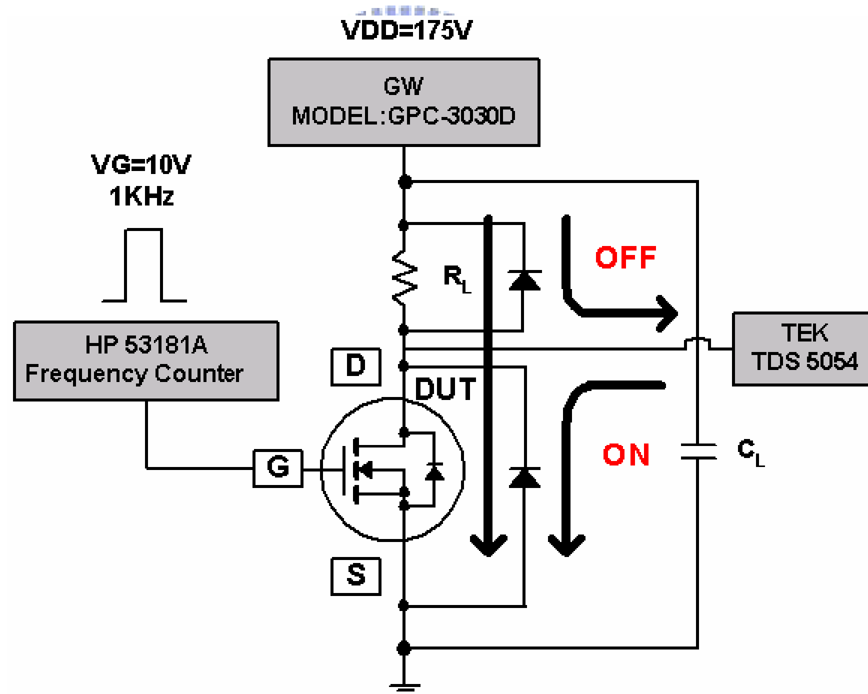

Fig. 2-7. (a) Schematic measurement circuit with HP 53181A frequency counter for contributing 1 KHz gate pulse, GW power supply for supplying high static drain voltage of 175-V, and TEK TDS5054 oscilloscope for detecting the output waveforms.

Figure 2-7 (a), (b), (c) and (d) illustrated the SOI LDMOS turn-on and turn-off transient characteristics obtained using a HP 53181A frequency counter, GW power supply, and TEK TDS5054 oscilloscope. The measurement was performed under a 10 V pulse gate voltage (Vgs) of 1 KHz frequency, an off-state voltage (Vds) of 175 V, a resistive load of 10 KΩ and protective freewheeling diodes (FWD) across a switching transistor. The turn-on time (ton) was defined as the interval between the time when the minimum Vgs increase to 10 % and the maximum Vds decreased by 90 % of the respective initial states as well as the definition for turn-off time (toff).

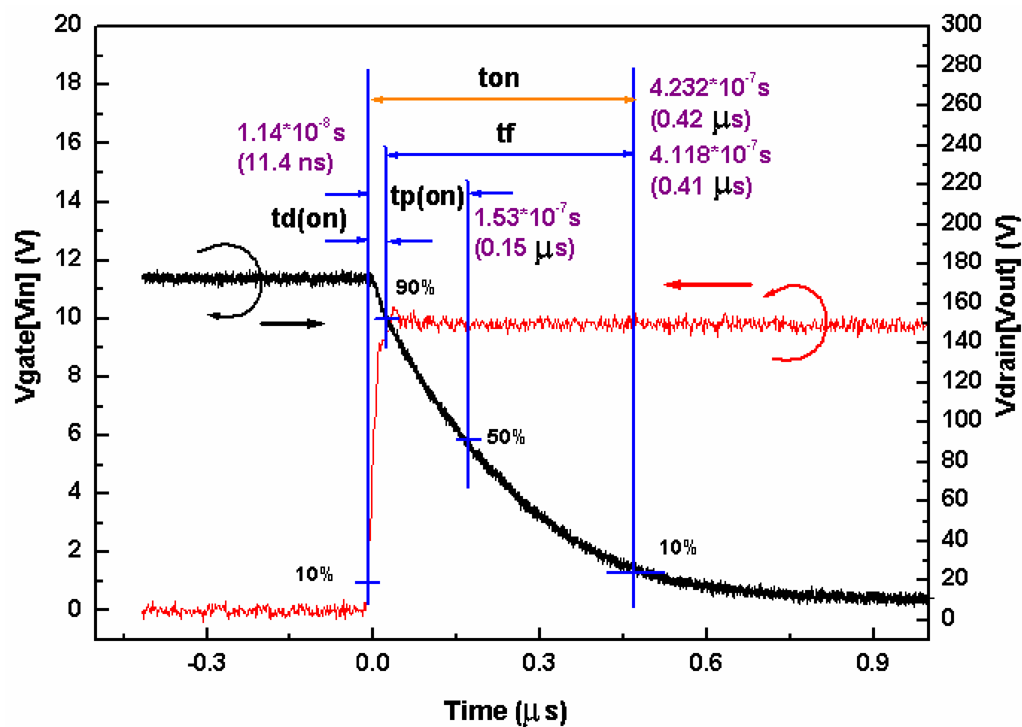

Fig. 2-7. (b) Illustration of turn-on switching waveforms during the gate transience from low to high state with the delay time, propagation time, falls/rise time, and switch time of 11.4-ns, 150-ns, 410-ns, and 420-ns, respectively.

For the turn-on state (420 ns), the effective load capacitance was discharged by a current difference of 13.6 mA from the resistor (10 KΩ) and the transistor (248.82 mΩ-cm^2). Time was mainly wasted at the load and transistor because the gate capacitance (Cgs) is only 5.86 pF from the Taurus extraction (70 nF/cm2, L=9-μm, W=930-μm) in Fig. 2-7 (c). For the turn-off state (3000 ns), the effective load capacitance of the interconnect lines must be charged by a current through a resistive load. According to the above-mentioned, it could be concluded that the BCD-compatible transistor had a nanosecond speed as similarly to HV output driving circuits, HV operational amplifiers, level shifters, high efficiency DC-DC converters, HV DAC and various protection circuits in HVIC switches for use in power control systems—such as motor drive, electronic ballasts, resonant half-bridges, high-frequency power amplifiers and switching power supplies [2.25], [2.26].

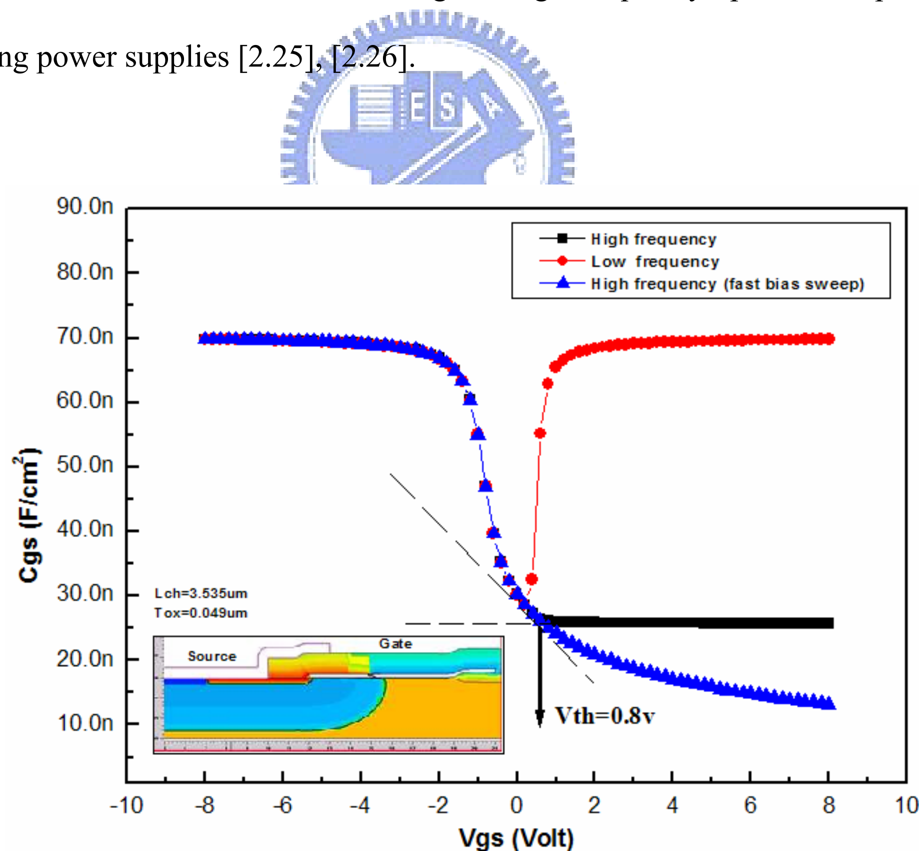

Fig. 2-7. (c) Relationship between gate-to-source capacitances and gate-to-source voltages under different frequency measurements from Taurus extraction.

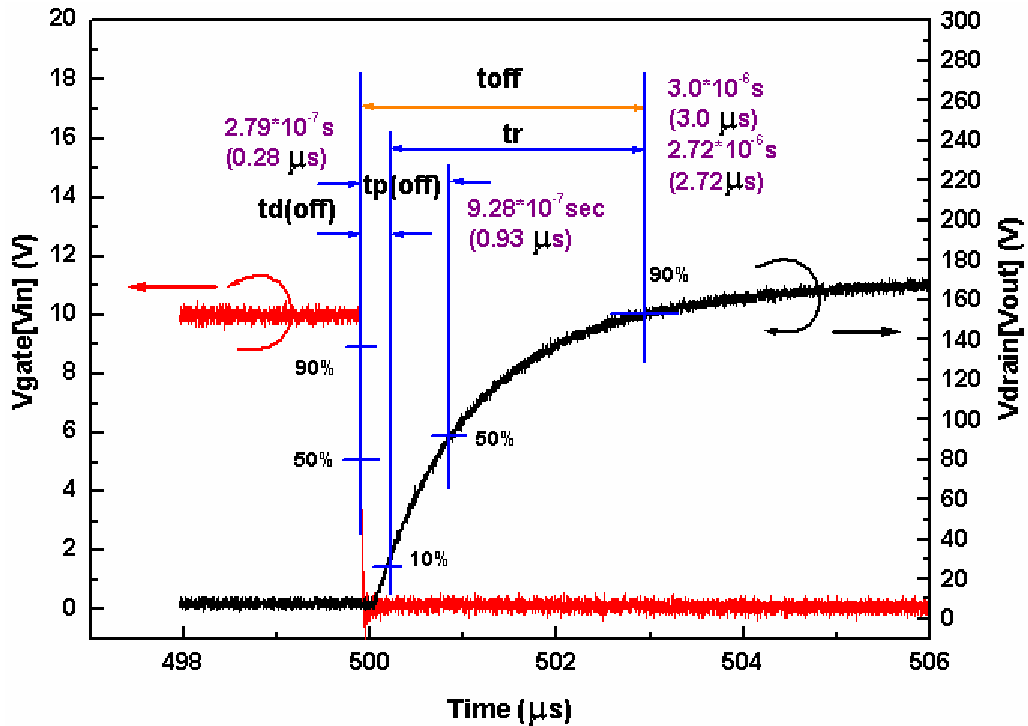

Fig. 2-7. (d) Illustration of turn-off switching waveforms during the gate transience from high to low state with the delay time, propagation time, falls/rise time, and switch time of 280-ns, 930-ns, 2700-ns, and 3000-ns, respectively.

2.3.5 RF Characteristics of Compatible BCD SOI-LDMOS

Power devices working at high frequency are needed in all kinds of personal communication systems. Mainly discrete silicon bipolar devices are used for reasons of cost. Philips has a long-standing experience with bipolar power transistors and has introduced the silicon-on-anything gluing technology for fabricating discrete bipolar transistors with little or no package parasitics [2.27]. The advantages are low cost standard bipolar processing, very good radio frequency (RF) and thermal grounding and strong reduction of parasitic capacitances. In recent years another device [2.28], [2.29], the LDMOS power transistor has been receiving much attention because of its superior

performance with respect to linearity and efficiency [2.30]. However, in this device complicated process steps are needed to avoid the gate oxide degradation due to hot carrier generation [2.31]-[2.33]. Integration of such high-quality RF active devices with high-quality RF passives is also very difficult in such a bulk Si technology. High quality matching circuitry has to be added in a different technology which significantly adds to the expense of the final product. SOI LDMOS transistors significantly enhance the possibilities of integrating high quality passive components due to the inherent insulation produced by the buried dielectric.

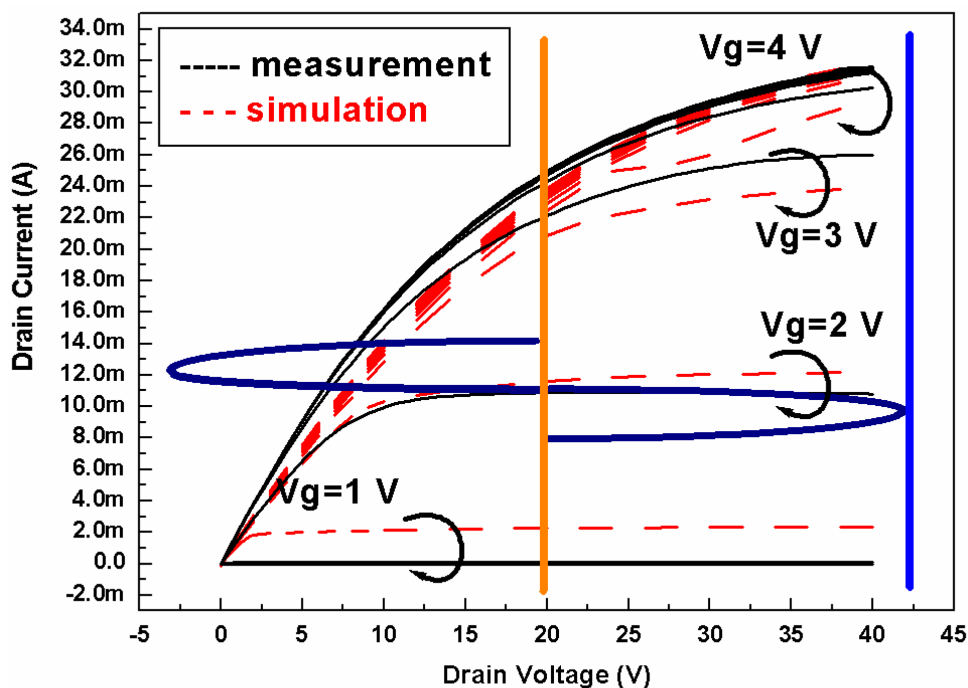

Fig. 2-8. (a) Establishment of corresponding maximum output swing at a drain voltage of 20-V between the experiment and simulation. The maximum voltage was set at drain bias of 40-V according to the maximum power limit of safe-operating area.

Figure 2-8 (a) and (b) showed the radio frequency (RF) characteristics of the (1) quiescent point choice and (2) the corresponding short-circuit forward frequency response obtained from the two-dimensional (2-D) ATHENA/ATLAS (process/device) simulators with consideration of all capacitance effects [2.34]. All simulation results were based on the measured I-V characteristics showing a good match in Fig. 2-8 (a). The unity current gain frequency (f_T) and maximum frequency of oscillation (f_{max}) were calculated by extrapolating the magnitude of h_{21} and g_{ma} to 0 dB. To operate in the maximum output swing without destructive failure, the DC drain voltage should be set in the middle of the maximum DC thermal dissipation limit at Vd=40 V under various DC gate biases. Consequently, scattering parameters (S-parameters) were established at a drain bias of 20 V over the frequency range of 3 MHz to 220 MHz for a gate signal biased from 0.1 V to 12 V. The maximum f_T and f_{max} were found to be 124MHz and 220MHz, respectively, at Vg=1 V and the SOI LDMOS also presented a suitable current range at high-power operations (0.23 A~2.39 A). As illustrated in Fig. 2-8 (b), the magnitudes of f_T and f_{max} still varied with transconductance (g_m) while gate voltage (Vg) increased [2.35], [2.36]. However, there existed a large drop between Vg=2 V and Vg=4 V, which was also the range from the saturation region to the non-saturation region. According to these data, it could be attributed to the facts that a portion of the output signal was clipped or distorted thereby affecting the small-signal gain. In other words, the transistor would not be working as a linear power amplifier when outside the saturation region.

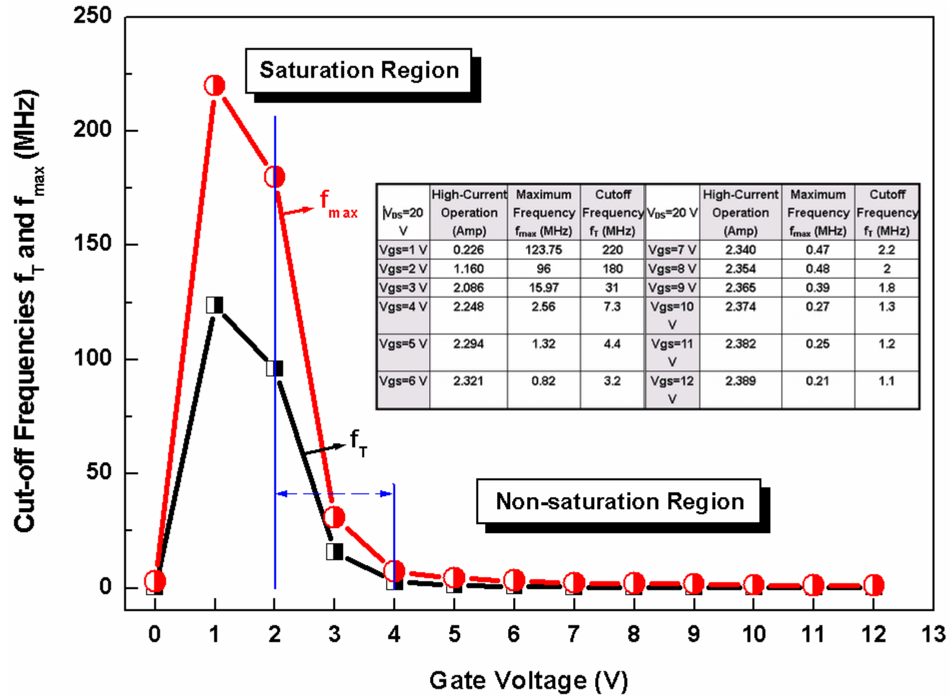

Fig. 2-8. (b) Simulation of small-signal characteristics with respect to the cut-off frequencies f_T and f_{max} at various gate biases from two-dimensional (2-D) ATHENA/ATLAS (process/device) simulators.

Table 2-2. Summary of small-signal characteristics with the parameters of operation current, maximum frequency, and cutoff frequency from gate bias of 1-V to 12-V.

V_{DS}=20 V	High-Current Operation (Amp)	Maximum Frequency f_{max} (MHz)	Cutoff Frequency f_T (MHz)	V_{DS}=20 V	High-Current Operation (Amp)	Maximum Frequency f_{max} (MHz)	Cutoff Frequency f_T (MHz)
Vgs=1 V	0.226	123.75	220	Vgs=7 V	2.340	0.47	2.2
Vgs=2 V	1.160	96	180	Vgs=8 V	2.354	0.48	2
Vgs=3 V	2.086	15.97	31	Vgs=9 V	2.365	0.39	1.8
Vgs=4 V	2.248	2.56	7.3	Vgs=10 V	2.374	0.27	1.3
Vgs=5 V	2.294	1.32	4.4	Vgs=11 V	2.382	0.25	1.2
Vgs=6 V	2.321	0.82	3.2	Vgs=12 V	2.389	0.21	1.1

2.3.6 Compatible High-Voltage BCD SOI-LDMOS for High-Frequency Applications

The developed transistor could be made to function as an output-tuning network, a voltage source inverter and a high-voltage modulator for class F power amplifiers, HID lamps circuits and RF power supply applications. The characteristics of class F power amplifier was dependent on the designs of the power output, frequency band and operation efficiency, which was determined on the basis of the LDMOS performance [2.37]. The high-resolution display required high voltage (color) and high frequency (scan lines) to realize low-dissipation video amplifiers. Amplifiers for medical use required both conditions to enable the construction of a high-bandwidth circuitry for amplification [2.38], [2.39]. These above high-voltage power amplifiers could be applied to induction heating, plasma generation, FM broadcasting and HDTV transmitters with their broad band of up to MHz range.

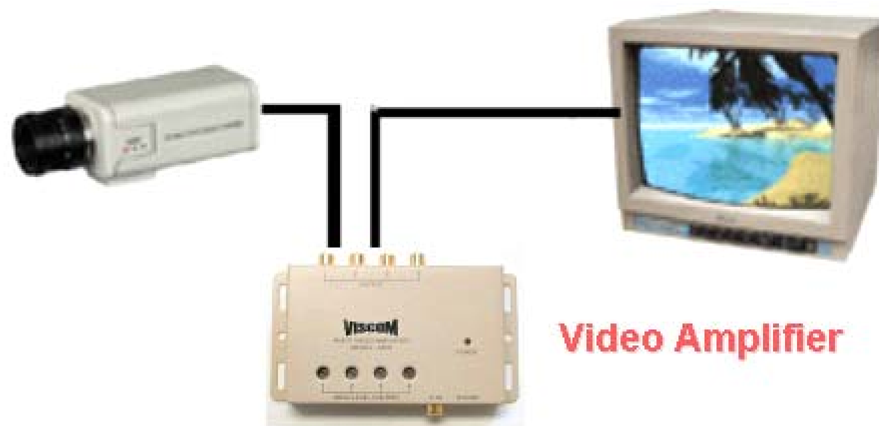

Fig. 2-9. Low dissipation video amplifier application for high-resolution display by high voltage and high frequency device operations.

Recently, high intensity discharge (HID) lamps have been attractive for high-voltage and high-frequency operation due to their highly efficient operation and excellent color characteristics. Moreover, high-frequency ballast (10 KHz~20 KHz) has also been developed to reduce the ballast size for use in HID lamps. The function of ballast can supply HID lamp with high voltage to initiate discharge and also can supply with stable current during lamp running condition through distributed constant line (λ/4 wavelength). However, the arc in the HID lamp would induce an unstable phenomenon called "acoustic resonance" when operating in certain high frequency ranges. Thus, to avoid this phenomenon, the operation frequency of the LDMOS voltage source inverter should be set above the unstable frequency range to 1 MHz [2.40]. Power supplies, that offered the power outputs from 10 W to 150 KW and frequencies of 5 KHz to 150 MHz,

Fig. 2-10. Power LDMOS voltage source inverter in high frequency ballast system of high intensity discharge (HID) lamp for use in automobile headlamp application.

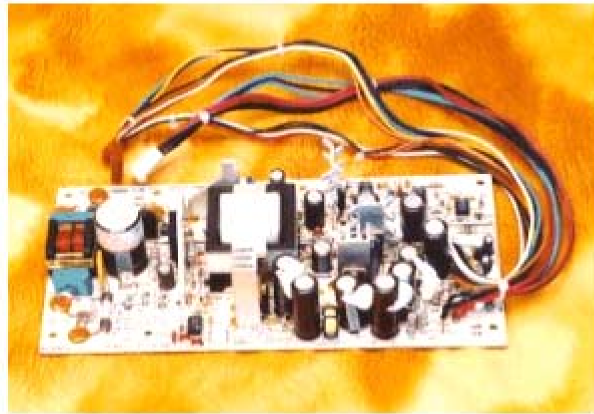

Fig. 2-11. Power MOSFETs in power factor correction (PFC) controller IC for use in low power (less than 150 Watt) switch mode power supply (SMPS) application.

are used in the radar transmitters, power conditioning systems, X-ray irradiation and RF electromagnetic irradiation. The weight of electrical equipment could be reduced in high-frequency operations [2.41].

The SOI process, in specific functions of implement, allows the circuit designer considerable freedom in the choice of active and passive components compared with bulk technologies. In other words, it allows more favorable specifications toward low system cost (integration without package bond wires) and power dissipation (few parasitics) in the use of power amplifiers, HID lamps and RF power supplies.

2.4 Summary

A 450 V rating SOI-LDMOS integration has been demonstrated by traditional 0.5-μm Bulk-BCD technology for economy. The silicon film layer of 5-μm thickness, which is not too thick for easy isolation, is selected in order to obtain a wider process window, a higher breakdown voltage and a lower on-resistance at a suitable RF operation frequency (MHz range to GHz range) than those of the thin films. Although the extended drift length was expected to obtain a higher blocking capability, the breakdown voltage was still sustained at a constant value of 461.5 V as the drift length increased. It was because that the vertical breakdown voltage limited the maximum breakdown voltage above 40-μm drift length in this SOI structure. The metal extension in blocking voltage enhancement has a limit until affecting the electric field distribution in the drift region and will increase the drain capacitance (Cd) so as to decay the operation speed. The power limit line is moved from a snapback boundary to the maximum DC thermal dissipation due to its small area as well as its large power density (1.27 W, 2636.3 W/cm^2).

The switching times are mainly wasted at the load and transistor because the gate capacitance (Cgs) is only 5.86 pF from the Taurus extraction (70 nF/cm2, L=9-μm, W=930-μm). The compatible SOI LDMOS exhibits rudimentary electrical characteristics with a specific on-resistance of 248.82 mΩ-cm^2, a breakdown voltage of 461.5 V, a turn-on time of 420 ns, a maximum f_{max} of 220 MHz and a maximum f_T of 124 MHz at a high-voltage bias of Vgs=1 V and Vds=20 V. However, to investigate all characteristics in high power, high speed and high frequency operations, suitable data should be chosen under non-optimum conditions due to the trade-off relationship between them. Thus, the main purpose of the experiment is to give complete

information that the conventional Bulk-BCD technology can possess a wider range of applications through the use of SOI wafers without modifying any processes for HVIC switches, power amplifiers, HID lamps, and RF power supply applications.

Chapter 3

Modeling and Design of the High Performance Step -Doping Silicon On Insulator Lateral Insulated Gate Bipolar Transistor (SOI-LIGBT) Power Devices by Partition Mid-Point Method

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A partition method is proposed to study the high-voltage silicon on insulator lateral insulated gate bipolar transistor (SOI-LIGBT) devices with the step doping profile for the first time. R. Sunkavalli *et al.* have reported that the breakdown voltage using step doping can be approached to that of the linearly graded doping devices. In this chapter, the on-state characteristics will be present with the similar forward voltage drop (Vce) value between the step doping and linearly graded doping devices. The breakdown voltage can be deduced by the partition mid-point method and the corresponding breakdown electric field will also be fingered out in the step drift region. Furthermore, in order to reduce the undesirable additional masks, the degraded factor (D) is developed to evaluate the minimum number of frames with the better performance. Eventually, a 660 V step analytical results will be exemplified to compare with a 606.6 V MEDICI simulation, which shows very good agreement by this proposed method.

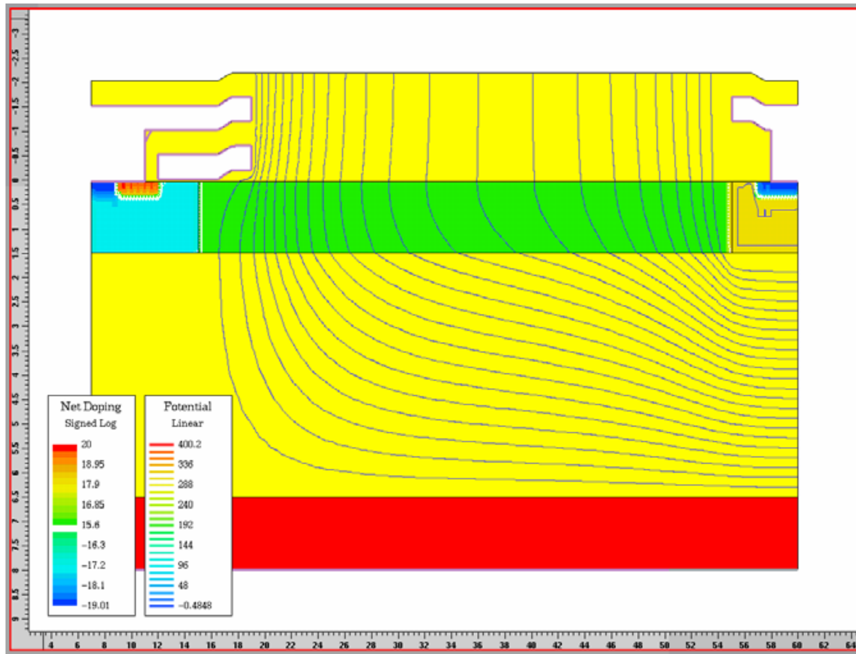
3.1 Merits of Silicon-On-Insulator (SOI) devices

System-on-a-chip (SOC) is a major revolution to take place the unprecedented levels of integrated circuits possible [3.1]-[3.4]. As a result, new methodologies and tools are demanded to address design and verification in this rapidly evolving area. Thus, in the field of the high-voltage applications, silicon-on-insulator (SOI) seem to be a promising technology to realize it because of its superior isolation characteristics to the junction isolated (JI) devices [3.5]-[3.7], reducing the LIGBT turn-off time with thin SOI layer [3.8], and increasing the blocking voltage under well-RESURF design [3.9], [3.10]. While considering the merits of SOI low-voltage applications, it provides immunizing from the ionization via radiations [3.11], reducing parasitic capacitances [3.12], short-channel effects [3.13]-[3.15], hot-carrier effects [3.16], and static power consumption [3.17].

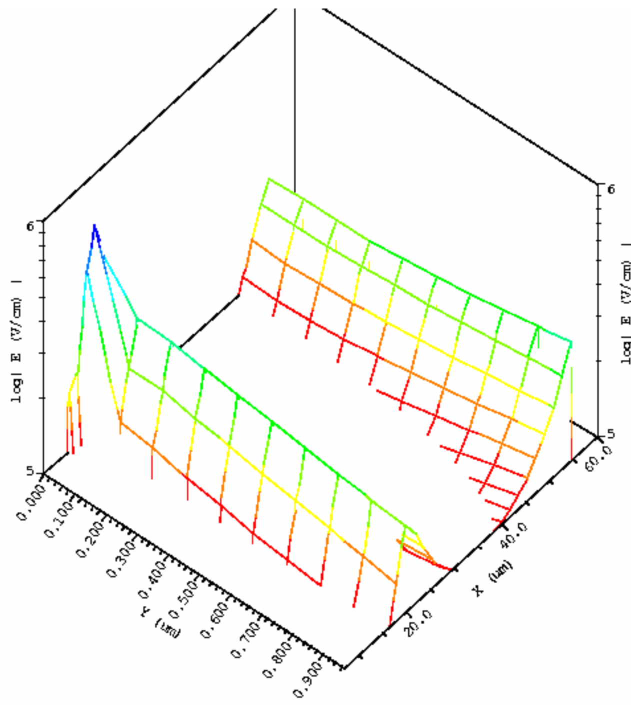
However, there have two significant problems in the SOI devices—such as self-heating effect and lower breakdown than JI devices. Self-heating effect is due to the buried oxide layer acting a barrier which prevents the heat dissipating to the silicon substrate [3.18], [3.19]. As shown in Fig. 3-1, the lower breakdown voltage is due to less RESURF effect with strong vertical electric field from buried oxide layer [3.20]. Thus, in order to achieve high breakdown voltage in SOI devices, a linearly graded doping profile in the drift region is necessary to provide a more uniform electric filed distribution along the drift region and so to optimize the RESURF condition [3.21].

3.1.1 Linearly Graded Doping Profile for Superior Breakdown Voltage

Smart power technology [3.22], which integrates both logic and power devices on



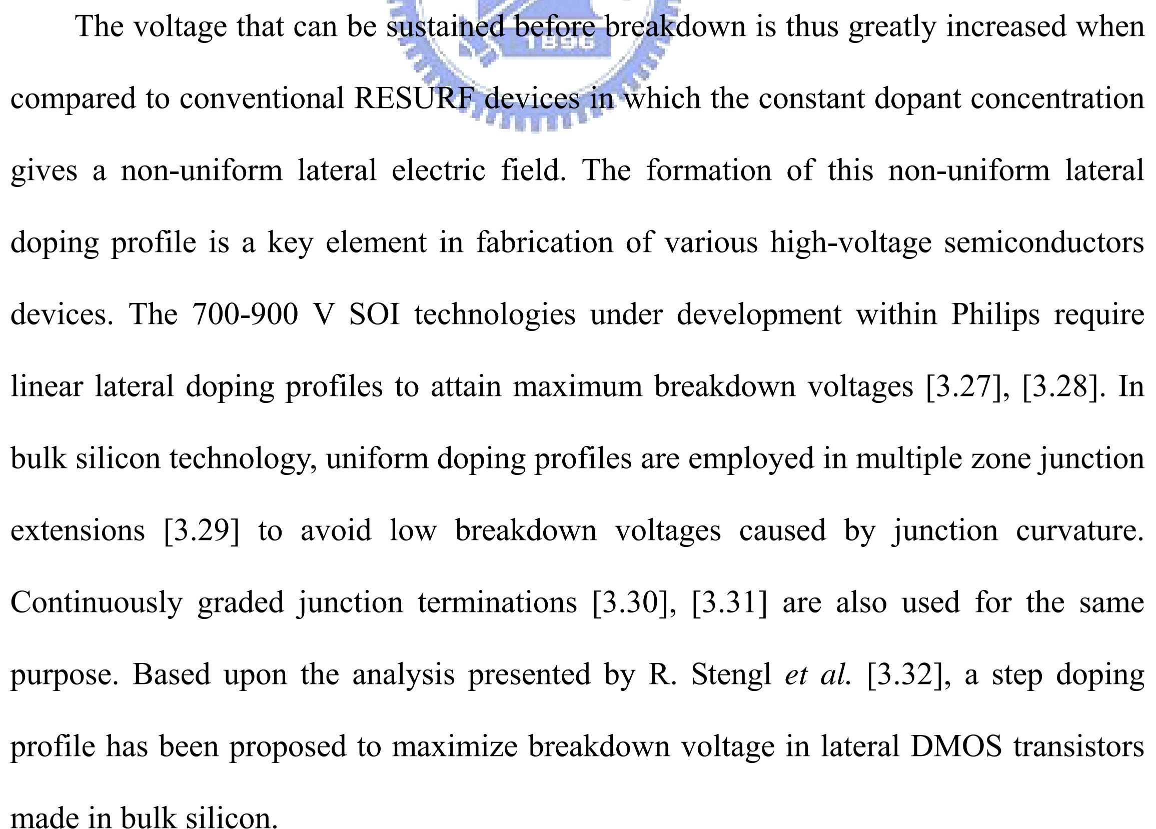
(a)



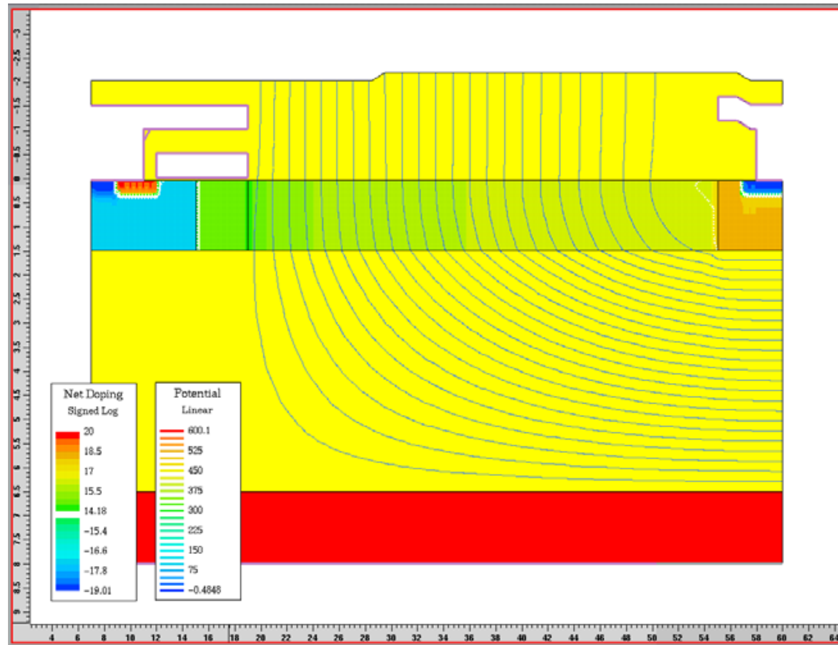
(b)

Fig. 3-1. Simulation of uniform doping device for (a) 2-D potential curves and (b) 3-D electric field distribution at breakdown voltage of 402-V by Taurus extraction. The electric field distribution shows the two sharp edge triangular peaks and a large middle dip in the drift region.

the same chip, is more readily implemented in silicon-on-insulator (SOI) substrates than bulk substrates [3.23]. Previous studies on SOI power devices [3.24]-[3.26], however, are limited mainly to thick (>10 μm) SOI layers in which complicated trench etching and refilling have to be used for lateral isolation. Device isolation and low power integration can be greatly simplified if an ultra-thin (<1 μm) SOI layer is used. Recently, there have been reports of PIN diodes [3.27] and LDMOS devices [3.28] in ultra-thin (0.1-0.2 μm) SOI substrates with breakdown voltages with breakdown voltages over 700-V. Nevertheless, if the SOI layer is too thin, the mobility degradation increases the on resistance sharply. In high-voltage applications, as shown in Fig. 3-2, a promising technology is to use linearly graded doping profile in the drift region of the power device built in a very thin SOI layer on a thick buried oxide. A linearly graded doping profile is used in the drift region of these devices to achieve a uniform lateral electric field.



The voltage that can be sustained before breakdown is thus greatly increased when compared to conventional RESURF devices in which the constant dopant concentration gives a non-uniform lateral electric field. The formation of this non-uniform lateral doping profile is a key element in fabrication of various high-voltage semiconductors devices. The 700-900 V SOI technologies under development within Philips require linear lateral doping profiles to attain maximum breakdown voltages [3.27], [3.28]. In bulk silicon technology, uniform doping profiles are employed in multiple zone junction extensions [3.29] to avoid low breakdown voltages caused by junction curvature. Continuously graded junction terminations [3.30], [3.31] are also used for the same purpose. Based upon the analysis presented by R. Stengl *et al.* [3.32], a step doping profile has been proposed to maximize breakdown voltage in lateral DMOS transistors made in bulk silicon.



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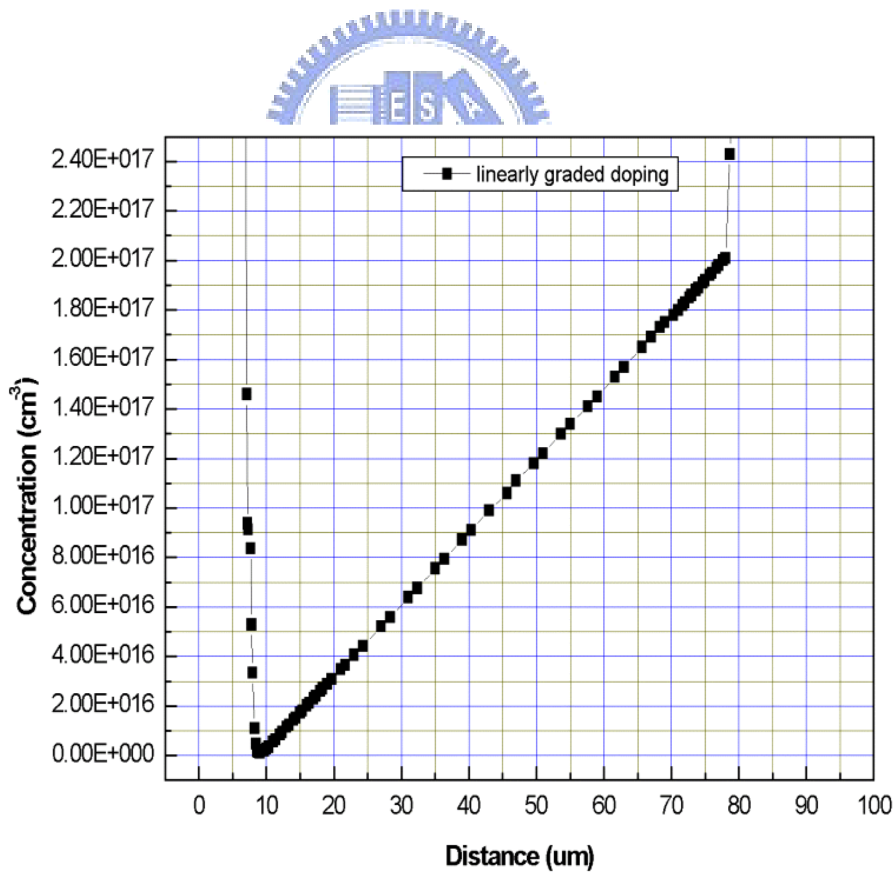


(b)

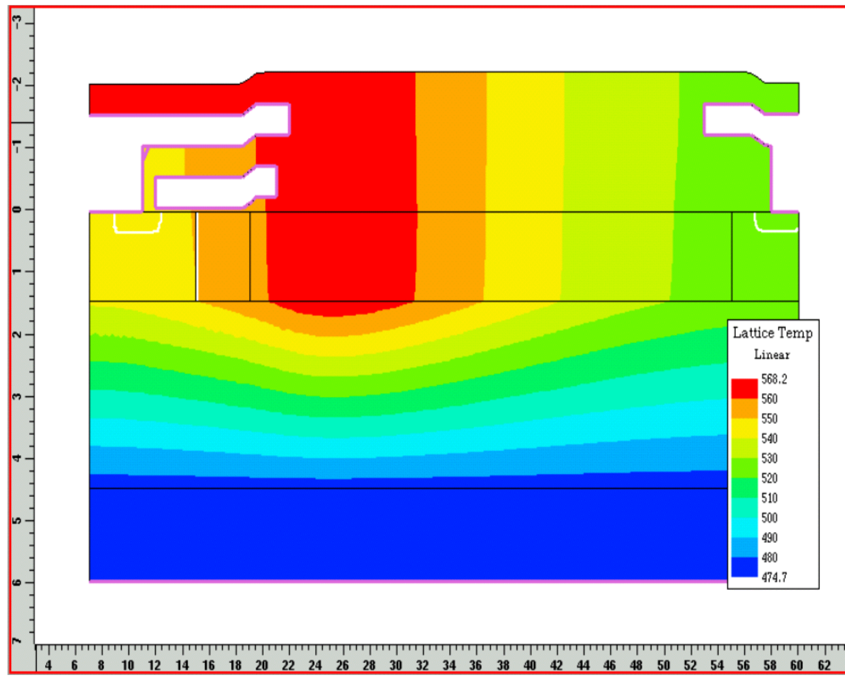
Fig. 3-2. Simulation of linearly graded doping device for (a) 2-D potential curves and (b) 1-D doping concentration distribution by Taurus extraction.

3.1.2 Linearly Graded Doping SOI-LDMOS and SOI-LIGBT

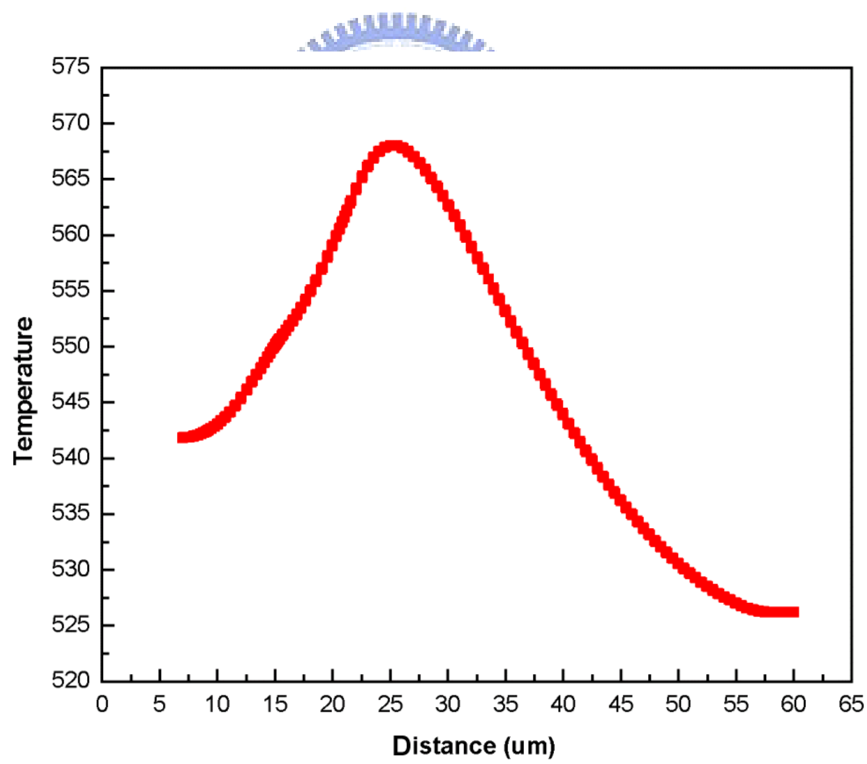
3.1.2.1 Local Heating in Linearly Graded Doping SOI-LDMOS

An important consideration in the evaluation of silicon-on-insulator technology is the contribution of the thermal resistance of the buried oxide layer to the steady state and transient characteristics of SOI power devices. Of special concern is the temperature increase resulting from transient self-heating of the SOI devices during large transient power overloads [3.33], [3.34]. It is concluded that differences in self-heating between SOI and bulk-Si devices are greatest for short power transients, because the initial temperature rise in SOI device is more rapid. As the pulse length increases, the difference in temperature rise between SOI and bulk-Si devices converges to a constant value, proportional to the thickness of the buried oxide. For oxide thickness under ~2 μm, the steady-state temperature is determined essentially by the thermal properties of the substrate and device package. The thin SOI layer on thick buried oxide, however, has already been shown to worsen the self-heating problem in SOI LDMOS devices with uniformly doped drift regions [3.35]. With a linearly graded drift region, the on-state resistance in the drift varies with location.

The power dissipation and thus the temperature distribution in these devices in these devices will be quite non-uniform. Most of power is dissipated in a small region near the source end because of the lightest concentration as well as the high electric resistance there. This will give rise to serious local heating in this lightest region and the resulting temperature profile will be skewed towards the source side. The part of the drift region near the source is found to be much hotter than the region near the drain side in Fig. 3-3. In comparing the devices built in two different SOI thicknesses, the temperature gradient in the thinner SOI is higher due to the poor lateral thermal



(a)



(b)

Fig. 3-3. Simulation of local heating effect in linearly graded doping device near the source side with (a) 2-D and (b) 1-D temperature distribution by Taurus extraction.

conduction in the SOI film steeper concentration gradient in the drift region. This substantial local heating near the source may aggravate device performance and cause reliability problems in the gate and source metallization.

3.1.2.2 Temperature Relaxation by Linearly Graded Doping SOI -LIGBT

The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the SOI film. Different power devices have different current conduction mechanisms and heat generation profiles. Thermal conduction is determined by structural parameters like the SOI layer thickness and the buried oxide thickness. If a thick SOI layer is used, the lateral thermal conduction inside the device will be quite effective and the temperature rise will be relatively uniform. In an ultra thin SOI film, lateral heat conduction is not very effective and the temperature in the device is closely linked to the heat generation profile. For SOI LDMOS devices with a linearly graded doping profile in the drift region, the part near the source is more resistive, which results in a higher heat generation rate and thus a larger temperature rise.

As shown in Fig. 3-4, for the case of SOI LIGBT, the minority carrier injection from the p+ collection leads to recombination heat which is highest near the collector (drain) and gradually decreases toward the emitter side (source). This is opposite to the trend of Joule heating and makes the total heat generation profile more uniform than in LDMOS structure. In addition, when the holes are collected by the p-well, the aligned current flow with the high electric field in the depletion region gives rise to a large amount of energy released. This shift of peak power dissipation in the LIGBT toward the emitter (source) metallization eases heat conduction and helps reducing the

maximum temperature rise in the device. These two effects reduce the temperature rise and gradient in the device. In other words, the main drawback of the SOI LDMOS devices is its high on-resistance and thus high power dissipation in the on-state. In contrast the SOI LIGBT has a much lower on-state forward drop due to the conductivity modulation inside the drift region in the on state.

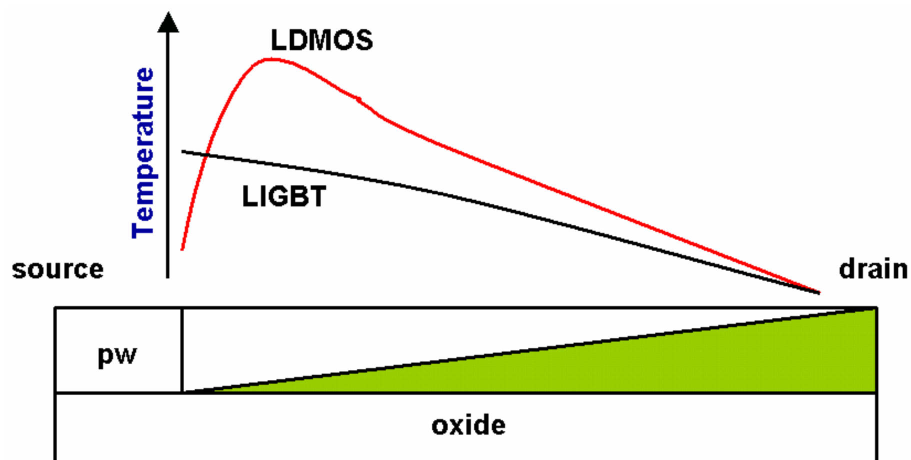


Fig. 3-4. Schematic diagram of temperature distribution in linearly graded doping SOI-LDMOS and SOI-LIGBT structures. The minor carrier in the SOI-LIGBT can relax the local heating effect.

The long storage time of the carriers inside the drift region, nonetheless, gives rise to a long turn-off time for the SOI LIGBT. By reducing the thickness of the SOI layer, it is possible to reduce the turn-off time of an LIGBT [3.8]. With a linearly dopant profile in the drift region, one would expect an LIGBT built in an ultra-thin SOI substrate to have low forward drop, high breakdown voltage and fast switching speed [3.36]-[3.37], which is idea for high voltage and high speed power integrated circuit (PIC) applications. However, the thickness of the SOI layer used for these devices is very critical as it controls the amount of the stored carriers in the drift region. If the SOI layer

is too thin, surface recombination at the top and bottom interfaces may render conductivity modulation ineffective and a high forward voltage drop will result.

3.1.3 Challenges for Linearly Graded Doping Design

Using a Variation in Lateral Doping (VLD) technology in a sequence of small opening oxide slits, which can achieve the linearly graded doping profile to relax the 2-dimension electric-field effect and bring lower on-resistance with high breakdown voltage in the drift region. The shape of the profile is controlled by the geometry of the implantation mask and the characteristic length for diffusion (times, temperature, and species). This technique uses a layer of oxide or photoresist with a sequence of slit openings for masking of the impurity implantation. These silts are increasingly smaller toward the P/N^- voltage blocking junction from the N side as shown in Fig. 3-5. The N-type dopants implanted through the slits act as sources in the subsequent drive-in process. If the drive-in time is long enough, the implanted dopants will be smeared out, resulting in a continuous lateral doping profile. By optimizing the location and size of these small silt openings, a linear doping profile for high breakdown voltage can be achieved. Unfortunately, there are two drawbacks of this structure: firstly, the linearly graded doping profile needs complicated mask layout to be fabricated. Furthermore, it is difficult to know whether the doping profile is certainly satisfied [3.38]; Secondly, the local self-heating is arose near the lightly doping side and it influences the reliability of surrounding low power cells on the same chip [3.39]. At present, when replacing the linear profile by the distinct doping region along lateral direction [3.40], the separated uniform doping can effectively avoid the former descriptions and can be easily realized by different implant dosages. Nevertheless, the additional mask of the step doping case is a serious problem in the cost aspect. Hence, this paper is to offer a choice of either

increasing the masks with step doping or longer thermal process with linearly graded doping for designs.

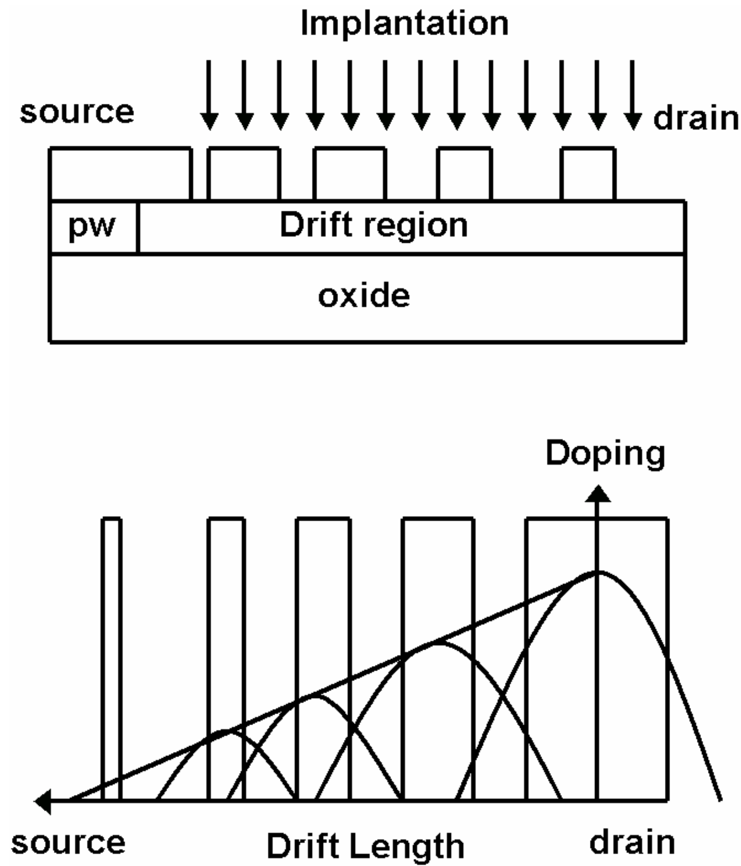


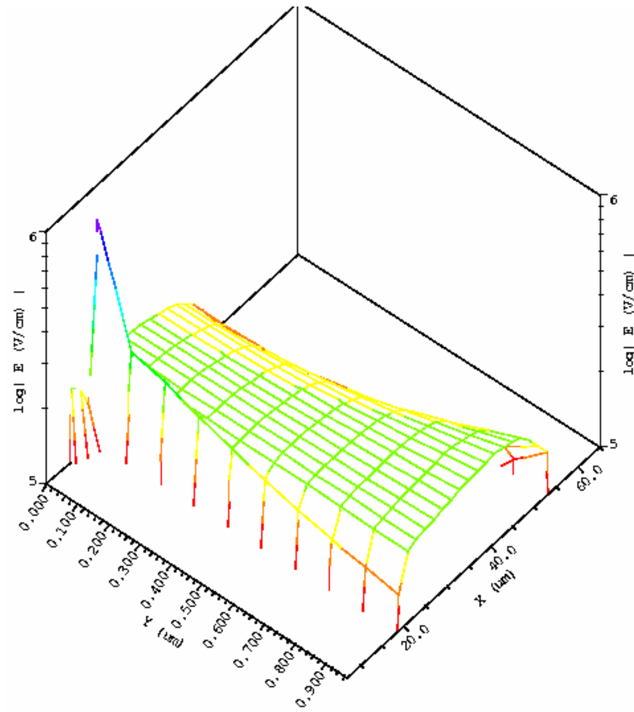
Fig. 3-5. Fabrication of linearly graded doping profile with a precise sequence of slit openings for making impurity implantation and a long drive-in time at 1200 °C.

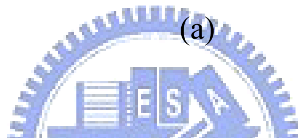
3.2 Modeling Descriptions and Verifications

3.2.1 Comparison of Step Doping Profile and Linearly Graded Doping

It is generally assumed that that the breakdown voltage of SOI RESURF (REduced SURface Field) scales up linearly with increasing drift region length until a limit

associated with vertical breakdown voltage is reduced. However, the breakdown voltage of SOI PiN diodes indicate non-ideal electric field distribution in the drift region with two sharp triangular peaks in electric field near the drain and source regions and a large dip in the field in the middle of the drift region. Hence, the middle portion of the drift region supports only a small fraction of the voltage, necessitating a much wider drift region than required for a case with a uniform lateral electric field profile in the drift region. An optimal approach to RESURF is the use of thin SOI layers with a linearly graded doping profile in the drift region to achieve high breakdown voltage in Fig. 3-6. Nevertheless, in practice, it is impossible to obtain a perfectly linear variation in the drift region from the drain to the source side. Thus, the step doping profile is developed that can replace the linearly graded doping profile and can be easier to fabricate in Fig. 3-7. For the step profile, the drift region of the device is equally divided into a number of uniformly doped regions, typically two or three. The net charge in each uniformly doping region is chosen to be equal to the average charge within that region for the case of the optimum linearly graded doping profile. This suggest for the step doping profile that the vertical breakdown voltage has to be increased by increasing the buried oxide thickness to take advantage of the step doping profile for longer drift lengths. The incorporation of the step in the doping profile cause an additional peak in the electric field distribution to appear at the step in the middle of the drift region. Further increase in number of step regions leads to provide only marginal increase of the breakdown voltage.





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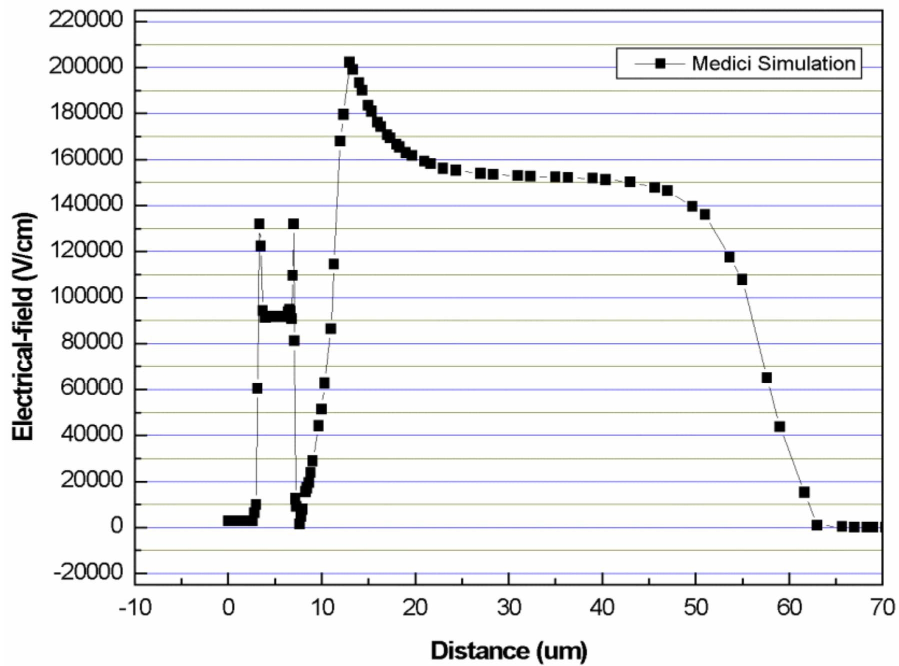
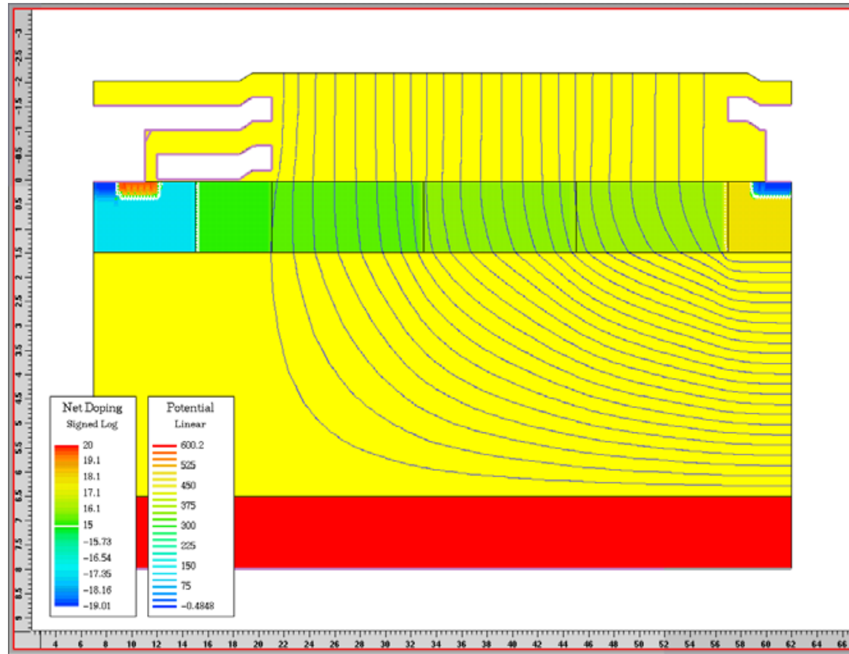
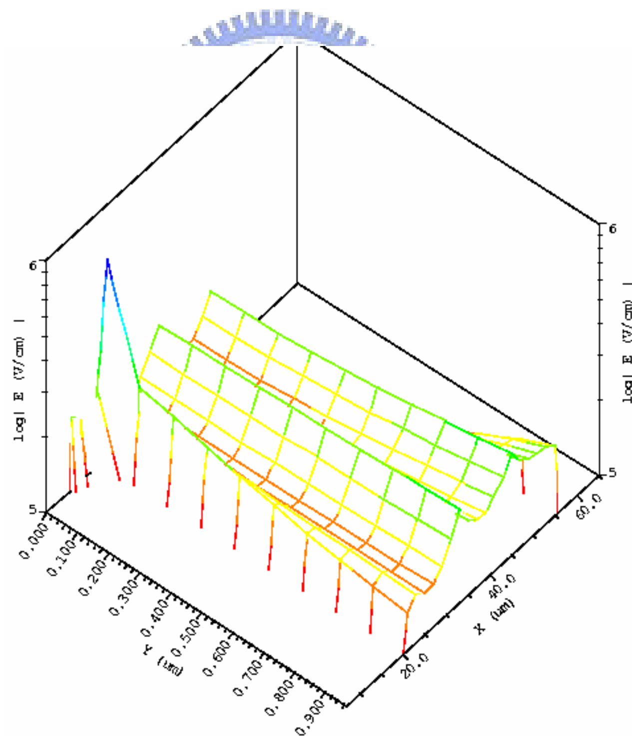


(b)

Fig. 3-6. Simulation of linearly graded doping device for (a) 3-D and (b) 1-D electric field distribution breakdown voltage of 617-V by Taurus extraction. The electric field in the middle of drift region is raised against a large dip for uniform doping profile.



(a)



(b)

Fig. 3-7. Simulation of step-doping device for (a) 2-D potential curves and (b) 3-D electric field distribution at breakdown voltage of 607-V by Taurus extraction. The additional electric peak appear at the step in the middle of drift region.

3.2.2 General Equation of Step-Doping SOI-LIGBT

While deriving an n-separate frames in drift region, as shown in Fig. 3-8, the neighborhood frame with a pervious frame is conjugated to find its individual boundary parameters.

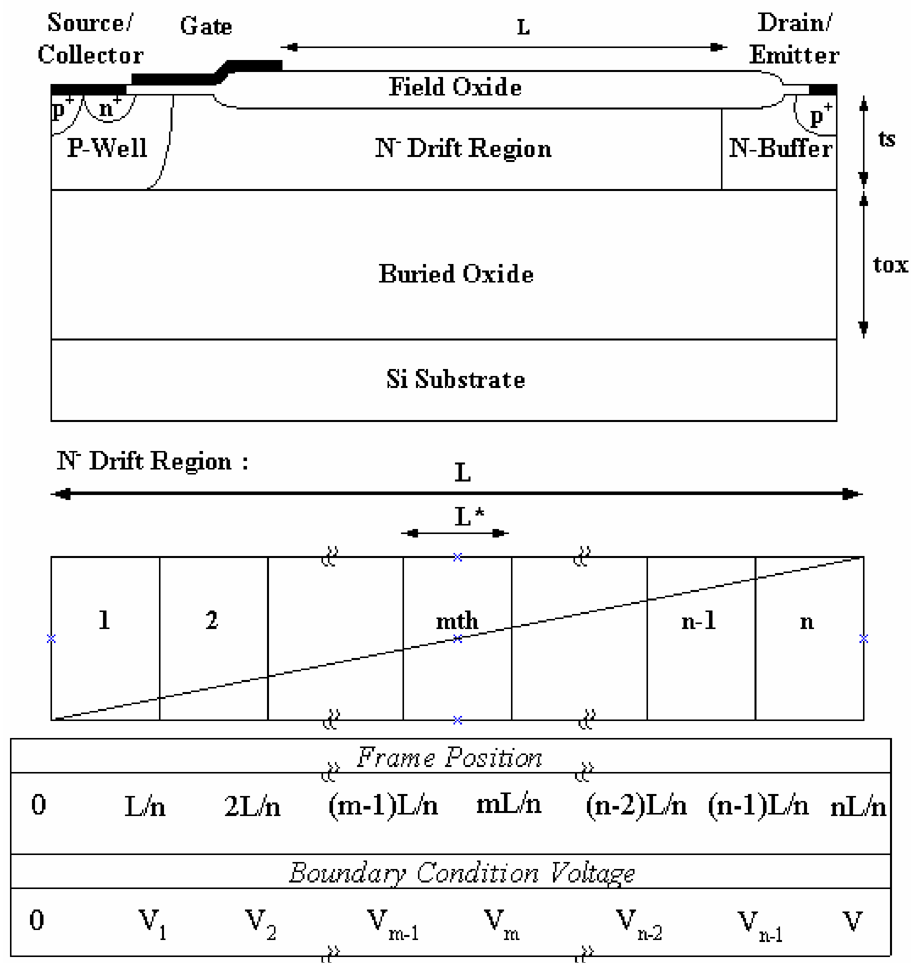


Fig. 3-8. Corresponding structure and frame architecture of step-doping SOI-LIGBT device. The concentration of the first frame is equal to the background doping which is also replicated from p-well to gate edge.

Assuming that the SOI layer is completely depleted and the buried oxide is charge-free, the frame 2-D Poisson equation is given with a parabolic approximation approach [3.41]

$$\frac{\partial^2 \psi}{\partial^2 x}+\frac{\partial^2 \psi}{\partial^2 y}=-\frac{qN}{\varepsilon_{si}}, \qquad \text{(Eq 3-1)}$$

and

$$\psi(x,y)=u(x)+u_1(x)y+u_2(x)y^2, \quad 0 \leqq y \leqq ts \qquad \text{(Eq 3-2)}$$

where $u(x)$ is the top surface potential at y= 0 and "N" is the concentration of each frame.

the potential lines are almost perpendicular to the top surface in whole drift region so that the electric filed in the top surface only exists the x-direction vectors. Thus, the top surface (y= 0) electric filed at y-direction is set up the zero point.

$$\mathrm{E_y}(x,0)=-(\frac{\partial \psi(x,y)}{\partial y})|_{y=0}=0, \qquad \text{(Eq 3-3)}$$

according to Eq (2-2), the partial y-differential equation in Eq. (3-3) is derived as

$$(\frac{\partial \psi(x,y)}{\partial y})|_{y=0}=u_1(x), \qquad \text{(Eq 3-4)}$$

putting Eq. (3-4) into Eq. (3-3), the value of $u_1(x)$ is found to be zero ($u_1(x)= 0$). The bottom surface (y= ts) electric field at y-direction is given by

$$\mathrm{E_y}(x,ts)=-(\frac{\partial \psi(x,y)}{\partial y})|_{y=ts}, \qquad \text{(Eq 3-5)}$$

according to Eq (2-2), the partial y-differential equation in Eq. (3-5) is derived as

$$(\frac{\partial \psi(x,y)}{\partial y})|_{y=ts}=2u_2(x)\,ts, \qquad \text{(Eq 3-6)}$$

From the displacement continuity at the Si/SiO_2 surface (ε_{si} E_{si} = ε_{ox} E_{ox}) and the equation of V=E × d, the relationship of E_y (x, ts) and $u(x)$ can be obtain in Eq. (3-7).

$$u(x)=(\frac{ts}{2}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}tox)\,\mathrm{E_y}(x,ts),$$

$$\mathrm{E_y}(x,ts)=\frac{u(x)}{(\frac{ts}{2}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}tox)}, \qquad \text{(Eq 3-7)}$$

Putting the results of Eq. (3-7) and Eq. (3-6) into Eq. (3-5), the electrostatic potential of

$u_2(x)$ will be calculated as function of $u(x)$ in Eq. (3-8).

$$u_2(x) = \frac{-u(x)}{2\,ts\,(\frac{ts}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} tox)} \qquad \text{(Eq 3-8)}$$

Finally, the potential of Eq. (3-2) can be simplified to be

$$\psi(x, y) = (1 - \frac{y^2}{2\,ts(\frac{ts}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} tox)})\,u(x), \qquad \text{(Eq 3-9)}$$

Substituting Eq. (3-9) into Eq. (3-1), the surface potential equation (including of the top and bottom surface) can be expressed as

$$(1 - \frac{y^2}{2ts(\frac{ts}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} tox)})\frac{\partial^2 u(x)}{\partial x^2} - \frac{u(x)}{ts(\frac{ts}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} tox)} = -\frac{qN}{\varepsilon_{si}}, \qquad \text{(Eq 3-10)}$$

the $u(x)$ is electrostatic potential at the top surface (y= 0) of the SOI layer ($u(x)=\varphi(x,0)$). Substituting y= 0 into Eq. (3-10), the top surface potential can be yielded as

$$\frac{\partial^2 u(x)}{\partial x^2} - \frac{u(x)}{t^2} = -\frac{qN}{\varepsilon_{si}}, \qquad \text{(Eq 3-11)}$$

where

$$t = \sqrt{ts\,(\frac{ts}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} tox)}, \qquad \text{(Eq 3-12)}$$

the solution of Eq. (3-11) is

$$u(x) = qt^2 N / \varepsilon_{si} + C_1 e^{x/t} + C_2 e^{-x/t}, \qquad \text{(Eq 3-13)}$$

Assuming that mth frame (m) has existed at n-separate (n) frames. Each frame concentration (N) is the mean value of the linearly graded slope (a), which is spread into the individual frame. The relationship of its position and concentration (N) are mL/n and $a(2m-1)L/2n$, respectively.

Position: L/n, 2L/n, …, mL/n, …, (n-1)L/n, nL/n

Mid position of each frame: L/2n, 3L/2n, …, $\frac{\mathrm{mL/n + (m-1)L/n}}{2} = \frac{\mathrm{2mL - L}}{\mathrm{2n}}$, …..

Concentration of each frame:

$$a(L/2n),\ a(3L/2n),\ \ldots,\ a\left(\frac{mL/n+(m-1)L/n}{2}\right)=a\left(\frac{2mL-L}{2n}\right),\ldots.. \quad \text{(Eq 3-14)}$$

The linearly graded slope (a) have been reported by 1991 S. Merchant and 1998 Y. K. Leung *et. al* [3.27], [3.42].

$$a=\frac{9.5\times10^{20}(\mathrm{cm}^{-4})}{ts\left(\frac{ts}{2}+\frac{\varepsilon_{si}}{\varepsilon_{ox}}tox\right)\ \ln(70.3L)}, \quad \text{(Eq 3-15)}$$

where the unit of drift length (L), SOI layer thickness (ts), and buried oxide thickness (tox) is micrometer (µm).

According to the quasi-neutral drift region under low-level injection condition, the surface potential of the mth frame in reach and non-reach boundary condition is given

Reach-Through boundary condition:

$$u_m\left(\frac{(m-1)L}{n}\right)=V_{m-1}\ ,\ u_m\left(\frac{mL}{n}\right)=V_m, \quad \text{(Eq 3-16)}$$

Non-Reach-Through boundary condition:

$$u_{mw}\left(\frac{(m-1)L}{n}\right)=V_{m-1}\ ,\ u'_{mw}(w_m)=0, \quad \text{(Eq 3-17)}$$

where "w" is presented as the non-reach-through length. The corresponding voltage is called the non-reach through voltage u_{mw}. Hence, combining Eq. (3-16) and Eq. (3-17) with Eq. (3-11), the surface potential $u(x)$ will be solved while the value of y= 0 is substituted into Eq. (3-10).

As the applied voltage increases, the impact ionization rate will determine whether the non-reach through of the mth frame can eventually deplete to the end. With deducing its ionization integral over the horizontal and vertical surface path, the mth frame's breakdown testing equation defined as [3.27]

$$I\ Hori_{m(w)}=\int_{\frac{(m-1)L}{n}}^{\frac{mL}{n}}\left[\mathrm{A}\left(\left|E_{x(w)}(x,0)\right|\right)^7\right]dx, \quad \text{(Eq 3-18)}$$

$$I\ Vert_{m(w)}=\int_0^{ts}\left[\mathrm{A}\left(\left|E_{y(w)}(K,y)\right|\right)^7\right]dy+\int_{\frac{(m-1)L}{n}}^{\frac{mL}{n}}\left[\mathrm{A}\left(\left|E_{x(w)}(x,ts)\right|\right)^7\right]dx, \quad \text{(Eq}$$

3-19)

where

$$K = \frac{\mathrm{mL}}{\mathrm{n}}\, or\, W, \qquad \text{(Eq 3-20)}$$

A= 1.8 × 10^{-35} when E(x, y) is expressed in V/cm [3.43]. "IHori" and "IVert" is the lateral and vertical impact ionization rates.

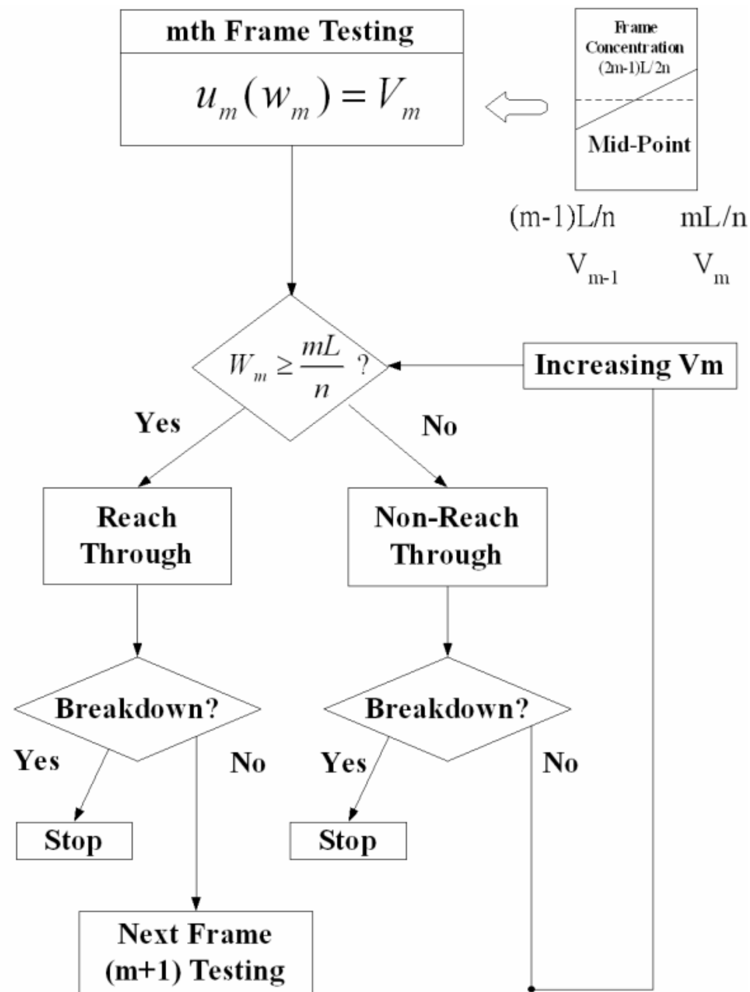


Fig. 3-9. Illustration of the partition method with a testing flowchart and single frame diagram. The key point is to determine whether the applied voltage will attain reach-throughout for each frame.

To simplify the analysis, only consider the two high-field locations are considered: (1) the first frames along y= 0, where "IHori" is high and (2) the last frame at point (x= K, y= ts), where "IVert" is high. Moreover, the critical electric field and potential of the mth frame are obtained as one of the value "I" approaches to the value 1. To make a summary, the mth frame-testing flowchart descried above is illustrated in Fig. 3-9.

3.2.3 Specific Equation of Step-Doping SOI-LIGBT for Three Frames

To achieve higher breakdown voltage, the difference between maximum and minimum electric fields must be eliminated in each frame. For this reason, a degraded factor "D" is provided to ensure near ideal-breakdown voltage as expected. It can be written as

$$D = Exp\,[-x/t] + Exp\,[(x - L^*)/t], \quad \text{(Eq 3-21)}$$

where

$$t = \sqrt{ts\,(\frac{ts}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} tox)}, \quad \text{(Eq 3-22)}$$

$$L^* = \frac{L}{n}, \quad \text{(Eq 3-23)}$$

this factor "D" include SOI layer thickness (ts), buried oxide thickness (tox), frame length (L*), and the number of frames (n). Among these the optimum structure parameters will be found at approaching D= 1. To simplify the mathematics in solving Eq. (3-19), it is convenient to assume the minimum electric field is located in the coordinate of x= L*/2. In place of the x-coordinate, the general solution is

$$D = 2 * Exp[-\frac{L}{2nt}] \quad \leq 1, \quad \text{(Eq 3-24)}$$

$$n \geq \frac{L}{2 * t * \ln 2}, \quad \text{(Eq 3-25)}$$

where the number of frames (n) is proportional to drift length (L) and inversely proportional to the term "t"--is associated with the buried oxide and SOI layer thickness. It is apparent that the thicker buried oxide and shorter drift length will promote smaller number of frames, especially if the SOI layer thickness is large enough. This makes it possible to reduce production cost. A relationship of breakdown voltage and degraded factor is demonstrated in Fig. 3-10. The optimum value of 0.6 is corresponding to the "three frames", which is chosen under economical consideration.

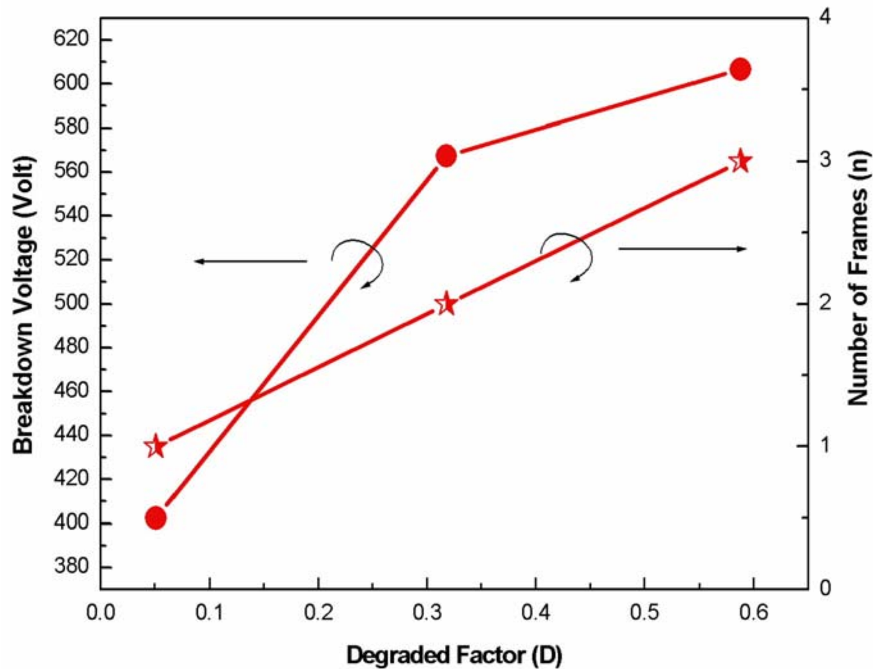


Fig. 3-10. Dependence of the breakdown voltage and frame number with degraded factor. The improvement of breakdown voltage is enough to use three frames in the drift region.

From the equations of Eq. (3-14) and Eq. (3-15), the three frames concentration and top surface potential at 0, $L/3$, $2L/3$, L are set up with $aL/6$, $aL/2$, $5aL/6$ and 0, V_1,

V_2, Vo, respectively. Solving the Eq. (3-13) with boundary conditions of Eq. (3-16) and Eq. (3-17), the top surface potential at reach-through and non-reach-through cases can be expressed as follows.

3.2.3.1 Surface Potential at Top Si/SiO$_2$ Interface for Three Frames

Reach-Through Case

In case of reach-through, the lateral depletion width "*w*" at the top surface of drift region is fully depleted and reached the N-buffer drain contact.

Region I ($0 \le x \le$ L/3)

With the boundary conditions of $u(0)=0$ and $u(L/3)=V_1$ from Eq. (3-16) at region I, the resultant of Eq. (3-13) can be expressed as

$$qt^2(aL/6)/\varepsilon_{si} + Ci_1 + Ci_2 = 0, \qquad \text{at } x=0 \qquad \text{(Eq 3-26)}$$

$$qt^2(aL/6)/\varepsilon_{si} + Ci_1 e^{L/3t} + Ci_2 e^{-L/3t} = V_1, \qquad \text{at } x=L/3 \qquad \text{(Eq 3-27)}$$

Solving the above Eq. (3-26) and Eq. (3-27), Ci_1 and Ci_2 are given

$$Ci_1 = \frac{qaLt^2(1-e^{L/3t}) + 6\varepsilon_{si}V_1 e^{L/3t}}{6(e^{2L/3t}-1)\varepsilon_{si}}, \qquad \text{(Eq 3-28)}$$

$$Ci_2 = \frac{qaLt^2(1-e^{L/3t}) - 6\varepsilon_{si}V_1}{6(e^{L/3t}-e^{-L/3t})\varepsilon_{si}}, \qquad \text{(Eq 3-29)}$$

Substituting into Eq. (3-13) and simplifying it, the final result of top surface potential in Region I can be derived to be

$$UIx = \frac{(qaLt^2\,Cosh[\frac{2L-3x}{6t}] + (6\varepsilon_{si}V_1 - qaLt^2)\,Cosh[\frac{x}{2t}])\,Csch[\frac{L}{3t}]\,Sinh[\frac{x}{2t}]}{3\varepsilon_{si}},$$

(Eq 3-30)

Region II (L/3 ≤ x ≤ 2L/3)

With the boundary conditions of $u(L/3)= V_1$ and $u(2L/3)= V_2$ from Eq. (3-16) at region II, the resultant of Eq. (3-13) can be expressed as

$$qt^2(aL/2)/\varepsilon_{si} + Cii_1 e^{L/3t} + Cii_2 e^{-L/3t} = V_1, \quad \text{at } x= L/3 \quad \text{(Eq 3-31)}$$

$$qt^2(aL/2)/\varepsilon_{si} + Cii_1 e^{2L/3t} + Cii_2 e^{-2L/3t} = V_2, \quad \text{at } x= 2L/3 \quad \text{(Eq 3-32)}$$

Solving the above Eq. (3-31) and Eq. (3-32), Cii_1 and Cii_2 are given

$$Cii_1 = \frac{qaLt^2(1-e^{L/3t}) + 2\varepsilon_{si}(V_2 e^{L/3t} - V_1)}{2(e^{L/t} - e^{L/3t})\varepsilon_{si}}, \quad \text{(Eq 3-33)}$$

$$Cii_2 = \frac{qaLt^2(1-e^{L/3t}) + 2\varepsilon_{si}(V_1 e^{L/3t} - V_2)}{2(1 - e^{-2L/3t})\varepsilon_{si}}, \quad \text{(Eq 3-34)}$$

Substituting into Eq. (3-13) and simplifying it, the final result of top surface potential in Region II can be derived to be

$$UIIx = \frac{qaLt^2\ Sinh[\frac{L}{3t}] + (qaLt^2 - 2\varepsilon_{si}V_2)\ Sinh[\frac{L-3x}{3t}]) + (2\varepsilon_{si}V_1 - qaLt^2)\ Sinh[\frac{2L-3x}{3t}]}{2\varepsilon_{si}\ Sinh[\frac{L}{3t}]},$$

(Eq 3-35)

Region III (2L/3 ≤ x ≤ L)

With the boundary conditions of $u(2L/3)= V_2$ and $u(L)= Vo$ from Eq. (3-16) at region III, the resultant of Eq. (3-13) can be expressed as

$$qt^2(5aL/6)/\varepsilon_{si} + Ciii_1 e^{2L/3t} + Ciii_2 e^{-2L/3t} = V_2, \quad \text{at } x= 2L/3 \quad \text{(Eq 3-36)}$$

$$qt^2(5aL/6)/\varepsilon_{si} + Ciii_1 e^{L/t} + Ciii_2 e^{-L/t} = Vo, \quad \text{at } x= L \quad \text{(Eq 3-37)}$$

Solving the above Eq. (3-36) and Eq. (3-37), $Ciii_1$ and $Ciii_2$ are given

$$Ciii_1 = \frac{5qaLt^2(1-e^{L/3t}) + 6\varepsilon_{si}(Vo\, e^{L/3t} - V_2)}{6(e^{4L/3t} - e^{2L/3t})\varepsilon_{si}}, \quad \text{(Eq 3-38)}$$

$$Ciii_2 = \frac{5qaLt^2(1-e^{L/3t}) + 6\varepsilon_{si}(Be^{L/3t} - Vo)}{6(e^{-L/3t} - e^{-L/t})\varepsilon_{si}}, \quad \text{(Eq 3-39)}$$

Substituting into Eq. (3-13) and simplifying it, the final result of top surface potential in Region III can be derived to be

$$UIIIx = \frac{Csch[\frac{L}{3t}](5qaLt^2\ Sinh[\frac{L}{3t}] + (5qaLt^2 - 6\varepsilon_{si}Vo)\ Sinh[\frac{2L-3x}{3t}] + (6\varepsilon_{si}V_2 - 5aqLt^2)\ Sinh[\frac{L-x}{t}])}{6\varepsilon_{si}},$$

(Eq 3-40)

Non-Reach-Through Case

In case of non-reach-through, the lateral depletion width "*w*" at the top surface of drift region is partially depleted and not reached the N-buffer drain contact.

Region I ($0 \leqq x \leqq wa \leqq L/3$)

With the boundary conditions of $u(0)= 0$ and $u'(wa)= 0$ from Eq. (3-17) at region I, the resultant of Eq. (3-13) can be expressed as

$$qt^2(aL/6)/\varepsilon_{si} + Ci_1 + Ci_2 = 0, \quad \text{at } x= 0 \qquad \text{(Eq 3-41)}$$

$$Ci_1 e^{wa/t} - Ci_2 e^{-wa/t} = 0, \quad \text{at } x= wa \qquad \text{(Eq 3-42)}$$

Solving the above Eq. (3-41) and Eq. (3-42), Ci_1 and Ci_2 are given

$$Ci_1 = \frac{-qaLt^2}{6(1+e^{2wa/t})\varepsilon_{si}}, \qquad \text{(Eq 3-43)}$$

$$Ci_2 = \frac{-qaLt^2}{6(1+e^{-2wa/t})\varepsilon_{si}}, \qquad \text{(Eq 3-44)}$$

Substituting into Eq. (3-13) and simplifying it, the final result of top surface potential in Region I can be derived to be

$$UIx = \frac{qaLt^2\ Sech[\frac{wa}{t}]\ Sinh[\frac{2wa-x}{2t}]\ Sinh[\frac{x}{2t}]}{3\varepsilon_{si}}, \qquad \text{(Eq 3-45)}$$

From Eq. (3-42) to Eq. (3-44), the depletion width "*wa*" in region I can be obtained

$$wa = 2t\ Cosh^{-1}[\frac{\sqrt{3A\varepsilon_{si} - qaLt^2}}{\sqrt{6A\varepsilon_{si} - qaLt^2}}], \qquad \text{(Eq 3-46)}$$

Region II (L/3 ≦ x ≦ wb ≦ 2L/3)

With the boundary conditions of $u(L/3)= V_1$ and $u'(wb)= 0$ from Eq. (3-17) at region II, the resultant of Eq. (3-13) can be expressed as

$$qt^2(aL/2)/\varepsilon_{si} + Cii_1 e^{L/3t} + Cii_2 e^{-L/3t} = V_1, \quad \text{at } x= L/3 \quad \text{(Eq 3-47)}$$

$$Cii_1 e^{wb/t} - Cii_2 e^{-wb/t} = 0, \quad \text{at } x= wb \quad \text{(Eq 3-48)}$$

Solving the above Eq. (3-47) and Eq. (3-48), Cii_1 and Cii_2 are given

$$Cii_1 = \frac{e^{L/3t}(2V_1\varepsilon_{si} - qaLt^2)}{2(e^{2L/3t} + e^{2wb/t})\varepsilon_{si}}, \quad \text{(Eq 3-49)}$$

$$Cii_2 = \frac{e^{L/3t+2wb/t}(2V_1\varepsilon_{si} - qaLt^2)}{2(e^{2L/3t} + e^{2wb/t})\varepsilon_{si}}, \quad \text{(Eq 3-50)}$$

Substituting into Eq. (3-13) and simplifying it, the final result of top surface potential in Region II can be derived to be

$$UIIx = \frac{qaLt^2 + (2\varepsilon_{si}V_1 - qaLt^2)\,Cosh[\frac{wb-x}{t}]\,Sech[\frac{L-3wb}{3t}]}{2\varepsilon_{si}}, \quad \text{(Eq 3-51)}$$

From Eq. (3-48) to Eq. (3-50), the depletion width "wb" in region II can be obtain

$$wb = \frac{L}{3} + t\,Sech^{-1}[\frac{qaLt^2 - 2V_2\varepsilon_{si}}{qaLt^2 - 2V_1\varepsilon_{si}}], \quad \text{(Eq 3-52)}$$

Region III (2L/3 ≦ x ≦ wc ≦ L)

With the boundary conditions of $u(2L/3)=V_2$ and $u'(wc)=0$ from Eq. (3-17) at region III, the resultant of Eq. (3-13) can be expressed as

$$qt^2(5aL/6)/\varepsilon_{si} + Ciii_1 e^{2L/3t} + Ciii_2 e^{-2L/3t} = V_2, \quad \text{at } x= 2L/3 \quad \text{(Eq 3-53)}$$

$$Ciii_1 e^{wc/t} - Ciii_2 e^{-wc/t} = 0, \quad \text{at } x= wc \quad \text{(Eq 3-54)}$$

Solving the above Eq. (3-53) and Eq. (3-54), $Ciii_1$ and $Ciii_2$ are given

$$Ciii_1 = \frac{e^{2L/3t}(6V_2\varepsilon_{si} - 5qaLt^2)}{6(e^{4L/3t} + e^{2wc/t})\varepsilon_{si}}, \quad \text{(Eq 3-55)}$$

$$Ciii_2 = \frac{e^{2L/3t+2wc/t}(6V_2\varepsilon_{si} - 5qaLt^2)}{6(e^{4L/3t} + e^{2wc/t})\varepsilon_{si}}, \quad \text{(Eq 3-56)}$$

Substituting into Eq. (3-13) and simplifying it, the final result of top surface potential in

Region III can be derived to be

$$UIIIx = \frac{5qaLt^2 + (6\varepsilon_{si}V_2 - 5qaLt^2)\,Cosh[\frac{wc-x}{t}]\,Sech[\frac{2L-3wc}{3t}]}{6\varepsilon_{si}}, \qquad \text{(Eq 3-57)}$$

From Eq. (3-54) to Eq. (3-56), the depletion width "*wc*" in region III can be obtain

$$wc = \frac{2L}{3} + t\,Sech^{-1}[\frac{5qaLt^2 - 6\,Vo\,\varepsilon_{si}}{5qaLt^2 - 6V_2\varepsilon_{si}}], \qquad \text{(Eq 3-58)}$$

In this methodology, an algorithm is developed to obtain systematic n-separate frames cogitation. In the first part, the user is demanded to offer some fundamental parameters that comprise the drift length (L) with respond to linearly graded slope definition (a) [3.42]. Then, the algorithm works are listed as follows.

1) Set up the structure parameter from the degraded factor (D).

2) By dint of the flowchart in Fig. 2. Each frame electric and potential function can be obtained step by step. The n-separate frames will donate 2n states that include reach and non-reach through case. If some frame breaks down during examination, the program will be claimed to stop.

3) Be sure that each frame's electric and potential function comprises not only device dimension parameters but also its neighbor boundary value.

4) Start from the left side zero point and equalize its individual functional equation with its neighbor frame equation. Substitute all derivational boundary value into the next unknown frame equation to evaluate its unknown electric and potential value in turn. Then these frames boundary values are functions of *V* eventually.

$(x_m = x_{m+1},\ x_{m+1} = x_{m+2}\ \ \ldots\ldots\ldots)$

5) Substitute the desired breakdown voltage into the final value "*Vo*". Then the value "*V*" will be gained, so every boundary condition value can be discovered from the right-side to left-side.

In the following, the breakdown voltage, weak-point, optimum design parameters, and low-cost way are taken systematically.

3.2.3.2 Surface Electric Field at Top Si/SiO_2 Interface

Solving the differential equation of Eq. (3-13) with boundary conditions of Eq. (3-16) and Eq. (3-17), the top surface electric field at reach-through and non-reach-through cases can be expressed as follows. Recalling the $\varphi(x, y)$ in Eq. (3-9), the equation will be illustrated anew with the notation "*t*" and differentiated by the x and y vectors.

$$\psi(x, y) = (1 - \frac{y^2}{2t^2})\, u(x), \qquad \text{(Eq 3-59)}$$

where

$$t = \sqrt{ts\,(\frac{ts}{2} + \frac{\varepsilon_{si}}{\varepsilon_{ox}} tox)}, \qquad \text{(Eq 3-60)}$$

the lateral (x) and vertical (y) components of electric field are obtained from Eq. (3-59) as

$$\mathrm{E_x}(x, y) = -(\frac{\partial \psi(x, y)}{\partial x}) = -(1 - \frac{y^2}{2t^2})\frac{\partial u(x)}{\partial x}, \qquad \text{(Eq 3-61)}$$

$$\mathrm{E_y}(x, y) = -(\frac{\partial \psi(x, y)}{\partial y}) = \frac{y}{t^2}\, u(x), \qquad \text{(Eq 3-62)}$$

the magnitude of the total electric field is given by

$$\mathrm{E}(x, y) = \sqrt{\mathrm{E}_x^{\,2} + \mathrm{E}_y^{\,2}}, \qquad \text{(Eq 3-63)}$$

Reach-Through Case

In case of reach-through, the lateral depletion width "*w*" at the top surface of drift region is fully depleted and reached the N-buffer drain contact.

Region I ($0 \leqq x \leqq L/3$)

From the Eq. (3-13), the final result of top surface potential in Region I has been derived and listed anew as follows.

$$UIx = \frac{(qaLt^2\, Cosh[\frac{2L-3x}{6t}] + (6\varepsilon_{si}V_1 - qaLt^2)\, Cosh[\frac{x}{2t}])\, Csch[\frac{L}{3t}]\, Sinh[\frac{x}{2t}]}{3\varepsilon_{si}},$$

(Eq 3-64)

according to the Eq. (3-61) and Eq.(2-62), the electric field of $E_x(x, y)$ and $E_y(x, y)$ in region I were expressed as

$$E_x(x,y) = ExI = -(1-\frac{y^2}{2t^2})\frac{\partial UIx}{\partial x}$$

$$= \frac{(2t^2 - y^2)((qaLt^2 - 6V_1\varepsilon_{si})\, Cosh[\frac{x}{t}] - qaLt^2\, Cosh[\frac{L-3x}{3t}])\, Csch[\frac{L}{3t}]}{12t^3\,\varepsilon_{si}},$$

(Eq 3-65)

$$E_y(x,y) = \frac{y}{t^2}UIx = \frac{y\,(qaLt^2\, Cosh[\frac{2L-3x}{6t}] + (6V_1\varepsilon_{si} - qaLt^2)\, Cosh[\frac{x}{t}])\, Csch[\frac{L}{3t}]\, Sinh[\frac{x}{2t}]}{3t^2\,\varepsilon_{si}},$$

(Eq 3-66)

the ionization rates of electrons and holes in silicon p-n indicate that

$$\alpha = a\, e^{-b/E},$$ (Eq 3-67)

where a= 7.03×10^5 cm^{-1} and b= 1.47×10^6 cm^{-1}, for the electric field magnitude $1.75 \times 10^5 < E < 6.4 \times 10^5$ V cm^{-1}. The ionization integral first approaching unity determines the onset of avalanche breakdown. The breakdown voltage may be defined as the first root of the following product:

$$\prod_{i=1}^{\infty}(1-I_i) = (1-I_1)(1-I_2)(1-I_3)\ldots = 0$$ (Eq 3-68)

where I_i denotes the ionization integral over the ith path. Using the results of Eq. (3-18) and Eq. (3-19), the two high-field locations in region I will become as

$$I\,Hori_1 = \int_0^{\frac{L}{3}} \left[\mathrm{A}\,(|E_x(x,0)|)^7 \right] dx, \qquad \text{(Eq 3-69)}$$

$$I\,Vert_1 = \int_0^{ts} \left[\mathrm{A}\,\left(\left|E_y(\frac{\mathrm{L}}{3}, y)\right|\right)^7 \right] dy + \int_0^{\frac{L}{3}} \left[\mathrm{A}\,(|E_x(x,ts)|)^7 \right] dx, \qquad \text{(Eq 3-70)}$$

A= 1.8 × 10^{-35} V/cm

Region II (L/3 ≦ x ≦ 2L/3)

From the Eq. (3-13), the final result of top surface potential in Region II has been derived and listed anew as follows.

$$UIIx = \frac{qaLt^2\ Sinh[\frac{L}{3t}] + (qaLt^2 - 2\varepsilon_{si}V_2)\ Sinh[\frac{L-3x}{3t}]) + (2\varepsilon_{si}V_1 - qaLt^2)\ Sinh[\frac{2L-3x}{3t}]}{2\varepsilon_{si}\ Sinh[\frac{L}{3t}]},$$

(Eq 3-71)

according to the Eq. (3-61) and Eq.(2-62), the electric field of $E_x(x, y)$ and $E_y(x, y)$ in region II were expressed as

$$\mathrm{E_x}(x,y) = \mathrm{ExII} = -(1 - \frac{y^2}{2t^2})\frac{\partial\, UIIx}{\partial x}$$

$$= \frac{(2t^2 - y^2)((qaLt^2 - 2V_2\varepsilon_{si})\,Cosh[\frac{L-3x}{3t}] + (2V_1\varepsilon_{si} - qaLt^2)\,Cosh[\frac{2L-3x}{3t}])}{4\,Sinh[\frac{L}{3t}]\,t^3\ \varepsilon_{si}},$$

(Eq 3-72)

$$\mathrm{E_y}(x,y) = \frac{y}{t^2}\,UIIx =$$

$$\frac{y\,(qaLt^2\ Sinh[\frac{L}{3t}] + (qaLt^2 - 2V_2\varepsilon_{si})\,Sinh[\frac{L-3x}{3t}] + (2V_1\varepsilon_{si} - qaLt^2)\,Sinh[\frac{2L-3x}{3\,\mathrm{t}}])}{2\,Sinh[\frac{L}{3t}]\,t^2\ \varepsilon_{si}},$$

(Eq 3-73)

using the results of Eq. (3-18) and Eq. (3-19), the two high-field locations in region II will become as

$$I\,Hori_2 = \int_{\frac{L}{3}}^{\frac{2L}{3}} \left[\mathrm{A}\,(|E_x(x,0)|)^7 \right] dx, \qquad \text{(Eq 3-74)}$$

$$I\,Vert_2 = \int_0^{ts} \left[\mathrm{A}\,\left(\left|E_y(\frac{2L}{3}, y)\right|\right)^7 \right] dy + \int_{\frac{L}{3}}^{\frac{2L}{3}} \left[\mathrm{A}\,(|E_x(x,ts)|)^7 \right] dx, \qquad \text{(Eq 3-75)}$$

A= 1.8 × 10^{-35} V/cm

Region III (2L/3 ≦ x ≦ L)

From the Eq. (3-13), the final result of top surface potential in Region III has been derived and listed anew as follows.

$$UIIIx = \frac{Csch[\frac{L}{3t}](5qaLt^2\; Sinh[\frac{L}{3t}] + (5qaLt^2 - 6\varepsilon_{si}Vo)\; Sinh[\frac{2L-3x}{3t}] + (6\varepsilon_{si}V_2 - 5aqLt^2)\; Sinh[\frac{L-x}{t}])}{6\varepsilon_{si}},$$

(Eq 3-76)

according to the Eq. (3-61) and Eq.(2-62), the electric field of $E_x(x, y)$ and $E_y(x, y)$ in region III were expressed as

$$\mathrm{E_x}(x,y) = \mathrm{ExIII} = -(1 - \frac{y^2}{2t^2})\frac{\partial\, UIIIx}{\partial x}$$

$$= \frac{(2t^2 - y^2)((5qaLt^2 - 6Vo\varepsilon_{si})\, Cosh[\frac{2L-3x}{3t}] + (6V_2\varepsilon_{si} - 5qaLt^2)\, Cosh[\frac{L-x}{t}])}{12\; Sinh[\frac{L}{3t}]\, t^3\; \varepsilon_{si}},$$

(Eq 3-77)

$$\mathrm{E_y}(x,y) = \frac{y}{t^2}UIIx =$$

$$\frac{y\,(5qaLt^2\; Sinh[\frac{L}{3t}] + (5qaLt^2 - 6Vo\varepsilon_{si})\; Sinh[\frac{2L-3x}{3t}] + (6V_2\varepsilon_{si} - 5qaLt^2)\; Sinh[\frac{L-x}{\mathrm{t}}])}{6\; Sinh[\frac{L}{3t}]\, t^2\; \varepsilon_{si}},$$

(Eq 3-78)

using the results of Eq. (3-18) and Eq. (3-19), the two high-field locations in region III will become as

$$I\ Hori_3 = \int_{\frac{2L}{3}}^{L} \left[A\left(\left|E_x(x,0)\right|\right)^7 \right] dx, \qquad \text{(Eq 3-79)}$$

$$I\ Vert_3 = \int_0^{ts} \left[A\left(\left|E_y(L,y)\right|\right)^7 \right] dy + \int_{\frac{2L}{3}}^{L} \left[A\left(\left|E_x(x,ts)\right|\right)^7 \right] dx, \qquad \text{(Eq 3-80)}$$

A= 1.8 × 10^{-35} V/cm

3.3 Results and Discussion

3.3.1 Derivation of Breakdown Voltage and Issue Location

In this section, a numerical example of this analysis is demonstrated. The data of the example is 600 V linearly graded SOI devices, whose specification is as follows: ts=1.5-μm, tox=5-μm, L=36-μm, slope (a)=5.05 × 10^{18} cm^{-4}. As the result of statistics, the required degraded factor (D), ranging from 0.5 to 0.7, is enough to achieve high breakdown voltage. So the value 0.6 is chosen such that three frames can be obtained under this economical mode.

Considering the continuity of electric field at x= 2L/3 (24 μm) with Eq. (3-72) of region II and Eq. (3-77) of region III, the anticipant breakdown voltage "Vo" of 600 V is substituted and the value of potential voltage "V_1" at x=$L/3$ (12 μm) can be derived as

$| ExII |_{x=2L/3} = | ExIII |_{x=2L/3}$

the "V_1" can be calculated with the value of 220.45 V. In order to verify whether the region I has been broken, the value of V_1 will be substituted into the impact ionization rates of Eq. (3-69) and Eq. (3-70), the "$I\ Hori_1$" and "$I\ Vert_1$" are obtained for the numbers of 0.3257 and 0.2331, respectively. The multiplication of ionization integrals is not approach to zero and the verification can be continued to next region (region II).

$(1- I\ Hori_1)\ (1- I\ Vert_1)$= 0.5171

Substituting the value of V_1 into Eq. (3-65) of region I and Eq. (3-72) of region II at x=*L/3* (12 μm), the value of potential voltage "V_2" is given

$| ExI |_{x= L/3} = | ExII |_{x= L/3}$

the "V_2" can be calculated with the values of 436.41 V or −1067.35 V. The negative voltage is unreasonable for −1067.35 V so that the value of 436.41 V was selected for V_2. In order to verify whether the region II has been broken, the values of V_1 and V_2 will be substituted into the impact ionization rates of Eq. (3-74) and Eq. (3-75), the "$I\ Hori_2$" and "$I\ Vert_2$" are obtained for the numbers of 0.2838 and 0.2406, respectively. The multiplication of ionization integrals is not approach to zero and the verification can be continued to next region (region III).

$(1- I\ Hori_2)\ (1- I\ Vert_2)= 0.5439$

Finally, in order to verify whether the region III has been broken, the values of V_2 and Vo will be substituted into the impact ionization rates of Eq. (3-79) and Eq. (3-80). The "$I\ Hori_3$" and "$I\ Vert_3$" are obtained for the numbers of 0.1081 and 0.9439, respectively. The ionization integral of "$I\ Vert_3$" is first approach to unity, which determines the onset of avalanche breakdown.

$(1- I\ Hori_3)\ (1- I\ Vert_3)= 0.0499$

the multiplication of ionization integrals of 0.0499 is the most approach to zero which means the weak is located at $x= L$ (36 μm) and $y= ts$ (1.5 μm) of region III and broken. A significant avalanche generation occurs near the buried oxide interface under drain side.

3.3.2 Analytical Results Compared with MEDICI Simulation

Figure 3-11 shows the electricity of various partition frames, linearly graded, and uniform type for comparison. In this Figure, the breakdown voltage of three-frame

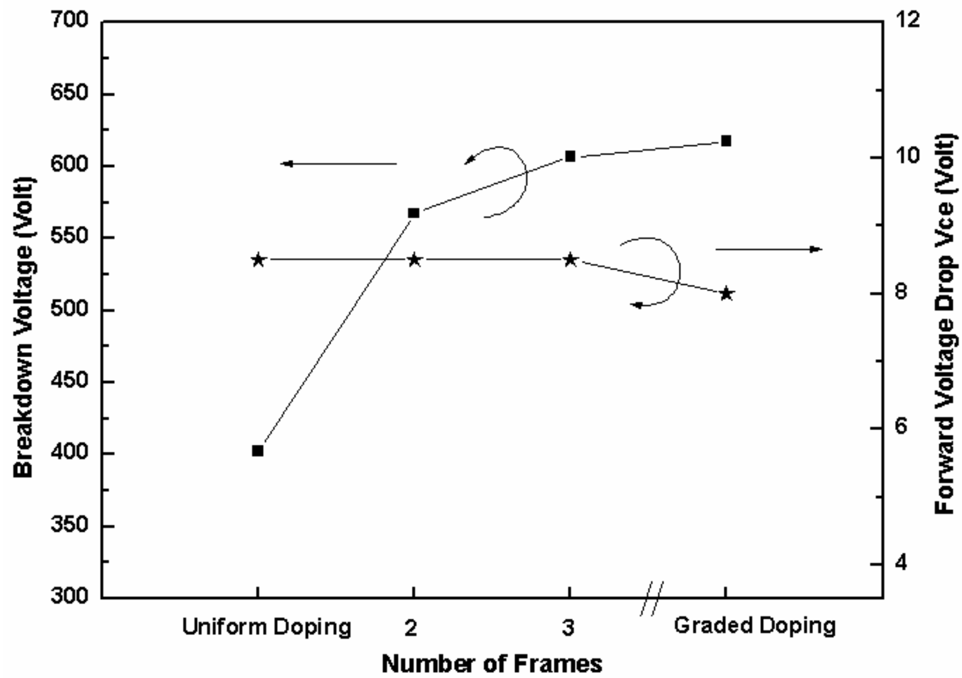


Fig. 3-11. Investigation of the optimum device characteristics in respect of breakdown voltage and forward voltage drop with various numbers of frames. Its SOI layer thickness, buried oxide thickness, and the drift length are 1.5-μm, 5-μm, and 36-μm, respectively.

Table 3-1. Summary of electrical characteristics of breakdown voltage and forward voltage drop for different frames and grading doping devices via the degraded factors.

	Degraded Factor (K)	Breakdown Voltage	Forward Drop (Vce)
1 Frames	0.051	124.7	8.5
2 Frames	0.318	567.5	8.5
3 Frames	0.588	606.6	8.5
Graded Doping	––	617.1	8.0

(607 V) is indeed nearly close to the linearly graded device (617 V) at similar Vce of

12 V-gate bias at 100 A/cm^2. However, the deviation of the graded doping Vce is caused by the different concentration between the p-well and the gate edge.

Moreover, for further comprehension, the three frame's potential and electric-matching curves are illustrated in Fig. 3-12 (a) and (b) with the fully reach through case. Its general equations for the electric field are given below

$$ExI = \alpha[(\beta - 6V_1\,\varepsilon_{si}) * \cosh(\frac{x}{t}) - \beta * \cosh(\frac{L/3 - x}{t})], \qquad \text{(Eq 3-81)}$$

$$ExII = 3\alpha[(\beta - 2V_2\,\varepsilon_{si}) * \cosh(\frac{L/3 - x}{t}) + (2V_1\,\varepsilon_{si} - \beta) * \cosh(\frac{2L/3 - x}{t})], \qquad \text{(Eq 3-82)}$$

$$ExIII = \alpha[(5\beta - 6V\,\varepsilon_{si}) * \cosh(\frac{2L/3 - x}{t}) + (6V_2\,\varepsilon_{si} - 5\beta) * \cosh(\frac{L - x}{t})], \qquad \text{(Eq 3-83)}$$

where

$$0 \le x(I) \le \frac{L}{3} \quad \frac{L}{3} \le x(II) \le \frac{2L}{3} \quad \frac{2\mathrm{L}}{3} \le x(III) \le L, \qquad \text{(Eq 3-84)}$$

and

$$\alpha = \frac{(2t^2 - y^2)}{12t^3\varepsilon_{si}}\operatorname{csc}h(\frac{L}{3t}), \qquad \text{(Eq 3-85)}$$

$$\beta = a\,q\,t^2L, \qquad \text{(Eq 3-86)}$$

where the relationship between V_1 and V_2 can be found from the algorithm in the fourth item. As pictured in Fig. 3-12 (b), the step doping devices exhibit 3 times improvement of the middle electric field with the uniform doping type and 0.75 times less than that of the linearly graded doping devices. These simulated results are compared to analytic data, that showing good qualitative and quantitative agreement in Fig. 3-12 (a) and (b). In these verification regulations, the highest impact ionization rate is found at the third (last) frame, where the value "IVert" is about 0.9 while substituting the voltage 660 into the value of "V". The breakdown voltage is over the prediction with only about 8.9 % of the MEDICI simulation value.

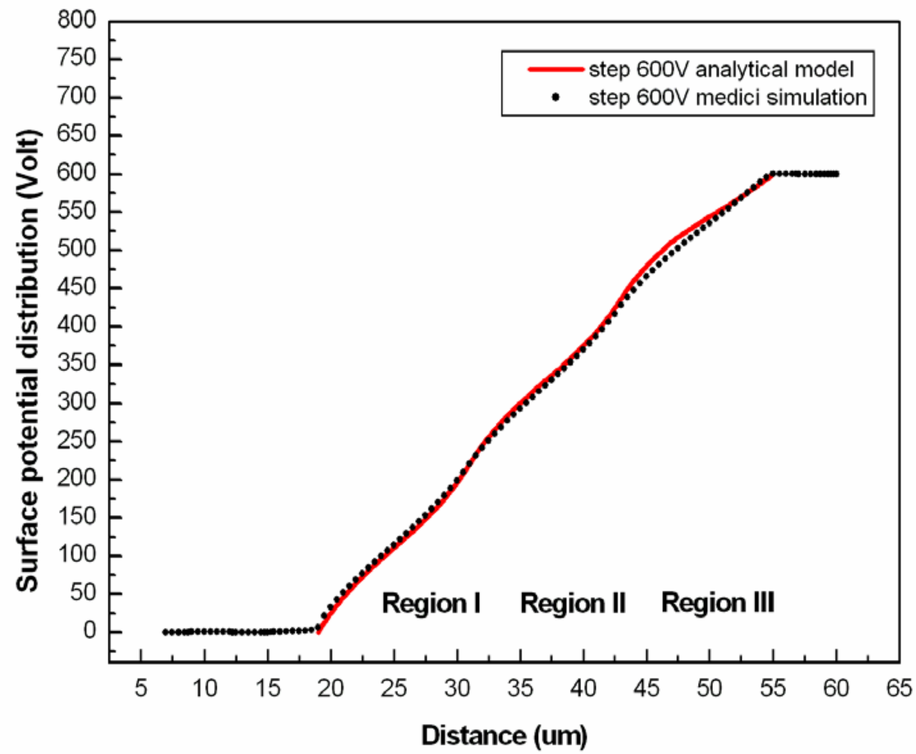


Fig. 3-12. (a) Comparison of the surface potential distribution with analytical model and MEDICI simulation. The analytical result is most in agreement with the data generated by MEDICI simulation.

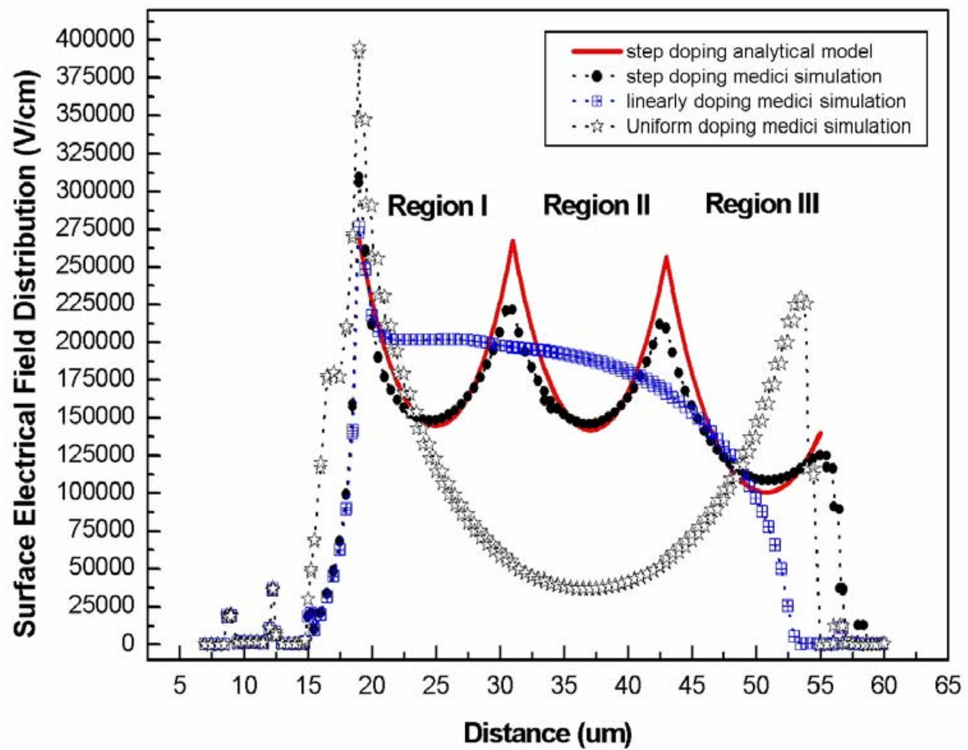


Fig. 3-12. (b) The different kinds of surface electric field distribution are shown in each drift region before the breakdown voltage happens. The step doping type exhibits a significant electric improvement compared to the uniformly doping type.

3.3.3 Deviation between Analytical Model and MEDICI Simulation

In respect of step doping device reliability, the deviation percentages would be provided between analytical model and MEDICI simulation, illustrated in Fig. 3-13 (a) and (b). As presented in these Figures, the ranges of data variation are available from –5 % to 5 % in surface potential part and –20 % to 20 % in surface electric field part. In Fig. 3-13 (b), the deviation of surface electric field become more severe than that of potential exhibition due to the differential at the corner of each frame, where exists the transitional tangent lines relative to high peak electric value. Moreover, the positions of frame boundary are located accurately in each frame with this method.

It should be emphasized that the point of 20-μm distance indicates a large surface potential deviation in Fig. 3-13 (a). The reason is that initial solution of the analytical model is set up the zero voltage value at the poly gate edge (20-μm). But in the MEDICI simulation, the zero value of the origin point is situated at the p-well edge (15-μm). It is allowed to modify the initial solution if you prefer to obtain less deviation at the origin point, but the modified initial solution (0 V⇒ 6 V) would not affect the previous consequence of this paper more seriously.

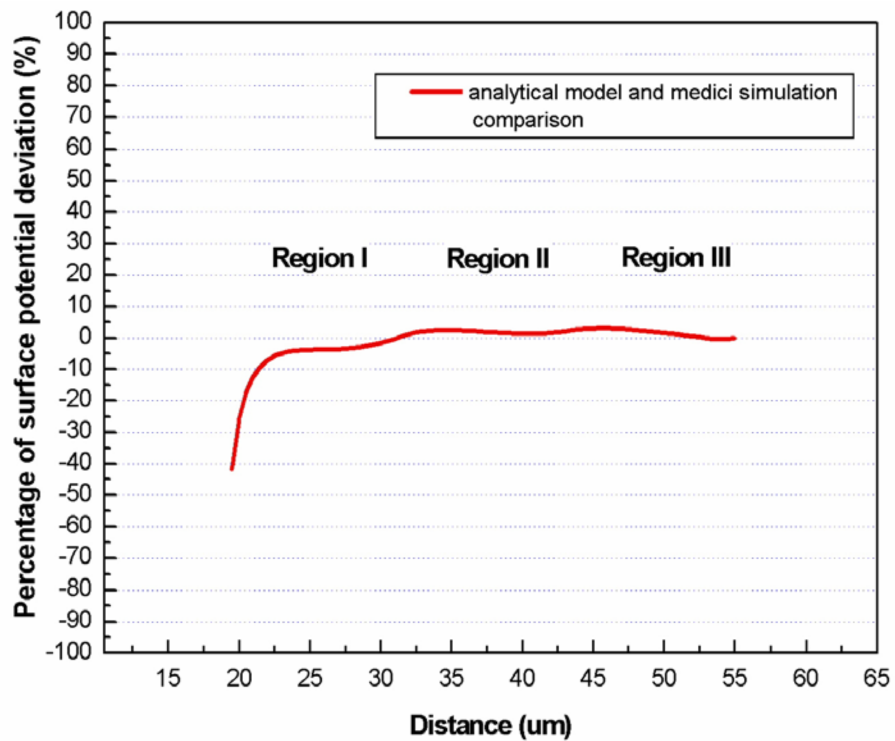


Fig. 3-13. (a) Percentage of the surface potential deviation as a function of the distance in three frames. It is worth to mention that the maximum error value is occurred on the outset.

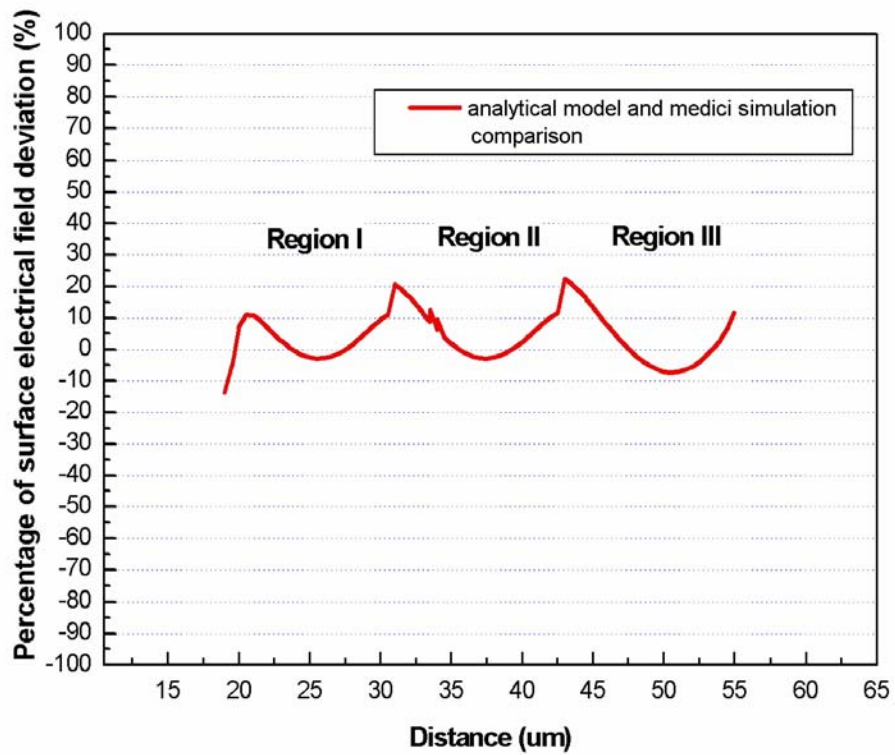


Fig. 3-13. (b) Percentage of the surface electric field deviation as a function of the distance in three frames. Each neighbor frame at their boundary exist a higher error value.

3.4 Summary

A partition method has been developed to model the high-voltage silicon on insulator lateral insulated gate bipolar transistor (SOI-LIGBT) devices by the step doping profile at the first time. The use of partition method is successful to explain the underlying reverse-bias performance, attain 50.7 % improvement of the breakdown voltage compared with the uniform doping, and decrease the undesirable additional masks in the step doping SOI devices. To achieve higher breakdown voltage, the difference between maximum and minimum electric fields must be eliminated in each frame. For this reason, a degraded factor "D" is provided to ensure near ideal-breakdown voltage and the least frame numbers as expected.

The thicker buried oxide and shorter drift length will promote smaller number of frames, especially if the SOI layer thickness is large enough. This makes it possible to reduce production cost. The optimum value of 0.6 is corresponding to the "three frames", which is chosen under economical consideration. The highest impact ionization rate is found at the third (last) frame, where the value "IVert" is about 0.9 while substituting the voltage 660 into the value of "V". The breakdown voltage is over the prediction with only about 8.9 % of the MEDICI simulation value. The ranges of data variation are available from –5 % to 5 % in surface potential part and –20 % to 20 % in surface electric field part.

It can also be implemented in the vertical devices by multi-epitaxy or multi-implanted technology without any additional masks, and superior device characteristics can be achieved as well. This method offer the designers with a choice between the step doping required more mask and the linearly graded doping required precise design and longer thermal process flexibly. Although the electric characteristics

of step doping SOI-LIGBT can also be simulated by the ISE™, TMA™ or SIVALCO™, the simple equation is beneficial for designers to plan the structure architecture by the software of mathematica™ on a cheap personal computer or notebook computer everywhere instead of running the program with the expensive and heavy workstation.

Chapter 4

A LDMOS with Low-Temperature Poly-Si Power Device via Excimer Laser Crystallization at Room Temperature

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A new low-temperature polycrystalline silicon high-voltage LDMOS (LTPS HVLDMOS) using excimer laser crystallization has been proposed for the first time. However, in order to enhance LTPS HVLDMOS characteristics, there are two starting points: 1) integrate the thin film technology with the power device, 2) clarify the requirement of excimer laser treatment for low temperature power devices. As a result, the ON/OFF current ratio after laser treatment is improved over 10^6 times than that before laser treatment at L_{drift}=15-μm and Vds=25 V. The LTPS HVLDMOS after laser treatment also demonstrates the better trade-off between the specific on-resistance and breakdown voltage against the previous HVTFTs by solid phase crystallization—such as semi-insulating (SI), metal-field-plated (MFP), and offset-drain (OD) HVTFTs.

4.1 Poly-Si Grain Growth Technology

4.1.1 Solid Phase Crystallization (SPC)

A remarkable improvement of polysilicon active layers in polysilicon thin film transistors (TFTs) performance is achieved by introduction of solid phase crystallization (SPC) of amorphous silicon (a-Si) films, deposited by low-pressure chemical vapor deposition (LPCVD) [4.1], [4.2]. In fact, typical values of field-effect mobility in optimized SPC n-channel TFTs are reported in the range of 30-40 cm^2/V-s [4.1], [4.2].

The a-Si films, deposited by LPCVD at temperatures below 600 °C from silane, can be converted into polysilicon by prolonged (10-100 hrs) thermal annealing at temperatures between 530-600 °C [4.3]. The SPC takes place by nucleation of crystalline clusters which grow spontaneously when a critical size is reached. The grain size, which depends on both annealing and deposition temperature [4.3], is much larger than direct-deposited polysilicon films in the range from 0.2-μm to 1-μm.

The grain sizes up to 3-5 μm have been obtained by amorphous silicon (a-Si) deposition at 460-480 °C from disilane and annealing of 65 hrs at 580-600 °C [4.4], [4.5]. This is related to the formation of few nuclei in the a-Si so that they can grow larger before impinging on their neighbors. If compared with those for a-Si deposited from silane, a disadvantage of a-Si deposited from disilane by SPC process is represented by the much longer incubation and characteristic crystallization time [4.4]. Furthermore, the microtwins generation allows a fast incorporation of the atoms in the crystal lattice during the SPC process, resulting in a fast reduction of the free energy of the system by creating large and highly twinned grain. This implies that a high density of localized states is expected not only at the grain boundaries but also within the grain. This explains how, even in large grain (up to 5 μm) polysilicon TFTs, the electron field-effect mobility is limited to values of 120 cm^2/V-s [4.6].

4.1.2 Excimer Laser Crystallization (ELC)

Further improvement of the polysilicon TFTs performances has been obtained by introduction of ELC polysilicon acive layers, which lead to electron field mobilities > 100 cm^2/V-s [4.7]-[4.12]. The excimer laser emits in the UV region (wavelengths 193 nm, 248 nm, 308 nm for ArF, KrF and XeCl, respectively) with the short pulse duration (10-30 ns). As the energy density is above some threshold energy, the amorphous layer