undergoes partial melting at the surface of Si-film. It results the structure to consist with two layers: an upper large grained layer (whose thickness is related to the primary melt induced by the laser) and a lower fine-grained layer (related to the explosive crystallization) [4.13].

As the energy is further increased, the Si film will be achieve the maximum grain size, which is almost totally melted and only few unmelted crystalline clusters are sparsely distributed. When this condition occurs, the grains grow laterally around the seeds until they impinge on each other and then grain size in excess of 1-μm can be reached. This particular condition is often referred to as super lateral growth (SLG) [4.14]. The excellent performance in TFTs can be obtained with field-effect mobility in the range of 300-400 cm^2 cm^2/V-s due to a good crystallinity with very few in-grain defects during the melt-regrowth process. [4.15]-[4.16].

However, at excess energy density, the Si film will be completely melted and a small grain structure will be appeared because the substantial undercooling of the liquid occurs before solidification via homogeneous nucleation and growth can take place [4.14]. Additionally, the combination in Si of strong optical absorption of the UV light and small heat diffusion length during the laser pulse (~100 nm) implies that Si surface region can be melted by high temperature but without appreciable damage (< 400 °C) of the substrate. This makes ELC process compatible with glass substrates that is one of the major advantage of this technique.

4.1 Conventional SPC HVTFTs and Novel ELC HVLDMOS

Low-temperature polysilicon high-voltage thin film transistors (LTPS HVTFTs) are widely studied and discussed for liquid crystal displays, field emission displays,

plasma displays, high speed printers, and so on [4.17], [4.18]. In recent years, a variety of HVTFT structures have been proposed in order to carry out the three-dimensional (3-D) circuit integrations and system-on-panel (SOP) applications. They include the offset-drain (OD), lightly-doped-drain (LDD), metal-field-plated (MFP), multi-gate (MG), and semi-insulating (SI) HVTFTs. As shown in Fig. 4-1, Offset-drain (OD) HVTFT has been established as a fundamental structure for high voltage operation in large area applications in 1982 [4.19], [4.20]. The drain region is offset from the channel region to provide high breakdown voltage by reducing the electrical field peaks in high voltage operation. However, the improvement in off state for high blocking capability accompanied with an undesirable high series resistance, which associated with the offset region and caused the degradation in on state performance. In 1988, a

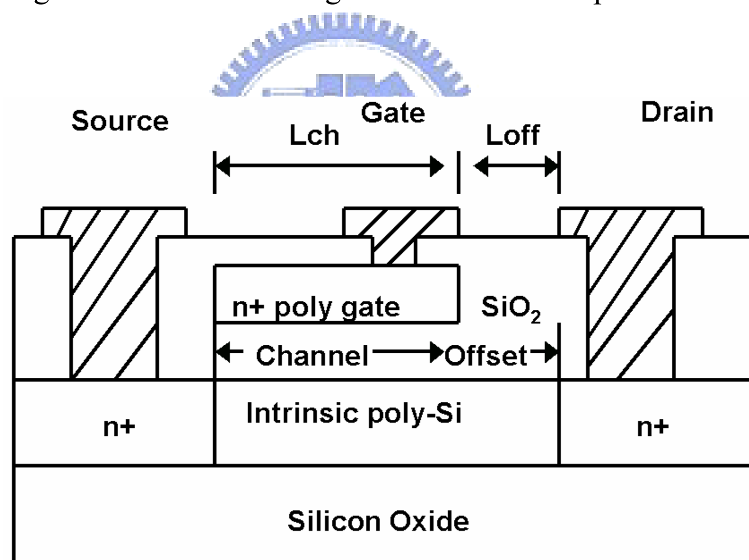


Fig. 4-1. Schematic structure of offset-drain (OD) high-voltage thin film transistor (HVTFT) with a high resistance offset region from drain to source.

lightly doped drain (LDD) HVTFT has been proposed to utilize an ion implantation process in the offset region [4.21], [4.22]. As shown in Fig. 4-2, the lightly dope in offset region can improve the device on state performance due to an increased

conductivity in the offset region. But, the improvement in the on state performance by lightly dope may result in a degradation of the blocking voltage capability.

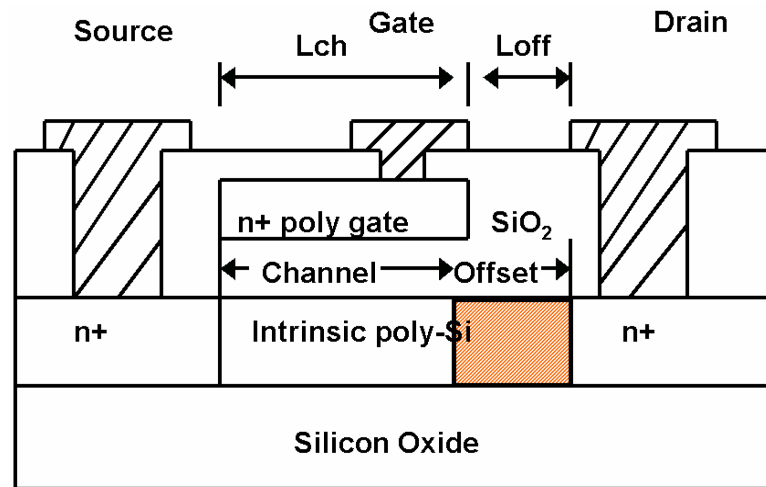


Fig. 4-2. Schematic structure of lightly doped drain (LDD) HVTFT with a lightly doping implantation in the offset region.

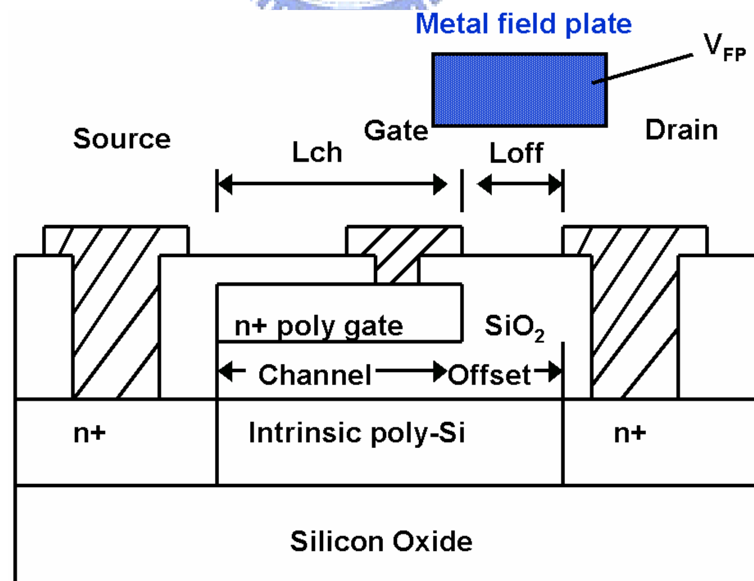


Fig. 4-3. Schematic structure of metal-field-plate (MFP) HVTFT with a metal field plate across the offset region.

In 1990, metal-field-plated (MFP) HVTFT has been developed by implementation of a metal field plate on top of the field oxide [4.23]. As shown in Fig. 4-3, this field plate covers the entire offset region, thus directly modulating the conductivity of the offset region. The major advantage of this structure is that the current pinching phenomenon can be eliminated and much improved the on state characteristics. However, the blocking voltage capability is reduced due to the potential discontinuity on both ends of the field plate, which will induce oxide failure. Moreover, it requires an additional external bias line to supply voltage to the field plate, which may lead to a significant increase in the complexity of display applications. In 1991, multi-gate (MG)

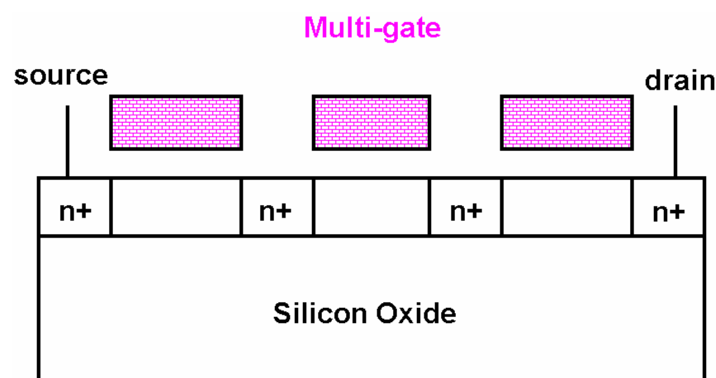


Fig. 4-4. Schematic structure of multi-gate (MG) HVTFT with many gate elements between the drain and source region.

HVTFT has been demonstrated with combination of several small TFTs in a device [4.24]. By this structure in Fig. 4-4, the drain voltage is divided equally across each elemental TFT thereby lowering the operation voltage in each element to cause large increase of breakdown voltage. However, it requires a large number of TFT elements to handle high voltage and thereby the parasitics from each elemental TFT are cumulative. Moreover, it also has the reliability problem as the high electric field is across the thin

gate dielectric.

In 1997, Semi-insulating (SI) HVTFT has been proposed with semi insulating field plate in lieu of metal field plate, which covers the entire offset region and connects the drain to the gate in Fig. 4-5 [4.25]. In the on state, the potential difference between the semi insulator and the underlying intrinsic polysilicon extends the electron accumulation layer under the gate into the offset region there by improving the on state performance. In the off state, the semi insulator acts to smooth the potential distribution across the entire offset region thereby reducing the field peaks near the gate and drain which are responsible for premature breakdown. However, such structure is susceptible to misalignment and the deposition of a semi insulator layer directly on silicon often induces surface contamination leading to large leakage currents and poor reproducibility. Moreover, the use of a semi insulator layer will decrease the switching speed due to the extra resistance-capacitance charging path.

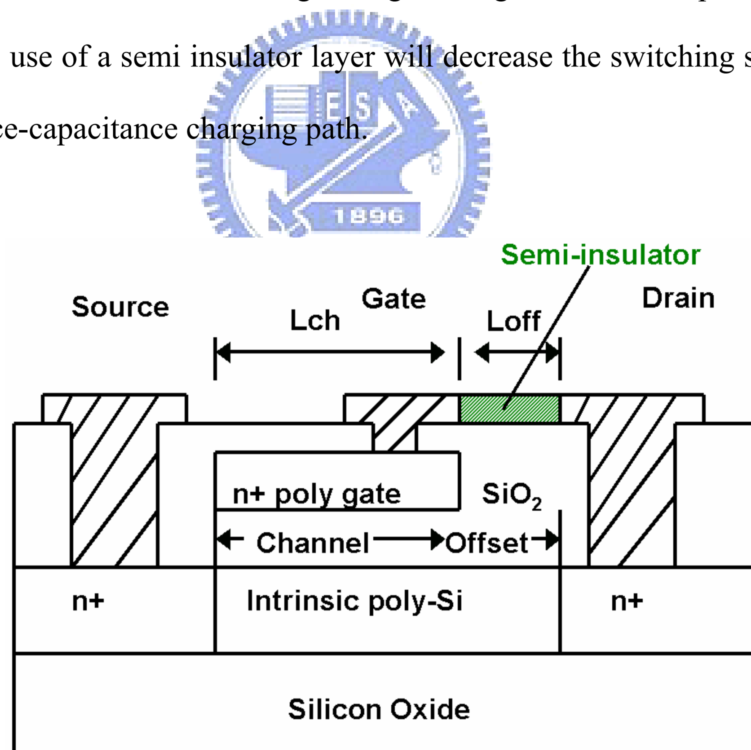
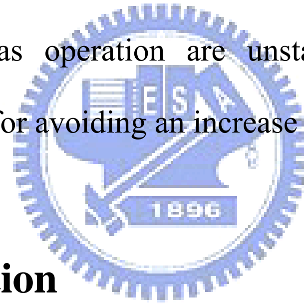


Fig. 4-5. Schematic structure of semi-insulating (SI) HVTFT with connect of semi insulating field plate from drain to gate electrode over the offset region.

Although these devices provide the high blocking or current capability, most of them are not easy or effective to apply in the glass-compatible electronic systems. In this study, the low-temperature polysilicon high-voltage lateral double diffused MOS (LTPS HVLDMOS) has been demonstrated by combining the technology of thin film transistor into the power device at the first time. The power structure will led the LTPS HVLDMOS to possess the superior blocking capability from the reduced-surface-field (RESURF)—including of drift region (offset region), Pwell doping, field oxide, extended gate, and extended drain designs—against the previous HVTFTs with offset region only [4.26]. On the other hand, in order to obtain the high performance LTPS HVLDMOS, the influence and necessity of excimer laser crystallization for improving its current capability will be estimated as the following. Furthermore, since the hydrogen bonds under bias operation are unstable [4.27], the hydrogenation is temporarily not considered for avoiding an increase of issue complexity.



4.2 Device Fabrication

The key processes for fabricating high-performance LTPS HVLDMOS were illustrated by the sequence of Figs. 4-6 (a), (b), (c) and (d). At first, a 1.5-μm-thick wet oxide was grown on a (100) silicon wafer to be as a glass base. A 1000-Å-thick amorphous silicon (a-Si) was deposited on it with the pure silane (SiH_4) source by LPCVD at 550 °C to become the device layer in Fig. 4-6 (a). Secondly, the a-Si drift region was implanted with 50 KeV phosphorous dose of 7×10^{11} cm^{-2} to reduce the current path resistance. P-type well with 60 KeV boron dose of 3×10^{13} cm^{-2} was created to increase the depletion width in high doping N-type drift region ($N_pW_p=N_nW_n$). Then, the 1000-Å-thick a-Si was crystallized using KrF excimer pulse

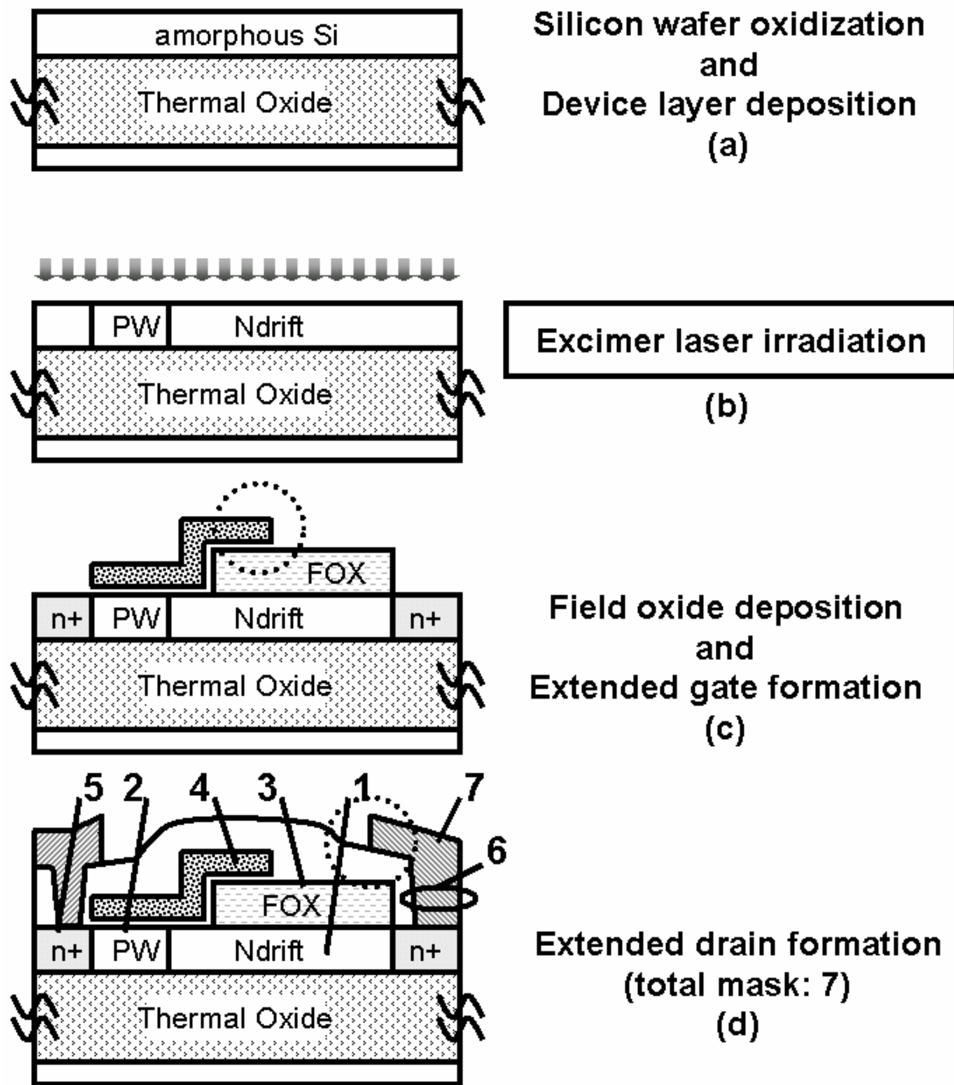


Fig. 4-6. Key processes for fabricating the high performance LTPS HVLDMOS using excimer laser crystallization in the sequence of (a), (b), (c) and (d).

laser (λ=248-nm) with an energy density of 470 mJ/cm^2 and a shot density of 100 per area at room temperature in Fig. 4-6 (b). Thirdly, a 5000-Å-thick field oxide (FOX) was formed by plasma enhanced chemical vapor deposition (PECVD) at 350 °C to reduce the surface electric field (RESURF) from gate and drain edges in the drift region. A 1000-Å-thick gate oxide was deposited by PECVD at 350 °C and a 2000-Å-thick a-Si gate electrode was deposited by LPCVD at 550 °C. The a-Si gate electrode was defined

across the FOX to split the Pwell/Ndrift junction electrical field. High dosage phosphorous and boron implantation were carried out to form n+ drain, source, gate and p+ butting regions in Fig. 4-6 (c). Finally, a 5000-Å-thick PECVD passive oxide was deposited and then all dopants were activated by furnace annealing at 600°C for 12 hrs without hydrogenation. A 5000-Å-thick aluminum was defined overlap the passive oxide and the extended metal drain was functioned to split the Ndrift/n+ drain junction electrical field in Fig. 4-6 (d). Moreover, the LTPS HVLDMOS except the laser treatment was also fabricated with the same conditions for comparison.

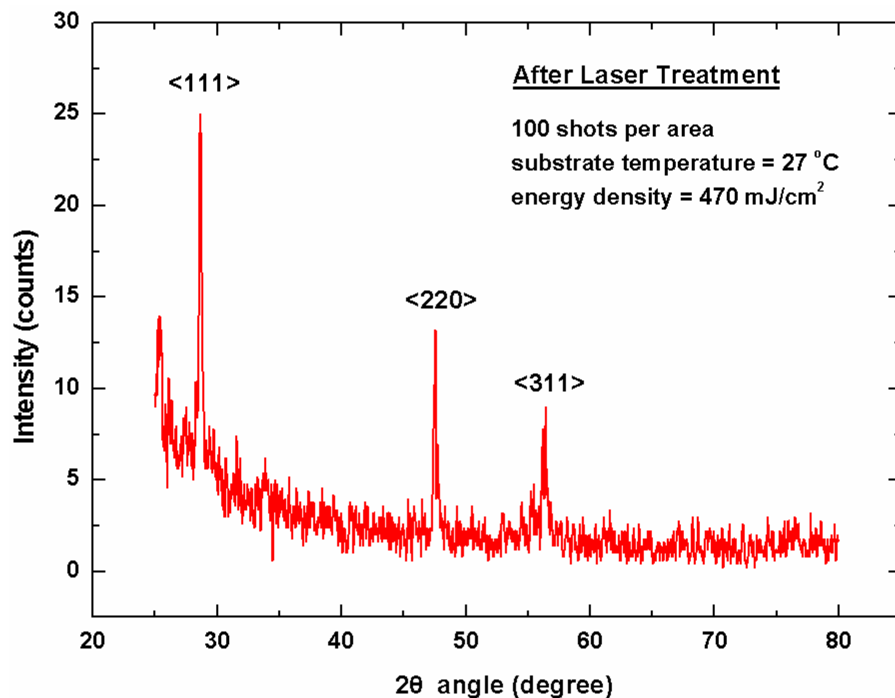


Fig. 4-7. X-ray diffraction spectra of polycrystalline silicon film crystallized by excimer laser annealing with an energy density of 470 mJ/cm^2 and a shot density of 100 per area at room temperature.

4.3 Results and Discussion

4.4.1 X-Ray Diffraction and SEM Photography

To investigate the mechanism of grain growth phenomenon, the poly-Si films after excimer laser treatment were evaluated by x-ray diffraction spectra. According to C. V. Thompson *et al.* experimental results [4.28]-[4.31], the grain growth in thin films is affected by anisotropy of the surface free energy. As shown in Fig. 4-7, it is known that the (111) peak intensity is the trend of minimum surface free energy and the (100) texture is the minimum Si/SiO_2 interface energy. In other words, it also could be thought that the magnitude of the free surface energy is larger than the magnitude of the Si/SiO_2 interface energy. The (111) peak intensity would be radically increased and the (220) peak simultaneously disappeared as the number of laser shots was increased. Figure 4-8 (a) and (b) showed the scanning electron microscopy (SEM) images of secco-etched poly-Si films after different laser energy fluence treatment. The films produced had a maximum grain size of 3-μm with strong (111) crystallographic orientation and a mono-modally distributed grain size of 1.5-μm, on average. The surface morphology of these films was very smooth and the crystallinity was excellent with minimal interface defects. The resulting of thin poly-Si film could be further improved with decreasing the film thickness, increasing the substrate temperature, increasing the average surface energy anisotropy, and increasing the average grain boundary mobility—such doping with phosphorus or arsenic in the n-drift region (offset region).

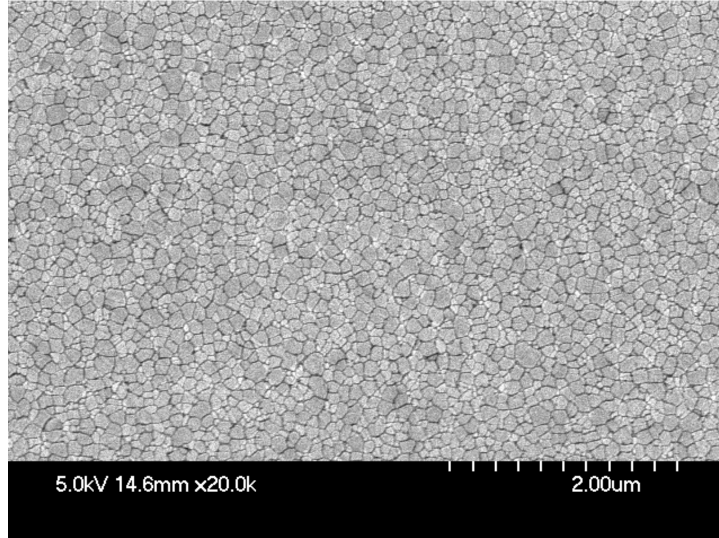


Fig. 4-8. (a) Scanning electron microscopy (SEM) image of Secco-etched poly-Si film crystallized in the partial melting regime by a low energy density of 435 mJ/cm^2 and a shot density of 100 per area at room temperature.

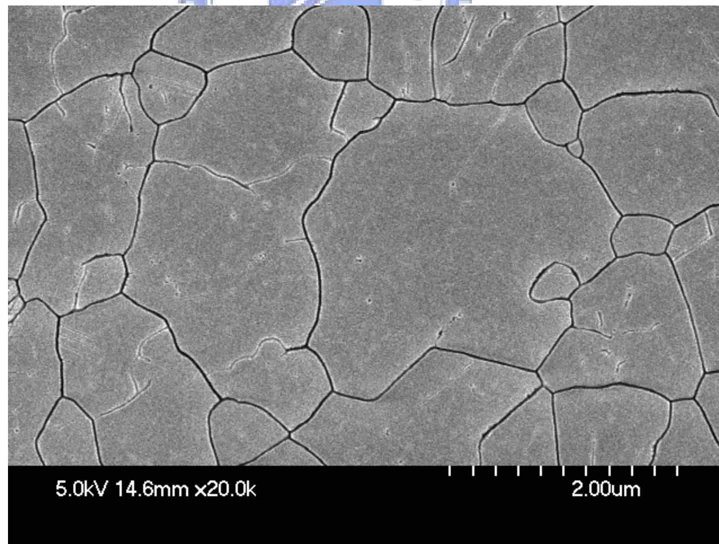


Fig. 4-8. (b) Scanning electron microscopy (SEM) image of Secco-etched poly-Si film crystallized in the super lateral growth (SLG) regime by a high energy density of 458 mJ/cm$_2$ and a shot density of 100 per area at room temperature.

4.4.2 Transfer Characteristics before/after Excimer Laser Treatments for LTPS HVLDMOS

Figure 4-9 and Table 4-1 showed the gate transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS. The device dimensions and doping concentration were listed: W=600-μm; L_{ch}=12-μm; L_{drift}=15-μm; N_{drift}=7 × 10^{11} cm^{-2}; t_{si}=0.1-μm; t_{oxide}=1.5-μm. For the conventional low voltage TFT, the I_{OFF} current would be increased as negative gate and positive drain voltage increased. This phenomenon, called anomalous leakage current, was generated via grain boundary traps by the field emission [4.32]. However, for the LTPS HVLDMOS, the negative gate bias current was almost constant regardless of the drain voltage increase even up to Vds=25 V. The reason was that the extended gate and drift region design could effectively reduce the Pwell/Ndrift junction electric field [4.33]. The threshold voltage after/before laser treatment was not changed at 4 volts due to the similar well concentrations, which replaced the channel defects domination in the intrinsic well region. The subthreshold swing (SS), depended on the number of the deep state [4.34], was significant improved from 16.15 V/decade to 1.36 V/decade after laser treatment. The ON/OFF current ratios (I_{ON}/I_{OFF}) after laser treatment showed the excellent promotion with the magnitudes of 3.73 × 10^5 and 2.37 × 10^6 against the magnitudes of 1.71 and 1.93 before laser treatment at Vds=5 V and Vds=25 V. Additionally, it was worth to mention that there was a valley near the gate bias of 0 V as the LTPS HVLDMOS after laser treatment biased at Vds=5 V but at Vds=25 V the phenomenon was not appeared. It was because the leakage current was generated less at enough low drain bias (0.1 Vì Vdsì 5 V) and limited by the drift region (offset region) even at Vds=-30 V. However, as the drain bias was large (10 Vì Vdsì 25 V), the leakage current was directly up to high value so that the valley will not appear.

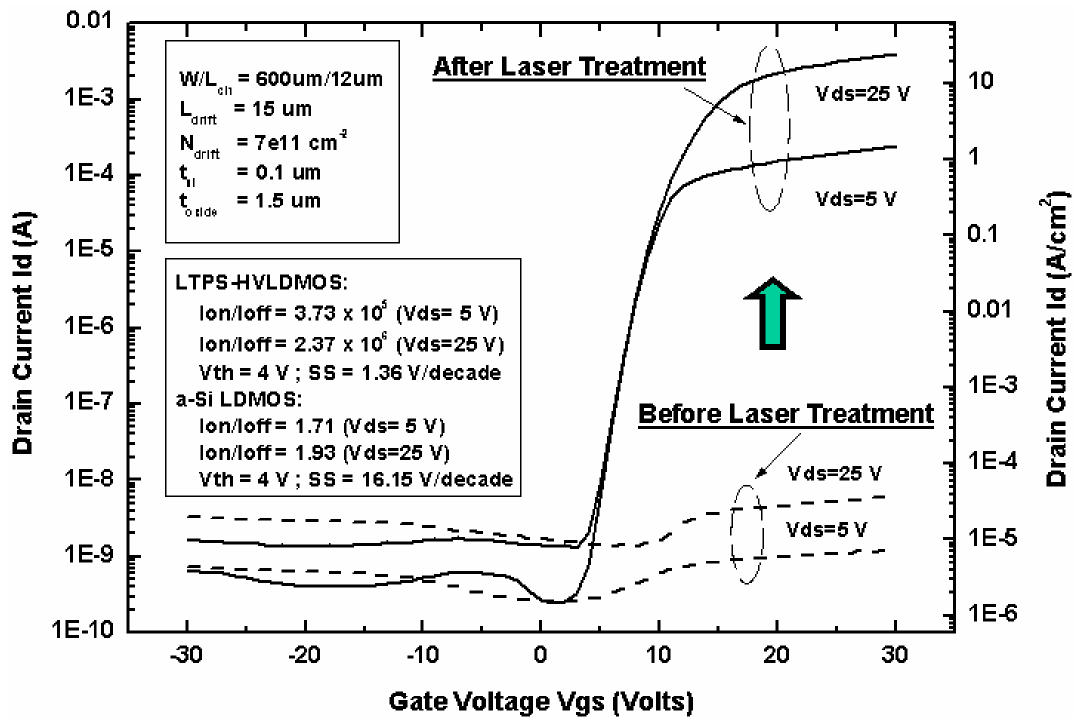


Fig. 4-9. Transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS with W/L_{ch}=600-μm/12-μm and L_{drift}=15-μm.

Table 4-1. Summary of the transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS with optimal room temperature irradiation.

	Before laser treatment	After laser treatment
Threshold Voltage (V)	4	4
Subthreshold Swing (V/dec)	16.15	1.36
Max. I_{ON}/I_{OFF} at Vds=5 V	1.71	3.73×10^5
Max. I_{ON}/I_{OFF} at Vds=25 V	1.93	2.37×10^6
Breakdown Voltage (V)	285	240

4.4.3 Relationship between ON/OFF Current Ratio and Drift Length before/after Excimer Laser Treatments for LTPS HVLDMOS

Figure 4-10 (a) and (b) showed the relationship of ON/OFF current ratios and drift length before and after excimer laser treatments for LTPS HVLDMOS at drain bias of 5-V and 25-V, respectively. The observed drift lengths (L_{drift}) of LTPS HVLDMOS were varied from 15-μm to 40-μm with a step of 5-μm. The on-state current (I_{ON}) and off-state current (I_{OFF}) of ON/OFF current ratio were defined at the gate biases of 30-V and –30-V, respectively. While the drain voltage was biased at small value of 5-V in figure 4-10 (a), the ON/OFF current ratios of LTPS HVLDMOS after excimer laser treatment

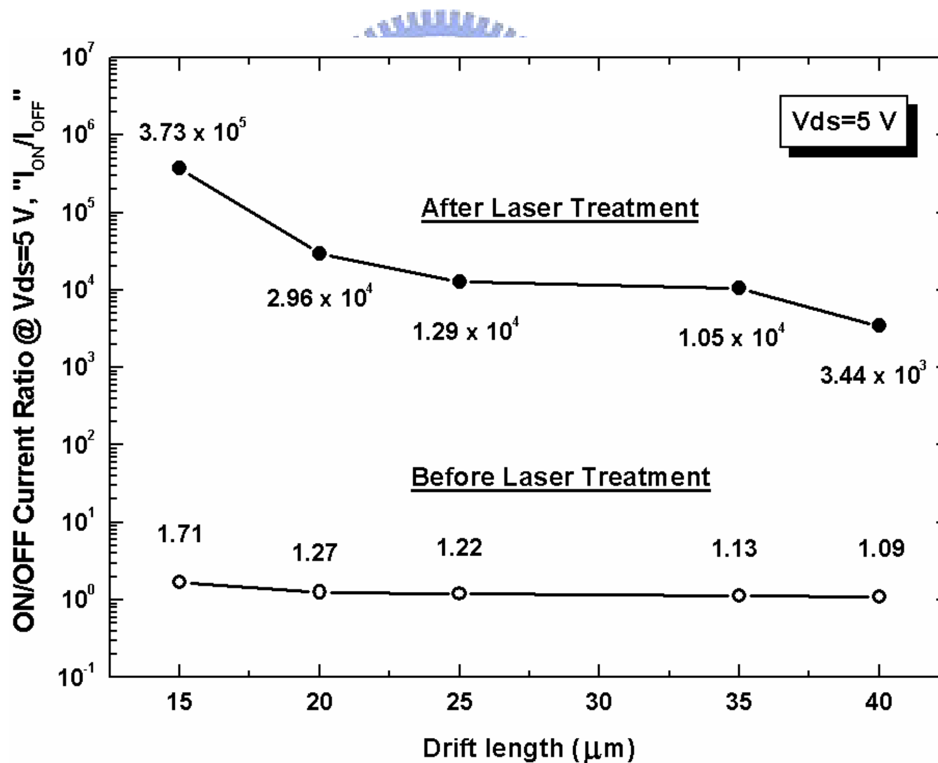


Fig. 4-10. (a) Relationship between ON/OFF current ratio and drift length before and after excimer laser treatments for LTPS HVLDMOS at the drain bias of 5-V.

were abruptly decayed about 29 times from 3.73×10^5 to 1.29×10^4 as the drift length variation from 15-μm to 25-μm. The ON/OFF current ratios of LTPS HVLDMOS before excimer laser treatment were also decayed abruptly about 1.4 times from 1.71 to 1.22 as the drift length variation from 15-μm to 25-μm but the decayed degree was much smaller than that after excimer laser treatment. As the drift length was extended from 25-μm to 35-μm, the decrease in ON/OFF current ratios was slow down and almost not changed regardless of the LTPS HVLDMOS after/before excimer laser treatment. After the drift length is over 35-μm, the ON/OFF current ratios of LTPS HVLDMOS after excimer laser treatment started to decay about 3 times from 1.05×10^4 to 3.44×10^4 but that before excimer laser treatment was still almost not changed.

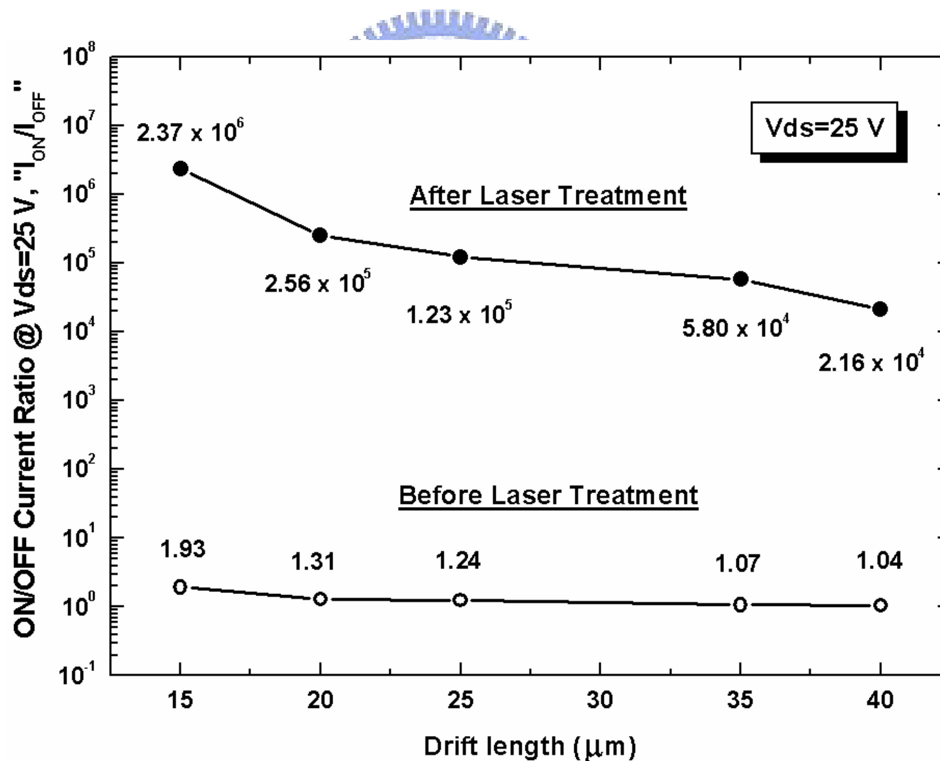


Fig. 4-10. (b) Relationship between ON/OFF current ratio and drift length before and after excimer laser treatments for LTPS HVLDMOS at the drain bias of 25-V.

While the drain voltage was biased at large value of 25-V in figure 4-10 (b), the ON/OFF current ratios of LTPS HVLDMOS after excimer laser treatment were abruptly decayed with the smaller magnitude of 19 times from 2.37×10^6 to 1.23×10^5 as the drift length variation from 15-μm to 25-μm. The ON/OFF current ratios of LTPS HVLDMOS before excimer laser irradiation was also decayed abruptly with smaller variation of 1.55 times from 1.93 to 1.24 compared to that at drain bias of 5-V. From the drift length extension of 25-μm to 35-μm, the decrease in ON/OFF current ratios was still slow down and almost not changed regardless of the drain bias of 5-V or 25-V after/before excimer laser treatment. After the drift length is over 35-μm, the ON/OFF current ratios of LTPS HVLDMOS after excimer laser treatment started to decay about smaller 2.68 times from 5.80×10^4 to 2.69×10^4 but that before excimer laser treatment was still almost not changed. The ON/OFF current ratios variation at drain bias of 25-V was smaller than that at drain bias of 5-V so that the variations could be suppressed by higher drain voltage as the drift length extension.

Above the mentioned results, the ON/OFF current ratios and its variations before excimer laser treatment were entirely much smaller than those after excimer laser treatment as the increase in the drift length. It was because the low quality poly-Si film before excimer laser treatment was dominated the whole resistance with large trapping defect density which resulting in a huge specific on-resistance of $1.02 \times 10^6\ \Omega\text{-cm}^2$ at drift length of 15-μm in the LTPS HVLDMOS. Thus, even if the drift length was extension about 3 times from 15-μm to 40-μm, the drift length extension with several times deviation was still finite. All gate transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS from the drift length of 20-μm to 40-μm were showed in Fig. 4-11~Fig. 4-14.

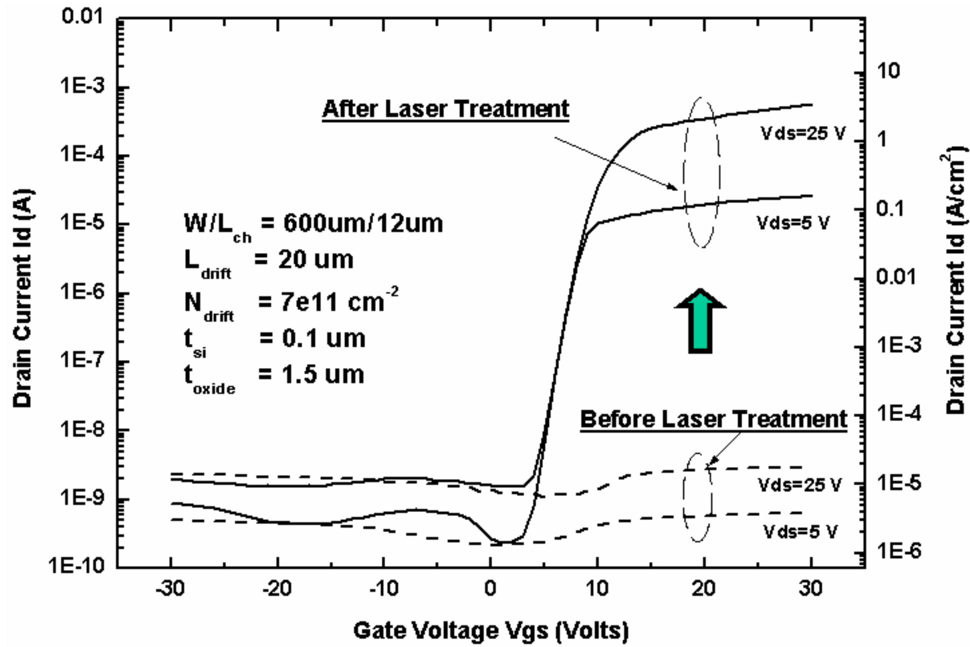


Fig. 4-11. Transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS with W/L_{ch}=600-μm/ 12-μm and L_{drift}=20-μm.

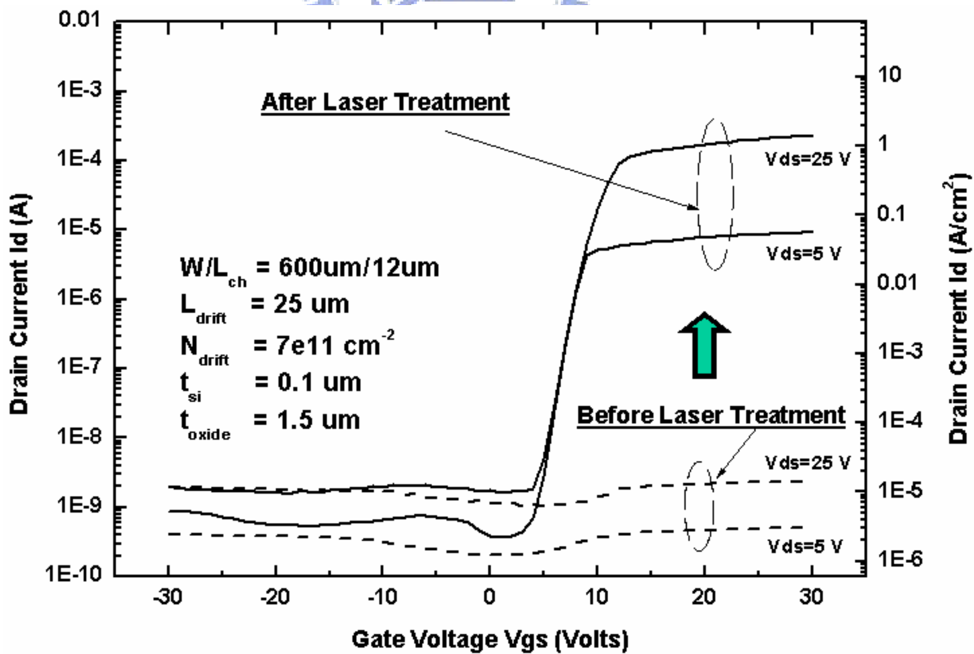


Fig. 4-12. Transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS with W/L_{ch}=600-μm/12-μm and L_{drift}=25-μm.

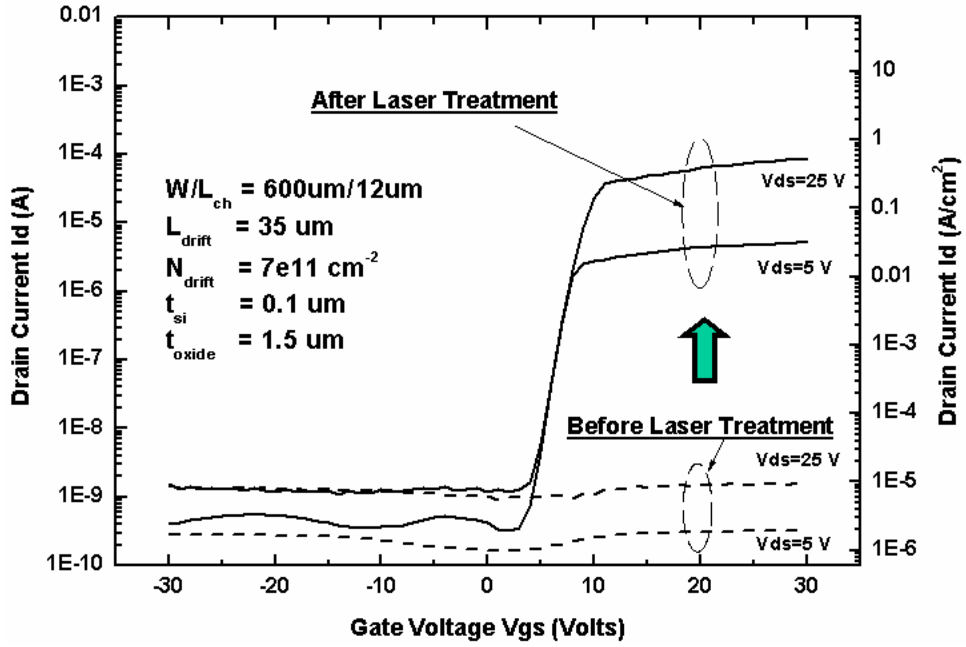


Fig. 4-13. Transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS with W/L_{ch}=600-μm/12-μm and L_{drift}=35-μm.

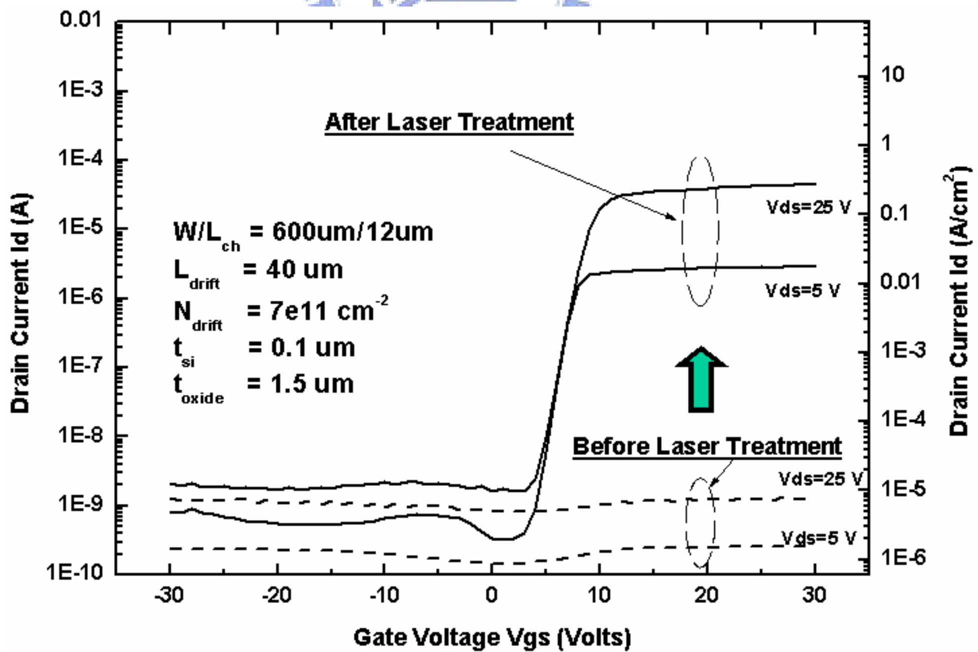


Fig. 4-14. Transfer characteristics before and after excimer laser treatments for LTPS HVLDMOS with W/L_{ch}=600-μm/12-μm and L_{drift}=40-μm.

4.4.4 Output Characteristics before/after Excimer Laser Treatments for LTPS HVLDMOS

There are three distinct features of output characteristics, which are deliberately emphasized in laser annealed poly-Si devices. Firstly, at low gate voltage, the soft breakdown at high drain voltage is evidence of a floating substrate effect. Secondly, a moderate gate voltage, the output drain current does not saturate. This lack of saturation is directly attributable to modulation of the potential barrier at grain boundaries [4.44]. Thirdly, as the gate voltage is further increased, the output drain current does not tend to

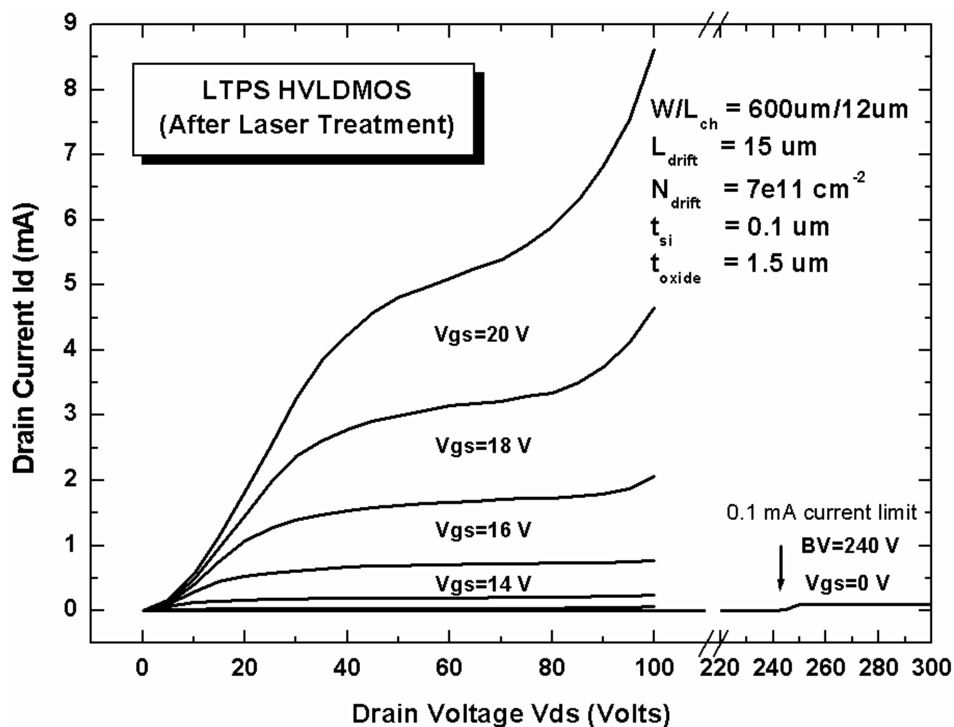


Fig. 4-15. (a) Output characteristics after excimer laser treatments with the linear scale drain current for LTPS HVLDMOS with W/L_{ch}=600-μm/12-μm and L_{drift}=15-μm. The breakdown voltage was measured by the protective current limit of 0.1 mA.

saturate and eventually the output conductance become negative. The negative output conductance does not occur in bulk silicon transistors. However, it has been observed in thin film transistors, attributed to self-heating, due to its low thermal conductivity of the insulating substrate [4.45], [4.46]. It is particularly apparent in short channel SOI devices at relatively high output power levels because of the high mobilities which can arise due to laser annealing.

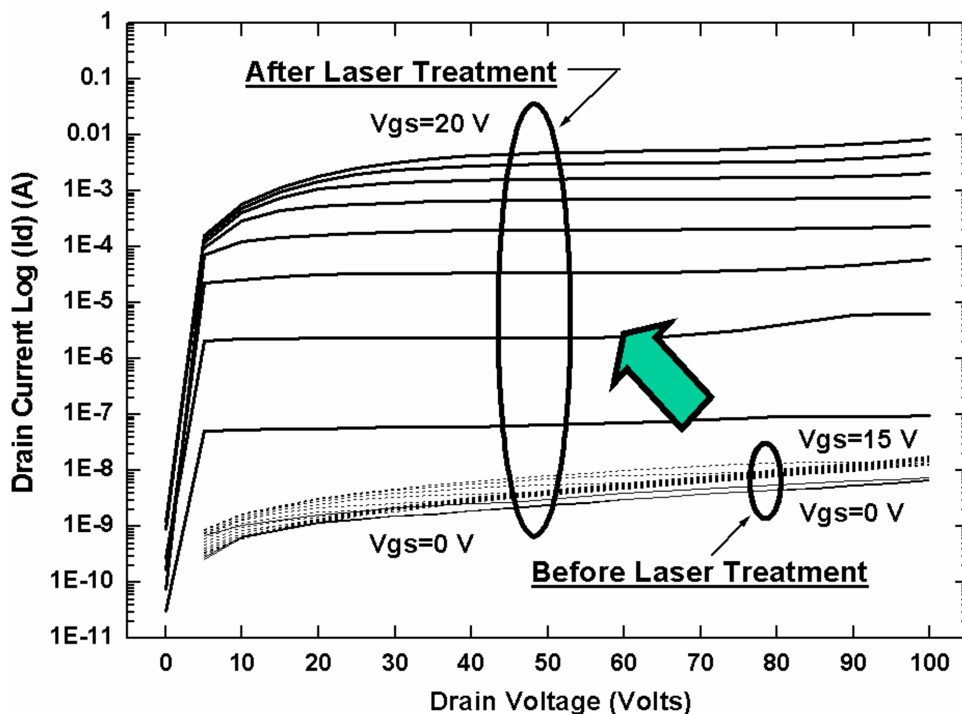


Fig. 4-15. (b) Output characteristics before and after excimer laser treatments with the logarithm scale for LTPS HVLDMOS with W/L_{ch}=600-μm/12-μm and L_{drift}=15-μm.

Figure 4-15 (a) and (b) showed the drain output characteristics before and after excimer laser treatments by the linear and logarithm scales for LTPS HVLDMOS. The logarithm scale block diagram, for observing small drain current, displayed that the current capability was greatly increased from 10^{-9} to 10^{-3} ampere after laser treatment. The safe-operating-area (SOA) was also enhanced with the low specific on-resistance

and large maximum voltage limit (Breakdown voltage) of 1.78 Ω-cm^2 (|Vgs-Vth|=15 V, Vds=20 V) and 240-V, respectively. The maximum power limit, which was mostly defined on the set of snapback boundary, was great in 0.41 Watts (1305 W/cm^2) at Vgs=20 V and Vds=75 V. The latch-up voltage of parasitic bipolar could be suppressed up to 95 V drain voltage with high level saturation drain current of 1.5 mA at Vgs=16 V. In summary, the current driving capability of LTPS HVLDMOS after laser treatment exhibited the superior characteristics in the subthreshold swing, I_{ON}/I_{OFF} ratio, SOA, on-state resistance, maximum power limit, and latch-up voltage than that before laser treatment.

4.4.5 Comparison of LTPS HVLDMOS before/after Laser Treatments together with Conventional OD, MFP, and SI HVTFTs

Figure 4-16 showed the relationships of the specific on-resistance and breakdown voltage for LTPS HVLDMOS before/after laser treatments together with OD, MFP, and SI HVTFTs. The specific on-resistances of the above structures were all defined at the |Vgs-Vth|=15 V and Vds=20 V. The breakdown voltage was defined as a drain current of 1 nA/μm channel width at a gate voltage of 0 V. The drift lengths (L_{drift}) of LTPS HVLDMOS after laser treatment were varied from 15-μm to 35-μm with a step of 5-μm. The equation of specific on-resistance could be written as

$$R_{on,sp} = [V/I] \times [W \times (L_{ch} + L_{drift})] \qquad \text{(Eq 4-1)}$$

the symbol "V" and "I" were the drain voltage of 20-V and its corresponding current at |Vgs-Vth|=15 V. The symbol "W", "L_{ch}", and "L_{drift}" indicated the device width, channel length, and drift length in the proposed HVLDMOS. As expected, the specific on -resistance of 29 Ω-cm^2 at 300-V (L_{drift}=25-μm) after laser treatment was lower about

10^5 times than that of 1.9 × 10^6 Ω-cm^2 at 315-V (L_{drift}=20-μm) before laser treatment. The un-optimized LTPS HVLDMOS after laser treatment showed the better characteristics with 1.78 Ω-cm^2 at 240-V (L_{drift}=15-μm) compared to the SI HVTFT with 3.5 Ω-cm^2 at 230-V, MFP HVTFT with 1.17 Ω-cm^2 at 125-V, and OD HVTFT with 10 Ω-cm^2 at 115-V under solid phase crystallization (SPC) and 4~12 hrs hydrogenation [4.47], [4.48]. It was because the depletion width of the previous HVTFTs needed to firstly compensate its many grain boundary trap states and then extended to support the blocking voltage [4.49]. However, by laser treatment and the RESURF designs in LTPS

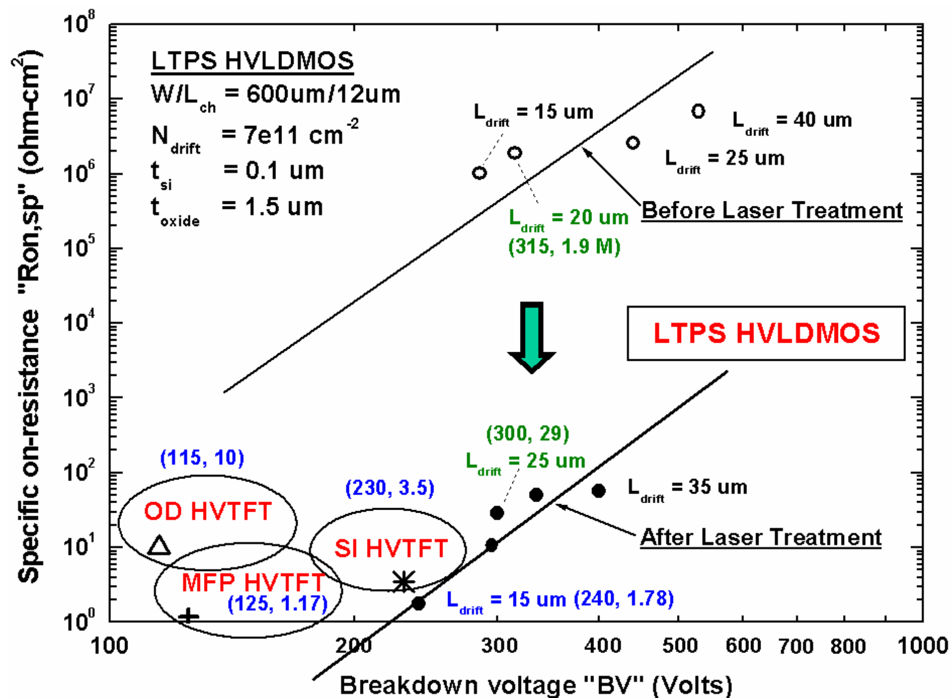


Fig. 4-16. Relationships of the specific on-resistance and breakdown voltage in the LTPS HVLDMOS before/after laser treatments against the previous OD, MFP, and SI HVTFTs. The (x, y) represented the coordinates in X-axis and Y-axis, which meant the values of breakdown voltage and specific on-resistance, respectively.

HVLDMOS, the grains could be grown relatively large with less in-grain defects from the molten phase and then the polysilicon depletion width could be effectively increased even in the high doping (~10^{17} cm^{-3}) drift region [4.26], [4.50].

4.5 Summary

The high-performance LTPS HVLDMOS is successfully fabricated using the excimer laser crystallization process. The films produced have a maximum grain size of 3-μm with strong (111) crystallographic orientation and a mono-modally distributed grain size of 1.5-μm, on average. The threshold voltage after/before laser treatment is not changed at 4 volts due to the similar well concentrations, which replaced the channel defects domination in the intrinsic well region. The subthreshold swing (SS) is significant improved from 16.15 V/decade to 1.36 V/decade after laser treatment. The ON/OFF current ratios (I_{ON}/I_{OFF}) after laser treatment show the excellent promotion with the magnitudes of 3.73×10^5 and 2.37×10^6 against the magnitudes of 1.71 and 1.93 before laser treatment at Vds=5 V and Vds=25 V. The ON/OFF current ratios and its variations before excimer laser treatment are entirely much smaller than those after excimer laser treatment as the increase in the drift length.

The ON/OFF current ratios variation at drain bias of 25-V is smaller than that at drain bias of 5-V so that the variations can be suppressed by higher drain voltage as the drift length extension. The current driving capability of LTPS HVLDMOS after laser treatment exhibits the superior characteristics in the subthreshold swing, I_{ON}/I_{OFF} ratio, SOA, on-state resistance, maximum power limit, and latch-up voltage than that before laser treatment. The specific on-resistance of 29 Ω-cm^2 at 300-V (L_{drift}=25-μm) after laser treatment is lower about 10^5 times than that of 1.9×10^6 Ω-cm^2 at 315-V

(L_{drift}=20-μm) before laser treatment.

The LTPS HVLDMOS after laser treatment shows the better characteristics with 1.78 Ω-cm^2 at 240-V (L_{drift}=15-μm) compared to the SI HVTFT with 3.5 Ω-cm^2 at 230-V, MFP HVTFT with 1.17 Ω-cm^2 at 125-V, and OD HVTFT with 10 Ω-cm^2 at 115-V. It possesses the superior current capability and blocking capability by the combination technology of power devices and thin film transistors. It is also verified that the eximer laser crystallization is very important to obtain the extreme current capability against the previous HVTFT structures. The LTPS HVLDMOS after laser treatment is attractive for the future 3-D circuit integrations and SOP applications.

Chapter 5

LDMOS Devices of Low-Temperature Polycrystalline -Silicon Crystallized at 400 °C Substrate Heating

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Low-temperature poly-Si lateral double diffused metal oxide semiconductor (LTPS LDMOS) with high voltage and very low on-resistance has been achieved using excimer laser crystallization at 400 °C substrate heating for the first time. The ON/OFF current ratios were exhibited with 2.96×10^5 and 6.72×10^6 while operating at Vds=0.1 V and 10 V, respectively. The maximum $R_{DS,ON}$ current limit was up to 10 mA and maximum power limit could be enhanced over 1 Watt at Vds=90 V and Vgs=20 V. The Ron,sp with dimensions of W/L_{ch}=600-μm/12-μm could be significantly decreased 6.67×10^2 times in the magnitude as compared with the conventional offset drain (OD) TFTs.

5.1 Advanced LTPS LDMOS for 400 °C Irradiation

Low-temperature poly-Si high-voltage thin-film-transistors (LTPS HVTFTs) have been widely studied in order to realize the glass compatible driver circuits for light valves, high speed printers, liquid crystal displays, plasma displays, and so on [5.1]-[5.2]. High voltage thin film transistors (HVTFTs) differ from low voltage devices in that the drain is offset with respect to the gate edge. This offset drain (OD) structure reduces the electric field peaks associated with high voltage operation thereby increasing the breakdown voltage and reducing the off state leakage [5.3]. In the

absence of the offset region, most of the applied drain voltage appears across the gate oxide lead to a large electric field in the oxide region, and a correspondingly large filed in the silicon active layer underneath the gate electrode. The impact ionization charge can be generated in the heavily doped n+ region, but the offset region can be depleted much more significantly to support larger this voltage. So the breakdown voltage with offset region can be sustained by the impact generation in the silicon active layer just beyond the heavily doped n+ drain region. Nevertheless, these improvements are accompanied by degradation in the device on state performance due to the series resistance of the offset region.

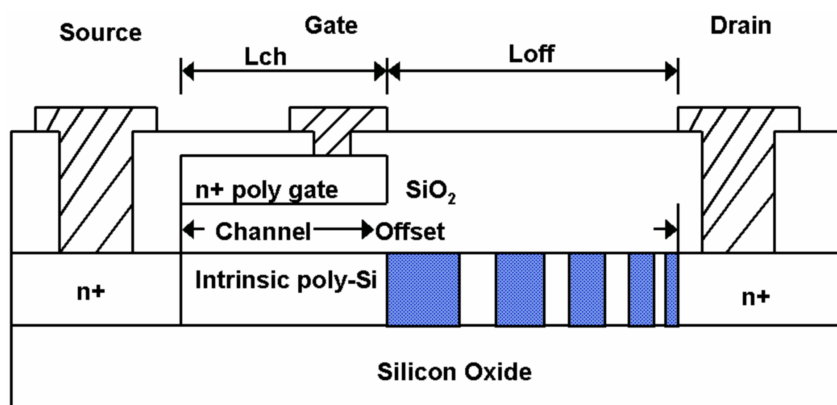


Fig. 5-1. Schematic structure of various doping slit (VDS) thin film transistor (TFT) with a continuous shallow doping profile in the offset region.

As shown in Fig. 5-1, variable doping slots (VDS) TFT is proposed in 2002 and similar to the OD TFT except that an undoped intrinsic polysilicon offset region is replaced by a set of variable doping slots [5.4]. In this structure, the on state resistance is reduced, while alleviating the stringent requirement to dopant control in the OD TFT. Different doping levels between the slots and the intrinsic polysilicon will split the potential drop across the offset region, thereby avoiding the electric field crowding and

improving the trade off between the on state performance and the blocking capability. However, the previous works still exist a lot of issues—such as on-state degradation, gate dielectric reliability, circuit/operation complexity, and surface contamination—resulting in the unsuitable implementation of the integration electronic systems for future system-on-a-panel (SOP) applications.

In this letter, the LTPS LDMOS using excimer laser crystallization has been demonstrated by combination of the thin film transistor (excimer laser crystallization) and power device technologies (LDMOS architecture) for the first time. The excimer laser crystallization (ELC) is the promising technology to obtain the high current capability due to the large grains, less defects, and compatible glass substrate against the solid phase crystallization (SPC) of HVTFTs [5.5]. The LDMOS architecture is the promising design to obtain high blocking capability due to the reduced-surface-field (RESURF) against the only offset drain (drift) region of HVTFTs [5.6]. Hence, the LTPS LDMOS at room temperature irradiation can exhibit the better characteristics than the conventional HVTFTs. Moreover, the LTPS LDMOS at 400 °C irradiation can further present the close performance like the single crystalline silicon (c-Si) LDMOS.

5.2 Experiments

Poly-Si devices have been attracted much attention in the field of large-electronics. Of the various approaches available, excimer laser annealing is a very promising technique for large-scale fabrication of high-performance poly-Si device on glass substrate with high throughput because of the large beam size and high beam energy. In addition, since the absorption coefficient of amorphous silicon (a-Si) is quite high in the UV-light region of the excimer laser, it is possible to recrystallize a-Si film without

thermal damage to the glass substrates. However, a rather serious problem is that poly-Si films obtained by this technique have a small grain size outside the super lateral growth regime [5.7]-[5.9]. This is because solidification velocity during excimer laser annealing is extremely fast—i.e. the duration is in the order of nano seconds [5.10]. Therefore, in order to further enhance the current driving capability, the solidification velocity of molten Si must be controlled by three factors: laser pulse width, energy density, and substrate temperature during excimer laser annealing. However, the substrate temperature is the most effective among the three factors. Low temperature (ò 400 °C) substrate heating during excimer laser annealing is effective for controlling the solidification velocity of molten-Si without thermal damage to the glass substrate. But, in the case of substrate heating over 400 °C, the reduction of solidification velocity will not be continued but tend to result in saturation [5.11].

The fundamental structure of LTPS LDMOS under room temperature (RT) or 400°C irradiation was shown with the labels of RESURF design from “A” to “E” in Fig. 5-2. The conventional offset drain (OD) TFT structure was also exhibited for comparison. At first, a 1.5-μm-thick wet oxide was grown on a silicon wafer. Then, an amorphous-silicon (a-Si) of 0.1-μm thickness was deposited on it by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Next, as shown in label “A”, the 50 KeV phosphorous dose of 7×10^{11} cm^{-2} was implanted into the above a-Si drift region to reduce the current path resistance. However, the conventional OD TFT was lack of this drift implantation so as to possess the large on-resistance with its intrinsic region. At label “B”, the high energy of 60 KeV boron dose of 3×10^{13} cm^{-2} was created as the buried P-well region to increase the depletion width in the N-drift region without adding the threshold voltage. The laser crystallization was performed using KrF excimer laser (λ=248 nm) with the energy densities from 400 to 470 mJ/cm^2 and 99 % overlapped shot density at room temperature or 400 °C substrate heating. However, the

conventional OD TFT was crystallized by furnace at 600 °C so as to possess the small grain sizes in its intrinsic region. After that, a 5000-Å-thick field oxide (FOX) at label "C" was formed by plasma enhanced chemical vapor deposition (PECVD) at 350 °C to reduce the surface electric field (RESURF). A 1000-Å-thick PECVD gate oxide and a 2000-Å-thick LPCVD a-Si gate were defined across the FOX to split the P-well/N-drift

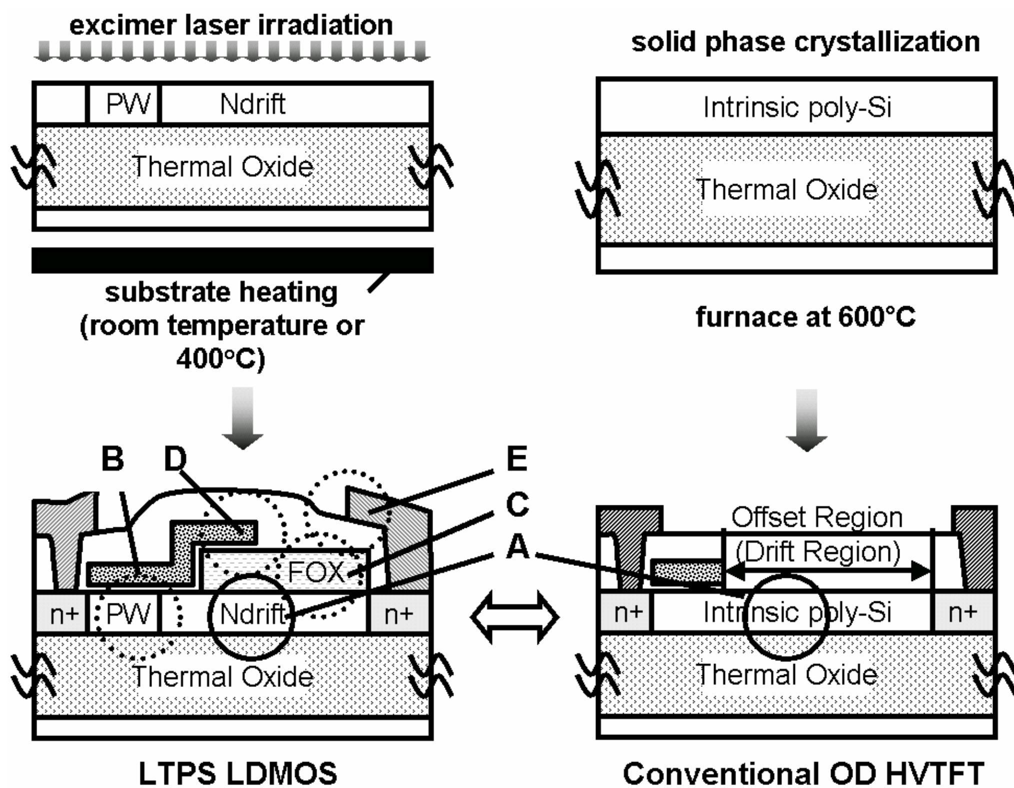


Fig. 5-2. LTPS LDMOS structure fabricated by excimer laser crystallization under room temperature or 400°C irradiation. The broken circles represented the RESURF design and the solid circles indicated the drift with/without doping for reducing the resistance of drift region in LTPS LDMOS and OD TFT devices.

junction electric field at label "D". The 50 KeV phosphorous and boron doses of 5 × 10^{15} cm^{-2} were carried out to form n+ drain, source, gate and p+ butting regions. Finally,

a 6000-Å-thick Al extended drain was defined to overlap the 5000-Å-thick passive layer and pass through the N-drift/n+ drain junction to split its electric field at label "E". All of the steps were compatible for the standard TFT fabrication and glass process with the maximum temperature of 600 °C.

5.3 Results and Discussion

5.3.1 Transfer Characteristics of Conventional OD TFT and Novel LTPS LDMOS with Room Temperature Irradiation

Table 5-1 lists the transfer characteristics of the conventional OD TFT and the proposed LTPS LDMOS with optimal room temperature irradiation. The LTPS LDMOS was obtained from the following parameters: W=600-μm, L_{ch}=12-μm, L_{drift}=15-μm, N_{drift}=7 × 10^{11} cm^{-2}, t_{si}=0.1-μm, and t_{oxide}=1.5-μm. The OD TFT was established from the parameters: W/L_{ch}=100-μm/16-μm, L_{drift}=20-μm, t_{si}=0.3-μm, and t_{oxide}=2-μm [5.4]. The difference of LTPS LDMOS without and with excimer laser crystallization (ELC) had been compared by Chang *et al* [5.12]. As shown in this table, the OD TFT exhibited the low threshold voltage (Vth) of 0.5-V from the intrinsic well region, which would make the device more sensitivity for signal noises. In order to avoid the phenomenon, the suitable high threshold voltage was required for circuit designs. The LTPS LDMOS presented a higher threshold voltage of 4-V at room temperature irradiation due to the doped P-well region with a dose of 3 × 10^{13} cm^{-2} which was beneficial to increase the threshold voltage and operate stably. In respect of the subthreshold swing (SS), the LTPS LDMOS at room temperature irradiation had smaller value of 1.18-V than OD TFT one of 1.92-V. Before discussing the ON/OFF current ratios, the on-state current (I_{ON}) and off-state current (I_{OFF}) of ON/OFF current ratio were defined at the gate biases

of 35-V and −10-V, respectively. As listed in Table, the LTPS LDMOS at room temperature irradiation would display a better I_{ON}/I_{OFF} current ratios of 2.19×10^4 and 1.23×10^6 than OD TFT ones of 3×10^3 and 5×10^3 at the drain biases of 0.1-V and 10-V. The breakdown voltage (BV) of LTPS LDMOS at room temperature irradiation was also expressed a high value of 240-V than the conventional OD TFT with the breakdown voltage of 155-V. Thus, in terms of the on-state (Vth, SS, I_{ON}/I_{OFF}) and off-state (BV) characteristics, the proposed LTPS LDMOS at room temperature irradiation was entirely better than the conventional OD TFT.

Table 5-1. Summary of the transfer characteristics for the conventional OD TFT and the proposed LTPS LDMOS under optimal room temperature irradiation.

	Conventional OD TFT	**Room temperature LTPS LDMOS**
Threshold Voltage (V)	0.5	4
Subthreshold Swing (V/dec)	1.92	1.18
Max. I_{ON}/I_{OFF} at Vds=0.1 V	3×10^3	2.19×10^4
Max. I_{ON}/I_{OFF} at Vds=10 V	5×10^3	1.23×10^6
Breakdown Voltage (V)	155	240

5.3.2 Transfer Characteristics of LTPS LDMOS at RT and 400 °C Irradiations

Figure 5-3 and Table 5-2 shows the transfer characteristics of LTPS LDMOS for optimal room temperature and 400 °C irradiations in the drift length of 15-μm. At the

negative gate bias (off state range), the I_{OFF} leakage current at Vds=0.1 V was reduced about 1.47 times from 10^{-10} A to 10^{-11} A by 400 °C substrate heating during excimer laser irradiation. The I_{OFF} at 400°C substrate heating was lightly lower than that at room temperature due to the reduction in the defect trap states [5.13]. As the drain voltage was up to 10 V, the decrease in I_{OFF} leakage current was slow down from 1.47 times to 1.32 times for 400 °C irradiation. The anomalous I_{OFF} leakage current could be restrained by the drift region (offset region) at the negative gate voltages regardless of the gate and drain voltage increase even up to Vgs=−35 V and Vds=10 V [5.14]. The threshold voltages in polycrystalline silicon devices were dominated by the defect trapping density unlike the threshold voltages of single crystalline by Fermi potential and intrinsic carrier density. But, in this case, the well region was no longer undoped and replaced by a P-type Boron implantation. The doped P-well region not only could suppress the source/drain punch-through but also could increase the domination in the threshold voltage. In addition, the threshold voltage for the proposed LTPS LDMOS device was evaluated and almost the same at 4 volts at 400 °C and room temperature irradiations. The reason was that the same concentrations in P-well regions resulted in the similar threshold voltage at 400 °C and room temperature irradiations. The subthreshold swing was reduced from 1.15 V/decade at 400 °C irradiation to 1.18 V/decade at room temperature irradiation. It was revealed the finite improvement of 2.5 % by 400 °C irradiation. As the gate voltage was increased to attain the on state, the I_{ON} current at Vds=0.1 V could be raised about 10 times from 10^{-6} A to 10^{-5} A by 400 °C substrate heating during excimer laser irradiation. But, while the drain voltage was raised to 10 V, the increment of the drain currents between RT and 400 °C irradiations would be shorten from 10 times to 4 times. In summary, the I_{ON}/I_{OFF} current ratios through 400°C irradiation were further increased from 2.19×10^4 to 2.96×10^5 at

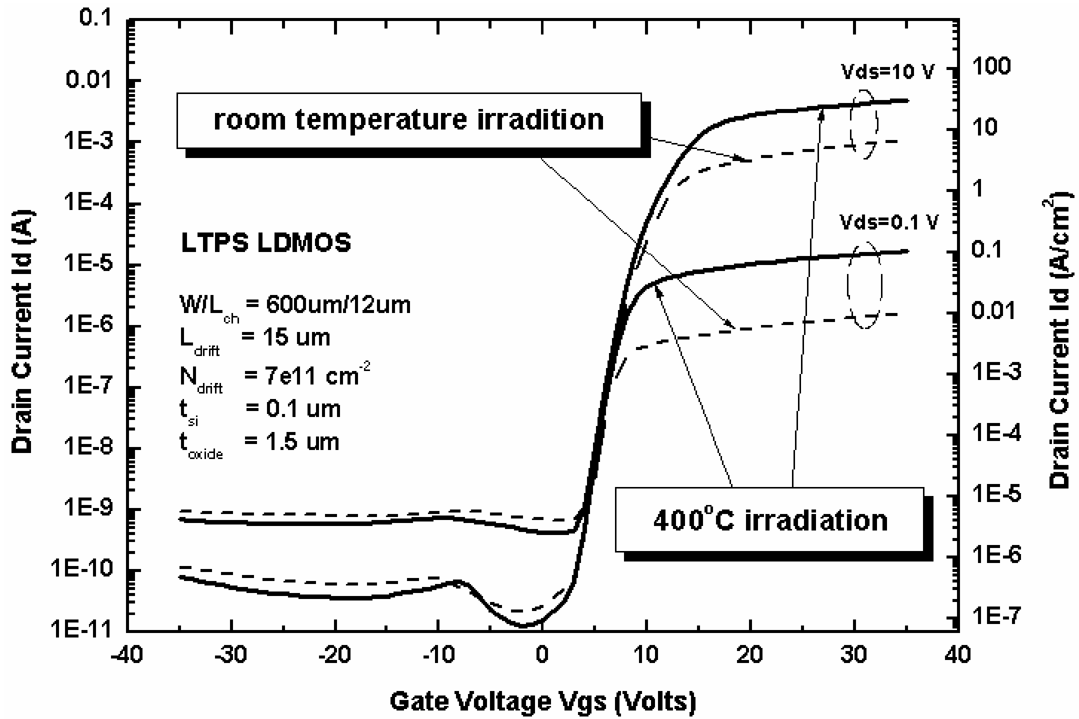


Fig. 5-3. Transfer characteristics of LTPS LDMOS for optimal room temperature and 400 °C irradiations with W/L_{ch}=600-μm/12-μm and L_{drift}=15-μm.

Table 5-2. Summary of the transfer characteristics of LTPS LDMOS at room temperature and 400 °C irradiations with optimal laser conditions.

	Room temperature LTPS LDMOS	400 °C irradiation LTPS LDMOS
Threshold Voltage (V)	4	4
Subthreshold Swing (V/dec)	1.18	1.15
Max. I_{ON}/I_{OFF} at Vds=5 V	2.19×10^4	2.96×10^5
Max. I_{ON}/I_{OFF} at Vds=25 V	1.23×10^6	6.72×10^6
Breakdown Voltage (V)	240	180

Vds=0.1 V and 1.23 $\times$ 10^6 to 6.72 $\times$ 10^6 at Vds=10 V, which were indicated about 14 and 5 times improvements for the room temperature ones, respectively.

5.3.3 Relationship between ON/OFF Current Ratio and Drift Length of LTPS LDMOS at RT and 400 °C Irradiations

Figure 5-4 (a) shows the variations of I_{ON} and I_{OFF} currents with the drift length extension at drains bias of 5 V for LTPS LDMOS at room temperature and 400 °C irradiations. The on-state current (I_{ON}) and off-state current (I_{OFF}) of ON/OFF current ratio were defined at the gate biases of 30-V and −30-V, respectively. As the drift lengths increased from 15-μm to 30-μm, the on-currents of 400 °C irradiation exhibited the large value than that of room temperature irradiation. The off-currents for 400 °C irradiation also maintained the less leakages than that for room temperature irradiation even if the drift length is extended to 30-μm. It is worth to mention that the on-current deviations between room temperature and 400 °C irradiations were not stable with the increase in drift length. In order to explain the difference, the on-current deviations will be divided into the three ranges from the drift length of 15-μm to 30-μm. At the short drift length of 15-μm, the magnitude of on-currents was determined on the quality of polycrystalline silicon film. As the drift length extended to 20-μm, the 33 % increase of the drift length would also involve the magnitude of on-currents. At this experiment, the on current for 400 °C radiation could still held the high value due to its good crystallinity but the on current for room temperature irradiation started to exhibit the mechanism of drift length domination. As the drift length increased to the range from 25-μm to 30-μm, the percentage of the drift length extension was raised from 66 % to 100%. The device current mechanism would be predominated by the drift length so that the on current for 400 °C radiation was gradually close to the on current for room

temperature radiation. The results were illustrated that the crystallinity domination was beneficial to obtain the high magnitude of on-currents but long drift length would suppress this mechanism. The long drift length increased the number of grain boundaries, which would non-linearly accelerate the total resistances in devices. Thus, in order to improve the phenomenon, the advanced growth technology for large grain size was necessary to reduce the number of grain boundaries in the drift region and promote the device performance. Additionally, as shown in figure, the off currents deviations were also presented the same phenomenon between room temperature and 400 °C irradiations.

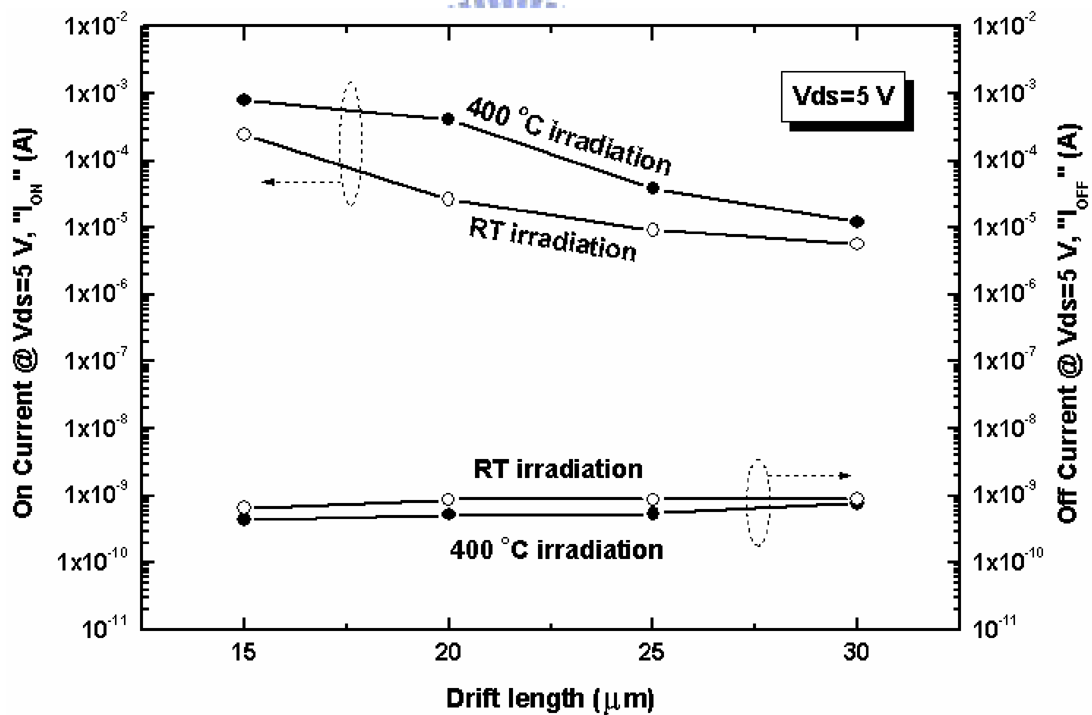


Fig. 5-4. (a) Dependence of on and off currents on the drift length variation from 15-μm to 30-μm at drains bias of 5 V for LTPS LDMOS at optimal room temperature and 400 °C irradiations.

Figure 5-4 (b) shows the variations of ON/OFF current ratios with the drift length extension at drains bias of 5 V for LTPS LDMOS at room temperature and 400 °C irradiations. The ON/OFF current ratios at 400 °C irradiation entirely exhibited the better characteristics than those at room temperature irradiation. At the drift length of 15-μm for crystallinity domination, the good quality of LTPS LDMOS at 400 °C irradiation presented a higher value of 1.79×10^6, which was about 4.80 times in the magnitude as compared with ON/OFF current ratio of 3.73×10^5 at the room temperature irradiation. As the drift length increased to 20-μm, the ON/OFF current ratio at room temperature irradiation was suffered from the drift length mechanism and decayed about 12 times from 3.73×10^5 to 2.96×10^4. However, the ON/OFF current

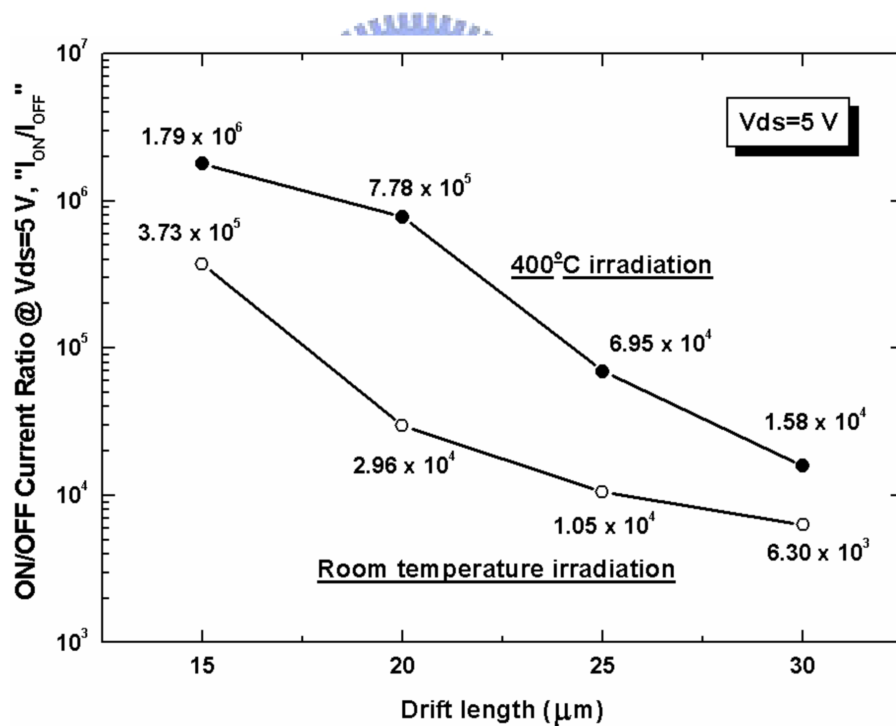


Fig. 5-4. (b) Relationship between of ON/OFF current ratios and the drift length variation from 15-μm to 30-μm at drains bias of 5 V for LTPS LDMOS at optimal room temperature and 400 °C irradiations.

ratio at 400 °C irradiation was varied only about 2.26 times from 1.79×10^6 to 7.78×10^5 due to its superior crystallinity than that in room temperature irradiation. At the drift length of 25-μm, the ON/OFF current ratios were gone into the strong mechanism of drift length domination regardless of room temperature or 400 °C irradiation. The ON/OFF current ratio at 400 °C irradiation could not sustain a high value and decrease sharply about 11.19 times from 7.78×10^5 to 6.95×10^4 but still higher than the ON/OFF current ratio of 1.05×10^4 at room temperature irradiation. At the drift length of 30-μm, the ON/OFF current ratio deviation between 400 °C and room temperature irradiation was very close to each other since the drift length mechanism was gradually dominated the device performance in spite of the quality of polycrystalline silicon film except the decrease in grain boundaries.

5.3.4 Output Characteristics of LTPS LDMOS at RT and 400 °C Irradiations

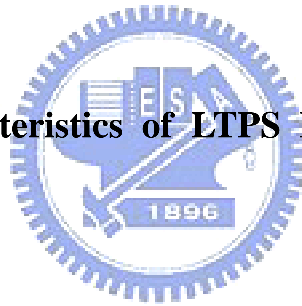


Figure 5-5 (a), (b), and (c) shows the output characteristics of LTPS LDMOS for optimal room temperature and 400 °C irradiations. The corresponding safe operating area (SOA) was described with the algorithmic scales of drain current and voltage in Fig. 5-5 (b). While the substrate was heated to 400 °C, the maximum $R_{DS,on}$ current limit was increased about 2 times from 5-mA to 10-mA at Vgs=20 V. The maximum power limit, where the LTPS LDMOS was burned out, was great in 1.11 Watts (6852 W/cm^2) at Ids=12.3-mA, Vds=90 V, and Vgs=20 V. The latch-up current at Vgs=16 V could be suppressed up to 90-V drain voltage with 2 times drain current from 1.5 mA to 3 mA. Nevertheless, the latch-up voltage (kink voltage) at Vgs=16 V was slightly decreased about 0.95 times from 95-V to 90-V. The maximum voltage limit (breakdown voltage) was reduced about 0.75 times from 240-V to 180-V in Fig. 5-5 (c). The reason might be

the impact ionization path and effective ionization rate (α) were raised by the less intra/inter-gain defects so that the breakdown voltage was dropped below that of room temperature irradiation [5.15], [5.16]. But, on the whole, the safe operating area (SOA) could be still improved about twice (1.5 times) with 2 times enhancement of the maximum $R_{DS,on}$ current and 0.75 times degradation of maximum voltage by the 400 °C irradiation relative to that at room temperature (RT) irradiation.

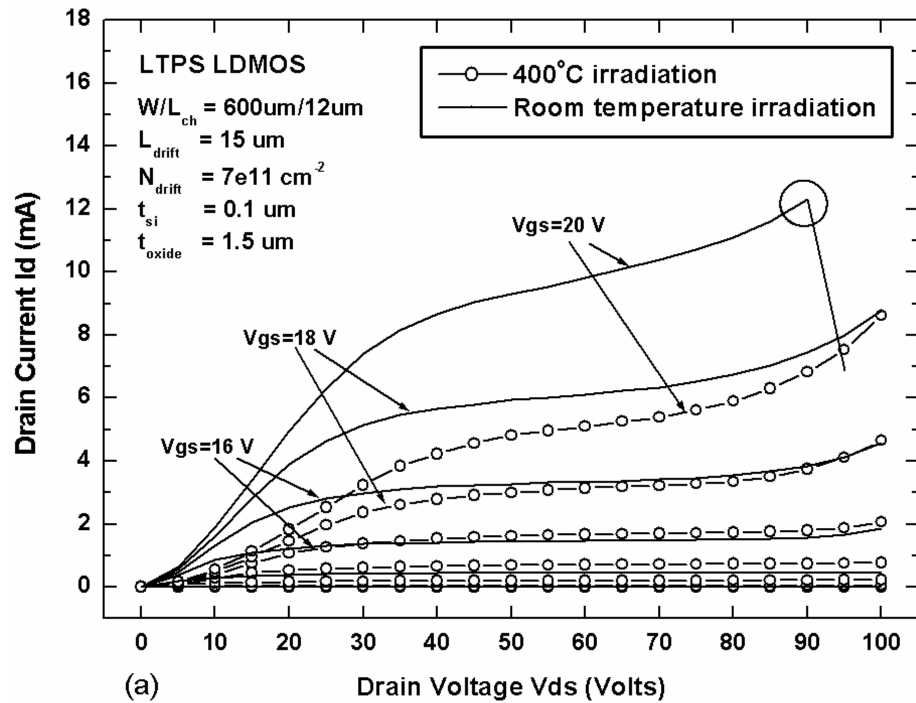


Fig. 5-5. (a) Output characteristics of LTPS LDMOS for optimal room temperature and 400 °C irradiations. The circle was indicated the maximum power limit point of 1.11 Watts.

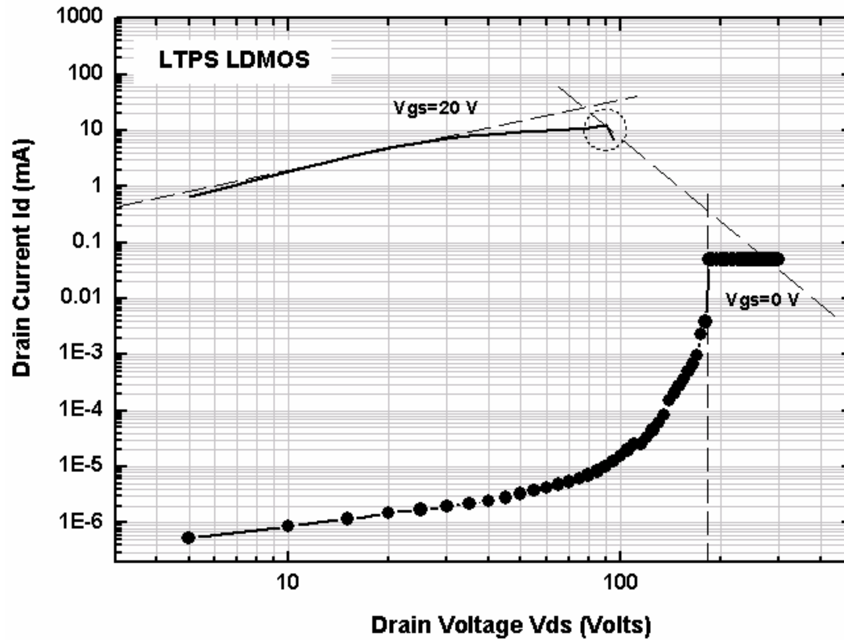


Fig. 5-5. (b) Corresponding safe operating area (SOA) with the algorithmic scales of drain current and voltage.

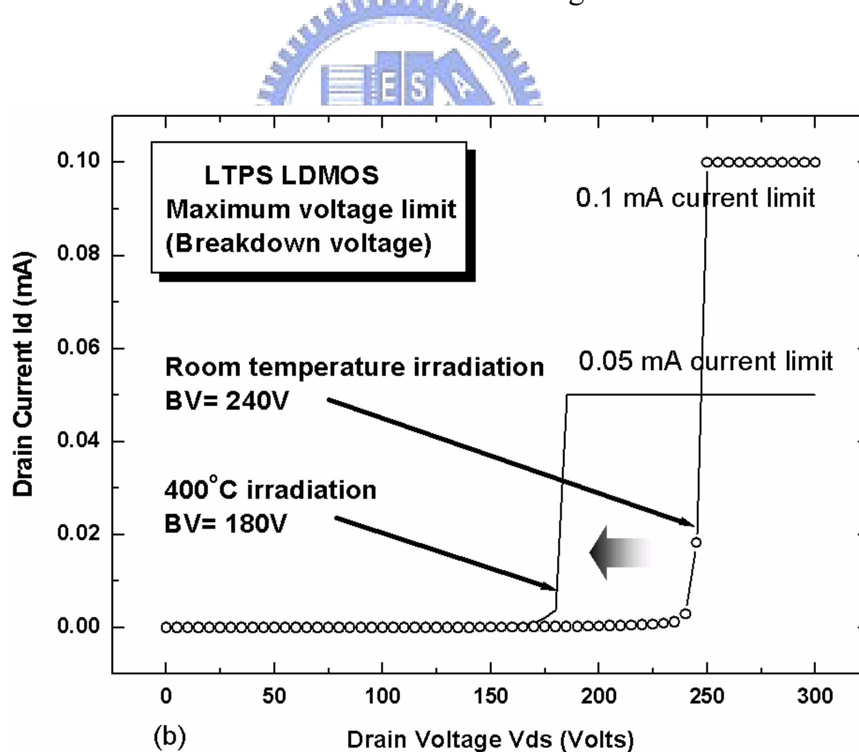


Fig. 5-5. (c) Output characteristics of LTPS LDMOS for optimal room temperature and 400 °C irradiations. The breakdown voltages were measured by the protective limits of 0.1 mA and 0.05 mA for room temperature and 400°C irradiations, respectively.

5.3.5 Comparison of LTPS LDMOS at RT and 400 °C Irradiations together with OD and VDS TFTs

5.3.5.1 Specific On-Resistance

Figure 5-6 (a) shows the relationships between the specific on-resistance and laser energy density for LTPS LDMOS at RT/400 °C irradiations together with OD TFT, variable doping slot (VDS) TFT, and c-Si LDMOS. The specific on-resistances (Ron,sp) of all structures were defined at Vgs=20 V and Vds=20 V. The grain growth regimes were divided into three parts: partial melting, super lateral growth (SLG)—the expected regime for the largest grain size—and ablation of Si film regimes. As the results, the

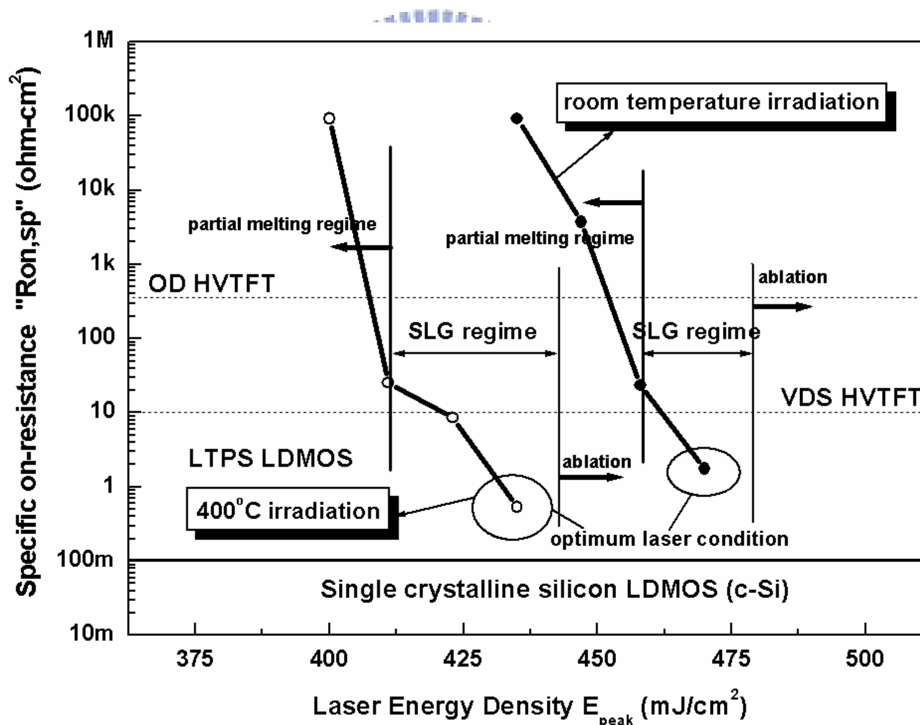
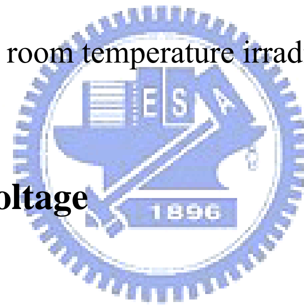


Fig. 5-6 (a) Relationships of the specific on-resistance and laser energy density for LTPS LDMOS at RT/400 °C irradiations together with OD TFT, VDS TFT and c-Si LDMOS. The optimal laser conditions were located at 470 mJ/cm^2 and 435 mJ/cm^2 for room temperature and 400 °C, respectively.

LTPS LDMOS at room temperature irradiation exhibited the better Ron,sp of 1.78 ohm-cm^2 by the ELC process and RESURF design than the conventional OD TFT of 360 ohm-cm^2 and VDS TFT of 10 ohm-cm^2 by offset region and SPC process [5.4]. Nevertheless, the Ron,sp of room temperature irradiation still fell about 18 times behind the 0.10 ohm-cm^2 of c-Si LDMOS from Taurus and ATHENA/ATLAS simulators [5.17], [5.18]. Fortunately, while crystallizing at 400 °C, the Ron,sp of room temperature irradiation could be further reduced around 3 times from 1.78 ohm-cm^2 to 0.54 ohm-cm^2 at the optimal laser conditions of 470 mJ/cm^2 and 435 mJ/cm^2, respectively. The Ron,sp of LTPS LDMOS could be greatly decreased from 18 times dropped to only 5 times higher than that of c-Si LDMOS. It was attributed that the solidification velocity at 400 °C irradiation could be reduced to about 1/5 and the crystallinity could become better as compared to that at room temperature irradiation [5.19].



5.3.5.2 Breakdown Voltage

Figure 5-6 (b) shows the comparison of the breakdown voltages for the LTPS LDMOS at RT/400 ºC irradiations together with OD TFT, VDS TFT, and c-Si LDMOS. The breakdown voltage was defined as a drain current of 1 nA/μm channel width at a gate voltage of 0 V. The Si atoms in the crystalline solids were arranged orderly unlike the segment order of polycrystalline ones. Consequently, the impact ionization path and effective ionization rate (α) of c-Si LDMOS is the longest and largest, which resulted in the minimum breakdown voltage of 145-V for comparison with the polycrystalline silicon devices [5.20], [5.21]. In regard to the conventional high-voltage TFT, the breakdown voltage of OD TFT (155-V) was slightly larger than that of VDS TFT (152-V). The reason was responsible for the slot dope in the offset region even though the VDS TFT had utilized a set of variable doping slots to alleviate the degradation in

blocking voltage capability. The proposed LTPS LDMOS at room temperature and 400 °C irradiations exhibited the excellent breakdown voltages of 240-V and 180-V, respectively. Therefore, according to the results of figure 5-6 (a) and (b), the LTPS LDMOS, regardless of room temperature or 400 °C irradiation, is really a promising power device in low temperature poly-Si application than the conventional high-voltage TFT.

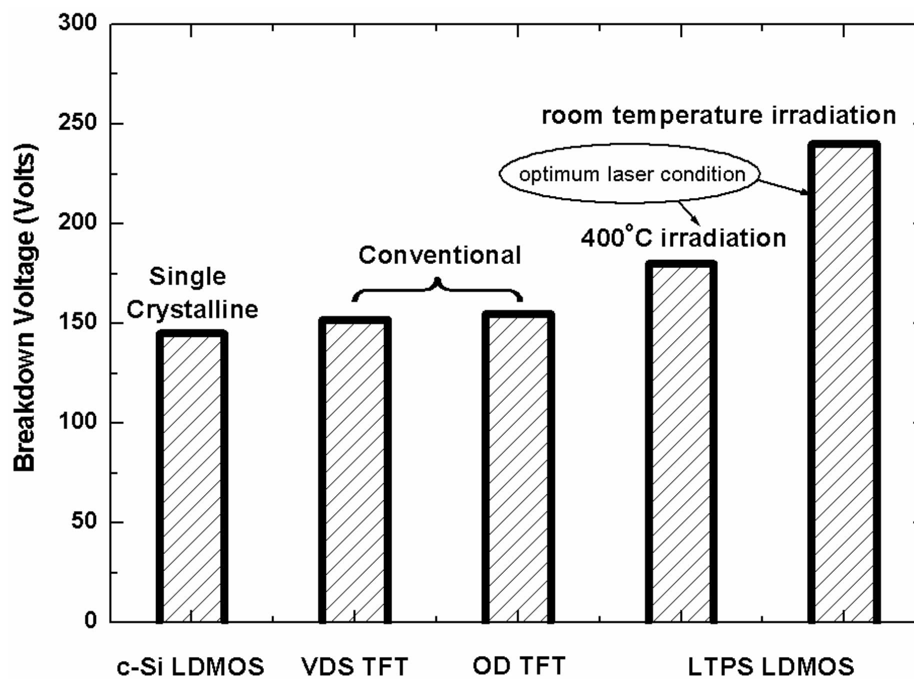


Fig. 5-6 (b) Comparison of the breakdown voltages for the LTPS LDMOS at RT/400 ºC irradiations together with OD TFT, VDS TFT, and c-Si LDMOS.

5.4 Summary

A new power device called LTPS LDMOS is reported for the first time to attain the high driving and high blocking capability with the excimer laser annealing at 400 °C substrate heating. The LTPS LDMOS presents a higher threshold voltage of 4-V due to the doped P-well region with a dose of 3×10^{13} cm^{-2} which is beneficial to increase the threshold voltage and operate stably. The subthreshold swing is reduced from 1.15 V/decade at 400 °C irradiation to 1.18 V/decade at room temperature irradiation. It is revealed the finite improvement of 2.5 % by 400 °C irradiation. The ON/OFF current ratios through 400°C irradiation are further increased from 2.19×10^4 to 2.96×10^5 at Vds=0.1 V and 1.23×10^6 to 6.72×10^6 at Vds=10 V, which are indicated about 14 and 5 times improvements for the room temperature ones, respectively. At the short drift length, the magnitude of on-currents is determined on the quality of polycrystalline silicon film. As the drift length increases, the device current mechanism will be predominated by the long drift length which increases the number of grain boundaries, and non-linearly accelerates the total resistances in devices. Thus, the advanced growth technology for large grain size is necessary to reduce the number of grain boundaries in the drift region and promote the device performance.

The device can handle a much higher current of 10mA, and a better power limit of 1.11 Watts. The safe operating area (SOA) can be improved about twice (1.5 times) with 2 times enhancement of the maximum $R_{DS,on}$ current and 0.75 times degradation of maximum voltage by the 400 °C irradiation relative to that at room temperature (RT) irradiation. While crystallizing at 400 °C, the Ron,sp of room temperature irradiation can be further reduced around 3 times from 1.78 ohm-cm^2 to 0.54 ohm-cm^2 at the optimal laser conditions of 470 mJ/cm^2 and 435 mJ/cm^2, respectively. The proposed

LTPS LDMOS at room temperature and 400 °C irradiations exhibit the excellent breakdown voltages of 240-V and 180-V against the conventional OD TFT, VDS TFT, and c-Si LDMOS with breakdown voltage of 155-V, 152-V, and 145-V, respectively. The resultant characteristics for the 400 °C annealing ones are even very close to the c-Si LDMOS. Hence, the proposed LTPS LDMOS devices are very suitable for future system-on-a-panel (SOP) applications.

Chapter 6

Thermal Analyses on Single-Crystalline and Low-Temperature Polycrystalline Silicon Power Devices

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Recently, there are many potential applications, in spite of low voltage, high voltage, single crystalline silicon, and polycrystalline silicon elements, which are demanded or required to operate at elevated temperatures. For low voltage polycrystalline silicon elements, such in active matrix liquid crystal display (AMLCD's), the back illumination behind the liquid crystal display will increase the operating temperature of the hydrogenated amorphous silicon (a-Si:H) TFT's up to over 70 °C. The high temperature operation may degrade the device performance or seriously cause the device permanent failure. These phenomena will make the image lag or cause the white points appear in the screen. The effects of a high temperature ambient will be exacerbated by power dissipation, called self-heating, which will also cause additional temperature rise within the device [6.1]. For high voltage single crystalline silicon elements, such in the lateral double diffused metal oxide semiconductor (LDMOS) devices, the elevated temperature will lead to the principal deleterious influences of the increase in the forward-blocking mode leakage current and an increase in forward-driving mode on-resistance. Although power devices are often expected to run hotter than other component, the excessive temperature rise of an inherently problem device will often lead to catastrophic failure. Failure of a single power device can shut down a computer, bring to halt a motor-driven system, or stop a vehicle dead in its tracks. The self-heating will also result in an increase of the interconnect temperature

which is critical for electro-migration considerations. In silicon on insulator (SOI) devices, the operation temperature will be raised with increasing the buried oxide thickness and may suffer the metal contact separation [6.2]. The reduction of temperature effect in SOI technology may require the device structure with optimized film and buried oxide thickness. In a word, the accurate characterization of the thermal properties of power transistors is more critical to the reliability of the systems using these devices.

6.1 Self-Heating Effects in SOI Devices

In silicon on insulator (SOI) devices, the self-heating phenomenon will be more serious than in bulk devices due to its low thermal conductivity of the buried oxide beneath the silicon active layer. In generally, on current will reduce at large drain bias, relative to large power dissipation, due to the degradation in mobility. The kink effect, also called floating body effect or snapback effect, will be appeared at largest drain bias, relative to high electric field, due to the onset of parasitic bipolar turn-on. However, in comparison to bulk devices, the higher temperature will degrade the field-effect mobility so much from the increase in channel temperature and the onset of negative output conductance, called snapback, will happen more early in the saturation region [6.3]. However, at this time, the heat dissipation only can depend on the source, drain, and interconnect electrodes to conduct and cool down this additional temperature [6.4]. Furthermore, if the package has not been optimally designed to dissipate the heat, the self-heating may cause thermal runaway in the device and also could lead to the increase in the interconnect temperature at silicon-metal contact. The un-optimum package design will cause negative differential resistance in the terminal characteristics

of device and cannot adequately dissipate the heat produced in the device. Therefore, in order to prevent SOI devices from self-heating, the present packages used in bulk devices will be not suitable for SOI devices and necessary to be modified.

As shown in Fig. 6-1 (a), the contact through buried oxide layer (CTBOX) technique is mainly addressed to the improvement of the thermal performance of SOI devices. In this case, the source and substrate electrodes of a thin film SOI device are usually grounded and the BOX/substrate interface results too if substrate doping concentration is suitable without the depletion or accumulation effect, which depend on the substrate type. The equipotential lines distribution across the devices will be not significantly modified if the source metal layer directly contacts the silicon substrate through the buried oxide layer. Hence, this trench metal contact provides a high conductive thermal path to evacuate the heat generation in the silicon active layer through the silicon substrate. However, there is the most important technological limitation that the buried oxide thickness of CTBOX technique has to be lower than 2-μm thick. This is because a consequence of the dry etch process at thick BOX layers will shorten the graphite electrode life or lead to a re-entrant trench shape not suitable for aluminum deposition. Additionally, this technique cannot be used in full isolating layer—such as glass substrates, quartz substrates, or plastic substrates. For this reason, the proper optimizations of the device layout and package design seem to be the good candidates in the devices fabrication for the SOI technology manufacturability. A backside drain contact helps in dissipating the heat with a great area and also allows for minimum lead inductance on the drain side. As shown in Fig. 6-1 (b), the heat sink, which sometimes be mounted with the additional cooling fan in order to promote heat dissipation effectively, will be utilized and connected with the package of power devices for advanced heat dissipation.

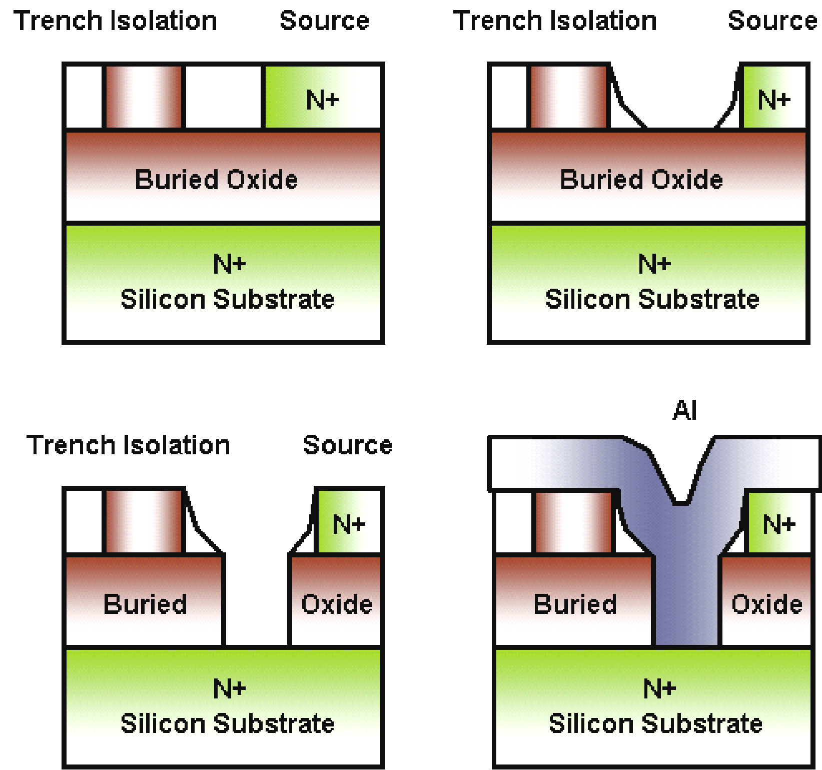

Fig. 6-1. (a) Contact through buried oxide layer (CTBOX) technique process flow.

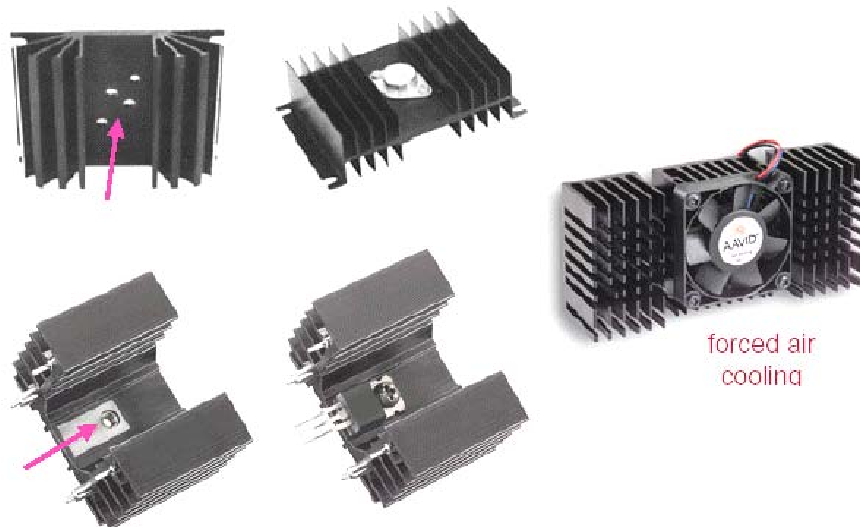

Fig. 6-1. (b) Power devices using a backside drain contact, heat sink, and even a forced air-cooling fan to help in dissipating the heat generation.

6.2 Comparison of Leakage Currents in Bulk and Different -Thickness SOI Devices at High Temperature Operation

At high temperature operation, the most significant effect of elevated temperature is an increase in the off state leakage current, which ultimately limits the upper operating temperature of the device. The silicon-on-insulator (SOI) devices are expected to exhibit lower parasitic leakage currents than their bulk silicon counterparts because of full dielectric isolation. Although many studies of high temperature properties for SOI devices have predominantly concentrated on the short-gate-length low-voltage SOI MOSFET's [6.5]-[6.7], there has been recent increasing interest in high-temperature performance of SOI high-voltage power transistors [6.8]-[6.10]. So several different design approaches have been proposed for high-voltage SOI lateral-double-diffused (LDMOS) transistors [6.11], it is instructive to evaluate these in the light of possible high-temperature applications.

While the applied bias is below avalanche voltage, the leakage current in the bulk-Si device increases with voltage in proportion to the depleted volume. At higher voltages, the SOI room-temperature leakage increases with voltage more steeply because of band-to-band tunneling [6.12]. At high temperature, the SOI leakage current increases less rapidly with voltage because of a weak temperature dependence of the tunneling current and enhanced generation current component so that the tunneling becomes insignificant at high temperature operation. Although the room-temperature leakage currents in SOI and bulk devices are almost similar, the SOI leakage current at high temperature is sometimes two orders of magnitude lower than bulk devices. Additionally, the much larger leakage current observes in thicker SOI power devices [6.9], whose magnitude is comparable to that found in bulk-Si transistors. Hence, the

low overall leakage current makes LDMOS transistors fabricated in thin SOI layers well suited for high-temperature power IC applications.

6.3 Experiments

The key processes for fabricating the novel LTPS LDMOS were shown in Fig. 6-2 (a). At first, an amorphous-silicon (a-Si) of 0.1-μm thickness was deposited by low-pressure chemical vapor deposition (LPCVD) on a 1.5-μm-thick wet oxide at 550 °C. The 50 KeV phosphorous dose of 7×10^{11} cm^{-2} was implanted into the a-Si drift region to reduce its resistance. The high energy of 60 KeV boron dose of 3×10^{13} cm^{-2} was created to increase the breakdown voltage without adding the threshold voltage. The laser crystallization was performed using KrF excimer laser (λ=248 nm) with the energy densities from 400 to 470 mJ/cm^2 and 99 % overlapped shot density at room temperature or 400 °C substrate heating. After that, a 5000-Å-thick field oxide (FOX) was formed by plasma enhanced chemical vapor deposition (PECVD) at 350 °C to reduce the surface electric field. A 1000-Å-thick PECVD gate oxide and a 2000-Å-thick LPCVD a-Si gate were defined across the FOX to split the P-well/N-drift junction electrical field. Finally, a 6000-Å-thick Al extended drain was defined on the 5000-Å-thick passive layer to split the N-drift/n+ drain junction electrical field. The novel poly-Si LDMOS fabrication (≤ 600 °C) was different from the high temperature (≅ 1100 °C) LDMOS processes. Figure 6-2 (b) illustrated the high temperature characteristics obtained using a HP 4156C low voltage analyzer, KEITHLEY model 237 high voltage analyzer, and Micromanipulator H1000 series high performance thermal chuck systems. In the on-state, the transfer and output characteristics were measured by HP 4156C under the gate biases from –35-V to 35-V and drain biases from 0-V to 20-V.

In the off-state, the blocking voltages were measured by KEITHLEY model 236 under grounded gate/source and drain biases from 100-V to 300-V. The thermal characteristics were measured by Micromanipulator thermal chuck systems under the temperatures from 300 K to 400 K.

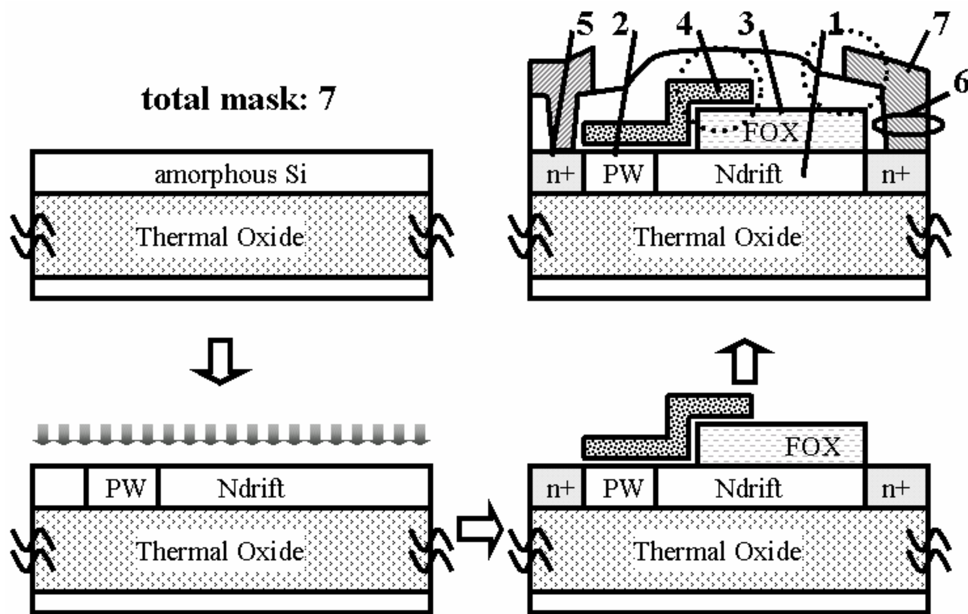

Fig. 6-2. (a) Key process for fabricating the novel LTPS LDMOS using excimer laser crystallization with dimension of W/L_{ch}= 600-μm/12-μm plus a 15-μm drift region.

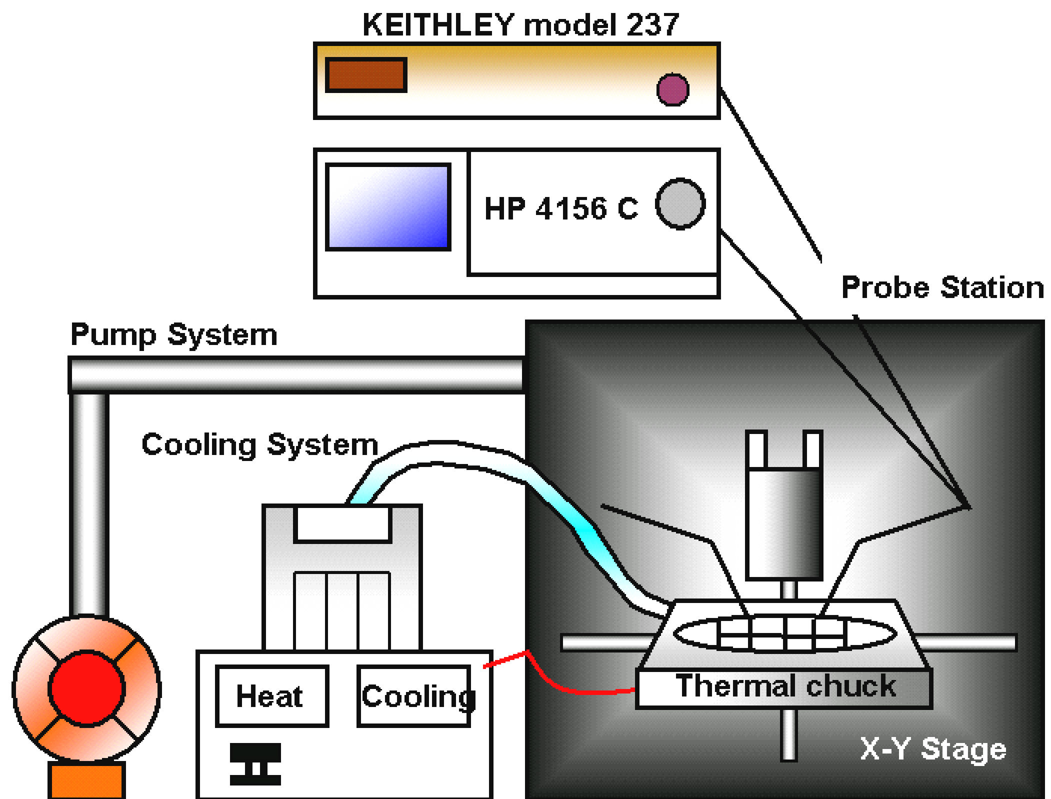

Fig. 6-2. (b) Instruments for measuring the novel LTPS LDMOS using excimer laser crystallization with w 100-V/w 100-mA HP4156C, 1100V KEITHLEY model 237, and –65 °C~400 °C Micromanipulator H1000 high performance series thermal chuck systems.

6.4 Results and Discussion

The various electrical characteristics of LTPS LDMOS at room temperature and 400 °C irradiations were shown over the temperature range of 300–400 K in this section. The on current (I_{ON}), off current (I_{OFF}), and subthreshold swing (SS) were raised as temperature increased. However, the threshold voltage (Vth) and specific on-resistance ($R_{on,sp}$) were exhibited the negative temperature relation.

6.4.1 Transfer Characteristics of LTPS LDMOS at RT and 400 °C Irradiations over Ambient Temperature Range of 300–400 K

6.4.1.1 Relationship between ON/OFF Currents and Ambient Temperatures for LTPS LDMOS

6.4.1.1.1 ON and OFF Currents at Drain Bias of 0.1 V

Figure 6-3 and Table 6-1 showed the I_{ON} and I_{OFF} currents at the drain bias of 0.1 V with increasing ambient temperature from 300 K to 400 K. The on-state current (I_{ON}) and off-state current (I_{OFF}) of ON/OFF current ratios were defined at the gate biases of 35-V and –35-V, respectively. For I_{ON} currents from the ambient temperature of 300 K to 400 K, the LTPS LDMOS at 400 °C irradiation demonstrated the less sensitivity with 3.68 times variation in ambient temperature than that at room temperature irradiation with 11.11 times variation. However, in the I_{OFF} currents as the increase in ambient temperature, the off state variations of LTPS LDMOS at room temperature and 400 °C irradiations were almost the same with the large values of 188 times and 172 times, respectively. At ambient temperature of 300 K, the difference of I_{ON} currents between

the room temperature and 400 °C irradiations was larger about 7 times than the difference of I_{OFF} currents between them. As the ambient temperature increased to 400 K, the difference of I_{ON} currents between the room temperature and 400 °C irradiations was shortened to about 2 times compare to the difference of I_{OFF} currents between them. The LTPS LDMOS at 400 °C irradiation exhibited superior characteristics with the higher I_{ON} current and lower I_{OFF} current as the increase in ambient temperature.

Table 6-1. Summary of on and off currents for LTPS LDMOS at RT and 400 °C Irradiations with Vds=0.1 V and over Ambient Temperature Range of 300 K–400 K.

I_{ON} (Vds=0.1 v)	300 K	325 K	350 K	375 K	400 K
Room temperature irradiation	1.17 E-6	2.27 E-6	4.51 E-6	7.82 E-6	1.30 E-5
400 °C irradiation	1.25 E-5	1.87 E-5	2.61 E-5	3.55 E-5	4.60 E-5

I_{OFF} (Vds=0.1 v)	300 K	325 K	350 K	375 K	400 K
Room temperature irradiation	1.09 E-10	4.20 E-10	1.81 E-9	6.50 E-9	2.05 E-8
400 °C irradiation	7.40 E-11	3.13 E-10	1.15 E-9	4.00 E-9	1.27 E-8

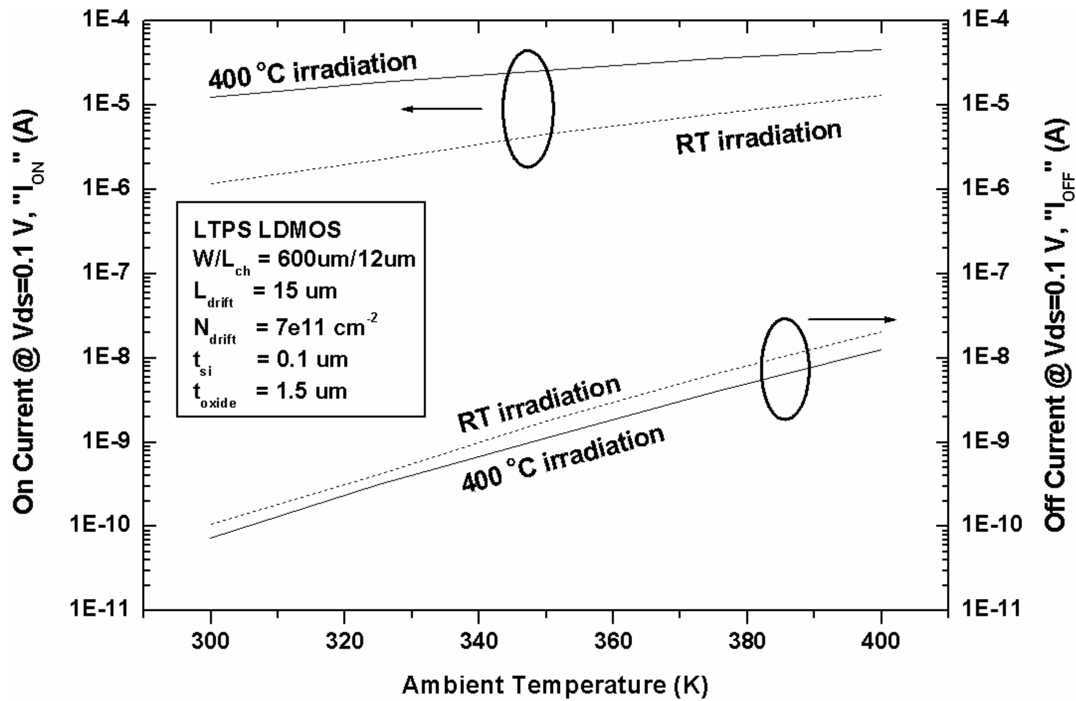

Fig. 6-3. Relationship between on and off currents and ambient temperature variation from 300-K to 400-K at drains bias of 0.1 V for LTPS LDMOS at optimal room temperature and 400 °C irradiations.

6.4.1.1.2 ON/OFF Current Ratios at Drain Bias of 0.1 V

Figure 6-4 and Table 6-2 showed the ON/OFF current ratios at the drain bias of 0.1 V with increasing ambient temperature form 300 K to 400 K. As shown in figure 6-4, both ON/OFF current ratio of LTPS LDMOS at room temperature and 400 °C irradiations were present a degradation phenomenon due to the large increase in I_{OFF} currents. The I_{ON} current was thermally activated and increased (different from c-Si [6.13]) slower than the I_{OFF} current, resulting from the deep level thermal emission via the grain boundary traps, so that the ON/OFF current ratio (I_{ON}/I_{OFF}) was decayed as temperature increased. At the ambient temperature of 300 K, the ON/OFF current ratio at 400 °C irradiation was about 16 times higher than that at room temperature

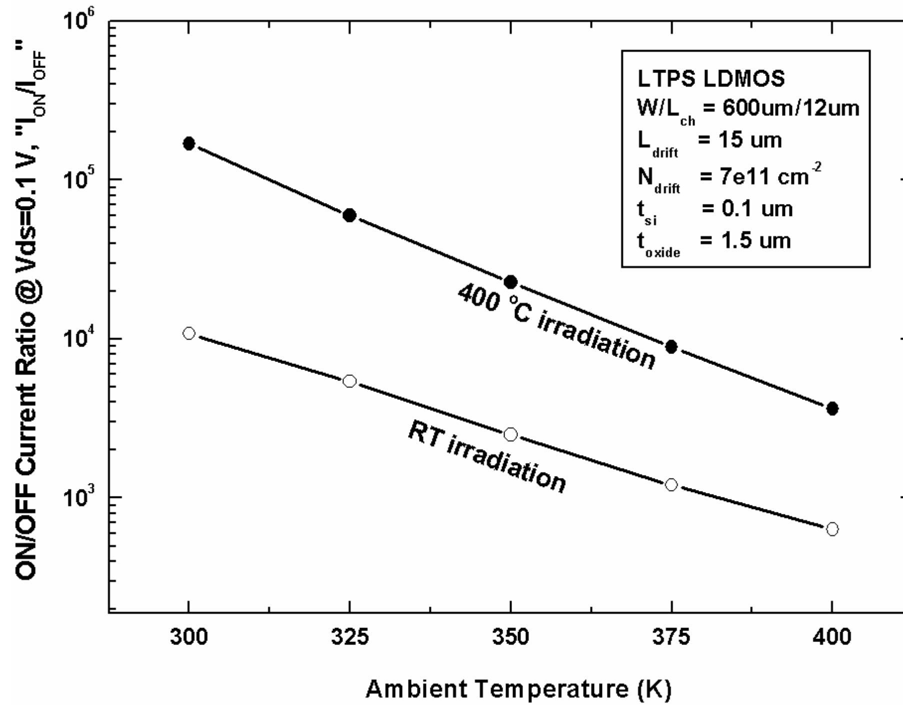

Fig. 6-4. Relationship between ON/OFF current ratios and ambient temperature variation from 300-K to 400-K at drains bias of 0.1 V for LTPS LDMOS at optimal room temperature and 400 °C irradiations.

Table 6-2. Summary of ON/OFF current ratios for LTPS LDMOS at RT and 400 °C Irradiations with Vds=0.1 V and over Ambient Temperature Range of 300 K–400 K.

ON/OFF (Vds=0.1 v)	300 K	325 K	350 K	375 K	400 K
Room temperature irradiation	1.08 E4	5.41 E3	2.50 E3	1.20 E3	6.34 E2
400 °C irradiation	1.69 E5	5.97 E4	2.28 E4	8.88 E3	3.62 E3

irradiation. As the ambient temperature increased to 400 K, the difference in ON/OFF current ratios between 400 °C and room temperature irradiations were varied greatly from 16 times to 6 times. From the ambient temperature from 300 K to 400 K, the ON/OFF current ratios at 400 °C irradiation were entirely larger than that at room temperature irradiation.

6.4.1.1.3 ON and OFF Currents at Drain Bias of 10 V

Figure 6-5 and Table 6-3 showed the I_{ON} and I_{OFF} currents at the drain bias of 10 V with increasing ambient temperature from 300 K to 400 K. The LTPS LDMOS at 400 °C irradiation still exhibited superior characteristics with the higher I_{ON} current and lower I_{OFF} current as the increase in ambient temperature at the drain bias of 10 V. For I_{ON} currents from the ambient temperature of 300 K to 400 K, the LTPS LDMOS at 400 °C irradiation demonstrated the less sensitivity with 1.52 times variation in ambient temperature than that at room temperature irradiation with 3.06 times variation. However, in the I_{OFF} currents as the increase in ambient temperature, the off state variations of LTPS LDMOS at room temperature and 400 °C irradiations were almost the same with the large values of 177 times and 174 times, respectively. At ambient temperature of 300 K, the difference of I_{ON} currents between the room temperature and 400 °C irradiations was shortened from 7 times at Vds=0.1 V to 5 times at Vds=10 V than the difference of I_{OFF} currents between them. As the ambient temperature increased to 400 K, the difference of I_{ON} currents between the room temperature and 400 °C irradiation was similar with the value of 2 times at Vds=0.1 V compare to the difference of I_{OFF} currents between them. As the drain voltage increased from 0.1 V to 10 V, the character differences in room temperature or 400 °C irradiation were entirely decayed.

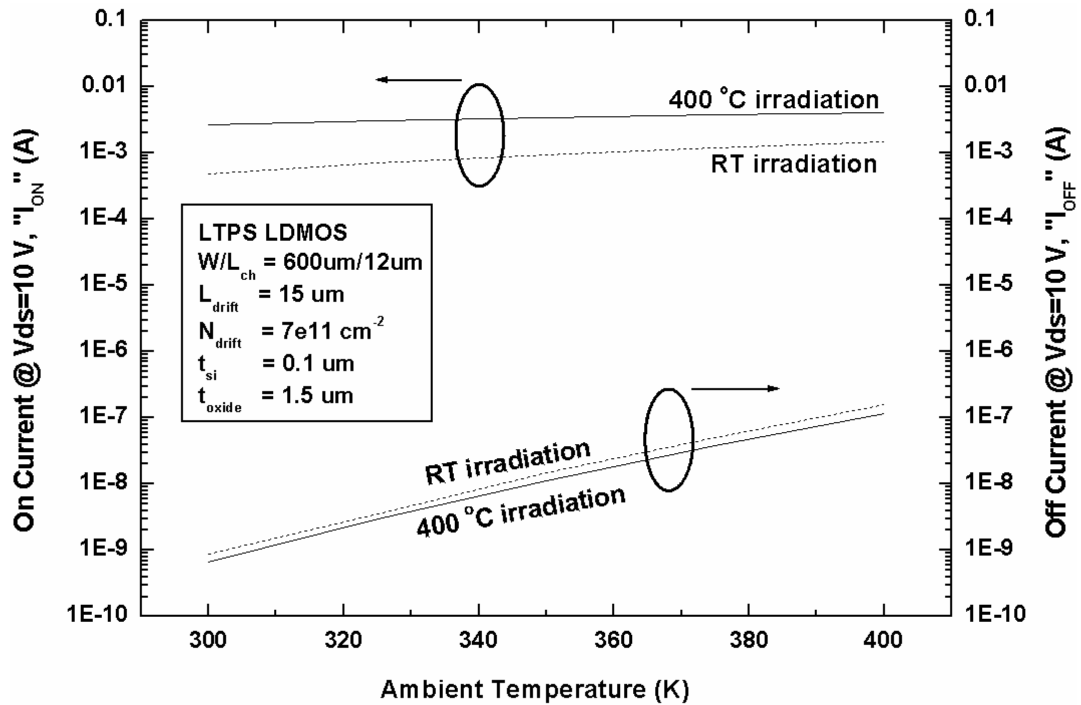

Fig. 6-5. Relationship between on and off currents and ambient temperature variation from 300-K to 400-K at drains bias of 10 V for LTPS LDMOS at optimal room temperature and 400 °C irradiations.

Table 6-3. Summary of on and off currents for LTPS LDMOS at RT and 400 °C Irradiations with Vds=10 V and over Ambient Temperature Range of 300 K–400 K.

I_{ON} (Vds=10 v)	300 K	325 K	350 K	375 K	400 K
Room temperature irradiation	4.83 E-4	7.01 E-4	9.26 E-4	1.17 E-3	1.48 E-3
400 °C irradiation	2.66 E-3	3.00 E-3	3.36 E-3	3.70 E-3	4.05 E-3

I_{OFF} (Vds=10 v)	300 K	325 K	350 K	375 K	400 K
Room temperature irradiation	8.85 E-10	3.57 E-9	1.50 E-8	5.04 E-8	1.57 E-7
400 °C irradiation	6.60 E-10	2.98 E-9	1.14 E-8	3.78 E-8	1.15 E-7

6.4.1.1.4 ON/OFF Current Ratios at Drain Bias of 10 V

Figure 6-6 and Table 6-4 showed the ON/OFF current ratios at the drain bias of 10 V with increasing ambient temperature form 300 K to 400 K. As shown in figure, both ON/OFF current ratios of LTPS LDMOS at room temperature and 400 °C irradiations were still present a degradation phenomenon due to the large increase in I_{OFF} currents at drain bias of 10 V. The ON/OFF current ratio (I_{ON}/I_{OFF}) was decayed as temperature increased because the I_{ON} current was thermally activated and increased (different from c-Si) more slowly than the I_{OFF} current, resulting from the deep level thermal emission via the grain boundary traps. For the ambient temperature from 300 K to 400 K at drain bias of 10 V, the ON/OFF current ratios at 400 °C irradiation were still larger than that at room temperature irradiation. At the ambient temperature of 300 K, the ON/OFF current ratio at 400 °C irradiation was about 7 times higher than that at room temperature irradiation. As the ambient temperature increased to 400 K, the difference in ON/OFF current ratios between 400 °C and room temperature irradiations were varied from 7 times to 4 times. As these results, it can be seen that the ON/OFF current ratio at large drain bias of 10 V was exhibited the more slight variation than that at small drain bias of 0.1 V. The reason was that the difference of I_{ON} currents between the room temperature and 400 °C irradiation was shortened with the increase in drain bias.

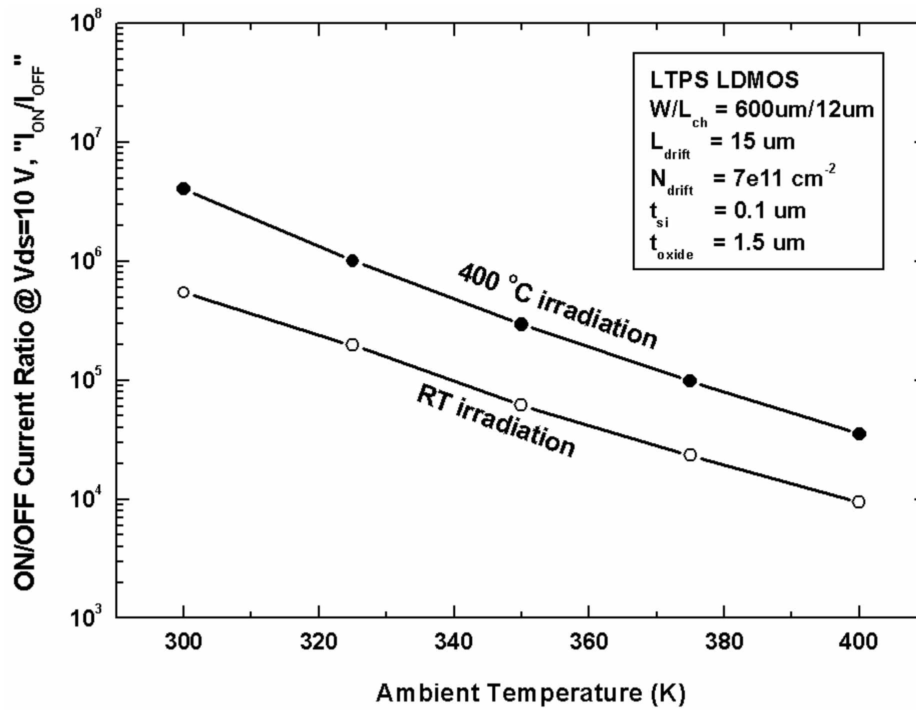

Fig. 6-6. Relationship between ON/OFF current ratios and ambient temperature variation from 300-K to 400-K at drains bias of 10 V for LTPS LDMOS at optimal room temperature and 400 °C irradiations.

Table 6-4. Summary of ON/OFF current ratios for LTPS LDMOS at RT and 400 °C Irradiations with Vds=10 V and over Ambient Temperature Range of 300 K–400 K.

ON/OFF (Vds=10 v)	300 K	325 K	350 K	375 K	400 K
Room temperature irradiation	5.46 E5	1.96 E5	6.18 E4	2.33 E4	9.45 E3
400 °C irradiation	4.03 E6	1.01 E6	2.94 E5	9.79 E4	3.53 E4

6.4.1.2 Relationship between Threshold Voltages and Ambient Temperatures for c-Si LDMOS and LTPS LDMOS

Figure 6-7 showed the dependence of the threshold voltage on ambient temperature for room temperature and 400 °C irradiations from 300 K-400K at 25 °C intervals. The threshold voltage was measured at a constant normalized drain current of (W/L)× 10^{-9} A (0.02 μA) and an absolute drain voltage of 0.1-V. For low voltage poly-Si TFT with W/L_{ch}=20-μm/4-μm and 40-μm/8-μm, the threshold voltages were decayed as a negative temperature coefficient of −42 mV/°C and −64 mV/°C [6.14]. It was indicated that the threshold voltage variation on temperature is more sensitive with the large device geometry. However, the threshold voltage variation of LTPS LDMOS at room temperature irradiation was presented with a much small negative temperature coefficient of −30 mV/°C for large dimension of W/L_{ch}=100-μm/12-μm and L_{drift}=15 -μm. The value of threshold voltage was determined only by the concentration of well region in spite of the possession of drift region (LDMOS) or not (MOS). Thus, in the case of single-crystalline silicon (c-Si) transistors, the threshold voltage of a MOS or LDMOS was given by [6.15]

$$V_{th}(T) = \varphi_{ms} + 2\varphi_f + \sqrt{\frac{2\varepsilon qN_{max}(x)(2\varphi_f)}{C_{ox}}} - \frac{Q_{ox}}{C_{ox}}, \qquad \text{(Eq 6-1)}$$

$$Q_{ox} = Q_f + Q_m + Q_{ot}, \qquad \text{(Eq 6-2)}$$

where $N_{max}(x)$ was the maximum net doping concentration in p-well region. Q_f, Q_m, and Q_{ot} indicated the fixed oxide charge, mobile ionic charge, and oxide-trapped charge, respectively. The total Q_{ox} components did not include the interface-trapped charge Q_{it}. The temperature dependence of Eq. (6-1) came about primarily through the Fermi potential which was written as

$$\varphi_f = \frac{kT}{q}\ln\left(\frac{N_{max}(x)}{n_i(T)}\right), \qquad \text{(Eq 6-3)}$$

the temperature dependence of the intrinsic concentration n_i was given by [6.16]

$$n_i(T) = 3.87 \times 10^{16} T^{3/2} e^{-Eg/2kT}, \quad \text{(Eq 6-4)}$$

the variation of the c-Si LDMOS threshold voltage with temperature was found by combing Eq. (6-1)-Eq. (6-4) and differentiating, which yielded

$$\frac{dV_{th}}{dT} = \frac{d\varphi_f}{dT}\left(1 + \frac{q}{C_{ox}}\sqrt{\frac{\varepsilon N_{max}}{kT \ln(N_{max}/n_i)}}\right), \quad \text{(Eq 6-5)}$$

the effects of temperature come both from the thermal voltage variations (KT/q) and from variations in the intrinsic carrier density. In the case of a thin film transistor, fully depleted device, the combined effect on threshold voltage can be approximated quite well as being linear in Eq. (6-6).

$$\frac{dV_{th}}{dT} = \frac{d\varphi_f}{dT}, \quad \text{(Eq 6-6)}$$

$$\frac{d\varphi_f}{dT} = 8.63 \times 10^{-5}\{\ln(N_{max}) - 38.2 - \frac{3}{2}[1 + \ln(T)]\}, \quad \text{(Eq 6-7)}$$

The threshold voltage variation of c-Si LDMOS device is significantly smaller than the noncrystalline LDMOS device but higher than the c-Si CMOS device. This is because the c-Si LDMOS device requires heavier P-/N-well concentrations (N_{max}), which make the higher threshold voltage than c-Si CMOS device, to push the depletion region extending in the drift region.

The single crystalline silicon devices depended directly on the position of the bulk Fermi level, which for a p-type substrate slowly increased with rising temperature, leading to the observed decrease of threshold voltage in c-Si LDMOS. However, for noncrystalline silicon devices, the excitation of trapped carriers from the tail states to the conduction band, but not the intrinsic carrier excitation, was the dominant mechanism for the reduction in threshold voltage. As shown in figure 6-7, the threshold voltage variation of LTPS LDMOS at 400 °C irradiation was presented a smaller negative temperature coefficient of −27 mV/°C than that of −30 mV/°C at room temperature irradiation. The reason was that: as the trap density increased, more carriers

were captured/released from these trapping sites at a given temperature, so an inversion layer would form at a smaller gate voltage compared to a low trapping density film. Therefore, the more trap density in LTPS LDMOS at room temperature irradiation require less gate voltage to create inversion at elevated ambient temperature against less trap density LTPS LDMOS at 400 °C irradiation. In other words, the novel LTPS LDMOS by excimer laser crystallization was exhibited the smaller negative temperature coefficient due to the low trapping density in comparison to the conventional solid phase crystallization (SPC) HVTFTs. Thus, the low quality poly-Si films with more defect trapping density would be possessed the higher negative temperature coefficient.

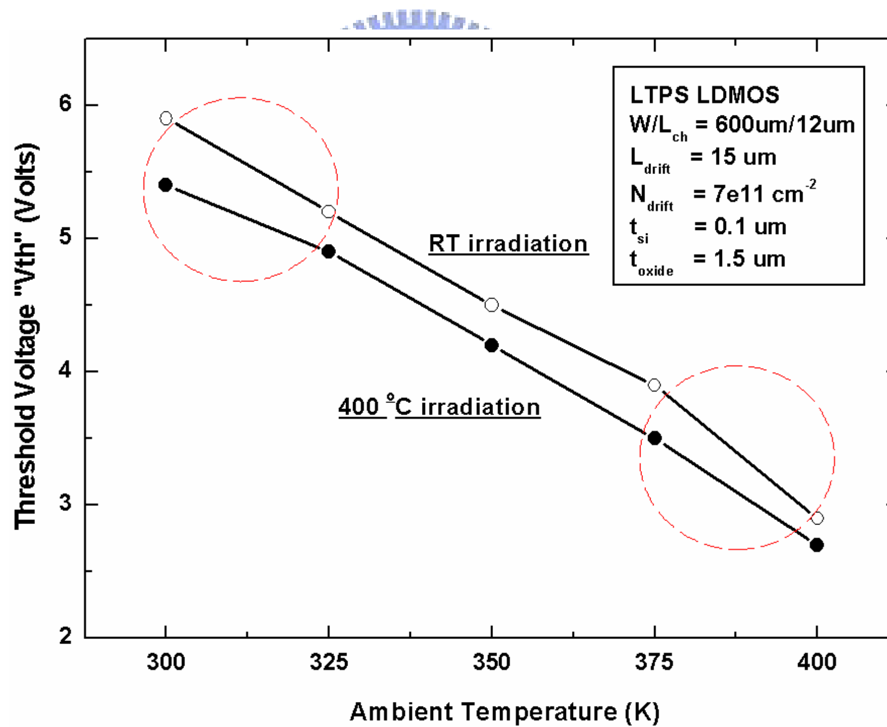

Fig. 6-7. Dependence of the threshold voltages on ambient temperatures from 300 K–400 K at 25 °C intervals for LTPS LDMOS at optimal room temperature and 400 °C irradiations.

6.4.1.3 Relationship between Subtrhreshold Swings and Ambient Temperatures for c-Si LDMOS and LTPS LDMOS

Figure 6-8 and Table 6-5 showed the subthreshold swing of LTPS LDMOS at room temperature and 400 °C irradiations with increasing the ambient temperature. The ambient temperatures were varied from 300 K to 400 K with a step of 25 K. The subthreshold swings were defined at the drain voltage of 0.1 V. As shown in figure, the subthreshold swing in LTPS LDMOS at 400 °C irradiation was displayed the superior characteristics with the smaller values against that in LTPS LDMOS at room temperature irradiation. The subthreshold swings of LTPS LDMOS were increased due to the degradation of I_{ON}/I_{OFF} with increasing the ambient temperature. From the ambient temperature of 300 K to 350 K, the variation in subthreshold swing was raised more smoothly with the value of 0.11 V/decade from 1.02 V/decade to 1.13 V/decade for LTPS LDMOS at 400 °C irradiation. The subthreshold swing variation of LTPS LDMOS at room temperature irradiation exhibited a higher value of 0.18 V/decade from 1.07 V/decade to 1.12 V/decade. From the ambient temperature of 350 K to 375 K, the variation in subthreshold swing at 400 °C irradiation was gradually increased from 1.13 V/decade to 1.33 V/decade with lower difference of 0.20 V/decade.

The variation in subthreshold swing at room temperature irradiation was also gradually increased from 1.25 V/decade to 1.83 V/decade with higher difference of 0.58 V/decade. As the ambient temperature increased to 400 K, the variation in subthreshold swing at 400 °C irradiation was steeply raised from 1.33 V/decade to 2.40 V/decade with maximum difference of 1.07 V/decade. The variation in subthreshold swing at room temperature was exhibited the very large difference of 2.01 V/decade from 1.83 V/decade to 3.84 V/decade. As the ambient temperature varied from 300 K to 400 K, the subthreshold swing at 400 °C irradiation was demonstrated about 3 times

improvement with the less deviation of 0.01 V/decade-K against that of 0.03 V/decade -K at room temperature irradiation. Finally, the transfer characteristics curves of LTPS LDMOS at room temperature and 400 °C irradiations would be plotted from Fig. 6-9 (a) to Fig. 6-9 (d) for summary comparison.

Table 6-5. Summary of subthreshold swings for LTPS LDMOS at RT and 400 °C irradiations over ambient temperature range of 300 K–400 K.

Subthreshold Swing (SS)	300 K	325 K	350 K	375 K	400 K
RT irradiation	1.07	1.12	1.25	1.83	3.84
400 °C irradiation	1.02	1.03	1.13	1.33	2.40

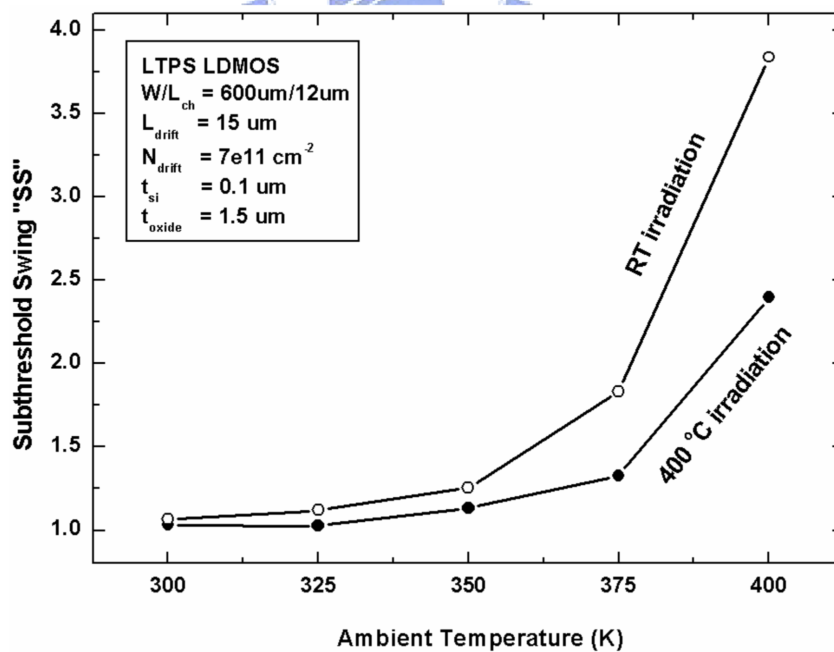

Fig. 6-8. Dependence of the subthreshold swings on ambient temperatures from 300 K–400 K at 25 °C intervals for LTPS LDMOS at optimal RT and 400 °C irradiations.

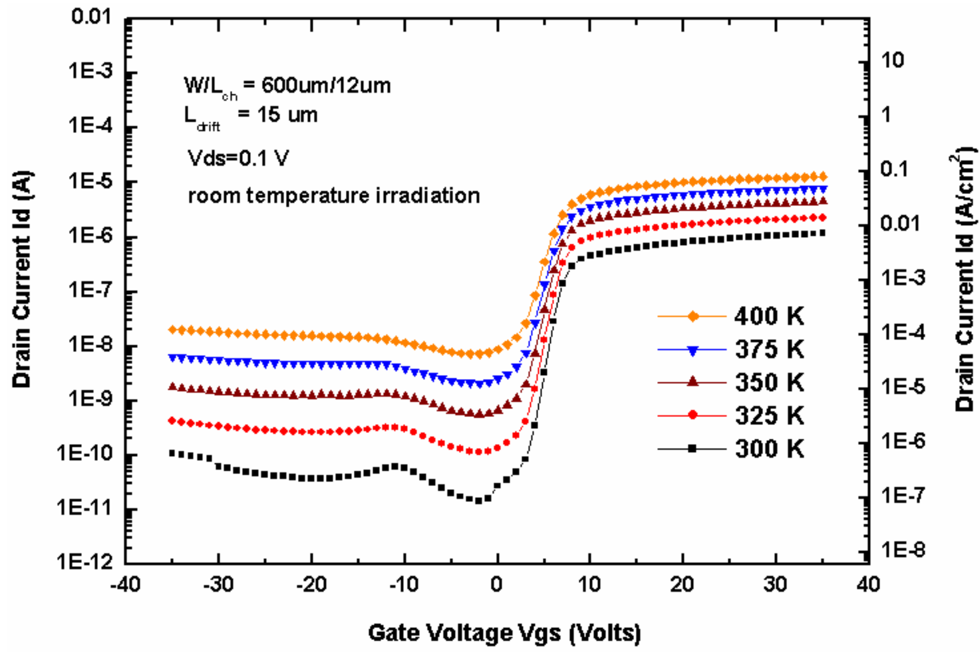

Fig. 6-9. (a) Transfer characteristics of LTPS LDMOS at drain bias of 0.1 V for optimal room temperature irradiation over ambient temperatures from 300-K to 400-K.

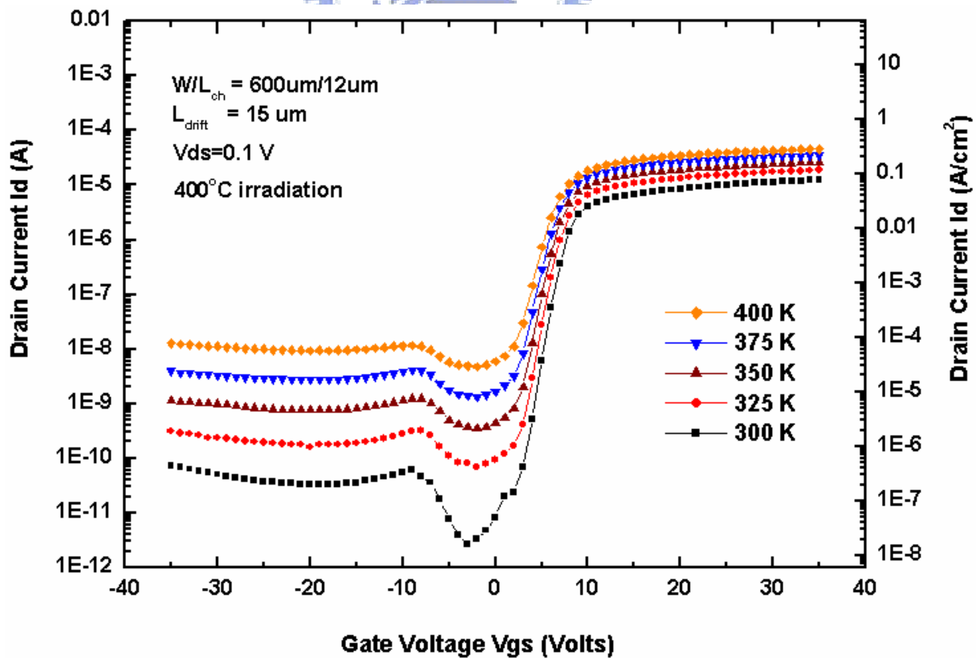

Fig. 6-9. (b) Transfer characteristics of LTPS LDMOS at drain bias of 0.1 V for optimal 400 °C irradiation over ambient temperatures from 300-K to 400-K.

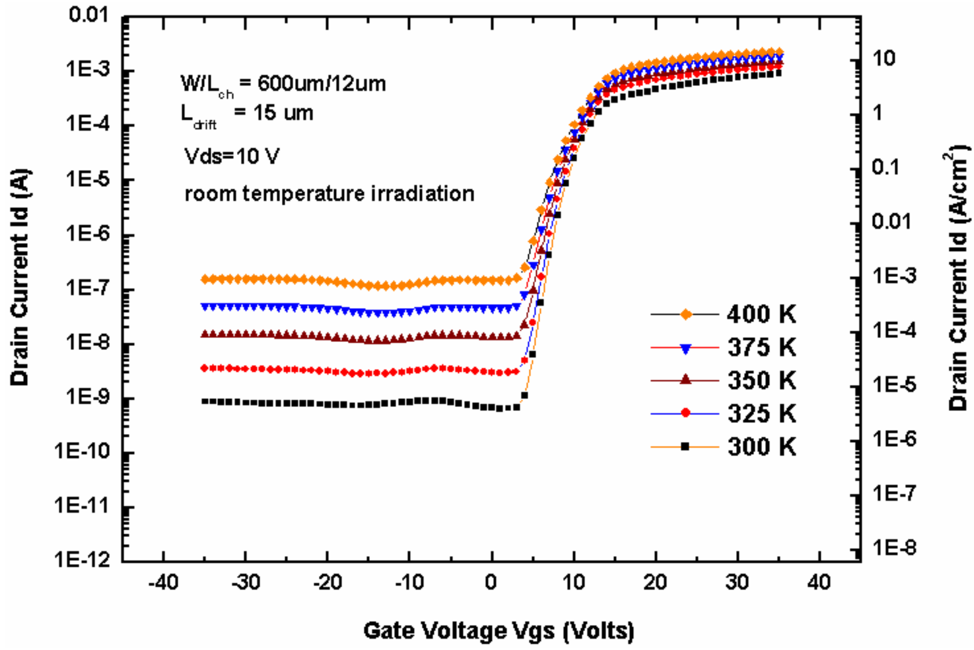

Fig. 6-9. (c) Transfer characteristics of LTPS LDMOS at drain bias of 10 V for optimal room temperature irradiation over ambient temperatures from 300-K to 400-K.

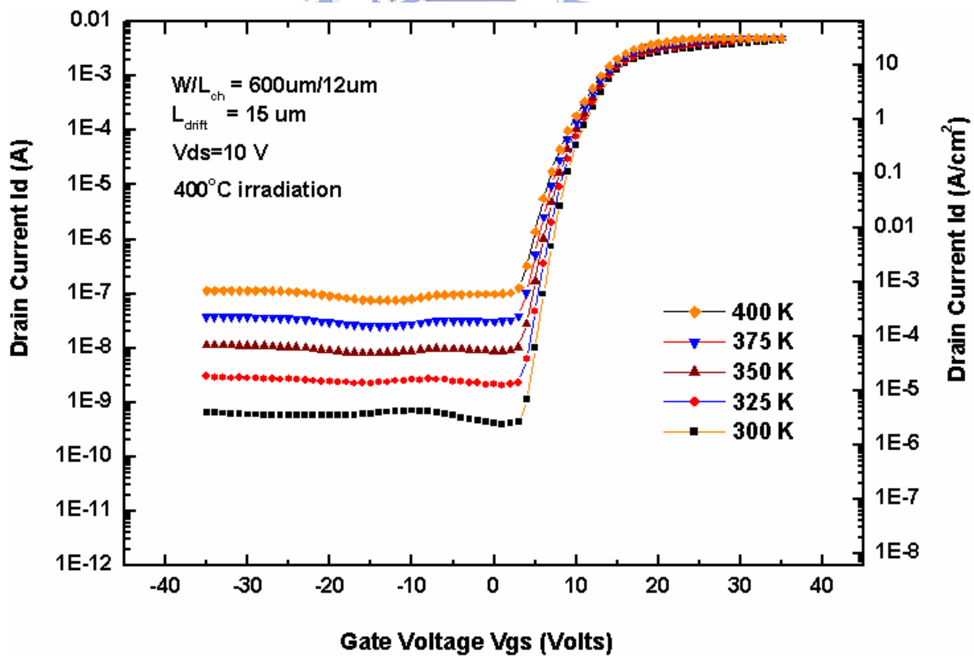

Fig. 6-9. (d) Transfer characteristics of LTPS LDMOS at drain bias of 10 V for optimal 400 °C irradiation over ambient temperatures from 300-K to 400-K.

6.4.2 Output Characteristics of LTPS LDMOS at RT and 400 °C Irradiations over Ambient Temperature Range of 300–400 K

6.4.2.1 Relationship between Specific On-Resistances and Ambient Temperatures for c-Si LDMOS and LTPS LDMOS

The temperature dependence of the channel mobility between LDMOS and CMOS devices in the single crystalline silicon can be modeled as

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m}, \quad \text{(Eq 6-8)}$$

where m=2.5 for the LDMOS device and 1.5 for the CMOS. The $T^{-2.5}$ temperature dependence observed for the LDMOS channel mobility is significantly more severe than in conventional CMOS [6.17]-[6.19]. Since the two devices were processed identically, the difference in mobility variation cannot be attributed to differences in processing conditions. The −2.5 power dependence of the LDMOS was equal to the normal bulk mobility temperature dependence, which resulted from acoustic, intervalley, and optical-phonon scattering. The decrease in channel mobility with increasing temperature tended to increase the channel resistance while the decrease in the threshold voltage tended to reduce channel resistance. However, the power LDMOS devices finally exhibited a positive temperature coefficient due to decrease in bulk mobility (drift region) with temperature. The on-resistance and transconductance of the silicon devices are related to the mobility of carriers. Due to the decrease in the mobility carrier, the on-resistance is expected to increase and the transconductor is expected to decrease with temperature. An equation has been proposed to predict the variation of on-resistance with temperature as follows:

$$R_{on}(T) = R_{on}(300K) \times \left(\frac{T}{300}\right)^{n}, \quad \text{(Eq. 6-9)}$$

where T is absolute temperature (K). The value of n over wide temperature range is about 2.0.

Figure 6-10 showed the variation in specific on resistance of the novel LTPS LDMOS at room temperature and 400 °C irradiations with increasing the ambient temperature. The specific on-resistances (Ron,sp) at room temperature and 400 °C irradiations were defined at Vgs=20 V and Vds=20 V. The corresponding I_D-V_D electrical curves at room temperature and 400 °C irradiations were plotted with different ambient temperature in Fig. 6-11 (a) and (b). The ambient temperature for LTPS HVLDMOS at room temperature and 400 °C irradiations were varied for 300 K to 400 K with a step of 25 K. As shown in Fig. 6-10, the specific on resistances at 400 °C irradiation were entirely smaller than that at room temperature irradiation in different ambient temperature. It indicated that the LTPS LDMOS for 400 °C irradiation exhibit a

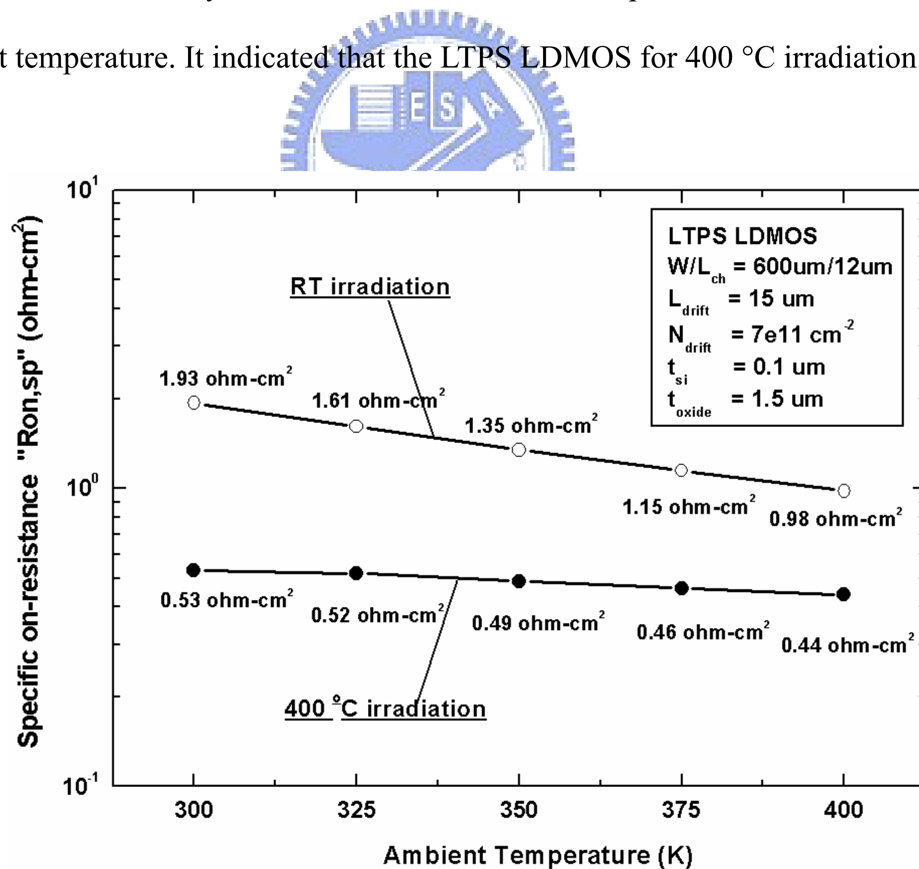

Fig. 6-10. Specific on-resistances of LTPS LDMOS at room temperature and 400 °C irradiations over the ambient temperatures from 300-K to 400-K.

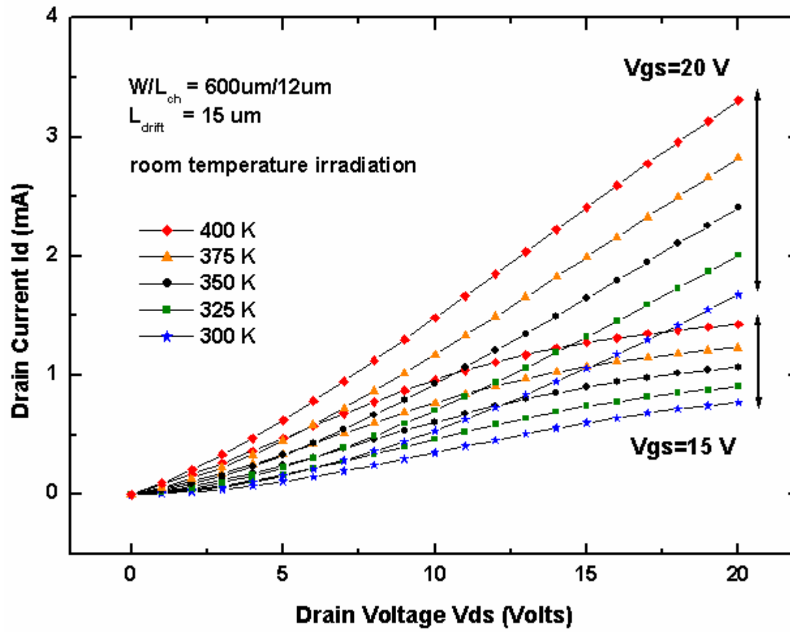

Fig. 6-11. (a) Output characteristics of LTPS LDMOS for optimal RT irradiation at gate biases of 15-V and 20-V over ambient temperatures from 300-K to 400-K.

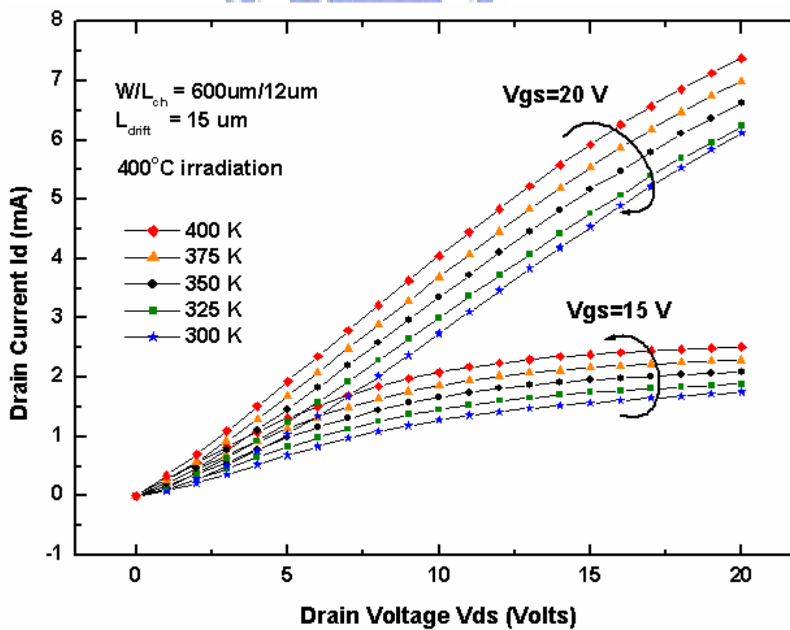

Fig. 6-11. (b) Output characteristics of LTPS LDMOS for optimal 400 °C irradiation at gate biases of 15-V and 20-V over ambient temperatures from 300-K to 400-K.

higher quality polycrystalline silicon film than the room temperature irradiation. The solidification velocity at 400 °C irradiation could be reduced to about 1/5 and the crystallinity could become better as compared to that at room temperature irradiation. As the ambient temperature increased from 300 K to 400 K, the reduction of specific on resistance at room temperature irradiation was exhibited about 1.97 times deviation from 1.93 ohm-cm^2 to 0.98 ohm-cm^2.

However, by 400 °C substrate heating during the excimer laser irradiation, the deviation of the specific on resistance at room temperature irradiation could be shorten to 1.20 times from 300 K to 400 K. Moreover, the difference of specific on resistance from 300 K to 400 K between room temperature and 400 °C irradiations would decay from 3.64 times to 2.23 times. To interpret the mobility variations with temperature in polycrystalline silicon, it is important to note that there are marked different mechanisms between single crystalline and polycrystalline silicon thin film devices. Unlike the single crystalline silicon, where the mobility of carriers was restricted by phonon scattering, the mobility in polycrystalline silicon films was restricted by the potential barrier height between the grains. This potential barrier arose from impurity segregation and carrier trapping at the grain boundary. The trapping states at the boundaries were mostly monovalent, and peaked at the midgap [6.20], [6.21]. For lightly doped or undoped polysilicon materials, the effective mobility was given by [6.22]

$$\mu_{eff} = qL(\frac{1}{\sqrt{2\pi m^* kT}})\exp(-\frac{E_B}{kT}), \qquad \text{(Eq 6-10)}$$

where L is the average grain size, m* is the effective mass of the carrier, and E_B is the energy barrier height. The increase in the temperature resulted in an increase in the mobility for lightly doped or undoped polysilicon, unlike single crystalline or heavily doped material, where is the opposite trend. Thus, the increase in mobility and the

decrease of threshold voltage with increasing temperature resulted in an increase in the device drain current, which meant the decrease in specific on resistance.

6.4.2.2 Relationship between Breakdown Voltages and Ambient Temperatures for c-Si LDMOS and LTPS LDMOS

Figure 6-12 showed the variation in breakdown voltage of the novel LTPS LDMOS before laser irradiation and at room temperature/400 °C irradiations with increasing the ambient temperature. The breakdown voltages of all conditions were defined as a drain current of 1 nA/μm channel width at a gate voltage of 0 V. At the ambient temperature of 300 K, the maximum breakdown voltage was located before laser irradiation for 278 V and the next was located at room temperature irradiation for 235 V. The minimum breakdown voltage belonged to 400 °C irradiation for 170 V with least trap defects. The reason might be the impact ionization path and effective ionization rate (α) were raised by the less intra/inter-gain defects so that the breakdown voltage was exhibited the minimum value at 400 °C irradiation [6.23]. As the ambient temperature increased above 300 K, the breakdown voltages were totally degraded in all conditions regardless of the quality of polycrystalline silicon film unlike the increase of breakdown voltage in single crystalline silicon device.

For the case of single crystalline silicon devices, the increase in ambient temperature led to the increase in the breakdown voltage because the carriers accelerated by an electric filed lost the energy through collisions with optical phonons. As the temperature increased in single crystalline silicon devices, the mean free path decreased, requiring a higher field to allow the carriers to obtain sufficient energy to initiate impact ionization [6.24], [6.25]. On this basis, the single crystalline silicon LDMOS drain-to-source breakdown voltage was expected to exhibit a small positive

temperature coefficient. For polycrystalline silicon LDMOS, the mobility was increased with the ambient temperature so that the velocity carriers in the polycrystalline silicon were accelerated with the increase in ambient temperature. Unlike single crystalline silicon, the impact ionization energy was raised and induced the lower breakdown voltage in polycrystalline silicon device.

As shown in figure, the degradation trends of “before laser irradiation” and room temperature irradiation was similar and larger than the trend in 400 °C irradiation. From the ambient temperature of 300 K to 400 K, the differences of breakdown voltages before laser irradiation, room temperature irradiation, and 400 °C irradiation was shown with 130 V, 120 V, and 37 V, respectively. Above the ambient temperature of 350 K, the breakdown voltage of room temperature irradiation would begin to smaller than that of

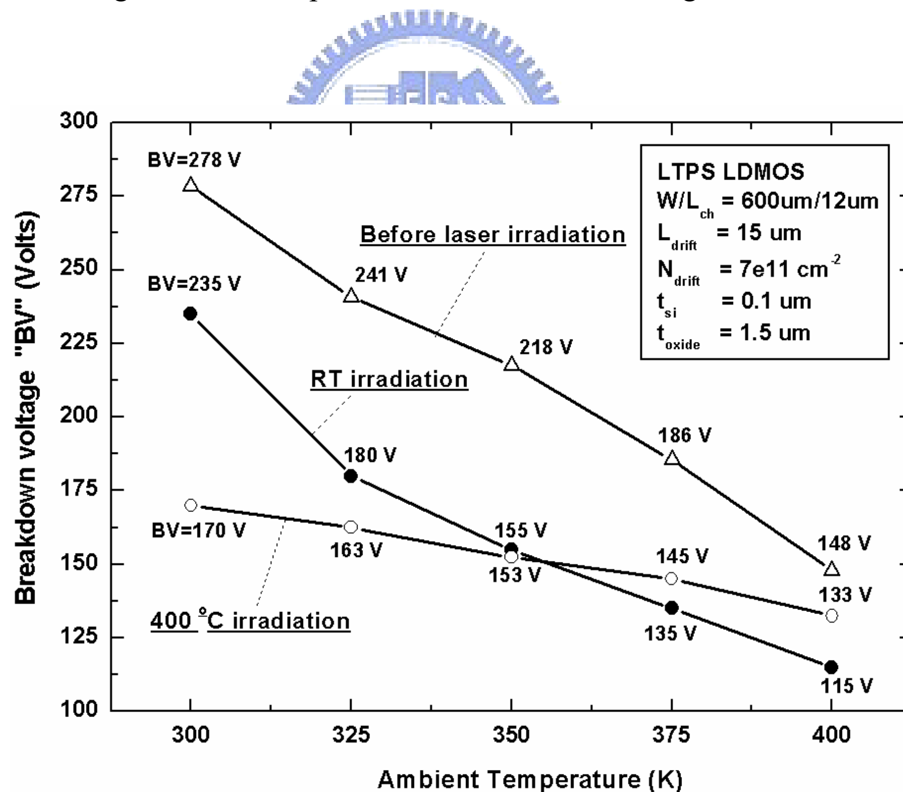

Fig. 6-12. Breakdown voltages of LTPS LDMOS at room temperature and 400 °C irradiations over the ambient temperatures from 300-K to 400-K.

400 °C irradiation. At the ambient temperature of 400 K, the breakdown voltage of room temperature irradiation was presented the 18 V difference compared with the breakdown voltage of 133 V at 400 °C irradiation. In summary, it was successfully proved that the breakdown voltage and specific on resistance at 400 °C irradiation exhibited the best reliability in different ambient temperatures with less variation even though its breakdown voltage was smaller than that at room temperature irradiation.

6.5 Summary

The ambient temperature effect in polycrystalline silicon LDMOS devices has been discussed with the single crystalline silicon LDMOS devices for the first time. The LTPS LDMOS at 400 °C irradiation exhibits superior characteristics with the higher I_{ON} current and lower I_{OFF} current as the increase in ambient temperature. For I_{ON} currents from the ambient temperature of 300 K to 400 K, the LTPS LDMOS at 400 °C irradiation demonstrates the less sensitivity with 3.68 times variation in ambient temperature than that at room temperature irradiation with 11.11 times variation. The threshold voltage variation of LTPS LDMOS at 400 °C irradiation is presented a smaller negative temperature coefficient of −27 mV/°C than that of −30 mV/°C at room temperature irradiation.

The subthreshold swing in LTPS LDMOS at 400 °C irradiation displays the superior characteristics with the smaller values against that in LTPS LDMOS at room temperature irradiation. The subthreshold swing at 400 °C irradiation is demonstrated about 3 times improvement with the less deviation of 0.01 V/decade-K against that of 0.03 V/decade-K at room temperature irradiation. The on current (I_{ON}), off current (I_{OFF}), and subthreshold swing (SS) were raised as temperature increased. However, the

threshold voltage (Vth) and specific on-resistance ($R_{on,sp}$) were exhibited the negative temperature relation. The breakdown voltage and specific on resistance at 400 °C irradiation exhibits the best reliability in different ambient temperatures with less variation even though its breakdown voltage is smaller than that at room temperature irradiation. The results of ambient temperature variation in LTPS LDMOS at 400 °C irradiation are demonstrated the less sensitivity than the LTPS LDMOS before laser irradiation and at room temperature irradiation. Hence, the LTPS LDMOS at 400 °C irradiation is very suitable for future system-on-a-panel (SOP) applications with higher temperature reliability.

Chapter 7

Summary and Conclusions

In this dissertation, the high performance integrated devices have been studied with the lateral double-diffused metal-oxide-semiconductor (LDMOS) and lateral insulated gate bipolar transistor (LIGBT) on silicon-on-insulator (SOI) structures. Many integration technologies, including of lateral device fabrication, silicon-on-insulator technology, Bipolar-CMOS-DMOS (BCD) design, and grain growth technique, have been used in order to achieve the target of system-on-a-chip. The Compatible BCD SOI-LDMOS design has been successfully developed for the realization of system circuit application with the integration of low voltage and high voltage devices. The advanced SOI-LDMOS has also been modeled with the step doping profile to attain the superior blocking capability for easy design than linearly graded doping profile. In order to implement the system-on-a-panel and three-dimensional integration, the lateral power LDMOS has been fabricated into the polycrystalline silicon by the excimer laser crystallization at room temperature and 400 °C irradiation. Finally, the temperature issues in the low temperature polycrystalline silicon (LTPS) LDMOS has been analyzed in comparison of single crystalline silicon LDMOS for further understanding the thermal problem between the future 3-dimensional interlayer devices.

In the chapter 2, a 450 V rating SOI-LDMOS integration has been demonstrated by traditional 0.5-μm Bulk-BCD technology for economy. The silicon film layer of 5-μm thickness, which is not too thick for easy isolation, is selected in order to obtain a wider process window, a higher breakdown voltage and a lower on-resistance at a suitable RF operation frequency (MHz range to GHz range) than those of the thin films. Although

the extended drift length was expected to obtain a higher blocking capability, the breakdown voltage was still sustained at a constant value of 461.5 V as the drift length increased. It was attributed that the vertical breakdown voltage limited the maximum breakdown voltage above 40-μm drift length in this SOI structure. The metal extension in blocking voltage enhancement has a limit until affecting the electric field distribution in the drift region and will increase the drain capacitance (Cd) so as to decay the operation speed.

The power limit line is moved from a snapback boundary to the maximum DC thermal dissipation due to its small area as well as its large power density (1.27 W, 2636.3 W/cm^2). The switching times are mainly wasted at the load and transistor because the gate capacitance (Cgs) is only 5.86 pF from the Taurus extraction (70 nF/cm2, L=9-μm, W=930-μm). The compatible SOI LDMOS exhibits rudimentary electrical characteristics with a specific on-resistance of 248.82 mΩ-cm^2, a breakdown voltage of 461.5 V, a turn-on time of 420 ns, a maximum f_{max} of 220 MHz and a maximum f_T of 124 MHz at a high-voltage bias of Vgs=1 V and Vds=20 V.

However, to investigate all characteristics in high power, high speed and high frequency operations, suitable data should be chosen under non-optimum conditions due to the trade-off relationship between them. Thus, the main purpose of the experiment is to give complete information that the conventional Bulk-BCD technology can possess a wider range of applications through the use of SOI wafers without modifying any processes for HVIC switches, power amplifiers, HID lamps and RF power supply applications.

In the chapter 3, a partition method has been developed to model the high-voltage silicon on insulator lateral insulated gate bipolar transistor (SOI-LIGBT) devices by the step doping profile at the first time. The use of partition method is successful to explain the underlying reverse-bias performance, attain 50.7 % improvement of the breakdown

voltage compared with the uniform doping, and decrease the undesirable additional masks in the step doping SOI devices. To achieve higher breakdown voltage, the difference between maximum and minimum electric fields must be eliminated in each frame. For this reason, a degraded factor "D" is provided to ensure near ideal-breakdown voltage and the least frame numbers as expected.

The thicker buried oxide and shorter drift length will promote smaller number of frames, especially if the SOI layer thickness is large enough. This makes it possible to reduce production cost. The optimum value of 0.6 is corresponding to the "three frames", which is chosen under economical consideration. The highest impact ionization rate is found at the third (last) frame, where the value "IVert" is about 0.9 while substituting the voltage 660 into the value of "V". The breakdown voltage is over the prediction with only about 8.9 % of the MEDICI simulation value. The ranges of data variation are available from –5 % to 5 % in surface potential part and –20 % to 20 % in surface electric field part.

It can also be implemented in the vertical devices by multi-epitaxy or multi-implanted technology without any additional masks, and superior device characteristics can be achieved as well. This method offer the designers with a choice between the step doping required more mask and the linearly graded doping required longer thermal process flexibly. Although the electric characteristics of step doping SOI-LIGBT can also be simulated by the ISE™, TMA™ or SIVALCO™, the simple equation is beneficial for designers to plan the structure architecture by the software of mathematica™ on a cheap personal computer or notebook computer everywhere instead of running the program with the expensive and heavy workstation.

In the chapter 4, the high-performance LTPS HVLDMOS is successfully fabricated using the excimer laser crystallization process. The films produced have a maximum grain size of 3-μm with strong (111) crystallographic orientation and a mono-modally

distributed grain size of 1.5-μm, on average. The threshold voltage after/before laser treatment is not changed at 4 volts due to the similar well concentrations, which replaced the channel defects domination in the intrinsic well region. The subthreshold swing (SS) is significant improved from 16.15 V/decade to 1.36 V/decade after laser treatment. The ON/OFF current ratios (I_{ON}/I_{OFF}) after laser treatment show the excellent promotion with the magnitudes of 3.73×10^5 and 2.37×10^6 against the magnitudes of 1.71 and 1.93 before laser treatment at Vds=5 V and Vds=25 V.

The ON/OFF current ratios and its variations before excimer laser treatment are entirely much smaller than those after excimer laser treatment as the increase in the drift length. The ON/OFF current ratios variation at drain bias of 25-V is smaller than that at drain bias of 5-V so that the variations can be suppressed by higher drain voltage as the drift length extension. The current driving capability of LTPS HVLDMOS after laser treatment exhibits the superior characteristics in the subthreshold swing, I_{ON}/I_{OFF} ratio, SOA, on-state resistance, maximum power limit, and latch-up voltage than that before laser treatment. The specific on resistance of 29 Ω-cm^2 at 300-V (L_{drift}=25-μm) after laser treatment is lower about 10^5 times than that of 1.9×10^6 Ω-cm^2 at 315-V (L_{drift}=20-μm) before laser treatment.

The LTPS HVLDMOS after laser treatment shows the better characteristics with 1.78 Ω-cm^2 at 240-V (L_{drift}=15-μm) compared to the SI HVTFT with 3.5 Ω-cm^2 at 230-V, MFP HVTFT with 1.17 Ω-cm^2 at 125-V, and OD HVTFT with 10 Ω-cm^2 at 115-V. It possesses the superior current capability and blocking capability by the combination technology of power devices and thin film transistors. It is also verified that the eximer laser crystallization is very important to obtain the extreme current capability against the previous HVTFT structures. The LTPS HVLDMOS after laser treatment is attractive for the future 3-D circuit integrations and SOP applications.

In the chapter 5, a new power device called LTPS LDMOS is reported for the first

time to attain the high driving and high blocking capability with the excimer laser annealing at 400 °C substrate heating. The LTPS LDMOS presents a higher threshold voltage of 4-V due to the doped P-well region with a dose of 3 $\times$ 10^{13} cm^{-2} which is beneficial to increase the threshold voltage and operate stably. The subthreshold swing is reduced from 1.15 V/decade at 400 °C irradiation to 1.18 V/decade at room temperature irradiation. It is revealed the finite improvement of 2.5 % by 400 °C irradiation. The ON/OFF current ratios through 400°C irradiation are further increased from 2.19 $\times$ 10^4 to 2.96 $\times$ 10^5 at Vds=0.1 V and 1.23 $\times$ 10^6 to 6.72 $\times$ 10^6 at Vds=10 V, which are indicated about 14 and 5 times improvements for the room temperature ones, respectively.

At the short drift length, the magnitude of on-currents is determined on the quality of polycrystalline silicon film. As the drift length increases, the device current mechanism will be predominated by the long drift length which increases the number of grain boundaries, and non-linearly accelerates the total resistances in devices. Thus, the advanced growth technology for large grain size is necessary to reduce the number of grain boundaries in the drift region and promote the device performance. The device can handle a much higher current of 10mA, and a better power limit of 1.11 Watts. The safe operating area (SOA) can be improved about twice (1.5 times) with 2 times enhancement of the maximum $R_{DS,on}$ current and 0.75 times degradation of maximum voltage by the 400 °C irradiation relative to that at room temperature (RT) irradiation.

While crystallizing at 400 °C, the Ron,sp of room temperature irradiation can be further reduced around 3 times from 1.78 ohm-cm^2 to 0.54 ohm-cm^2 at the optimal laser conditions of 470 mJ/cm^2 and 435 mJ/cm^2, respectively. The proposed LTPS LDMOS at room temperature and 400 °C irradiation exhibit the excellent breakdown voltages of 240-V and 180-V against the conventional OD TFT, VDS TFT, and c-Si LDMOS with breakdown voltage of 155-V, 152-V, and 145-V, respectively. The resultant

characteristics for the 400 °C annealing ones are even very close to the c-Si LDMOS. Hence, the proposed LTPS LDMOS devices are very suitable for future system-on-a-panel (SOP) applications.

In the chapter 6, the ambient temperature effect in the single crystalline and polycrystalline silicon LDMOS devices have been discussed for the first time. The LTPS LDMOS at 400 °C irradiation exhibits superior characteristics with the higher I_{ON} current and lower I_{OFF} current as the increase in ambient temperature. For I_{ON} currents from the ambient temperature of 300 K to 400 K, the LTPS LDMOS at 400 °C irradiation demonstrates the less sensitivity with 3.68 times variation in ambient temperature than that at room temperature irradiation with 11.11 times variation. The threshold voltage variation of LTPS LDMOS at 400 °C irradiation is presented a smaller negative temperature coefficient of −27 mV/°C than that of −30 mV/°C at room temperature irradiation.

The subthreshold swing in LTPS LDMOS at 400 °C irradiation displays the superior characteristics with the smaller values against that in LTPS LDMOS at room temperature irradiation. The subthreshold swing at 400 °C irradiation is demonstrated about 3 times improvement with the less deviation of 0.01 V/decade-K against that of 0.03 V/decade-K at room temperature irradiation. The on current (I_{ON}), off current (I_{OFF}), and subthreshold swing (SS) were raised as temperature increased. However, the threshold voltage (Vth) and specific on-resistance ($R_{on,sp}$) were exhibited the negative temperature relation. The breakdown voltage and specific on resistance at 400 °C irradiation exhibits the best reliability in different ambient temperatures with less variation even though its breakdown voltage is smaller than that at room temperature irradiation. The results of ambient temperature variation in LTPS LDMOS at 400 °C irradiation are demonstrated the less sensitivity than the LTPS LDMOS before laser irradiation and at room temperature irradiation. Hence, the LTPS LDMOS at 400 °C

irradiation is very suitable for future system-on-a-panel (SOP) applications with higher temperature reliability.

Chapter 8

Future Prospects

There are many interesting and importance researches that are valuable for further studies in the low-temperature polycrystalline silicon lateral double diffused metal oxide semiconductor (LTPS LDMOS) devices about future system-on-a-panel (SOP) and three-dimensional (3-D) circuit integration.

(1) The LTPS LDMOS at room temperature and 400 °C irradiation have uncompleted electrical measurements such as hydrogenation, direct current (DC), and alternating current (AC) stresses. For hydrogenation treatments, the device performance will show a lower threshold voltage and better subthreshold swing because the hydrogenation can be efficient to passive the trap state density at the grain boundaries [8.1], [8.2]. For DC stress measurements, the degradation characteristics can be tested with the parameters of threshold voltage, drain current, blocking voltage, and so on. A relationship between the effect of the hot carriers and the kink effect was discussed under DC stress. For this reason, reliability engineers have come to realize that DC stress testing, where the transistor is always on, grossly underestimates device lifetime. However, for AC stress measurements, when the LTPS LDMOS is stressed by periodically interrupted signal in normal frequency-dependent circuit operation, the degradation is at least partially recovered and lifetime is restored. The interface traps generated during the on state of the transistors are partially annealed during their off state.

(2) There are many structures that can be used to improve the LTPS LDMOS

performance—such as using the step doping profile, linearly graded doping profile, and super-junction in drift region; using MFP and SIPOS for additional test; using the conductivity modulation method to further enhance current driving; using copper metallization for thermal dissipation and low connect resistance.

The linearly graded and step doping profile can provide more uniform electric filed distribution along the drift region and so to optimize the RESURF condition. The superjuntion design can reduce the tradeoff between the specific on-resistance and breakdown voltage by the charge balance condition [8.3]-[8.7]. The different layout designs—such as interdigitated, hexagonal, square, and lattice arrangements—will also benefit to optimize the on-resistance [8.8]. The metal-field-plated (MFP) can directly modulate the conductivity of the drift region [8.9]-[8.12]. The semi-insulating (SI) can extend the electron accumulation layer in the on-state and smooth the potential distribution in the off-state across the entire drift region [8.13]. The conductivity modulation method can reduce the on-state resistance resulting in a significant increase in on-state current [8.14], [8.15]. The minority carriers are injected into the offset region and then the existence of minority carriers reduce the barrier height formed among the grain boundaries. Thus, the flows of both electrons and holes can be enhanced in the offset region. Additionally, the conductivity modulation in p-channel devices degrade the transient behavior compared to the conventional devices because the high trap density in polysilicon film shorten the minority carrier storage effect and its lifetime. The conductivity modulation method with semi-insulating structure can increase the on state current by a factor of 5 and reduce the turn on time over 10 % due to high driving capability compared to that of semi-insulating structure [8.16] Minority carrier stage does not significantly deteriorate the turn-off time due to high trap density in the offset region different from single crystalline silicon

devices. Additionally, it is worth to mention that the low carrier injection will not improve the on state performance and the high carrier injection will significantly degrade the off state blocking ability. Therefore, the level of minority carrier injection should be optimized by adjusting the applied biases, doping concentration, and material parameters like the minority carrier lifetime. The copper metallization can be used for thermal dissipation and low connect resistance to avoid the failure in interconnect at silicon-metal contact [8.17]. A backside drain contact allows for minimum lead inductance and also a greater area on the drain side, which help in dissipating the heat.

(3) In order to avoid the grains arrange randomly, the recessed-channel structure, and other lateral growth method can be attempted to use in the LTPS LDMOS [8.18]. When the supper lateral growth (SLG) mechanism is triggered, large (>1 μm) grains are formed and this crystallization regime appears very attractive from the device fabrication point of view. However, the SLG has a very narrow energy density window and, consequently, high uniform laser beam profiles and pulse-to-pulse stability are required to better than 2 %. Several approaches are to control the lateral solidification by inducing lateral thermal gradients [8.19], [8.20] or by sequential lateral solidification (SLS) [8.21]-[8.24]. Another approach is the combined use of solid phase crystallization (SPC) and excimer laser annealing (ELA) techniques [8.25].

(4) In order to obtain large grain size, continuous wave (CW) laser can be used with the laser light emitted in an uninterrupted beam. Excimer is a compound word describing an excited dimer laser. A dimer is a compound formed by two identical molecules. The excited dimer is "pumped" by an energy source to become excited to emit photons of a selected wavelength. In the case of excimer laser crystallization (ELC), the random grain boundary distribution results in the

inhomogeneous characteristics of integrated circuits. The seeds of growth are nuclei randomly generated at the Si/buried-oxide interface and the solidification proceeds radial from nuclei. For continuous wave laser lateral crystallization (CLC), it allows the crystal growth so large as $3 \times 20\ \mu m^2$ which exceed 5-μm and about 4 times larger than the grains made by excimer laser [8.26], [8.27]. The seeds vertically stand in the solid/liquid interface of Si layer and the solidification proceeds uniformly along the scanning direction of CW laser which leads to a long shaped grain growth apparently larger than the size of ELC poly-Si.

(5) Generally, in order to enhance the blocking voltage, the single crystalline silicon carbide (c-SiC) films have been development at high temperature of 500-800°C due to its higher critical electric field of 2.3×10^6 V/cm than that of Si with 3×10^5 V/cm [8.28]-[8.30]. The high resistance characteristics have been solved by superjunction structure on SiC materials [8.31]-[8.33]. However, it is not suitable for low temperature process of future 3-dimensional circuits integrations. Therefore, the amorphous silicon carbide films can be obtained by low-pressure vapor deposition (LPCVD) or plasma-enhanced vapor deposition (PECVD) at deposition temperature as low as room temperature, which allow depositing on variety of substrate [8.34]-[8.37]. It is also a good choice to use the electron cyclotron resonance (ECR) for fabricating the high quality silicon carbide films [8.38]-[8.40].

Another popular material is SiGe which have been widely used in polysilicon thin film transistors in order to enhance the driving current [8.41]-[8.44]. The mobility can be enhanced by Ge doping technique or strain layer formation [8.45]-[8.51]. By Ge doping technique of $Si_{1-x}Ge_x$, the hole mobility can be improved about 18 % at Ge fraction of x=0.12 and about 12 % at Ge fraction of x=0.09, respectively. This SiGe technique has also been applied in high voltage

poly-Si devices—such as poly-Si/$Si_{1-x}Ge_x$/Si sandwiched conductivity modulated thin film transistors (CMTFTs) [8.52]. The sandwiched CMTFT structures can avoid the poor interface between the gate oxide and poly-$Si_{1-x}Ge_x$ material [8.53]-[8.55]. The p-channel sandwiched CMTFT has 60 % current improvement than that of the poly-Si CMTFT due to the high hole mobility in the poly-$Si_{1-x}Ge_x$ film from the band discontinuity in the valence band confined holes (hole channel formation). However, the n-channel sandwiched CMTFT exhibits a 3.3 times lower driving current than that of poly-Si CMTFT due to the high trap density in the sandwiched poly-Si film. Thus, it is worth to mention that the SiGe materials may be only suitable for fabricating the p-channel thin film transistors than n-channel ones.

(6) Finally, the fundamental three-dimensional (3-D) device structures can be initially fabricated by the above new technology.