Effects of Isolation Oxides on Undercut Formation and Electrical Characteristics for Silicon Selective Epitaxial Growth

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ABSTRACT

Three isolation oxide structures have been prepared to study their resistance to the undercut formation during selective epitaxial growth (SEG) processes. The N_2O annealed oxide tetraethyoxysilane (TEOS) oxide stacked structure has the best resistance to the undercut formation and exhibits the best electrical characteristics compared to the other two isolation oxide structures prepared in the study, which are a wet oxide and a TEOS oxide. This is ascribed to a smaller interfacial stress between the isolation oxide and the silicon substrate for the stacked structure. The sidewall damage is the predominant factor deteriorating the current-voltage (I-V) characteristics of the N^+-P SEG diodes. When treated with a quick HF dip and followed by a low temperature desorption cleaning before the SEG process, the N^+-P SEG diode, which has no perceivable undercut, shows satisfactory I-V characteristics.

Introduction

Selective epitaxial growth (SEG) is one of the potential technologies for fabrication of novel structures for ultra-large scale integrated (ULSI) devices.[1-4] SEG represents an alternative to localized oxidation of silicon (LOCOS) for high density ULSI isolation.[5] Other applications of SEG include the formation of raised source/drain structure,[4,6,7] and the formation of retrograde wells in N-well and P-well CMOS devices without using ion implantation.[8] Unlike SEG in the conventional low-pressure chemical vapor deposition (LPCVD) system, of which the growth temperature is higher than 800°C, the growth temperature of ultrahigh vacuum chemical vapor deposition (UHV CVD) can be reduced to a temperature lower than 600°C.[9] A lower growth temperature may reduce thermal stress and improve the sidewall SEG material quality.[10] Before growing an SEG film, one has to do *ex situ* cleaning and *in situ* cleaning on the Si substrate. The *ex situ* cleaning can remove the dry etching damage and reduce the surface residuals, such as organic, metals, and carbon. The purpose of the *in situ* cleaning is to remove the RCA regrown oxide or native oxide before SEG. The most convenient and readily adaptable methods is high temperature thermal desorption or high temperature H_2 prebake. However, for the SEG process in an etched oxide window, this *in situ* cleaning step must be carefully controlled at low temperatures since the substrate surface now contains etched oxide features with the exposed Si-SiO_2 interface. Oxide undercut can be formed at the periphery of the oxide pattern at high temperature. The presence of the oxide undercut will increase the reverse leakage current at junctions, and degrade I-V characteristics. In addition, the high temperature process may cause surface damage in the Si layer and, therefore, cannot meet the low temperature trends for ULSI device fabrication. Hence, the Si SEG by UHV-CVD combining with low temperature *in situ* and *ex situ* cleaning processes is suitable for ULSI technologies.

In our previous works[11] we have obtained a clean Si surface in the patterned oxide windows for SEG using an efficient and convenient after-etching treatment with a CF_4/O_2 low energy plasma without the high temperature sacrificial oxide growth. In this study, we discuss the effects of different isolation oxides on undercut formation and I-V characteristics. The new process flow can suppress the undercut at the periphery of the oxide region and high quality SEG layers can be obtained.

Experimental

Boron-doped, (100), 6 in. Si wafers with a resistivity of 25 to 35 Ω-cm were used. Three different isolation oxides prepared in the study. For clarity, preparation conditions for the studied samples are listed in Table I. Sample A and D are prepared by wet thermal oxidation at 980°C in furnace. Sample B has a TEOS isolation oxide deposited at 700°C in an LPCVD system without the densifying step. For sample C, the nitrided oxide was prepared by oxidation in dry O_2 ambient at 900°C followed by an anneal in N_2O for 20 min at the same temperature. The nitrided oxide has the final thickness of 10 nm. Right after the nitrided oxide formation, TEOS oxide was deposited at 700°C in the LPCVD system without the densifying step. After oxide formation, wafers were patterned. The etching step was carried out in the RIE system, which is composed of two chambers using $CF_4/CHF_3/Ar$ and CF_4/O_2 gas mixtures, respectively. Using an efficient and convenient after-etching treatment with CF_4/O_2 low energy plasma, defects and contaminants induced by the RIE process can be removed without high temperature sacrificial oxide growth, a clean Si surface in the patterned oxide windows for SEG can be obtained.[11] Following the photoresist removal, two cleaning methods listed below were used before the N^+ Si SEG at 650°C.

Samples A, B, and C were dipped in a modified SC1 solution ($NH_4OH:H_2O_2:H_2O$ = 1:6:20 at 75°C, for 10 min) before being loaded into the UHV-CVD system. Before the SEG, the wafer received a thermal treatment at 950°C for 10 min. The regrown oxide formed during the wet cleaning was vaporized in the *in situ* thermal cleaning process. The base pressure of the UHV-CVD system was 2×10^{-10} Torr. Sample D was dipped in a solution of $HF:H_2O$ = 1:10 for 10 s without any further deionized (DI) water rinse after a wet cleaning procedure similar to the one described above.

Table I. Preparation conditions for the four samples before the Si SEG deposition.

	Isolation oxide materials			Cleaning methods	
	Wet oxide	TEOS oxide	N_2O annealed oxide/TEOS oxide	Modified SC1 cleaning + 950°C/10 min	Modified SC1 cleaning and HF-Dip + 850°C/1 min
Sample A	√	—	—	√	—
Sample B	—	√	—	√	—
Sample C	—	—	√	√	—
Sample D	√	—	—	—	√

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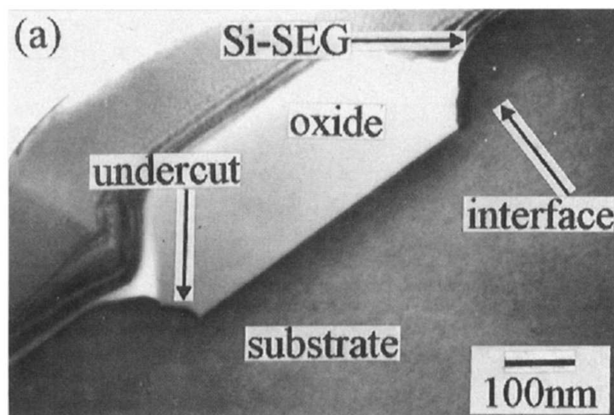
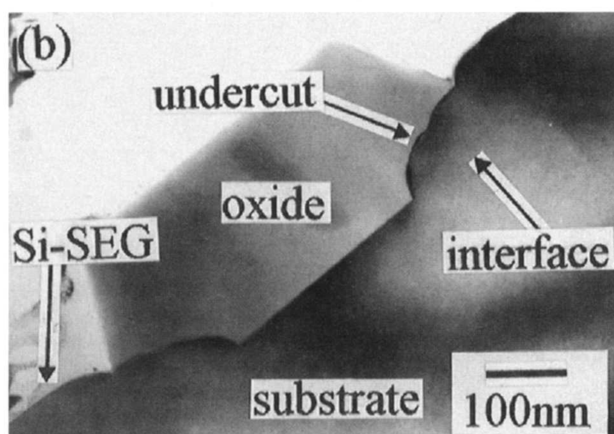
Then, a relatively low temperature *in situ* thermal cleaning at 850°C for 1 min was performed before the epi layer deposition.

After the above mentioned cleaning process, wafers were cooled down to the growth temperature. The gas mixture used in the SEG is composed of Si_2H_6 (1 sccm) and 0.1% PH_3/H_2 (1 sccm). Cross-sectional transmission electron microscopy (XTEM) was used to study the formation of undercut. After metal electrode deposition and patterning, we used HP4145B to measure I-V characteristics of the N^+-P SEG diodes.

Results and Discussion

Effects of different isolation oxide materials.—Figure 1a, b, and c show XTEM micrographs of Si SEG layers deposited at 650°C for 10 min with a Si_2H_6 flow rate of 1 sccm for samples A, B, and C, respectively. For sample A, an oxide undercut of about 80 nm was observed shown in Fig. 1a, and a clean interface between the Si SEG layer and the Si substrate was obtained. The undercut results from the *in situ* thermal cleaning before the SEG process. An XTEM micrograph for a patterned oxide (wet oxide) which received the same *in situ* thermal treatment but without the SEG deposition is shown in Fig. 2. In the *in situ* thermal cleaning (950°C for 10 min in UHV), the regrown oxide after wet cleaning can be removed from the Si surface by the reaction of $Si + SiO_2 \rightarrow 2\ SiO(\uparrow)$; where Si atoms are provided by the Si substrate and SiO_2 is from the regrown oxide.[12] Due to a higher mechanical stress, decomposition of SiO_2 at the periphery of the patterned region is likely to occur more easily than other open areas, and thus crevices can be created at the adjacent region between the SiO_2 and the exposed Si surface. Once crevices are developed at the periphery, the volume of crevices inside the SiO_2 continuously grows in terms of the same decomposition reaction; where Si atoms are supplied by the exposed Si surface via fast surface self-diffusion.[13] In addition, the high temperature thermal cleaning process may induce damages and defects in the structure. The influence of the defects on the I-V characteristics for N^+-P SEG diodes is discussed later. An oxide undercut of about 170 nm in size was observed in sample B, while a clean interface between the Si SEG layer and the Si substrate was obtained. Because TEOS is less dense than the wet oxide, and the stress of the TEOS oxide (−70 MPa) at the interface with the substrate is larger than that of the wet oxide (−22 MPa), the decomposition rate of TEOS must be larger than that of wet oxide due to a lower reaction barrier for oxide decomposition for the TEOS oxide. Therefore, undercut is more liable to be developed on the TEOS isolation oxide than the thermal oxide. For sample C, (N_2O annealed oxide/LPCVD TEOS stacked structure), an oxide undercut of about 40 nm is shown in Fig. 1c, and a clean interface between the Si SEG layer and the Si sub-





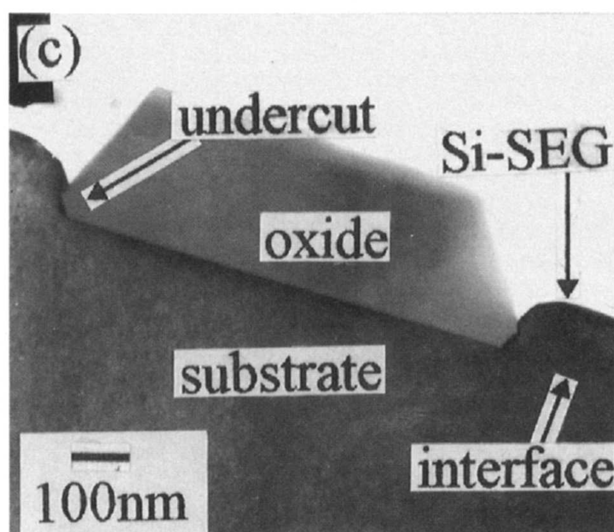


Fig. 1. Cross-sectional TEM micrographs of Si SEG layers deposited at 650°C for 10 min with a Si_2H_6 flow rate of 1 sccm for (a) sample A, (b) sample B, and (c) sample C. The thickness of the epi layer is about 100 nm.

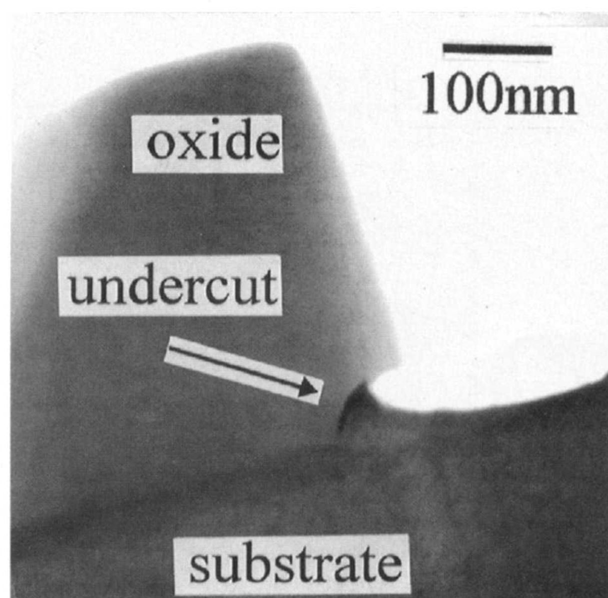


Fig. 2. Cross-sectional TEM micrograph of the sample treated with high temperature thermal cleaning (950°C for 10 min in UHV) without the SEG deposition.

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strate was observed. Because the undercut is created via reaction between the oxide and Si atoms at the peripheral area of the oxide window. Increasing the oxide strength and relieving the stress at the interface can resist the undercut formation. It has been reported that a thermal/CVD oxide stacked structure can reduce the stress at the interface between the thermal oxide and the Si substrates.[14] Therefore the thermal oxide/LPCVD TEOS stacked structure is good to suppress the undercut formation. On the other hand, extensive researches on N_2O-annealed oxide have revealed that the dielectric is an excellent candidate for gate oxides in future ULSI metal oxide semiconductor field effect transfer (MOSFET) devices as well as tunnel oxides for EEPROM applications.[15-18] Due to the accumulation of nitrogen at the Si/SiO_2 interface, stress relief at the Si/SiO_2 interface and suppressed process-induced damage are the advantages. Hence, in this study, the stacked isolation oxide is the best structure to suppress undercut formation. For raised source/drain MOSFET applications, the N_2O annealed oxide is prepared for the gate oxide and the TEOS oxide can be used as the oxide spacer.

Figure 3 shows I-V characteristics of N^+-P SEG diodes prepared with samples A, B, and C. The patterned window is 2000 × 2000 μm in size. We find that sample C has the smallest reverse leakage current and the largest slope in the forward bias region. Oppositely, sample B has the largest reverse leakage current and the smallest slope in the forward bias region. According to the XTEM micrographs in Fig. 1 all the three samples have perfect Si SEG layers and a clean interface between the Si SEG layer and the Si substrate. The obvious difference in I-V characteristics for the three diodes is very likely due to the formation of the undercut. Sidewall defects are considered as the major problem hindering the widespread use of SEG in semiconductor processing.[10] Defects may result in undesirable recombination-generation currents when junctions and depletion regions intersecting these sidewalls.

The reverse leakage current density as a function of the P/A ratio for different processes is shown in Fig. 4, where P is the perimeter length and A is the junction area. The reverse leakage current can be considered as a total of the leakage current of the exposed area and the peripheral region, and can be expressed as $I_R = J_A \times A + J_P \times P$, where J_A (nA/cm^2) is the area leakage current density and J_P (nA/cm) is the perimeter leakage current density. J_A can be extracted from the intercept of the Y-axis and J_P can be extracted from the slope of the regression line. Compared to the total area of the pattern window, the increase of the periphery area and the junction area due to the undercut formation is negligible. While all the three samples have a similar J_A value, sample C has the smallest J_P of the three samples and sample B has the largest J_P among the three samples. Since the differences among the three samples in J_P is larger than that in J_A, the sidewall damage resulting from the undercut formation is a major factor to degrade I-V characteristics. Apparently, a proper oxide layer, such as sample C, has a good I-V characteristics since the tendency to the undercut formation is suppressed. Table II lists the leakage current, the ideality factor, J_A and J_P for all samples.

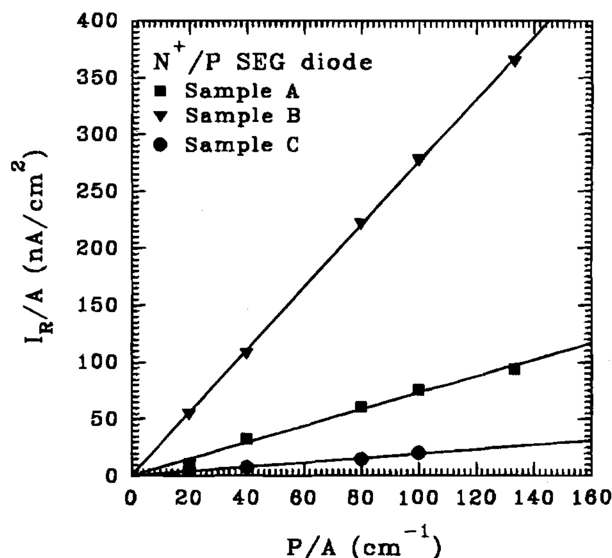

Fig. 4. Reverse leakage current density as a function of the *P/A* ratio for sample A, B, and C.

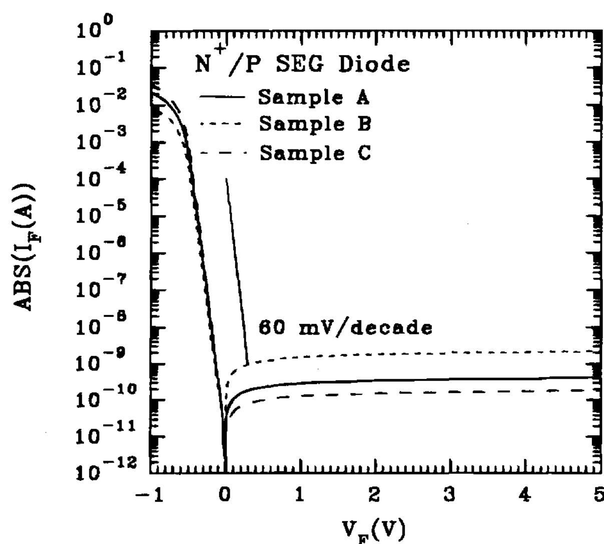

Fig. 3. *I-V* characteristics of N^+-P SEG diodes with an oxide patterning window of 2000 × 2000 μm for sample A, B, and C.

Effects of cleaning methods.—Because *in situ* thermal cleaning at high temperatures will lead to the undercut formation, developing a low-temperature cleaning methods is necessary to improve the performance of SEG diodes. Unlike sample A, B, and C, sample D, which uses wet oxide as the isolation oxide, has been dipped in an HF solution and treated with 850°C heating for 1 min. No perceivable oxide undercut was found in sample D and a clean interface between the Si SEG layer and the Si substrate can be obtained according to the XTEM micrograph shown in Fig. 5. For samples A, B, and C, the Si surface is protected by a relatively thick regrown oxide after wet cleaning. However, for sample D, a hydrogen-passivated surface obtained after the HF dip and a negligible regrown oxide is formed on the Si surface. The predominant passivating species is silicon hydride, and the Si surface is stable in air and free of SiO_2 for several minutes.[19-22] After a thermal cleaning process, the Si-H bonds will be broken, and a clean Si surface is obtained. Therefore, a relatively high temperature thermal cleaning was not necessary. I-V characteristics of the N^+-P SEG diodes for samples A and D are shown in Fig. 6. Sample D has a smaller reverse leakage current and a relatively large slope in the forward

Table II. *I-V* characteristics of N^+-P SEG diodes prepared from the four samples.

	Sample A	Sample B	Sample C	Sample D
Leakage current (at 5 V) Area = 4 × 10^{-2} cm^2	425 pA	2.22 nA	189 pA	44.1 pA
Ideality factor	1.05	1.07	1.03	1.02
J_A (nA/cm^2)	0.471	0.589	0.448	0.432
J_P (nA/cm)	0.728	2.751	0.194	0.0332

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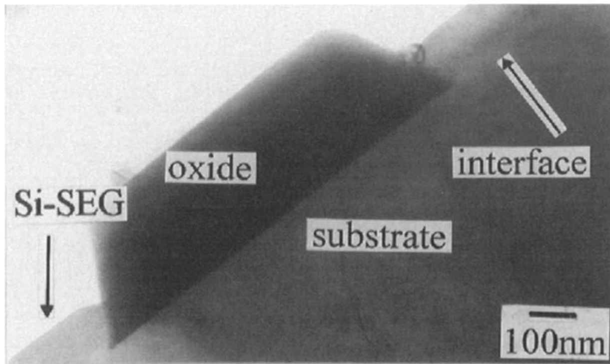

Fig. 5. Cross-sectional TEM micrograph of the Si SEG layer deposited at 650°C for 10 min with a Si_2H_6 flow rate of 1 sccm for sample D, which received an HF dip and a low temperature desorption cleaning. The thickness of the epi layer is about 100 nm.m

bias region than that of sample A. Figure 7 shows the reverse leakage current density as a function of the P/A ratio for samples A and D. Similarly, sample D has a smaller J_P than that of sample A, while both samples have a similar J_A. as shown in Table II. The difference between sample A and D in J_P is much larger than that in J_A. This again suggests that the sidewall damage is a predominant factor deteriorating the I-V characteristics. Without the undercut formation, sample D exhibits the best electrical performance for all samples.

Conclusion

Effects of isolation oxide materials on the undercut formation in N^+-P SEG diodes have been studied. Among the three isolation oxide materials, which are wet oxide, TEOS oxide, and N_2O annealed oxide/TEOS oxide stacked structure, the N_2O annealed oxide/TEOS oxide stacked structure exhibits the smallest undercut, and the best I-V characteristics. This is attributed to a better strength and a smaller interface stress for the stacked structure. In addition, we have concluded that the sidewall damage is a predominant factor deteriorating the I-V characteristics. With a hydrogen passivated silicon surface, an *in situ* low temperature (850°C) thermal cleaning is adequate to prepare a clean silicon surface for SEG by UHV-CVD. Alleviating the tendency to undercut formation and thermal sidewall damage, we are able to obtain an ideal N^+-p SEG diode, of which the ideality factor is 1.02, J_A is 0.432 nA/cm^2 and J_P is 0.0332 nA/cm.

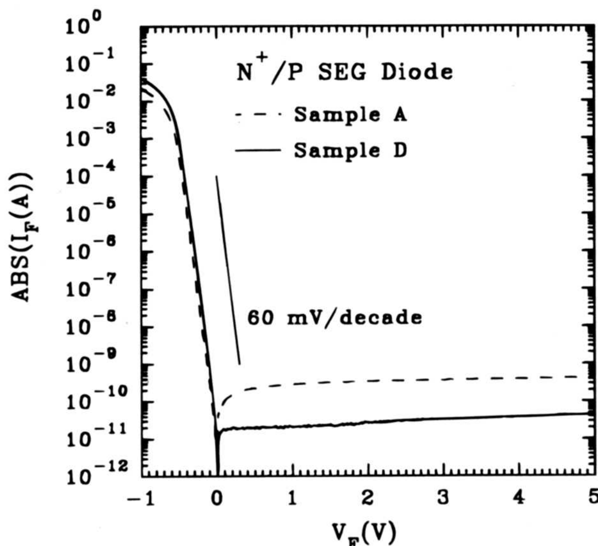

Fig. 6. I-V characteristics of N^+-P SEG diodes with an oxide patterning window of 2000 × 2000 μm for sample A and D.

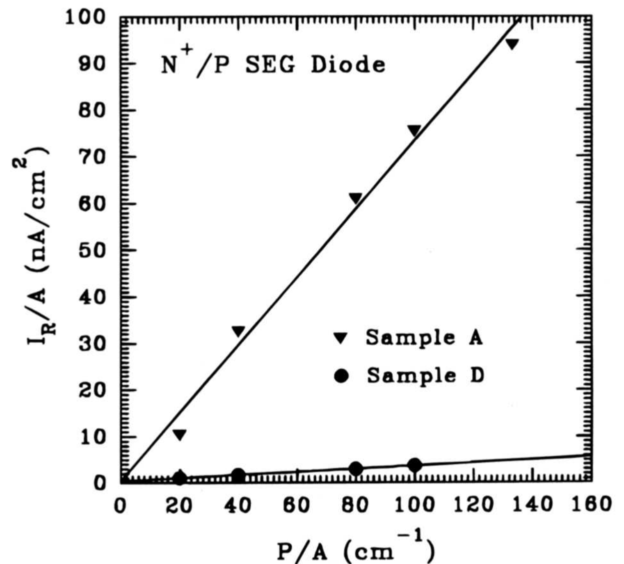

Fig. 7. Reverse leakage current density as a function of the P/A ratio for sample A and D.

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Assessment of Conditions Influencing Porous Si Electroluminescence

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ABSTRACT

Visible electroluminescence (EL) characteristics of porous Si formed on p, n, p^+-n, and n^+-p junction substrates are studied under pulse current regime. We provide experimental proof that porous Si structures characterized by highest EL intensity have simultaneously highest photoluminescence (PL) intensity and lowest surface roughness. PL and EL can be correlated via surface roughness. Two types of EL instabilities are observed: fast, with time constant in the milliseconds range and slow, with time constant in the hours range. The fast EL instability is affected by the type of ambient and/or sample temperature during electrical excitation and is likely to be associated with the charging of the porous network.

The observation of strong room temperature photoluminescence (PL) in porous Si[1] has generated immense interest in the development of porous Si based light emitting devices. A major obstacle to this development being the high resistivity (>10^5 ρ-cm) of porous Si.[2] It is extremely difficult to obtain efficient carrier injection in this material and therefore, electroluminescence (EL) efficiency of a solid-state porous Si diode is reportedly very low (10^{-6} to 10^{-3}%).[3-5] Although significant progress has been made in enhancing the EL performance of porous Si, primarily by improving the contact technology,[6,7] the EL characteristics are still not suitable for practical applications. Furthermore, the EL emission deteriorates over time under electrical excitation. It may be added that the PL emission from porous Si also exhibits decay under laser irradiation but its stability can be enhanced by a post anodic high temperature rapid thermal oxidation.[8] Adopting such a procedure is not conducive to porous Si EL because of higher resistivity of the oxide. In this work we compare the relative EL performances of porous Si formed on variety of substrates and show how EL, PL, and surface morphology are interrelated. EL (or current) degradation mechanism in porous Si and some techniques that influence EL durability are discussed.

Experiment

Porous Si layers were formed by the electrochemical anodization of different type of substrates, namely, p-type (3 to 5 ρ-cm), n-type (3 to 5 ρ-cm), p^+-n, and n^+-p junction type. The p^+-n and n^+-p substrates were formed by implanting 50 keV B (1e15 cm^{-2} dose) into n-type and 50 keV P (2e15 cm^{-2} dose) into p-type substrates, respectively. Implanted samples were annealed in flowing N_2 at 1000°C for 45 min for dopant activation and damage removal prior to anodization. The anodization parameters used in this study were: current density = 50 mA/cm^2, time = 5 min, $HF:C_2H_5OH:H_2O$ = 1:1:2, white light illumination = 100 mW/cm^2, and were held constant for all samples. On a particular type of substrate, the porous Si thickness was found to be very critical to the performance of a light emitting diode. Porous layers which were too thick resulted in very high diode resistance and layers which were too thin were weakly photoluminescent and did not exhibit detectable EL. The anodization condition for this study was chosen such that the porous layer of intermediate thicknesses were formed. The typical porous layer thicknesses for p^+-n and n^+-p samples were estimated to be 22 and 12 μm, respectively. Following anodization, semitransparent Au contacts (~130 Å thick) were evaporated on the porous surface for the purpose of EL measurements. The % transmission for the Au layer was estimated to be 50%. The back side of the substrate was Al evaporated prior to anodization. The PL spectra were recorded at room temperature using Ar laser (514 nm) as an excitation source at a power density of 160 mW/cm^2.

Results And Discussion

All samples investigated in this study exhibited EL emission under applied forward bias. No emission was observed under reverse bias suggesting that the observed EL is due to the recombination of injected carriers in the porous layer. The room temperature normalized EL and PL spectra for porous Si on a p^+-n substrate are shown in Fig. 1. EL has a narrower spectral distribution and while both the peaks are in the red region, the EL peak position is slightly blue-shifted compared to PL. Correlating EL and PL peak positions is difficult because PL peak posi-

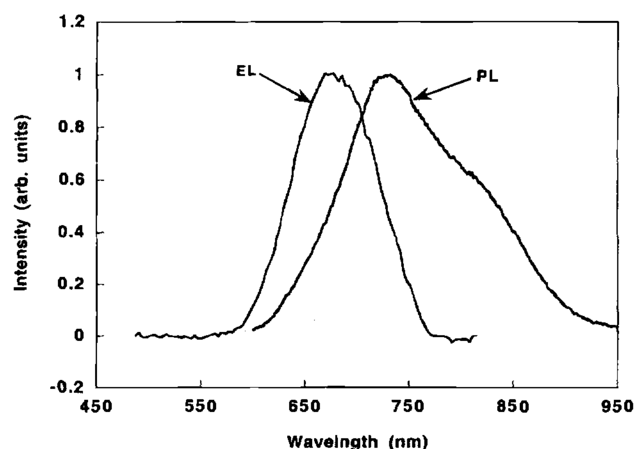

Fig. 1. The normalized room temperature EL and PL spectra of porous Si on p^+-n substrate.

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