Chapter 6

Triangular Current: Method for Measuring Hysteresis Loops of Ferroelectric Capacitors and Its Application

6-1. Introduction

Over the past few decades, various methods for obtaining the electrical polarization loops of capacitors have been presented [24-25, 28-29, 48]. The most often quoted method of hysteresis measurement is based mainly on the Sawyer-Tower method (STM) [24], which utilizes a sensing capacitor connected in series with the sample that collects the integrated current to determine the polarization charge. In the virtual ground method (VGM) [25], a technique of charge measurement, which converts current to charge, has recently changed from utilizing a large sensing capacitor to utilizing a virtual-ground operational-amplifier as a current-to-voltage converter with an integrating capacitor. More recently, Giacometti *et al.* proposed a CC method for obtaining the hysteresis loops of ferroelectric materials [28-29]. In this method, a constant charging current source is applied to a thick ferroelectric film (approximately 12 μm thick), to measure the corresponding voltage, which is almost noiseless.

In this chapter, we present a triangular current (TC) method, which applies a triangular charging current array to the specimen and measures the resulting voltage to derive the hysteresis loops of ferroelectric capacitors. For the comparison of the TC and CC methods, the CC method is utilized in the performance of the hysteresis measurements. Additionally, we adopted the TC method to perform the hysteresis measurement of a micron-sized $Pb(Zr,Ti)O_3$ ferroelectric capacitor (3 μm×3 μm) and also considered the parasitic effects of the probe setup. The parasitic capacitance (C_{para}) was determined by open contact measurement to yield the corrected hysteresis loops of the small-sized capacitors. The proposed method provides an approach for measuring the hysteresis loops of micro-sized ferroelectric capacitors. Moreover, application on the hysteresis measurements of metal-insulator-semiconductor (MIS) and metal-ferroelectric-insulator-semiconductor (MFIS) structures will be addressed. Furthermore, the temperature effect of switching current characteristics will also be discussed.

6-2. Experiments

$Pb(Zr_{0.3}Ti_{0.7})O_3$(PZT(30/70)) films 250 nm thick were deposited onto Pt(100 nm)/Ta(20 nm)/SiO2(100 nm)/Si substrates by a sol-gel-derived method (See chapters 2 and 5). The deposited films were then crystallized by annealing in a furnace at 600°C for 30 min in oxygen ambient. Then, 50-nm-thick platinum top electrodes were deposited onto the PZT films at room temperature by DC sputtering. A 20-nm-thick TiN layer was then deposited as a hard mask. Next, lithography and dry etching were applied to define the area of the capacitors. To remove the etching damage, postannealing was performed at 600°C for 1 min using rapid thermal annealing (RTA) in an O_2 atmosphere.

After the samples had been prepared, the capacitors were placed in contact with a needle having a tip radius of 0.2 μm. A triangular charging current with an optimized range was applied to a sample and the resulting voltage was measured using a Keithley 4200 semiconductor characterization system, to obtain its hysteresis loop. The hysteresis loop of a 100 μm×100 μm capacitor was also measured using the CC method to confirm the results obtained using the TC method.

6-3. Results and Discussions

The experimental procedures were mentioned in the previous section. In the following we will verify the TC method. The results of the TC method will also be compared with that of CC method. We will first compare charging current-measured voltage and hysteresis curves corresponding to both methods. Additionally, measured results with different step charging current and number of steps will be compared and discussed. Moreover, the performance on the measuring hysteresis loops of micro-sized ferroelectric capacitor and the effect of parasitic capacitance will be characterized. Furthermore, the P-V curves of MIS and MFIS structures are also investigated at low frequency of around 0.2 Hz. Finally, the temperature effect of switching current characteristics and hysteresis loops was addressed.

6-3-1. Verification of triangular current method

Figure 6-1(a) shows a complete cycle of positive and negative charging currents associated with the CC and TC methods. For both methods, the number of charging steps was fixed to 160 and a single cycle duration was approximately 0.69 s. The charging current for the CC method was approximately ± 20 nA and the step charging current for the TC method was approximately 1 nA. During these charging processes, the voltage profiles were recorded

simultaneously and the maximum resulting voltage was approximately ± 6.5 V. Figure 6-1(b) shows the measured voltage curves corresponding to both methods. It can be seen that a smooth voltage curve is found in the high-field region, when the TC method is utilized. For both methods, the voltage curves are virtually noiseless and plateau regions, which are strongly associated with the coercive voltage with which the dipoles are reoriented [28], are present in these measured voltage profiles.

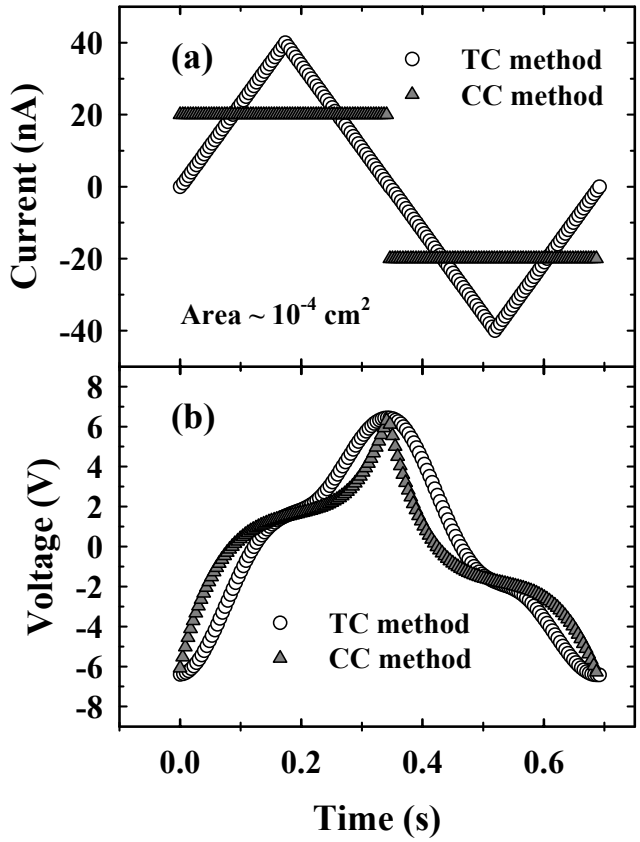

Fig. 6-1 (a) Constant charging current (solid triangles) and triangular charging current (open circles) versus time. (b) Measured voltage profiles obtained using the CC (solid triangles) and TC (open circles) methods, for 250-nm-thick PZT(30/70) film.

Figure 6-2(a) plots the charging current against the measured voltage obtained for both methods. The current-voltage plot for the TC method exhibits a peak current region near the coercive voltage, which is similar to the switching current-voltage plot of ferroelectric materials [48].

In contrast to the charging current of the CC method (2.0×10^{-8} A) or the maximum charging current of the TC method (4.0×10^{-8} A), the leakage current of the 100 μm×100 μm $Pb(Zr,Ti)O_3$ capacitor, which was approximately 3.0×10^{-11} A measured at a voltage of 6.5 V

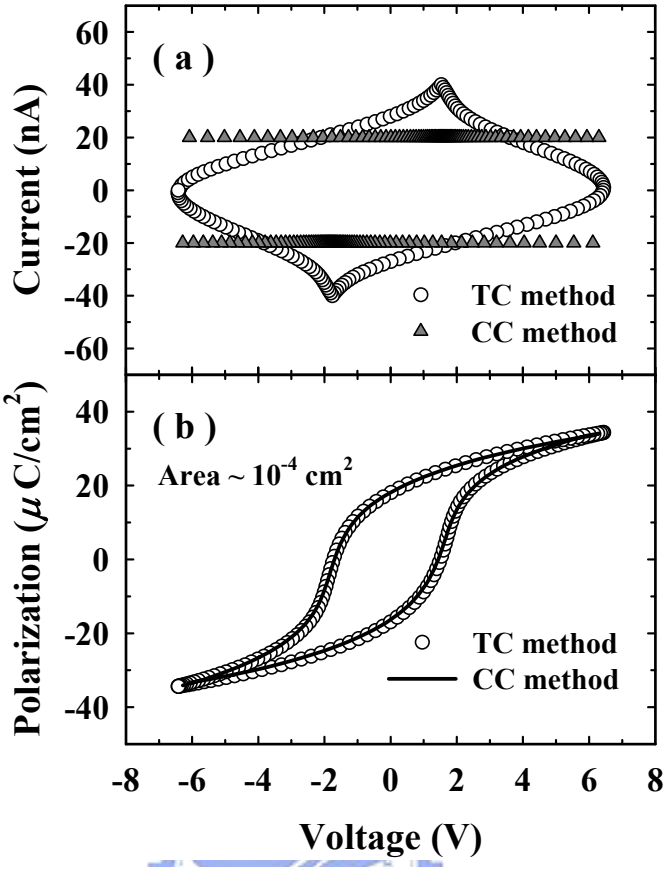

Fig. 6-2 (a) Charging current-measured voltage characteristics obtained using CC (solid triangles) and TC (open circles) methods. (b) Polarization-voltage (P-V) plots obtained using CC (full line) and TC (open circles) methods. Area of sample was 10^{-4} cm^2.

with a delay time of 1 s, was considerably smaller and can be neglected. In the case of a negligible conduction current I_C, the total current for both methods $I(t) = A \times dD(t)/dt + I_C$ can be written as [28-29]

$$I(t) = A\frac{dD(t)}{dt}, \tag{4-1}$$

where $D(t)$ represents the dielectric displacement, A is the area of the specimen, and t is the time. Using integral calculus ($D(t) = (1/A)\int I(t)dt$), the dielectric displacement can be calculated from the charging current of these methods. Figure 6-2(b) shows the hysteresis plots obtained using the CC and TC methods. The two plots are almost the same, even though the charging profiles differed.

6-3-2. Effect on step charging current and number of step

Figure 6-3 shows the polarization-voltage (P-V) curves for various step charging currents (I_S), obtained by adjusting the step charging time (t_S). For these measurements, the total number of charging steps was fixed to 160 and the maximum charging current was approximately $40 \times I_S$. The step charging current and the single cycle duration were changed from 1.0×10^{-9} A to 1.0×10^{-11} A and from 0.69 s to 67.37 s, respectively. Additionally, a relation $t_S = 4.22 \times 10^{-12} / I_S$ between the step charging time and the step charging current was found (shown in Fig. 6-4), which means that the step charging time (t_S) for various step charging current (I_S) can be approximately calculated. Under these charging conditions, the similarity of these hysteresis plots implies that the conduction current may not affect the P-V plots as the step charging current is reduced.

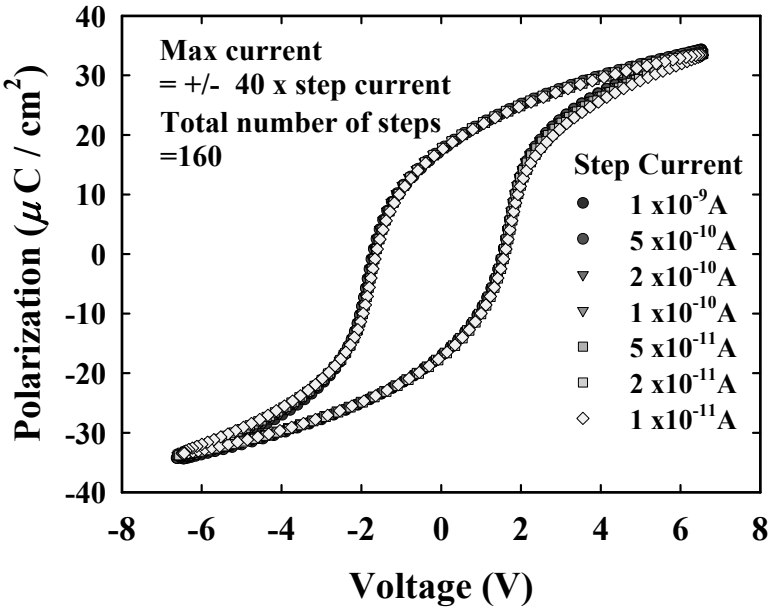

Fig. 6-3 Polarization-voltage (P-V) plots obtained using TC method, for various step charging currents.

To elucidate further the effect of the number of steps on hysteresis property, the maximum charging current and single cycle duration were fixed at 4.0×10^{-8} A and 0.69 s, respectively. The total number of steps was varied from 40 to 160. Figures 6-5(a) and 6-5(b) show the measured voltage profiles and P-V curves for various numbers of charging steps. As can be seen from these figures, the results for various numbers of charging steps are virtually identical. It also implies that the measured voltage profiles and P-V curves are independent of the number of steps.

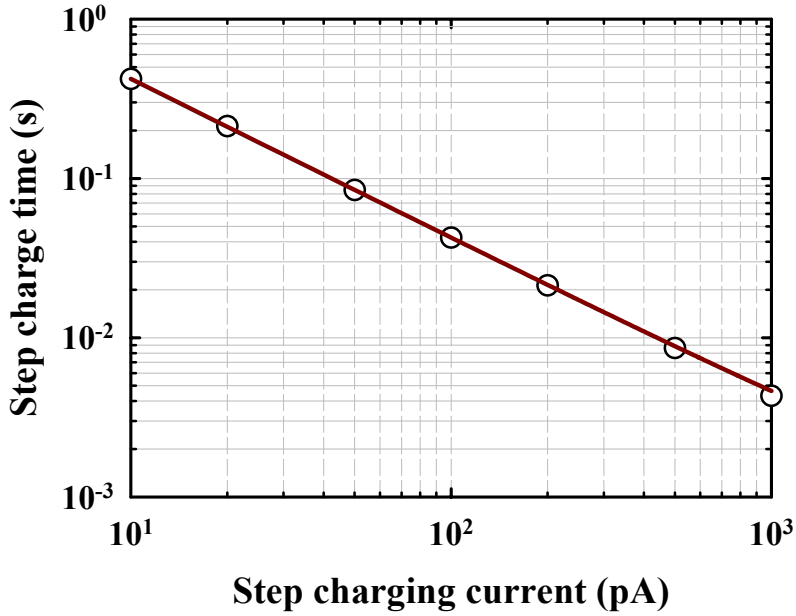

Fig. 6-4 Relation $t_S = a / I_S$ between the step charging time and the step charging current, where $a = 4.22 \times 10^{-12}$ is constant.

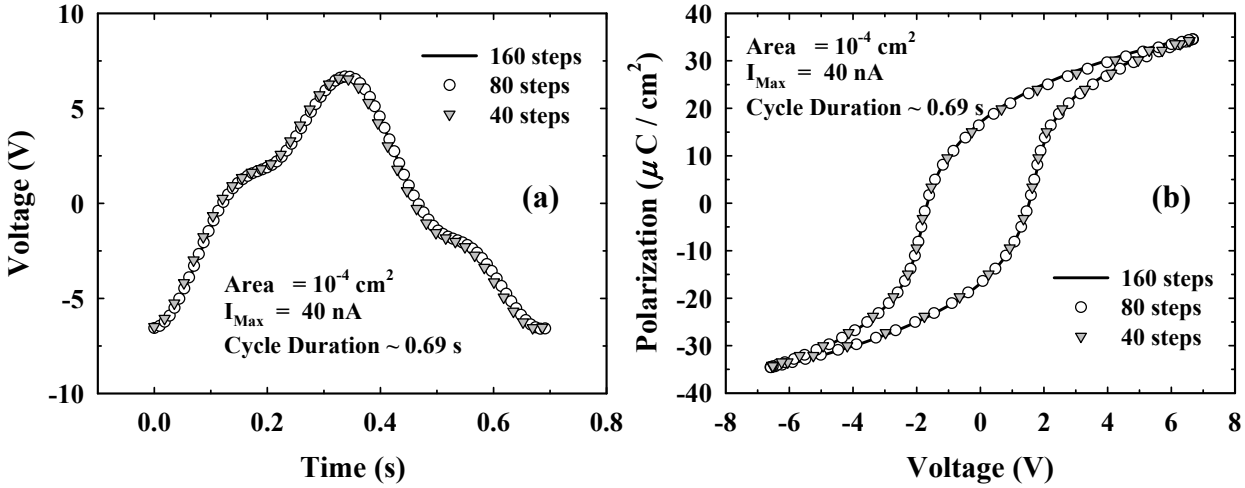

Fig. 6-5 (a) Measured voltage profiles and (b) polarization-voltage (P-V) plots obtained using TC method, for various numbers of charging steps. The maximum testing current and cycle duration were fixed at 40 nA and 0.69 s, respectively.

6-3-3. Hysteresis measurement of micron-sized ferroelectric capacitor

As reported elsewhere [31-32], the maximum polarization of the capacitor increases substantially as its area decreases, perhaps because the probe setup has a parasitic capacitance.

In this study, the parasitic capacitance (C_{para}) of the probe was assumed to act in parallel with the capacitance of the ferroelectric capacitors. The parasitic capacitance can be determined by open contact measurement. This measurement was performed by lifting the needle and using a triangular charging current to characterize the parasitic effect. The charging current versus measured voltage of the parasitic effect is shown in Fig. 6-6. It can be seen that the current-voltage plot has an elliptical shape, which is similar to the switching current-voltage plot of linear dielectric materials [48]. Additionally, the parasitic charge (Q_{para}), which was calculated from the triangular charging current using integral calculus ($Q_{\text{para}} = \int Idt$), is also shown in this figure. As can be seen from the parasitic charge-voltage (Q_{para}-V) plot, it is almost a straight line under the charging condition with a step charging current of 2×10^{-14} A and a step charging time of 0.174 s. From the slope of the Q_{para}-V plot, the parasitic capacitance can be determined using $C_{\text{para}} = Q_{\text{para}}/V$, and the calculated value of C_{para} was approximately 0.452 pF, which was close to our previous result (0.4357 pF) obtained using the CC method (Chapter 4).

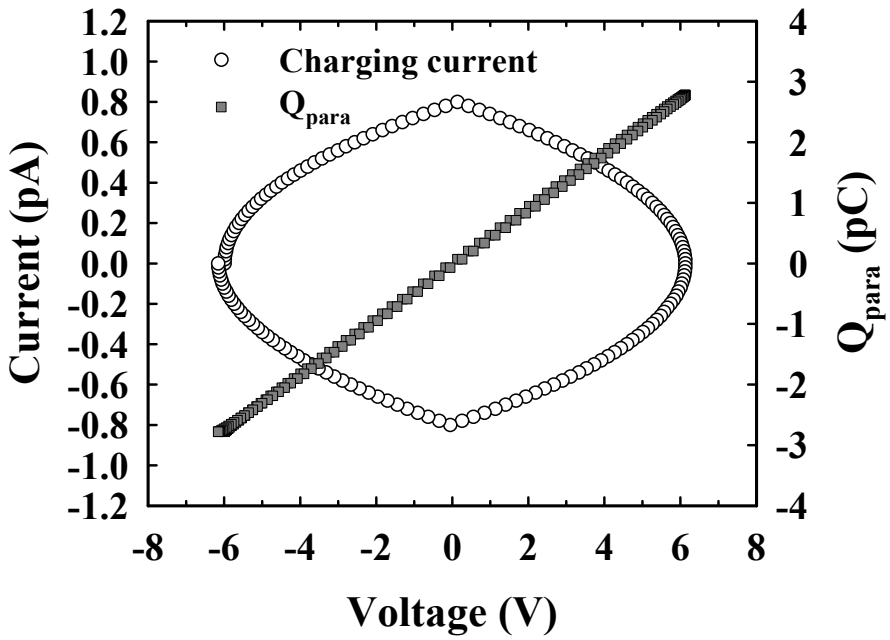

Fig. 6-6 Parasitic effect of probe setup: charging current versus measured voltage (open circles), and parasitic charge Q_{para} versus voltage (solid squares) obtained using TC method.

Figure 6-7 shows the hysteresis plots of a 3 μm × 3 μm capacitor with and without parasitic correction. As can be seen from this figure, a marked increase in the maximum polarization was found in the P-V curve, which is consistent with other reports [31-32]. By utilizing the TC method, the parasitic effect can be determined to yield corrected hysteresis plots using $D_C = (Q_D - C_{para} \times V) / A$, where D_C is the corrected dielectric displacement and Q_D is the uncorrected displacement charge of the specimen. These results indicate that parasitic capacitance strongly influences the hysteresis of a small capacitor, suggesting that the TC method constitutes an approach for investigating the ferroelectric characteristics of micron-sized ferroelectric capacitors.

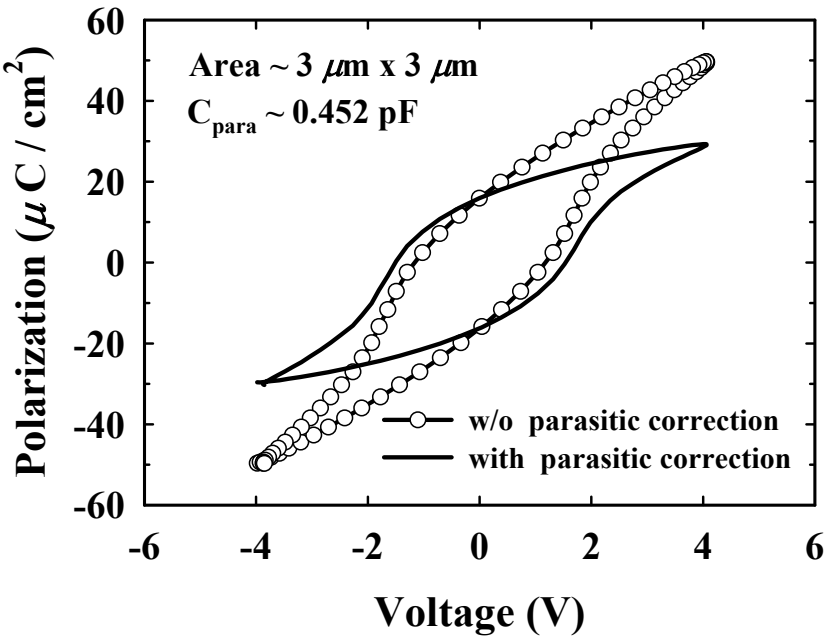

Fig. 6-7 Hysteresis plot of 3 μm × 3 μm capacitor obtained using TC method with (solid line) and without (open circles) parasitic correction.

6-3-4. Hysteresis measurement of MIS structure

Because of the difficulty of measuring P-V curves of MIS and MFIS structures at low frequency (< 1 Hz) [49], we adopt the TC method to perform the hysteresis measurement of both structures at the frequency of around 0.2 Hz.

Figure 6-8(a) shows the capacitance-voltage characteristic of MIS structure with 5.0 nm-thick SiO_2 film measured at small-signal frequency of 100 kHz. The electrode area of the

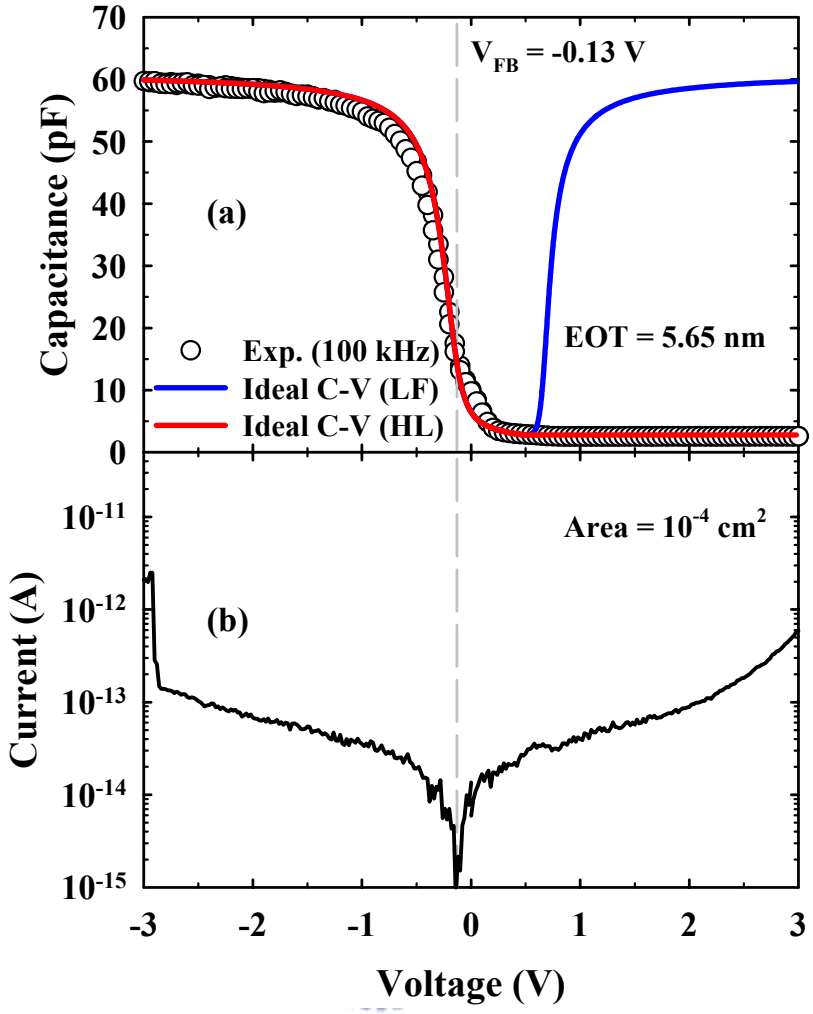

Fig.6-8 (a) Capacitance-voltage characteristics of MIS capacitor. Open circles represent the measured result at 100 kHz. Red and Blue lines represent ideal C-V curves of high frequency and low frequency, respectively. (b) The leakage current-voltage characteristic of this capacitor with 5.0 nm-thick SiO_2.ent ideal C-V curves of high frequency and low frequency, respectively. (b) The leakage current-voltage characteristic of this capacitor with 5.0 nm-thick SiO_2.

MIS capacitor was about 10^{-4} cm^2. The equivalent oxide thickness (EOT) of this capacitor was about 5.65 nm calculated from the ideal C-V curve. The accumulation capacitance of MIS capacitance was around 60.1 pF. A good agreement was found between these C-V curves. The flat-band voltage of this capacitor was around -0.13 V, which is close to the position of voltage with smallest leakage current, as shown in Fig. 6-8(b). From the leakage

current-voltage characteristic of this capacitor, it was found that the leakage current was around 1 pA measured at voltage of ±3.0 V with a delay time of 1 s.

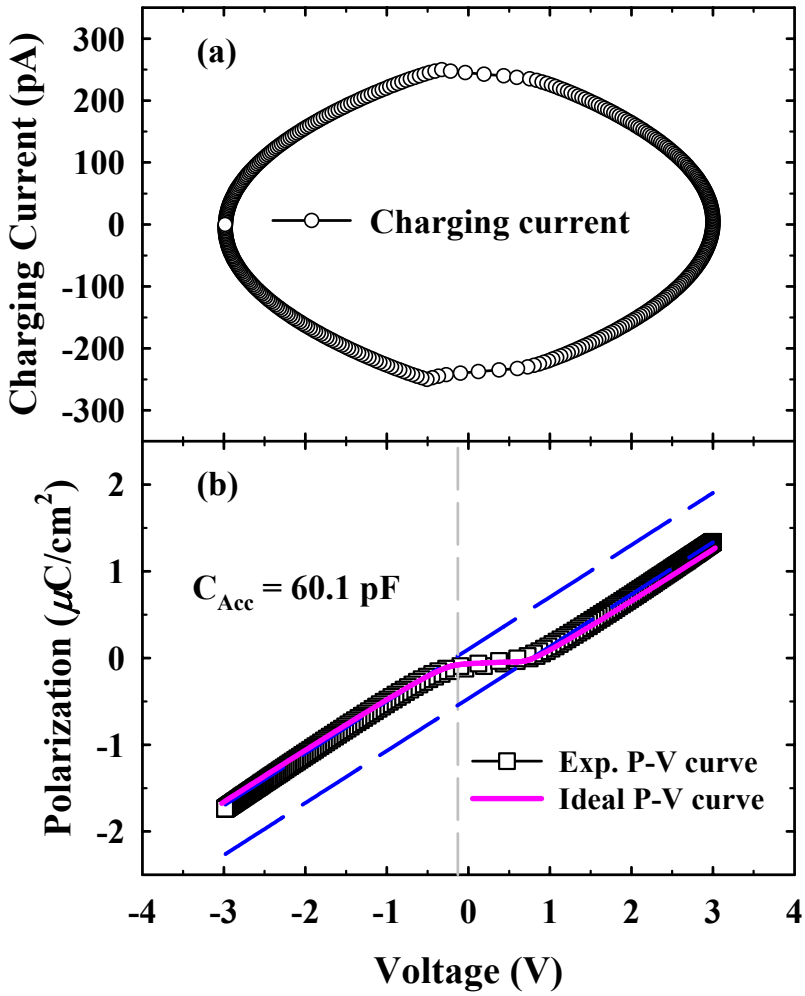

Fig. 6-9 (a) Charging current versus measured voltage (open circles). (b) Polarization-voltage curve of MIS capacitor with 5 nm-thick SiO_2. Open squares represent the experimental P-V curve. Pink line represents result of ideal one. Blue dash lines represent the auxiliary line of the result with C_{Acc} = 60.1 pF.

To obtain the P-V curves of the MIS capacitor, the triangular current (TC) method was utilized to measure the corresponding voltage. The charging current-voltage characteristics are shown in Fig. 6-9(a). The number of charging steps was fixed at 400 and single cycle duration was approximately 4.924 s (about 0.2 Hz). The maximum charging current for this method was about 250 pA. In contrast to the maximum charging current (2.5×10^{-10} A), the leakage current of the MIS capacitor (~1.0×10^{-12} A) was considerably smaller and can be

neglected.

Figure 6-9(b) shows the P-V curve of MIS capacitor with 5 nm-thick SiO_2 film, obtained using the integration of the charging current. It was found that the capacitance calculated from the high-field slope of this P-V curve was approximately 60.8 pF, which is close to the value of the accumulation capacitance (~ 60.1 pF). The shape of experiential P-V curve is similar to those of ideal P-V curve obtained from space charge density (Q_S)-voltage curve of ideal MOS capacitor using $Q_S = -P$. This strong agreement between experimental and ideal P-V curves reveals that the TC method was also suitable for measuring the hysteresis curve of MIS capacitor even though the frequency of single cycle (~ 0.2 Hz) was lower than 1 Hz.

6-3-5. Hysteresis measurement of MFIS structure

Figure 6-10 shows the capacitance-voltage characteristic of MFIS structure with 14.0 nm-thick HfO_2 film and 320 nm-thick $SrBi_2Ta_2O_9$ film measured at small-signal frequency of 100 kHz. The area of MFIS capacitor was around 3.5×10^{-4} cm^2. The C-V curves of this MFIS structure exhibit a ferroelectric-type hysteresis. It reveals that the memory window is a function of applied voltage. The accumulation capacitance of MFIS stack was about 93.3 pF. The leakage current of this stack was around 5.0×10^{-13} A measured at the voltage of ±5 V, which is also considerably smaller and can be neglected.

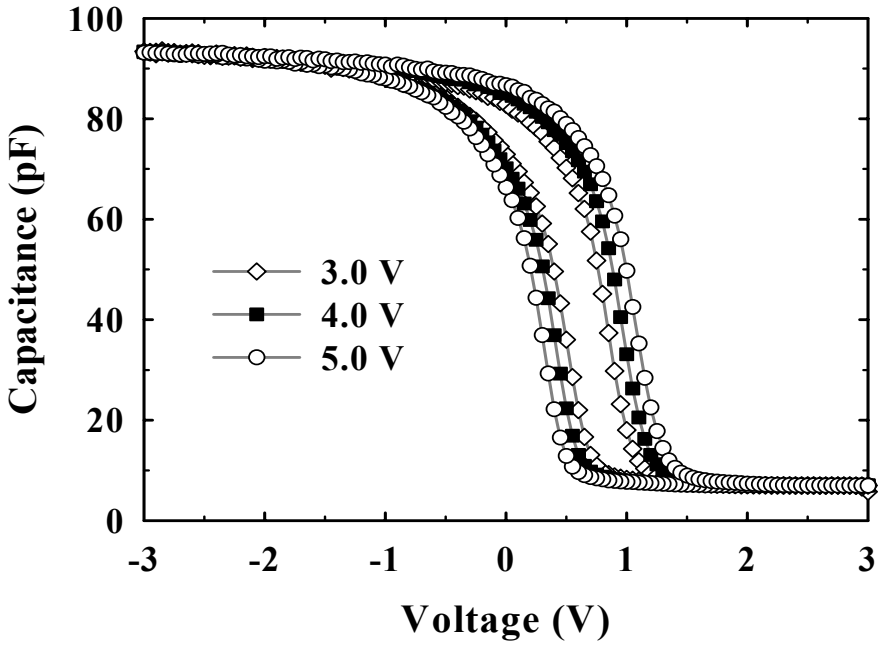

Fig. 6-10 Capacitance-voltage characteristics of MFIS capacitor for various sweeping biases.

To investigate the relationship between the C-V curve and the P-V curve of MFIS stack, the hysteresis measurements were also performed using the TC method. The number of charging steps was fixed at 400 and the frequency of single cycle was around 0.183 Hz. By adjusting maximum charging current (from 5×10^{-10} to 9.5×10^{-10} A), the resulting voltage can be tuned (from 3.0 to 5.0 V) to obtain the P-V curves. The P-V curves of $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ stack are shown in Fig. 6-11. As can be seen, it also exhibits a ferroelectric hysteresis. The shape of P-V curve of MFIS stack is unlike that of traditional MFM structure. It was also found that the capacitance obtained from the high-field slope of P-V curve was close to the value of accumulation capacitance of MFIS stack (around 93.3 pF). The result can be explained by the reversible component of the polarization obtained from P-V curve of MFM capacitor [06].

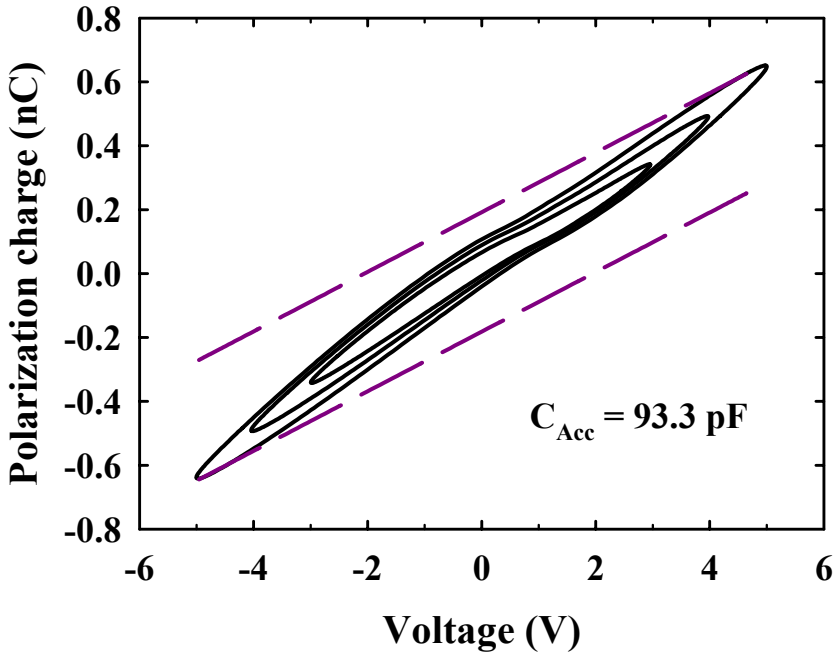

Fig. 6-11 Polarization charge of MFIS capacitor obtained using TC method for various biases. Purple lines represent the auxiliary line of the result with C_{Acc} = 93.3 pF.

Figure 6-12 shows the memory window (MW) of $Pt/SrBi_2Ta_2O_9/HfO_2/Si$ stack obtained from C-V and P-V curves. Both results indicate that the memory window of this stack increases with increasing the applied bias. The values of MW in C-V curve is less than that obtained from P-V curve (shown in Fig. 6-11), perhaps because the ramping rate of dc bias voltage of C-V measurement was small than that of polarization-voltage (P-V) hysteresis measurement. The details of the MW in both curves are currently under investigation. The

finding indicates that the TC method is also suitable for measuring the P-V curve of MFIS stack even though the frequency of single cycle was less than 1 Hz and is useful to investigate the relationship between the P-V and C-V curves.

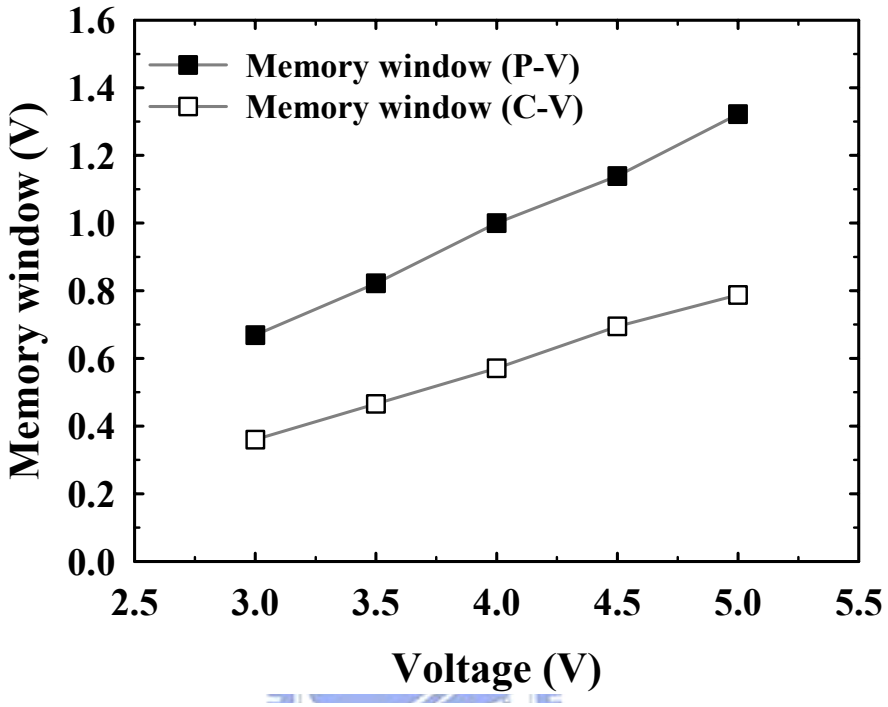

Fig. 6-12 Memory window of MFIS stack obtained from P-V (full squares) and C-V (open squares) curves for various biases.

6-3-6. Temperature effect of hysteresis measurement of ferroelectric capacitor

Before studying the temperature effect of hysteresis measurement of ferroelectric capacitor, the P-V loops for various number of step were first measured at room temperature (around 20 ^{o}C). The step time was around 4.3 ms. The number of the charging step N and the step charging current I_S were changed from 100 to 400 and from 1.92 × 10^{-9} A to 1.2 × 10^{-10} A, respectively. The maximum charging current was approximately $N \times I_S/4$ (from 4.8 × 10^{-8} A to 1.2 × 10^{-8} A). The frequency of single cycle was charged from 2.34 Hz to 0.58 Hz. The relevant results are shown in Fig. 6-13. These P-V curves are virtually identical, indicating that the conduction current is negligible at room temperature.

To study the temperature sensitivity of TC method, the hysteresis measurement was performed at various temperatures. Besides, the leakage current characteristics (shown in Fig. 6-14) of ferroelectric capacitor was also measured at those temperatures. The results indicate

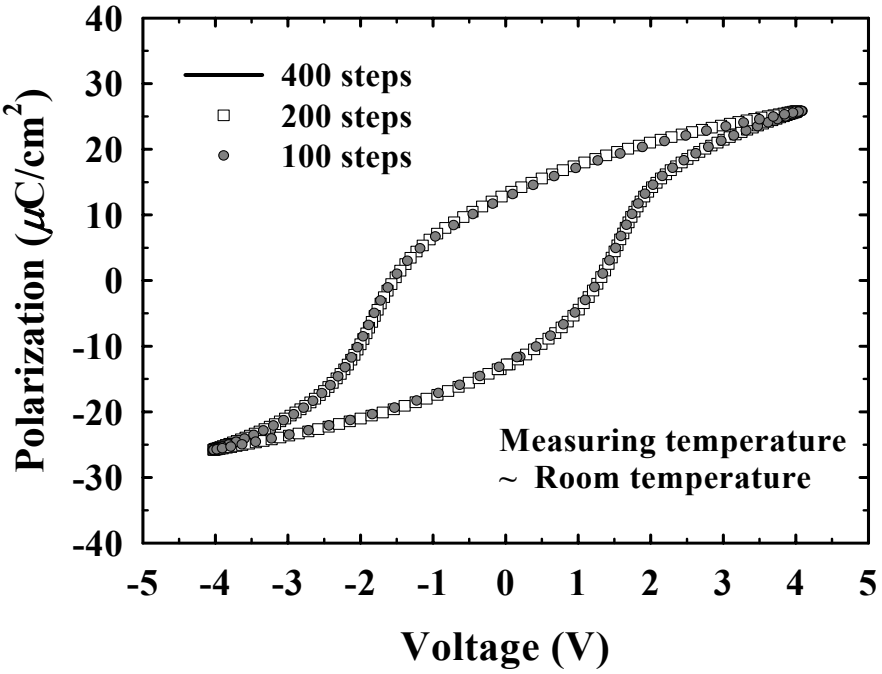

Fig. 6-13 Polarization-voltage (P-V) plots obtained using TC method, for various numbers of charging steps. The step charging time was around 4.3 ms. The number of charging step was changed from 100 to 400. The maximum testing current and the frequency of single cycle were changed from 4.8 × 10^{-8} A to 1.2 × 10^{-8} A and from 2.34 Hz to 0.58 Hz, respectively.

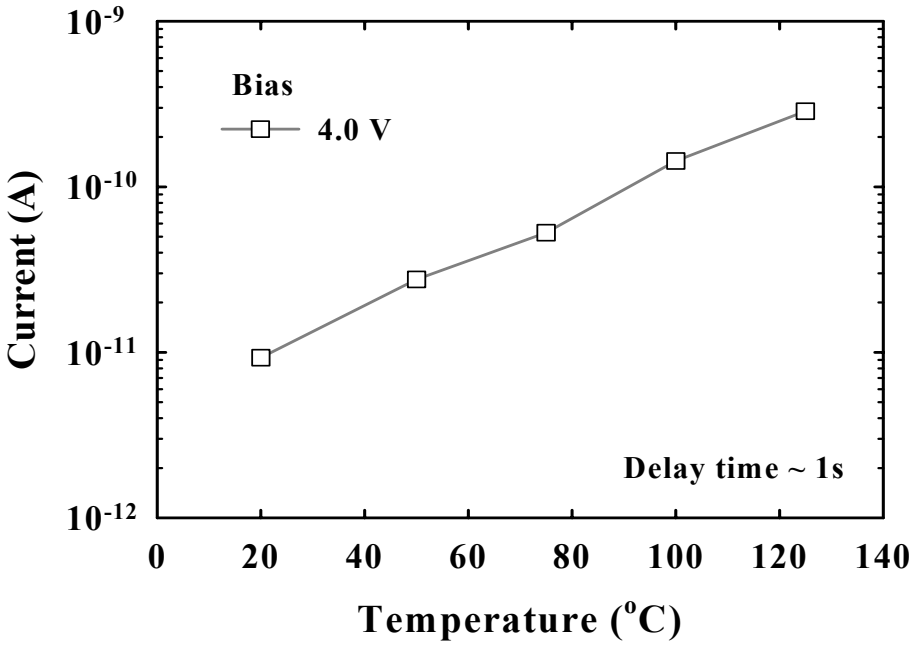

Fig. 6-14 Leakage current of PZT capacitors measured at various temperatures. The delay was around 1 s.

that the leakage current increased with the measurement temperature, which may result in the shape-distortion of P-V curves. As can be seen, the value of $I_{125\,^{o}C}(4\text{V})/I_{20\,^{o}C}(4\text{V})$ was around 30.9 and $I_{125\,^{o}C}(4\text{ V})$ was about 2.86×10^{-10} A. In contrast to the step charging current $I_S(N=400)$ ($\sim 1.2 \times 10^{-10}$ A), $I_{125\,^{o}C}(4\text{ V})$ (2.86×10^{-10} A) is large enough, implying that the conduction current of PZT capacitor is no longer negligible at 125 °C. Figure 6-15 shows the P-V loops for various number of charging step measured at 125 °C. It was found that a slight shape-distortion exhibits in the P-V curve as the number of charging step N was 400. Additionally, an enlarge remnant polarization and a gap of y-axis were also found. However, for the number of charging step $N=100$, the existence of shape-distortion was not found in the P-V loop, perhaps because of the larger step charging current ($\sim 1.92 \times 10^{-9}$ A) and maximum charging current ($\sim 4.8 \times 10^{-8}$ A). Figure 6-16 shows the P-V loop ($N=100$) measured at room temperature and high temperature of 125 °C. As can be seen, only a reduced coercive voltage appears in the P-V loops as temperature increased. The result implies that temperature sensitivity of TC method is smaller when the charging current and the frequency of single cycle were increased.

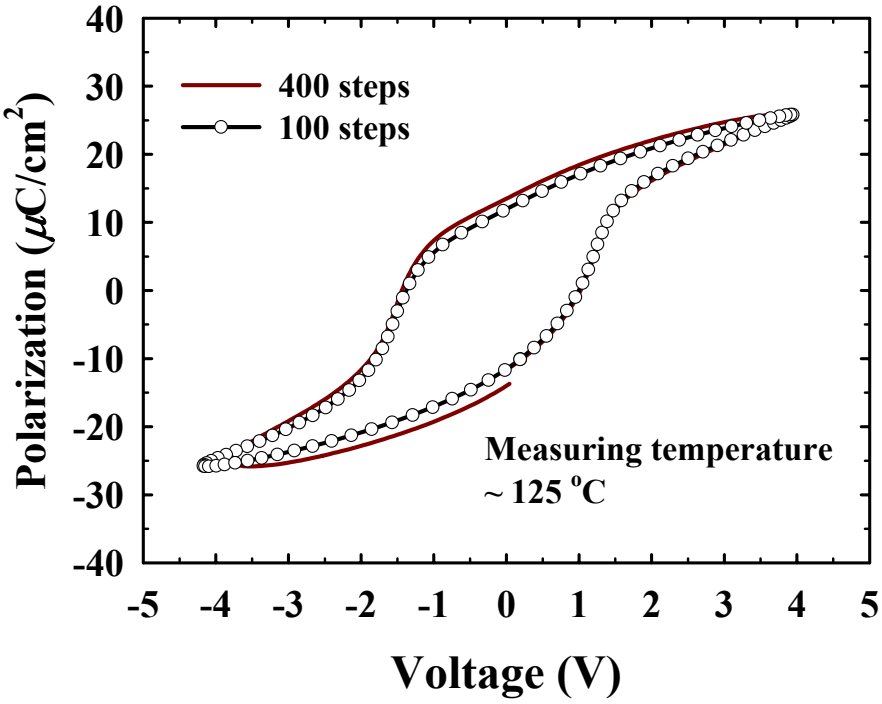

Fig. 6-15 Polarization-voltage loops of PZT capacitors measured at high temperature of 125 °C, for the various number of charging step.

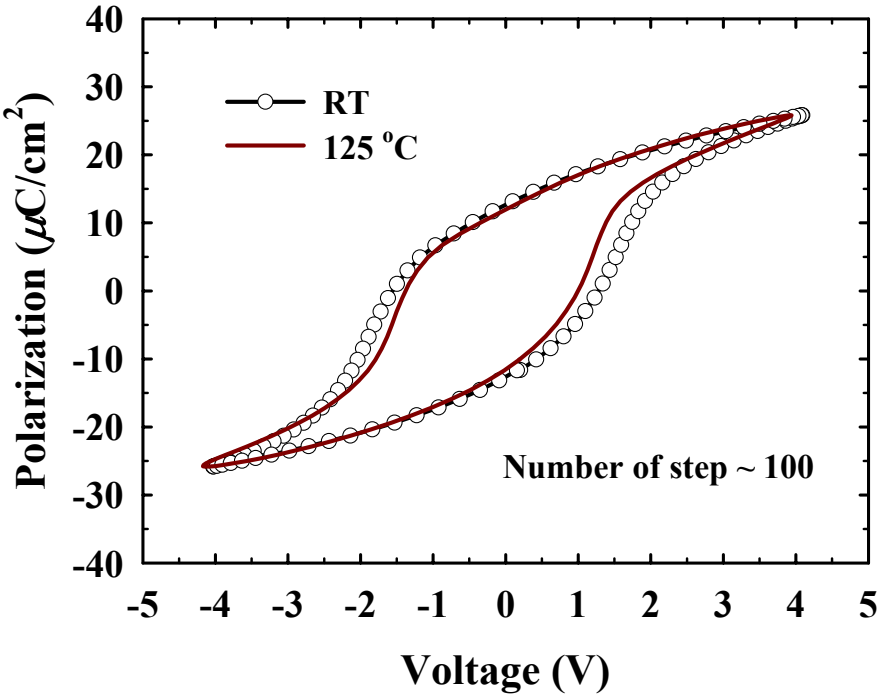

Fig. 6-16 Polarization-voltage loops of PZT capacitors measured at different temperature, for the number of charging step of 100.

6-4. Summary

In this chapter, a triangular current (TC) method was employed to measure the hysteresis loops of ferroelectric capacitors. This method yields an almost noiseless voltage profile and a smooth curve in the high-field region. Additionally, the similarity between the obtained hysteresis curves imply that neither the step charging current nor number of steps affects the P-V curve. Moreover, the results for a small capacitor reveal that the parasitic effect of the probe setup may markedly increase the maximum polarization as the area of the capacitor decreases. The triangular current method can be used to determine the parasitic capacitance of the probe setup and thus derive the corrected hysteresis loops. Furthermore, the TC method can also be utilized to determine the P-V curves of MIS and MFIS capacitors at very low frequency (< 1 Hz). The TC method also appears a smaller temperature sensitivity of hysteresis measurement as the charging current increased. The findings imply that the TC method constitutes an approach for investigating the ferroelectric characteristics of ferroelectric capacitors and MFIS stacks.