Chapter 1

Introduction

1-1. Introduction to the Ferroelectric Materials and Its Application on Nonvolatile Memory

1-1-1. High-k materials and ferroelectric materials [01-05]

High-dielectric-constant (high-k) materials have been served important function for semiconductor devices and DRAM circuits. For the DRAM application, there are two kinds of high-dielectric-constant materials. The first group consists of the "simple" high-k materials with an atomic composition similar to that of SiO_2. They include Ta_2O_5, TiO_2, Y_2O_3, HfO_2, and ZrO_2. They have a dielectric constant on the order of several tens. The second group of high-k materials consists of the "ferroelectric" materials. The dielectric constants of ferroelectric materials are very large in the form of thin films, often on the order of several hundreds. The ferroelectric materials for the VLSI applications are mostly of the perovskite crystal structure (shown in Fig. 1-1), having the atomic composition of ABO_3, where A represents a cation with a larger ionic radius. B represents a cation with a smaller radius, and O is oxygen. The ferroelectric materials show ferroelectric properties below the Curie temperature T_C and show paraelectric properties below the Curie temperature (mostly cases).

For the ferroelectric materials with paraelectric properties, they have the properties similar to the conventional dielectric materials. This means that polarization can be induced by an applied electric field even through no permanent electric dipole moment exists. The polarization ($P_{reversible}$) generally increase linearly with increasing the applied electric field (E). The relationship between polarization and electric field is expressed by

$$P_{revesible} = \chi\varepsilon_0 E \cong \varepsilon_0\varepsilon_r E = D, \qquad (1\text{-}1)$$

where $\chi = \varepsilon_r - 1$ is called dielectric susceptibility, ε_0 is the dielectric permittivity of free space, ε_r is the instantaneous dielectric constant, and D is dielectric displacement.

The polarization of ferroelectric materials with paraelectric properties is completely reversible. Removing the electric field returns to zero polarization. These ferroelectric materials can be used as the capacitor dielectric for DRAM devices.

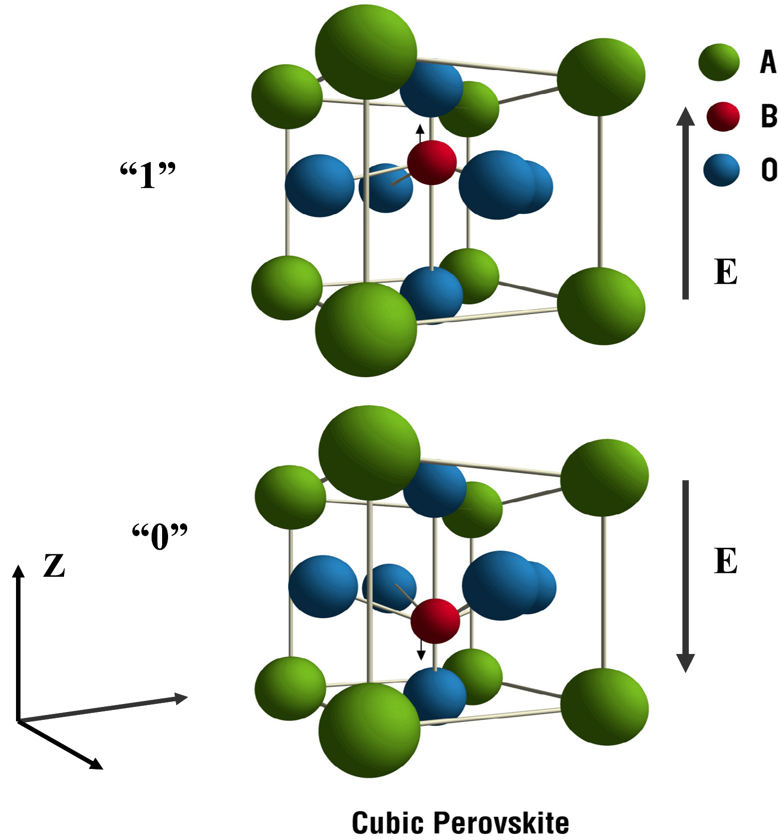


Fig. 1-1. Perovskite crystal structure, having the atomic composition of ABO_3, where A represents a cation with a larger ionic radius. B represents a cation with a smaller radius, and O is oxygen. (Ref. [03])

For the ferroelectric materials with ferroelectric properties, they contain a permanent dipole moment at a unit cell, resulting in a net polarization. In the recently yeas, the mostly used ferroelectric materials, such as $Pb(Zr,Ti)O_3$ (PZT), $SrBi_2Ta_2O_9$ (SBT) and $(Bi,La)_4Ti_3O_{12}$ (BLT), are investigated. Normally, these ferroelectric materials have a hysteresis property in the polarization-voltage curve and have two stable states at zero electric field (shown in Fig. 1-2(a)). These remanent polarization states are attributed to the fact that at least one set of ions in the crystal sits in double-well potentials, as shown in Fig.1-2(b). When the ferroelectric film is subjected to an electric field, the dipoles will preferentially line up along the applied field, resulting in a net dipole moment of the ferroelectric material. This phenomenon is called domain switching. For these ferroelectric materials, the dielectric displacement is composed of reversible and irreversible polarization charges and it can be expressed by [06]

$$D = P_{Total} = P_{reversible} + P_{irreversible}, \qquad (1-2)$$

where P_{Total} is total polarization charge, $P_{reversible} = \varepsilon_0 \varepsilon_r E$ is reversible component of

polarization charge (linear term), and $P_{irreversible}$ is irreversible component of polarization charge (non-linear term).

These features provide a natural memory element for nonvolatile memories. One of approaches is generally called the ferroelectric random-access memory (FeRAM). Two types of ferroelectric memory cells have been used (as shown in Figs. 1-3 and 1-4): (1) one-transistor/one-capacitor design (1T/1C) (1 cell per bit) and (2) two-transistor/two-capacitor design (2T/2C) (2 cells per bit).

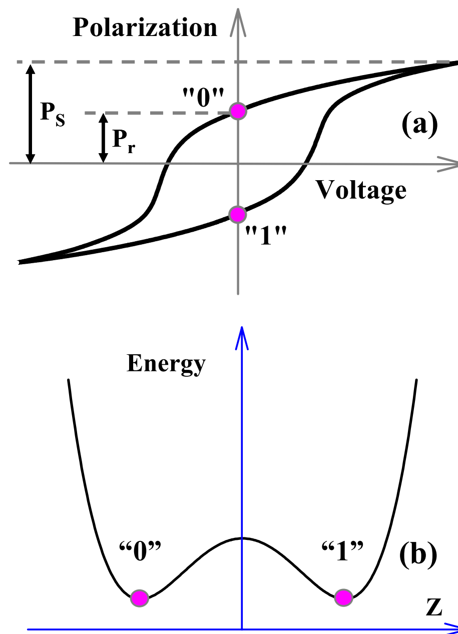


Fig. 1-2. (a) Ferroelectric materials exhibit spontaneous polarization with applied voltage due to the atomic displacement of the body-center atom in the perovskite structure (See Fig. 1-1). The polarization-voltage curve has two stable states at zero voltage after the removal of the field. (b) The energy potential-atomic displacement plot of ferroelectric material. (Ref. [04])

1-1-2. Basic operation of 1T1C FeRAM

For the most commonly used 1T1C FeRAM, a ferroelectric capacitor is series connected to a N-MOS field effect transistor. The word line (WL) and bit line (BL) are connected to the gate and drain of the transistor, respectively. The plate line (PL) is connected to one terminal of the ferroelectric capacitor. This circuit scheme is very similar to the structure of DRAM expect that an additional plate line is connected to the terminal of ferroelectric capacitor. The major difference between 1T1C FeRAM and DRAM is nonvolatility of datum storage. When

the power supply is turned off, the ferroelectric capacitor can still store the polarization charge.

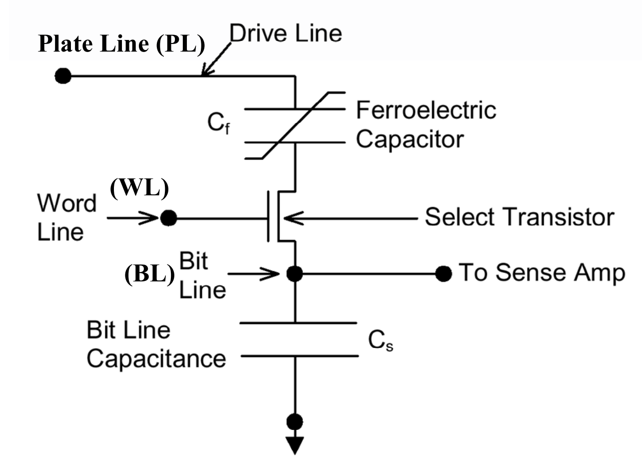


Fig. 1-3. Circuit scheme of one-transistor/one-capacitor (1T/1C) designed FeRAM. (Ref. [07])

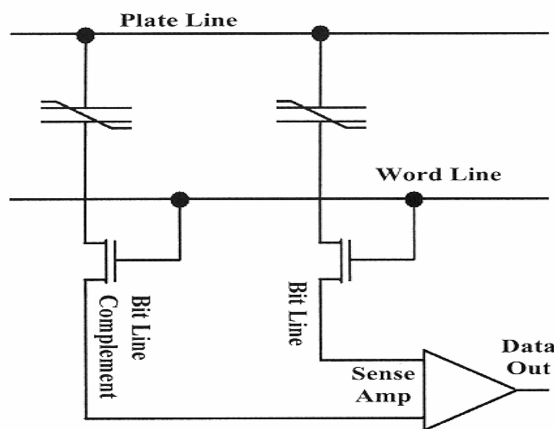
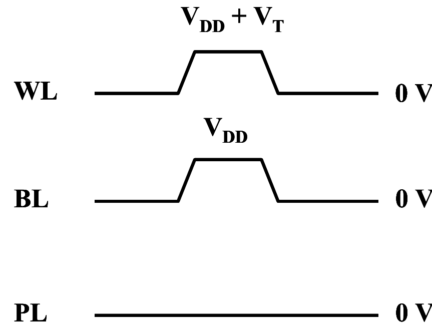


Fig. 1-4. Circuit scheme of two-transistor/two-capacitor (2T/2C) designed FeRAM. (Ref. [07])

For the writing procedure of 1T1C FeRAM, the polarization state can be written by applying voltage pulse (V_{DD}) to the BL for logic "1" or to the PL for logic "0". The timing diagram of writing procedure for each logic state is shown in Fig. 1-5. To write logic state "1" or "0" into the memory cell, the WL is first raised to V_{DD} + V_T, where V_T is the threshold voltage. Then the BL is raised to V_{DD} to set the polarization state of ferroelectric capacitor at $-P_r$ (logic "1"). Similarly, to write the logic '0', the PL is also raised to V_{DD} to set the polarization state at $+P_r$, as shown in Fig. 1-6(a). After writing procedure, the polarization state can be stored even though the power is turned off. During retention procedure, no leakage current exhibits in the ferroelectric capacitor to destroy the polarization state because of no electric field across the ferroelectric capacitor.



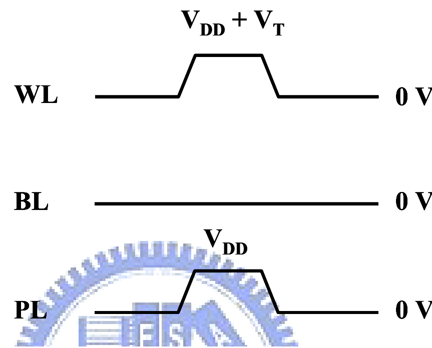


Fig. 1-5. Timing diagram of the writing operation of 1T1C FeRAM. (a) Writing for logic "1" and (b) Writing for logic "0". (Ref. [07])

For the reading procedure, the logic "0" or logic "1" can be identified by detecting the voltage difference on the BL. During reading process, the memory state is reset to logic "0" and then the memory state will be restored to its original state and the BL is precharged back to 0 V (See Fig. 1-7) [07]. This process is called the destructive readout operation (DRO). The voltage drop across the ferroelectric capacitor and BL can be obtained, using a load line of BL capacitance and the curves of $Q_{SW}(V)$ and $Q_{NSW}(V)$ to found out the interception, as shown in Fig. 1-6(b). The sense margin is the difference in voltage of BL (V_{BL}) of the two states. The equations concerning $V_{BL}(\text{"0"})$ and $V_{BL}(\text{"1"})$ can be written by the following:

$$Q_{NSW}(V) = C_{BL} \times V_{BL}(\text{"0"}), \tag{1-3(a)}$$

$$Q_{SW}(V) = C_{BL} \times V_{BL}(\text{"1"}), \tag{1-3(b)}$$

$$V_{BL}(\text{"0"}) = V_0 = \frac{Q_{NSW}(V)}{C_{BL}}, \tag{1-4(a)}$$

$$V_{BL}("1") = V_1 = \frac{Q_{SW}(V)}{C_{BL}}, \quad (1\text{-}4(b))$$

$$V_{PL} = V_F + V_{BL}, \quad (1\text{-}5)$$

and

$$V_{SENSE-MARGIN} = V_{BL}("1") - V_{BL}("0"), \quad (1\text{-}6)$$

where $Q_{NSW}(V)$ is non-switching charge, $Q_{NSW}(V)$ is switching charge, V_F is voltage across the ferroelectric capacitor, V_{PL} is the voltage of plate line, C_{BL} is BL capacitance, and $V_{SENSE-MARGIN}$ is the sense margin of voltage difference in BL between logic ”0” and logic “1”. Fig. 1-8 shows the result of BL capacitance (C_{BL}) dependence of sense margin. It was found that the maximum sense margin can be obtained by optimizing the C_{BL}.

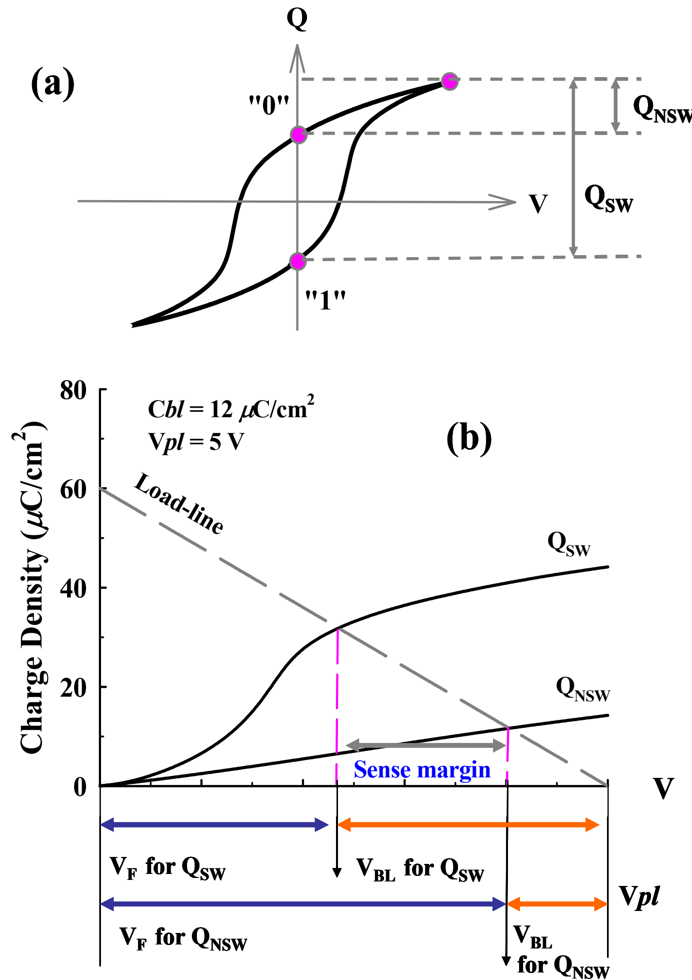


Fig. 1-6. (a) Hysteresis loop of the ferroelectric capacitor. (b) Charge density to voltage characteristics of ferroelectric capacitor. (Ref. [07])

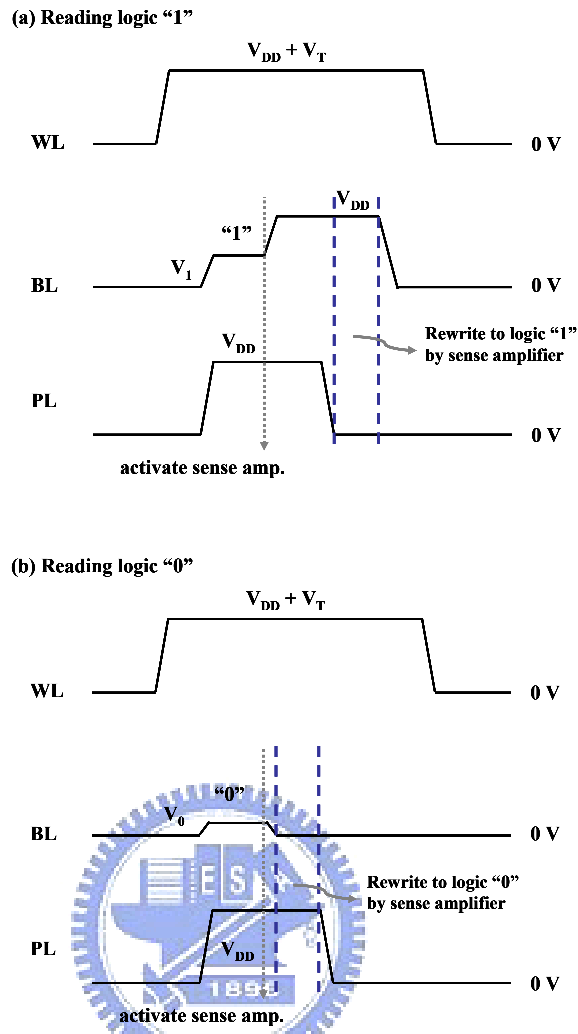


Fig. 1-7. Timing diagram of the reading operation of 1T1C FeRAM. (a) Reading logic ”1” and (b) Reading logic “0”. (Ref. [07])

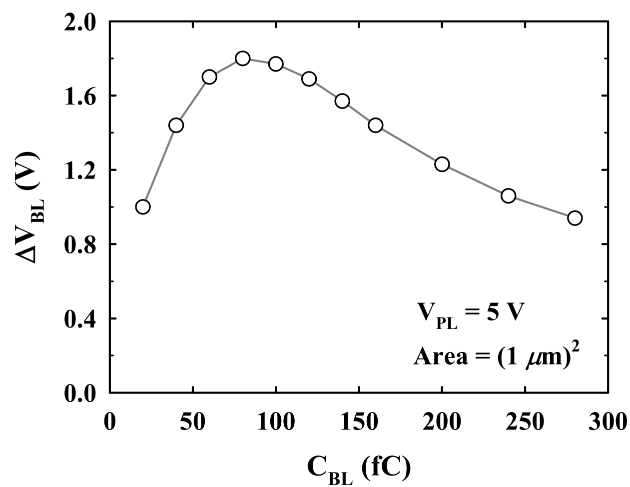


Fig. 1-8. BL capacitance (C_{BL}) dependence of sense margin for 1T1C FeRAM.

1-1-3. Other FeRAM Structures

There are many kinds of FeRAM structures, such as chain FeRAM and 1T FeRAM. The comparison of conventional and chain structures of FeRAM is shown in Fig. 1-9. The chain FeRAM has been proposed by Toshiba in the late 90's and exhibits several benefits over than conventional 1T1C FeRAM, such as faster operational speed, lower power consumption, smaller peripheral circuit overhead, and minimum cell size of around $4F^2$ [08-10]. However, the 1T1C FeRAM has certain limitation for its applications. To maintain an adequate stored charge for obtaining the sense margin, the area of ferroelectric capacitor would limit the memory density. Additionally, the destructive read-out (DRO) process, which must rewrite the memory state to its original state after reading process, may be another drawback for the FeRAM application.

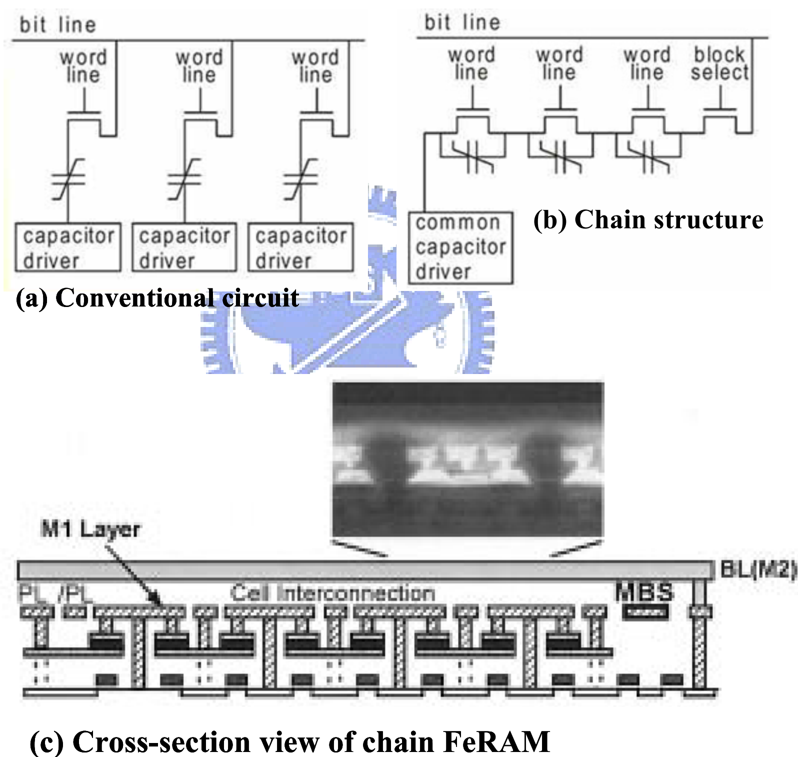


Fig. 1-9. Circuit schemes of (a) conventional and (b) chain 1T1C FeRAM. (c) Scheme of cross-section view of chain FeRAM. (Ref. [08-10])

For the 1 T FeRAM structure, two kinds of ferroelectric field effect transistors (FET) have also been studied for nonvolatile memory application. The ferroelectric FETs are proposed to overcome the limitation of 1T1C FeRAM, such as DRO process and larger area of ferroelectric capacitor. The Ferroelectric FETs include metal-ferroelectric-insulator-semiconductor MFIS (Fig. 1-10(a)) and metal-ferroelectric-metal-insulator-semiconductor MFMIS field effect transistors (Fig. 1-10(b)). The original 1T FeRAM is fabricated with

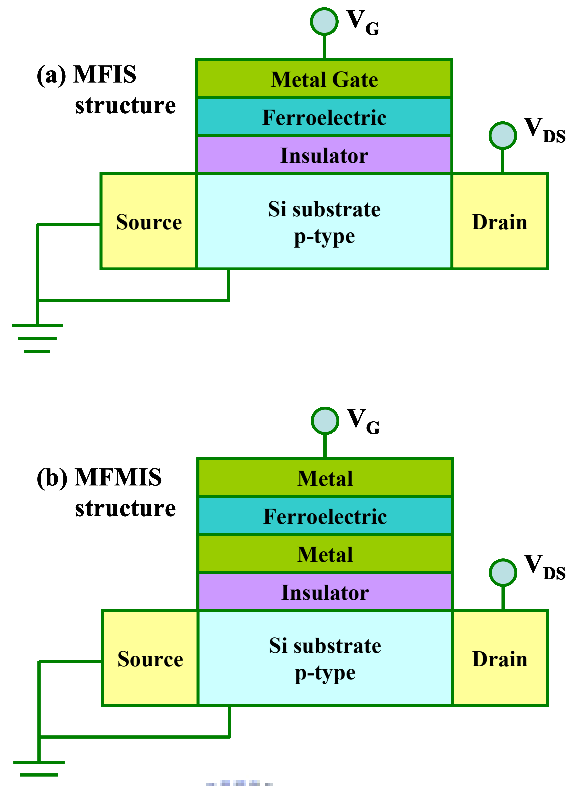


Fig. 1-10. Structure of 1T FeRAM: (a) MFIS FET and (b) MFMIS FET. (Ref. [04])

ferroelectric thin film on silicon substrate without buffer insulating layer [11]. However, the interdiffusion problem between the silicon substrate and the ferroelectric thin film may degrade the device performance significantly. To solve this problem, the buffer insulating layer is often inserted between the silicon substrate and ferroelectric film to act as a diffusion barrier. Various insulating materials have been reported to improve the barrier capability and to maintain a higher capacitance and a lower leakage current of insulator layer [12-19]. They include Si_3N_4, CeO_2, Ta_2O_5, ZrO2, $LaAlO_3$, HfO_2, Pr_2O_3 and other high-k materials. Even though some of these materials can maintain the physical thickness to prevent the interdiffusion problem, the voltage drop across the insulating layer is larger than that of ferroelectric layer, resulting in an insufficient voltage drop across ferroelectric film to polarize the memory state. Additionally, large voltage drop across the insulating layer may also result in charge injection or dielectric breakdown, which may decrease the memory window. To overcome these problems, low-dielectric-constant ferroelectric materials are also needed to decrease the voltage drop across the insulating layer. Therefore, finding either high-k insulating layer or low-dielectric-constant ferroelectric layer is important. However, they must require developments of the new materials. Besides these approaches, the MFMIS FET is proposed to overcome the low capacitance of insulator layer by adjusting the capacitor area of

ferroelectric layer to provide the matching of capacitance. However, either MFIS or MFMIS structure often shows short retention property. The reported data retention time is around 10^3 to 10^5 s, which is relatively short when compared with that of flash memory. The reason for this short retention time may be attributed to the charge injection induced by leakage current [20-22]. Additionally, trap density states of ferroelectric layer may be another important factor that affects the capacitance retention property of 1T-type ferroelectric FET [23]. Therefore, increasing the barrier of metal-ferroelectric (M-F) interface and obtaining a trap-less ferroelectric layer are very important to improve the memory retention.

1-2. Introduction to the Hysteresis Measurement of Ferroelectric Materials [03]

For obtaining the electrical hysteresis loop of ferroelectric materials, various methods have been proposed over the past few decades. The most often quoted method of hysteresis measurement is based mainly on the Sawyer-Tower method (STM) [24]. The circuit scheme of this method is shown in Fig. 1-11. The setup is composed of an oscilloscope, function generator and a large sense capacitor. The sinusoidal voltage signal is mostly used in this setup. This method utilizes a sensing capacitor connected in series with the sample that collects the integrated current to determine the polarization charge. Nowadays, a Radiant Technology Standardized Ferroelectric Test System RT66A is frequency used to perform the polarization measurement, operating in the virtual ground mode with a triangular signal of few volts of amplitude at different frequencies. In this method, a technique of charge measurement, which converts current to charge, has recently changed from utilizing a large sensing capacitor to utilizing a virtual-ground operational-amplifier as a current-to-voltage

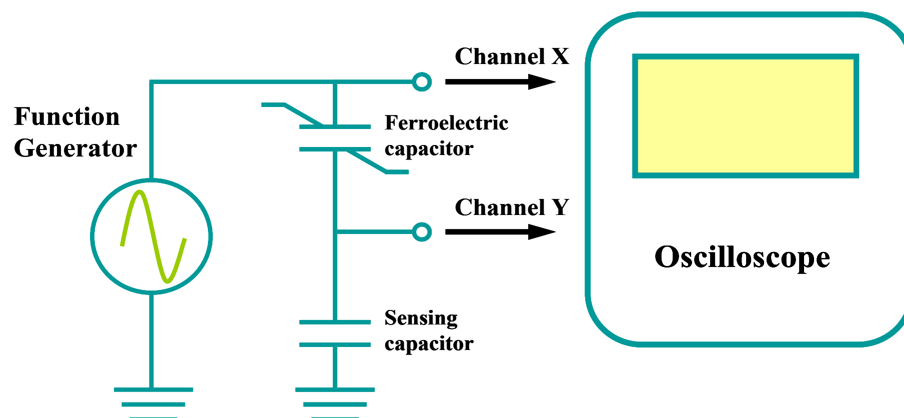


Fig. 1-11. Scheme of Sawyer-Tower circuit and setup to trace hysteresis loops. (Ref. [24])

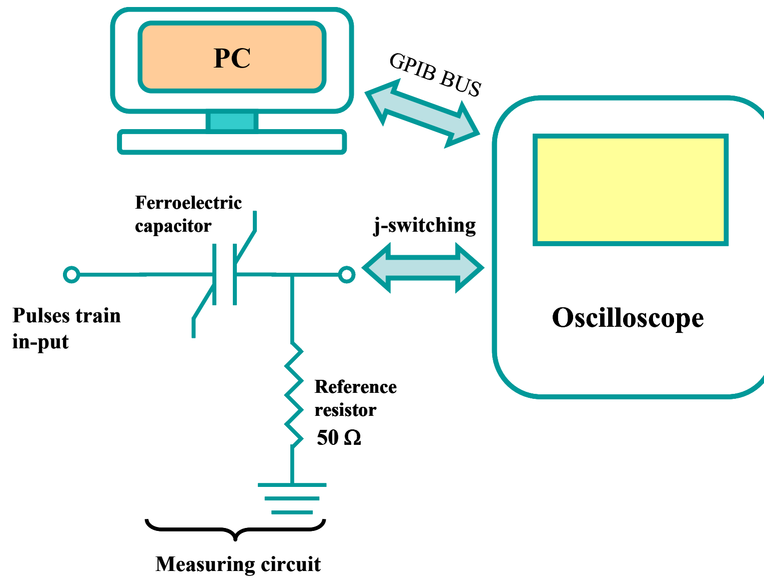


Fig. 1-12. Scheme of shunt method and setup to trace switching current. (Ref. [25])

converter with an integrating capacitor [25]. For measuring the switching current of ferroelectric capacitor, in the shunt method [26], the sensing capacitor is replaced with a reference resistor (R_{ref}) to perform the switching current measurement. The scheme of this measuring setup is shown in Fig. 12. In the retention and fatigue tests, polarization charge is determined by pulse polarization measurement (five-pulses method) [27] that applies pulse sequence to the top electrode of ferroelectric capacitor and the voltage drop (V_{ref}) across the reference resistor is measured simultaneously to obtain the switching current using $I_{switch} = V_{ref} / R_{ref}$. For the measurements, a sequence of square pulses is mostly applied to act the testing profile, as shown in Fig. 13. Several poling pulses of few volts and 200 μs width are applied to the top electrode of ferroelectric capacitor. Each pulse is separated by 20 μs interval. Two reading pulses of the same amplitude are then used for measuring the current curves. However, the rise time of the pulses should be low than the expected switching time of ferroelectric domains (around < 10 ns) to avoid the possible errors [03]. The time elapsed between the poling and measuring procedure may be 300 ms. The switching charge Q_{SW} can be obtained with the first measuring pulse by integration of the corresponding current throughout the measuring time, as shown in Fig. 14. The non-switching change Q_{NSW} is also obtained with the second pulse because no switchable charge is found. Therefore, the linear capacitance of ferroelectric capacitor can be measured. The nonvolatile polarization charge density ΔP is calculated from these charges and the area of top electrode of ferroelectric capacitor A, using the equation

$$\Delta P = (Q_{SW} - Q_{NSW}) / A, \qquad (1\text{-}1)$$

Besides these methods, a current source mode method, constant current method, is also proposed to measure the electrical hysteresis of ferroelectric capacitors [28-29]. In this method, a constant charging current source is applied to a thick ferroelectric film (approximately 12 μm thick), to measure the corresponding voltage, which is almost noiseless in its corresponding voltage profile.

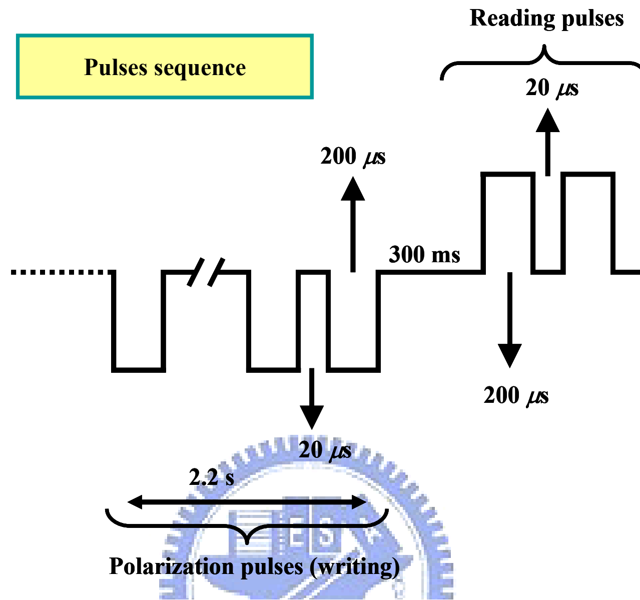


Fig. 1-13. Pulse sequence used to measure switching currents of ferroelectric capacitors (a five-pulses method). (Ref. [03])

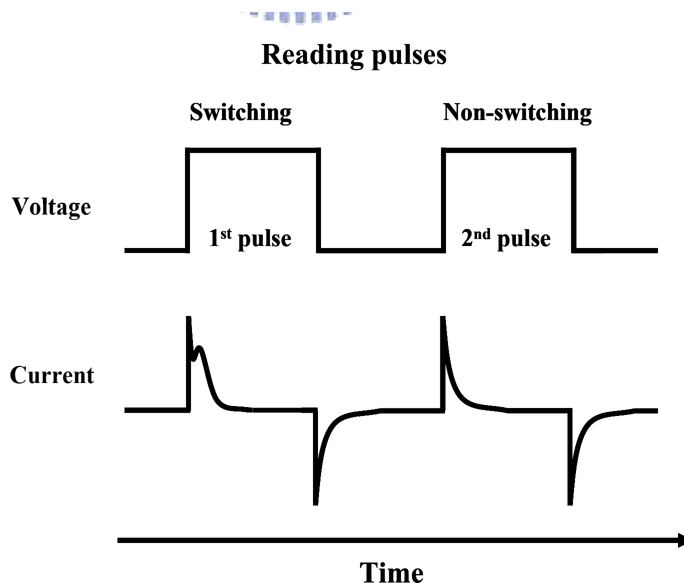


Fig. 1-14. Switchable current and non-switching current characteristics of ferroelectric capacitors. (Ref. [03])

1-3. Motivation

As mentioned in 1-1, the ferroelectric film can be used for 1T1C FeRAM application. However, for the embedded FeRAM applications, the ferroelectric materials are integrated in the logic CMOS process. Therefore, low-temperature crystallized ferroelectric materials are required to avoid the high temperature annealing (>500 ^{o}C) at back-end of CMOS technology. The ferroelectric material (PZT) has attracted much attention as a promising candidate for the embedded FeRAM applications because of its lower crystallization temperature than other materials. To decrease the crystallization temperature of PZT film and obtain a good ferroelectric property, one-step low-pressure crystallization process is performed. 120-nm-thick PZT thin films with well-saturated polarization behavior are successfully fabricated in chapter 3.

As mentioned in 1-1-3, the MFIS FET is the candidate for NDRO nonvolatile FeRAM applications. However, achieving good data retention is difficult for the MFIS structure. Therefore, in chapter 4, we utilized the HfO_2 insulating film to act as the diffusion barrier. High temperature oxygen annealing following the film deposition yields a good leakage property of insulating film because of the formation of interfacial layer in the HfO_2-Si interface. This interfacial layer can reduce the charge injection through the insulator-silicon (I-S) interface, only increasing the physical thickness of insulating film slightly. Additionally, the layer-by-layer crystallization is utilized to improve the metal-ferroelectric (M-F) interface and to reduce the trap states of SBT ferroelectric thin film, resulting in a good retention property.

As the area of ferroelectric capacitors declines toward the submicron regime, measuring their electrical hysteresis is becoming difficult and important. Up to date, only few studies had focused on the electrical hysteresis loops of ferroelectric capacitors with small areas. One approach uses an array of capacitors in parallel, but only average results can be obtained [30]. Recently, Tiedke *et al.* applied a virtual ground method (VGM) to obtain the electrical hysteresis loops of a single nanoscale ferroelectric capacitor using an atomic force microscope to make contact [31]. Open compensation and a linear correction yielded electrical hysteresis loops for small-sized capacitors. More recently, a numerical method for compensating Sawyer-Tower (ST) hysteresis measurements was recently presented [32]. This approach corrects the parasitic capacitance of the probe station and the sense capacitor to obtain the ferroelectric property of micron-sized PZT capacitors (2.5 μm×2.5 μm). In chapter 5, we introduce a constant current method (CCM) [29-30] to obtain the hysteresis plot for single

micron-sized ferroelectric capacitors and also to determine the parasitic effect of the probe station.

As mentioned above, the CC method can be used to determine the electrical hysteresis of small-sized ferroelectric capacitor. However, an abrupt slope of charging current-time curve at high-voltage region may result in some errors of hysteresis loops. Therefore, in chapter 6, we propose a triangular current (TC) method for measuring the hysteresis loop of ferroelectric capacitor to yield an almost noiseless voltage profile and a smooth curve in the high-voltage region. Additionally, the P-V curves of MIS and MFIS capacitors at very low frequency (< 1 Hz) are also addressed in this chapter. Furthermore, the temperature sensitivity of TC method is also discussed.

Either CC method or TC method, they are the current source mode methods. However, the polarization charge of ferroelectric capacitor in the retention and fatigue tests is difficult to determine by both methods. Up to date, only pulse polarization method can be used to determined polarization charge during the retention polarization test. However, it is difficult to record the dynamic variation on switching current during the retention test. Therefore, in chapter 7, the current-voltage (I-V) measurement method is utilized to determine the hysteresis switching current characteristics to yield the polarization-voltage loops of ferroelectric capacitor. In the retention polarization test, the dynamic half-hysteresis switching current characteristics are also recorded by this method, using a modified poling profile to determine the polarization charge. Additionally, the temperature effect of switching current characteristics is also addressed.

1-4. Thesis Outline

The dissertation is organized in to the 7 chapters:

In chapter 1, a brief overview of ferroelectric materials is given. The application of these materials for FeRAM is also introduced. Methods used to measure the hysteresis loops and polarization charge during fatigue and retention tests are also addressed. The motivation of the studies included in this dissertation is also briefly stated.

In chapter 2, the experiential details and measurement setup were addressed.

In chapter 3, we demonstrated low-voltage ferroelectric characteristics suitable for embedded ferroelectric nonvolatile memory applications with the proposed one-step low-pressure oxygen annealing of $PbZr_{0.52}Ti_{0.48}O_3$ thin films. Additionally, the electrical and dielectric properties of $PbZr_{0.52}Ti_{0.48}O_3$ thin films annealed at various oxygen pressures were

discussed and compared.

In chapter 4, layer-by-layer crystallization was applied to fabricate MFIS structure to improve the retention property. The electrical and physical characteristics of the layer-by-layer crystallized MFIS stacks are discussed and compared with that of conventionally crystallized MFIS stacks.

In chapter 5, we introduced a constant current (CC) method to measure the electrical hysteresis of micron-size ferroelectric capacitors. The parasitic effect of a probe station on small-sized ferroelectric capacitors was determined to construct the corrected hysteresis loops. Satisfactory agreement was obtained between the measured dielectric constants and those obtained from the high-field slopes of hysteresis loops that had been corrected for parasitic effects.

In chapter 6, we proposed a triangular current (TC) method to measure the hysteresis loops of ferroelectric capacitors. This method yields an almost noiseless voltage profile and a smooth curve in the high-field region. Additionally, the parasitic effect of the probe station was also determined to yield the corrected hysteresis loop of small-sized ferroelectric capacitors. Moreover, the polarization-voltage (P-V) curve of MIS and MFIS capacitors was determined at very low frequency (< 1Hz). The temperature sensitivity of TC method was also discussed.

In chapter 7, we presented the current-voltage (I-V) measurement method to determine the hysteresis switching current characteristics of ferroelectric capacitors to obtain the polarization-voltage (P-V) loops. Additionally, the dynamic switching current characteristic and retention property were determined. Moreover, the phenomenon of space charge switching was also discussed. Furthermore, the temperature effect of switching current characteristics was also addressed.

Finally, the results of our experiments and analysis are concluded.