

PAPER

An Integrated CMOS Front-End Receiver with a Frequency Tripler for V-Band Applications*

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SUMMARY A direct-conversion receiver integrated with the CMOS subharmonic frequency tripler (SFT) for V-band applications is designed, fabricated and measured using 0.13- μm CMOS technology. The receiver consists of a low-noise amplifier, a down-conversion mixer, an output buffer, and an SFT. A fully differential SFT is introduced to relax the requirements on the design of the frequency synthesizer. Thus, the operational frequency of the frequency synthesizer in the proposed receiver is only 20 GHz. The fabricated receiver has a maximum conversion gain of 19.4 dB, a minimum single-side band noise figure of 10.2 dB, the input-referred 1-dB compression point of -20 dBm and the input third order inter-modulation intercept point of -8.3 dB. It draws only 15.8 mA from a 1.2-V power supply with a total chip area of $0.794 \text{ mm} \times 0.794 \text{ mm}$. As a result, it is feasible to apply the proposed receiver in low-power wireless transceiver in the V-band applications.

key words: V-band, transceivers, CMOS subharmonic frequency tripler, monolithic microwave integrated circuit (MMIC)

1. Introduction

The 7-GHz unlicensed band around 60 GHz for short-range and high-speed communication is being used for new consumer applications such as wireless High-Definition Multimedia Interface (HDMI) for high-definition television (HDTV) video stream and high data-rate wireless personal area networks in recent years. Historically, the implementation of 60-GHz integrated circuits are designed and fabricated by using GaAs or advanced SiGe processes [1]–[3]. However, the advantages of low cost and of high-level integration with digital base-band blocks in CMOS technology are very attractive in wireless system design. As the transition frequency (f_T) of advanced CMOS technology is increased to beyond 400 GHz [4], the CMOS process becomes another potential solution to realize the millimeter-wave integrated circuits [5].

So far, some V-band receivers have been demonstrated in CMOS technology [6]–[10]. The direct-conversion receiver architecture is firstly implemented in the millimeter-wave receivers [6], [7] because of its advantages of high integration and low system complication. Since the frequency of the local oscillator (LO) signal should be nearly the same as the received frequency, high-frequency synthesizer and high-frequency dividers with large power consumption are

required. The heterodyne receiver architecture is the solution for the high-frequency synthesizers because of the twice of the frequency translation [8], [9]. The LO frequency is reduced to two-third [8] or half [9] of the received frequency. However, twice frequency translations make the architecture of the receiver more complicated for image signal processing. Thus, more inductors with large chip area are required. Therefore, the total chip area is increased compared to direct-conversion receiver. Another solution for the high-frequency synthesizers is the frequency multiplier. The new frequency doubler for the LO generation is proposed in [10]. Because of the even order frequency multiplier, the differential output cannot be provided for the mixer operation. Thus, extra effort is required for single to differential converter.

In this paper, a novel CMOS direct-conversion receiver front-end integrated with a fully differential CMOS subharmonic frequency tripler (SFT) [11] is proposed and fabricated. It consists of a two-stage LNA, a current-mode mixer, an output buffer and an SFT. The current-mode operation between the LNA and the mixer improves the linearity of the entire receiver. The proposed direct-conversion receiver front-end can be operated with 20-GHz frequency synthesizer because the SFT is used for 60-GHz LO signals generation. To improve the harmonic rejection ability, the common mode rejection resistor and inductor are applied in the SFT.

The measurement results have shown that the average receiver gain is 18.2 dB and the average single-side band (SSB) noise figure (NF) is 10.9 dB within a 3-dB bandwidth from 53.1 to 59.8 GHz. It only draws 15.8 mA from 1.2-V power supply including low-noise amplifier (LNA), down-conversion mixer, and the SFT. The total chip area of the proposed receiver is $0.794 \text{ mm} \times 0.794 \text{ mm}$ including all test pads and dummy cells. The proposed direct-conversion receiver offers the advantages of small chip area, lower power consumption and low LO frequency requirement with reasonable conversion gain and noise figure. These characteristics greatly ease the design of high-performance VCO and the integration with frequency synthesizers.

This paper is organized as follows. In Sect. 2, the proposed architecture of the direct-conversion receiver front-end that takes advantage of the SFT to reduce the requirement of LO frequency is described. The building blocks of the proposed receiver are also presented. The experimental results are shown in Sect. 3. Finally, conclusion and summary are given in Sect. 4.

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2. Proposed Direct-Conversion Receiver

A block diagram of the proposed direct-conversion receiver [11] is shown in Fig. 1. It consists of an LNA, a down-conversion mixer, an output buffer and an SFT. Here, the use of an SFT allows the LO reference signal to be one-third of the frequency used in a conventional architecture without the SFT. At lower operating frequency, the Q of tuned-circuit components is higher and parasitic capacitances have less impact which makes the VCO have lower phase noise and wider tuning range [2]. The circuit would also be easier to design as a VCO or phase locked loop (PLL) at a lower frequency because of the poor properties of both active and passive devices at V-band. More specifically, it is easier to design high-performance VCOs at low frequency rather than at high frequency. Moreover, the power consumption of the high frequency pre-scaler can be greatly reduced due to a lower operating frequency. For the measurement purpose, output buffers are adopted to match to the 50-ohm output impedance. Each building block in Fig. 1 is described in the following.

2.1 Low-Noise Amplifier

The LNA uses two-stage topology to achieve the required gain and the noise figure. The schematic of proposed LNA is shown in Fig. 2. The first stage is used to minimize the noise figure and provide reasonable gain to suppress the input noise contribution from the subsequent stages. To optimize the circuit performance, a common source (CS) amplifier with source degeneration topology is selected [12]. The degeneration inductor T1 and the gate inductor L1 are chosen here to change the input impedance of M1 to achieve the appropriate input matching and noise matching ability at the desired frequency band. The gate voltage of input stage is provided by the DC bias V_{BIAS} through a large resistor R1. The on-Chip MIM capacitor C1 is designed to block the dc level.

So far, most of the previously reported multi-stage cascaded LNAs use blocking capacitors to re-bias each stage in order to reduce power consumption. However, the parasitic capacitance of input MOSFET M3 in the second stage would make the voltage division with blocking capacitance. This would lead to the small signal gain decrease. Especially, when the circuit operating in the millimeter wave-band, the blocking capacitance is usually designed with a small value to avoid the parasitic capacitance caused by blocking capacitance and the voltage division effects become more serious. To solve this problem, a new inter-stage biasing scheme which gives the gate DC voltage of second stage from the DC drop through means of PMOS load M2 instead of re-bias scheme is proposed. The method can also save a dc pin and make the integration with other blocks easier. The bypass capacitance C2 gives the ac ground node to filter out the noise contributing from the PMOS load M2.

The second stage is optimized for gain and inter-stage

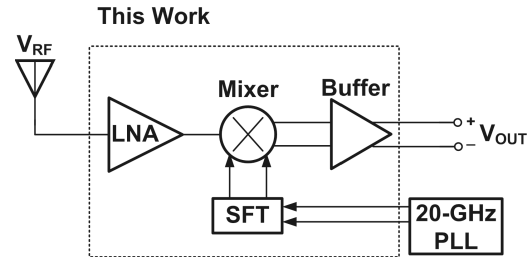


Fig. 1 Block diagram of the proposed 60-GHz direct-conversion receiver.

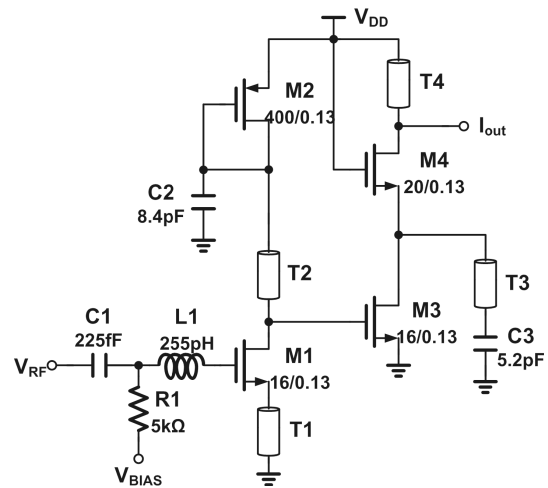


Fig. 2 Schematic of the 2-stage V-band LNA.

matching to provide the maximum output signal to the next stage. A cascode topology with M3 and M4 is used to provide the high isolation capability and improve the stability. A shunt inductor T3 is applied here to resonate out the parasitic capacitance at the drain of M3. This capacitance would cause the pole at frequency near $f_T/2$ and the performance decrease obviously when operating frequency becomes larger than the pole frequency. Therefore, using the scheme can not only provide better noise and gain performance but also improve the degrees of isolation at desired frequency band. A DC block capacitance C3 is applied to make sure the operation points of M3/M4 are not influenced by the inductor T3. The inductors T2 and T4 are loaded here to resonate out the total parasitic capacitance at output of first and second stage, respectively.

2.2 Down-Conversion Mixer and Output Buffers

The circuit diagram of the proposed down-conversion mixer is shown in Fig. 3. It consists of a differential MOS pair M5/M6 and a current mirror formed by M7/M8. In general, the mixer stage dominates the linearity of the entire receiver linearity. One of the most critical issues that affect the mixer linearity is its output signal headroom limitation. To alleviate this problem, the current mode interface between the LNA and the mixer [13] is adopted in this design. The RF current is coupled from the output of the LNA through the

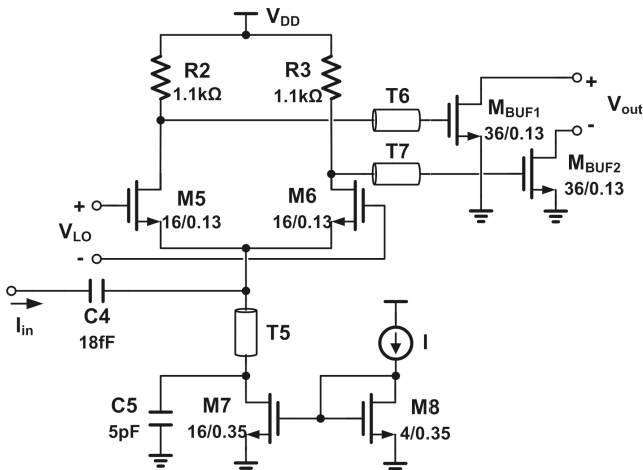


Fig. 3 Simplified schematic of down-conversion mixer and output buffer.

dc blocking capacitance $C4$ and fed into the source of the differential pair $M5/M6$ to mix with the LO signals.

The MOS $M7$ and $M8$ form the current mirror to provide the appropriate DC current for the differential pair. To avoid the noise contribution from the current source, a large bypass capacitance $C5$ is added to filter out the flicker noise from the circuit. The inductor $T5$ is used to resonate out the parasitic capacitance at the source terminal of $M5/M6$. This inductor can also reduce the signal loss caused by parasitic capacitance. The resistors $R2/R3$ are chosen for gain and linearity consideration. An increase in $R2/R3$ results in an increase in conversion gain but a decrease in the headroom at the output node. Thus, there is a trade-off between conversion gain and linearity. Moreover, the $R2/R3$ generates a pole and function as a low-pass filter to suppress the undesired signal. This can markedly improve the LO to IF isolation ability. For measurement considerations, the unity gain open-drain buffers are used to drive the 50-ohm measurement system. It can drive the 50-ohm instruments and obtain the desired output signal.

In comparison with a conventional mixer, the proposed down-conversion mixer has the following advantages. Firstly, the lower noise figure is achieved because of the absence of the noise generated from the transconductance stage in a conventional mixer. Secondly, the DC current through the transconductance stage is not required. Thus the DC current can be markedly reduced to improve the noise performance even more. At last, an improvement in linearity is expected due to the enhancement of voltage headroom at the mixer outputs.

2.3 CMOS Subharmonic Frequency Tripler

The circuit diagram of the proposed CMOS subharmonic frequency tripler is shown in Fig. 4. The proposed SFT can be divided into two stages: the harmonic generation stage and the LO amplification stage. The harmonic generation stage is formed by the NMOS $M9/M10$ and frequency-selected load $L2$. The third order harmonic of the input

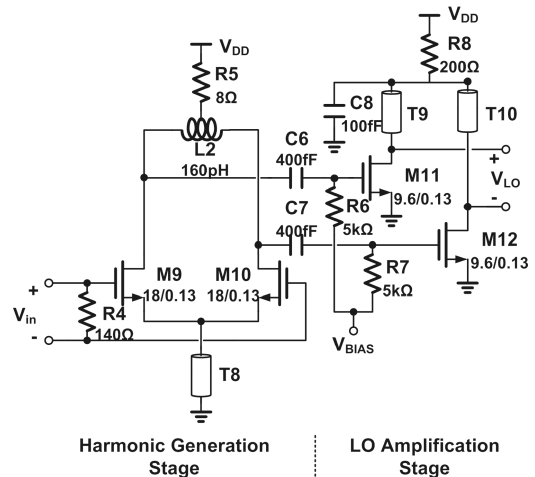


Fig. 4 Circuit diagram of the proposed SFT.

signal is generated by $M9/M10$. The $M9/M10$ is biased at 0.65 V for higher frequency conversion efficiency. The value of inductor $L2$ is chosen so that it can resonate with the total parasitic capacitances at the drain of $M9/M10$ at the third-order harmonic of the input frequency. The output drain current at 3rd order harmonic can be maximized with an appropriate gate-source bias [14]. Resistor $R5$ is designed for the improvement of harmonic rejection ratios (HRRs) to the undesired even-order harmonics because the even order harmonic signals are common-mode signals. The T-line type inductor $T8$ is also introduced to further reduce the even order harmonics. The LO amplification stage is formed by a CS amplifier with the frequency selected load $T9/T10$. The desired 3rd-order harmonic is amplified and all the undesired frequencies are decreased through the band-pass load $T9/T10$. To provide the maximum voltage swing to the mixer stage, the inter-stage ac coupling capacitor is not used. Therefore, the required DC bias value for the mixer is determined by the voltage drop on the resistor $R8$.

The simulated HRR as the function of the $T8$ inductance at 20-GHz input frequency with the input power of 0 dBm is shown in Fig. 5. The characteristics of those T-lines are simulated by the 3D EM CAD tool HFSS. As can be seen, the second HRR is improved with an increase of the $T8$ inductance when $T8$ is smaller than 300 pH. The fourth HRR can also be improved when $T8$ is smaller than 70 pH. However, the HRR improvement is decreased for a large $T8$ inductance.

The change of HRRs can be explained by the simplified half-circuit of the harmonic generation stage as shown in Fig. 6 where v_I is the input signal, v_O is the output signal, the generated current i_{gen} is modeled as the nonlinear characteristic function $f(v_I)$ [15], Y_S and Y_L are the admittance of the transmission line $T8$ and output load, respectively, and Y_{ds} is the effective admittance between drain and source. In general, Y_S is infinite for every odd-order harmonic signal because of their differential property. The output signal $v_{O,even}$ at the even-order harmonic frequency without source admittance Y_S can be expressed as

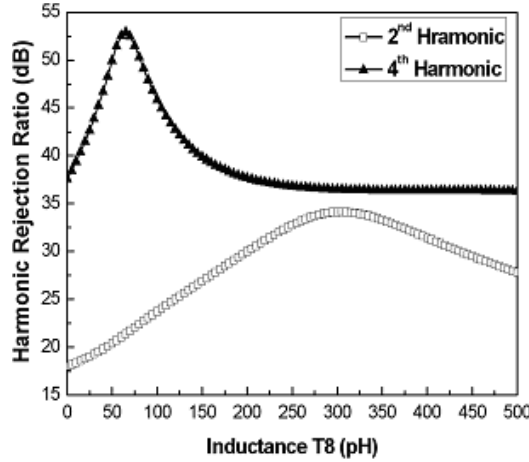


Fig. 5 The simulated HRR as a function of the T8 inductance.

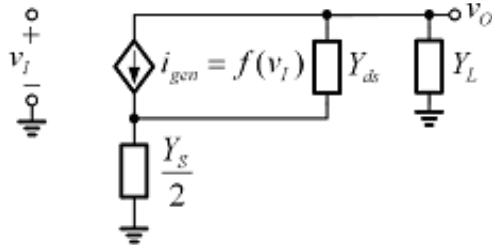


Fig. 6 HRR as a function of the T8 inductance.

$$v_{O,even} = \frac{-i_{gen,even}}{Y_L + Y_{ds}} \quad (1)$$

where $i_{gen,even}$ is the generated output current at the even-order harmonic frequency. If the source admittance Y_S is applied to the harmonic generation stage, the output signal at the even-order harmonic frequency can be expressed as

$$v_{O,even,Y_S} = \frac{-i_{gen,even}}{Y_L + Y_{ds} + \frac{2Y_L Y_{ds}}{Y_S}} \quad (2)$$

From (1) and (2), the improved HRRs can be written as

$$\begin{aligned} HRR_{imp} &= 20 \log \left(\frac{v_{Signal}}{v_{O,even,Y_S}} \right) - 20 \log \left(\frac{v_{Signal}}{v_{O,even}} \right) \\ &= 20 \log \left(\frac{v_{O,even}}{v_{O,even,Y_S}} \right) = 20 \log \left(1 + \frac{2Y_L Y_{ds}}{Y_S (Y_L + Y_{ds})} \right) \end{aligned} \quad (3)$$

can be seen from (3), the HRRs are improved for every even-order harmonic signal with the use of the admittance Y_S . Because the admittance Y_S is of the LC-tank, the maximum HRR improvement is the function of the T8 inductance as can be seen from Fig. 5. From the simulation, the 4th harmonic HRR is better than 2nd harmonic one. Therefore, the selected value of T8 inductance is 300 pH for the maximum HRR to second harmonic frequency.

The simulated output power as a function of input power at input frequency of 20 GHz with the input power range from -14 to 10 dBm is shown in Fig. 7. These characteristics of those T-lines are simulated by the Advanced

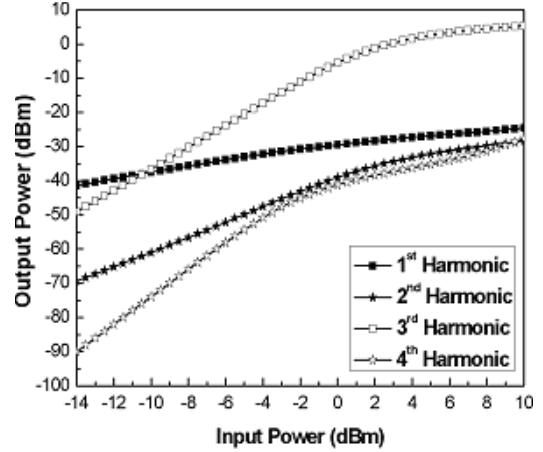


Fig. 7 The simulated output power as a function of the input power.

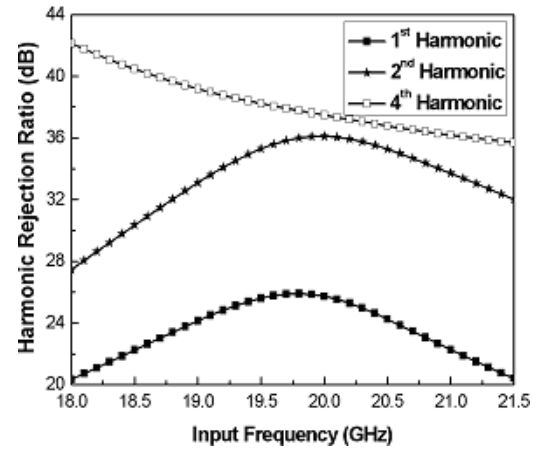


Fig. 8 The simulated HRR as a function of the input frequency.

Design System (ADS). When the input power is above -10 dBm, the desired 3rd-order harmonic output power starts to be larger than that of the fundamental. From -10 to 3 dBm, the 3rd-order harmonic increases with an increase of input power. When the input power is larger than 3 dBm, the output power at 3rd harmonic frequency is nearly saturated. Therefore, the selected input power for the proposed SFT is 3 dBm.

The simulated HRR with the input frequency range from 18 to 21.5 GHz is shown in Fig. 8. The maximum HRR to 2nd-order harmonic occurs at the input frequency of 20 GHz by using the appropriate admittance Y_S . Moreover, within the frequency range of interest, the HRRs are larger than 36 dB and 20 dB to 1st-order harmonic and 4th order harmonic, respectively. By increasing the HRRs, the output signal distortion caused by the undesired LO harmonic signals can be ignored.

3. Experimental Results

The proposed V-band direct-conversion receiver front-end is designed and fabricated using $0.13\text{-}\mu\text{m}$ IP8M Cu CMOS

technology with ultra thick metal of $3.3\ \mu\text{m}$. The chip microphotograph of the proposed direct-conversion receiver is shown in Fig. 9 where the chip area, including all the test pads and dummy metal is $0.794\ \text{mm} \times 0.794\ \text{mm}$. An on-wafer measurement system incorporating a probe station, ground-signal-ground (GSG) coplanar probes, ground-signal-ground-signal-ground (GSGSG) differential coplanar probes, and high-speed cables is used to measure chip performance. Because the differential input signal for the SFT is required, an off-chip 180-degree hybrid is used.

The measured input return loss (S11) at the RF port with the frequency range from 54 to 68 GHz is shown in Fig. 10. The measured S11 of the fabricated receiver front-end is better than 10 dB with the frequency range from 57 to 68 GHz. The measured whole receiver gain and SSB NF with the RF frequency range from 52 to 62 GHz, an intermediate (IF) frequency of 350 MHz, and an input power of 3 dBm for SFT is shown in Fig. 11. Due to model inaccuracies of the transmission line characteristics and possibly

transistor capacitances, the measured center frequency drifts to 57 GHz. The maximum receiver gain of 19.4 dB and the minimum SSB NF of 10.2 dB are measured at 57-GHz RF frequency. The average receiver gain of 18.2 dB and the average SSB NF of 10.9 dB within a 3-dB bandwidth from 53.1 to 59.8 GHz are achieved. This circuit is biased at a 1.2-V supply voltage with current dissipation of 5.76 mA from the LNA and 10.1 mA from the SFT and the mixer. The total dc power consumption is only 18.96 mW.

The measured receiver gain and SSB NF of the proposed receiver versus the SFT input power with the RF frequency of 57 GHz and IF frequency of 350 MHz is shown in Fig. 12. The performances of receiver gain and SSB NF are improved with an increase of the SFT input power. As the SFT input power is larger than 3 dBm, the performances of the receiver gain and SSB NF are nearly saturated as can be seen from Fig. 12. The measured receiver gain and SSB NF as a function of IF frequency with the RF frequency of 57 GHz and SFT input power of 3 dBm is shown in Fig. 13. It can be seen from Fig. 13 that the 3-dB IF bandwidth is around 650 MHz with an average SSB NF of 10.3 dB.

The linearity performances of the fabricated receiver are shown in Figs. 14(a) and 14(b). The measured input-

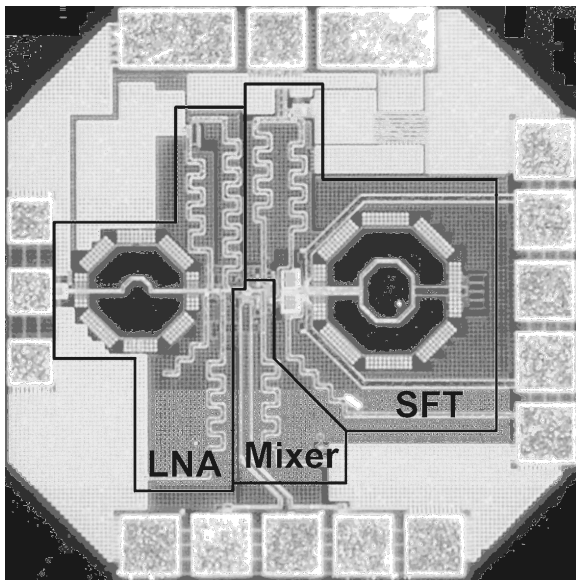


Fig. 9 Chip microphotograph of the proposed receiver.

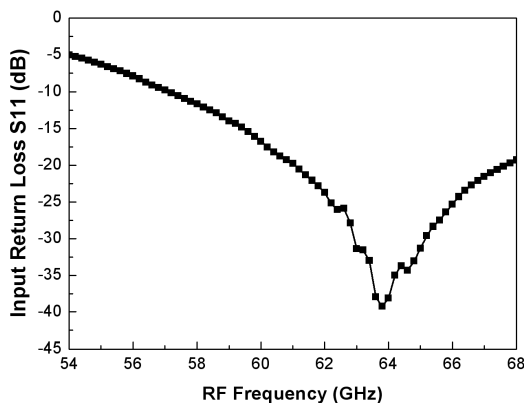


Fig. 10 The measurement result of input return loss S11.

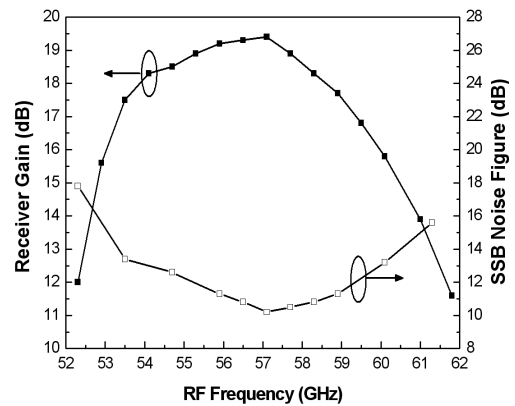


Fig. 11 The measured receiver gain and SSB NF with SFT input power of 3 dBm and IF frequency of 350 MHz.

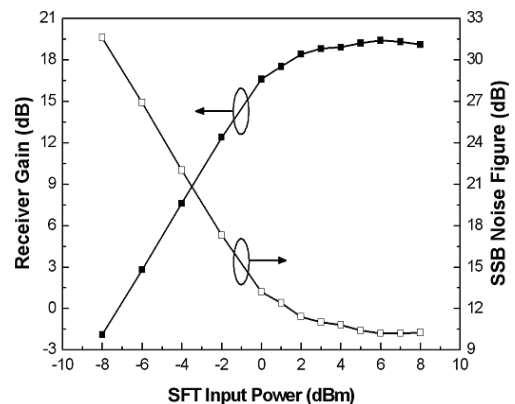


Fig. 12 The measured receiver gain and SSB NF with RF frequency of 57 GHz and IF frequency of 350 MHz.

referred 1-dB compression point (P1 dB) is -20 dBm with 57-GHz RF frequency, 350-MHz IF frequency, and 3-dBm SFT input power. The two tone test for the input third-order inter-modulation intercept point (IIP3) with the RF frequency of 56.5 and 57.5 GHz is also measured. The measured IIP3 is around -8.3 dBm.

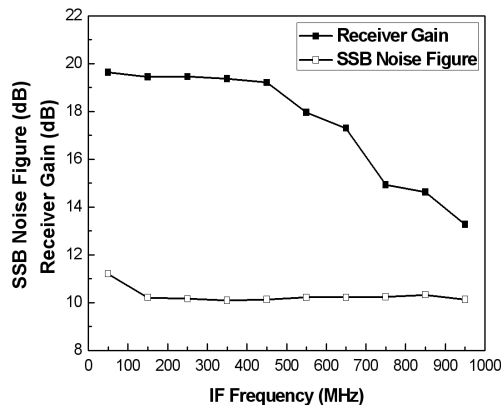


Fig. 13 The measured receiver gain and SSB NF versus IF frequency with 57-GHz RF frequency and 3-dBm SFT input power.

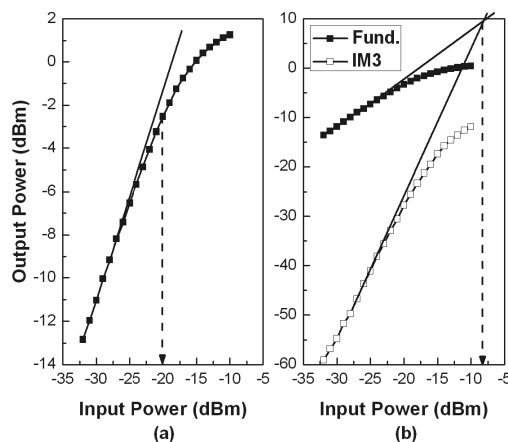


Fig. 14 The measured linearity (a) P1 dB. (b) IIP3.

In Table 1, the recently published CMOS receivers operating in the V-band are compared with the proposed receiver. It can be seen that the proposed receiver can be operated with a lower dc power consumption and reasonable NF. Moreover, this design is the first CMOS receiver integrated with the SFT in the millimeter-wave band.

4. Conclusion

The proposed direct-conversion receiver front-end integrated with the novel CMOS subharmonic frequency tripler is designed and fabricated by using $0.13 \mu\text{m}$ standard CMOS technology. The new SFT circuit is introduced and the optimization for undesired harmonic suppression on the proposed SFT is also developed. As seen from the measurement results, the proposed receiver delivers low power dissipation and small chip area with reasonable receiver gain and noise figure. More specifically, the use of an SFT allows the frequency synthesizer to operate at a lower frequency which has more flexibility in integrating with the frequency synthesizer at high frequency. The proposed SFT has a great potential in the application of LO signal generators for receivers in the millimeter-wave band. In addition, the maximum operation frequency of the frequency divider in a frequency synthesizer can be reduced to one-third and its power dissipation can be reduced significantly by using the proposed SFT. The proposed receiver provides a solution to the low power wireless transceiver in the millimeter-wave band.

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Table 1 Comparison with recently published CMOS receives.

	Tech.	Architecture	Freq. (GHz)	Gain (dB)	NF (dB)	P1dB (dBm)	Power (mW)	Supply Voltage (Volt)	Chip Area (mm ²)
This Work	130-nm CMOS	Homodyne receiver with SFT	53.1 – 59.8	16.4 – 19.4	10.2 – 13.0	-20.0	18.96 ^a	1.2	0.63
[8]	90-nm CMOS	Heterodyne receiver	49.0 – 53.0	26.0 – 31.5	6.9 – 8.3	-25.5	80.0 ^b	1.8	N/A
[9]	90-nm CMOS	Heterodyne receiver	57.0 – 61.0	18.3 – 22.0	5.7 – 8.8	-27.5	36.0 ^b	1.2	N/A
[7]	90-nm CMOS	Homodyne receiver	61.4 – 63.1	21.8 – 22.5	8.4 ^c	N/A	144 ^d	1.2	2.64 ^d
[10]	130-nm CMOS	Heterodyne receiver with frequency doubler	57.0 – 63.0	11.8	10.4	-15.8	76.8	1.2	3.8

a An external signal for RF signal down-conversion is required.

b These values exclude the I/Q modulator for a fair comparison.

c These values are double-side band (DSB) NF

d These values exclude the synthesizer for a fair comparison.

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