Investigation of Cell Stability and Write Ability of FinFET Subthreshold SRAM Using Analytical SNM Model

Ming-Long Fan, *Student Member, IEEE*, Yu-Sheng Wu, *Student Member, IEEE*, Vita Pi-Ho Hu, *Student Member, IEEE*, Pin Su, *Member, IEEE*, and Ching-Te Chuang, *Fellow, IEEE*

***Abstract*—In this paper, the static noise margin (SNM) of FinFET static random access memory (SRAM) cells operating in the subthreshold region was investigated using an analytical solution of 3-D Poisson's equation. An analytical SNM model for subthreshold FinFET SRAM was demonstrated and validated by 3-D technology computer-aided design (TCAD) mixed-mode simulations. When compared with bulk SRAM, the standard 6T FinFET cell showed larger nominal READ SNM (RSNM), better variability immunity, and lesser temperature sensitivity of cell stability. Furthermore, examination of the stabilities of several novel independently controlled gate FinFET SRAM cells by using the proposed SNM model showed significant nominal RSNM improvements in these novel cells. However, the write ability is found to be degraded, which thus becomes an important concern for certain configurations in the subthreshold region. The result obtained indicates that the READ/WRITE word line voltage control technique is more effective than transistor sizing in improving the stability and write ability of the FinFET subthreshold SRAM. Furthermore, the impacts of process-induced variations on cell stability were also assessed. When compared with RSNM, it was found that WRITE SNM is more susceptible to process variations. While 6T is not a viable candidate for subthreshold SRAM, and 8T/10T cells must be used in bulk CMOS, the present analysis established the potential of 6T FinFET cells for subthreshold SRAM applications.**

***Index Terms*—FinFET, Poisson's equation, static noise margin (SNM), subthreshold SRAM.**

I. Introduction

SUBTHRESHOLD circuit design by operating supply voltage $V_{\rm dd}$ below threshold voltage V_T has emerged as an effective solution for ultralow-power applications in portable devices, implanted medical instruments, and wireless body sensing networks [1]. However, with the scaling of $V_{\rm dd}$, static random access memory (SRAM) cell stability has been found to deteriorate. A conventional bulk 6T SRAM cell fails to offer adequate stability in the subthreshold region, and several novel 8T/10T cell structures have been proposed to maintain satisfactory stability and functionality [2]–[5]. Fig. 1 compares the I_d–V_g characteristics of 25-nm bulk and FinFET devices under the same $I_{d,\rm sat}$ at $V_{\rm ds} = 1.0$ V. Owing to its better gate control, the FinFET device has been observed to exhibit significant lower subthreshold swing and leakage current, and 100X greater $I_{\rm on}/I_{\rm off}$ ($V_g = 1.0$ V) ratio than the bulk device. Furthermore, the use of lightly doped (or undoped) silicon fin is found to improve the immunity to variations in the subthreshold region. As such, FinFET SRAM appears to be an ideal candidate for emerging subthreshold SRAM applications.

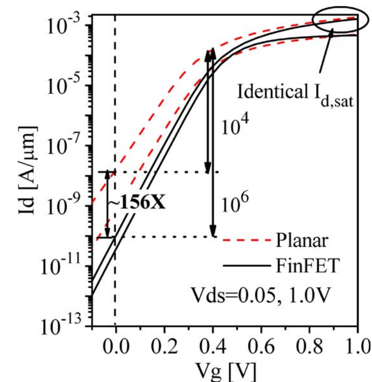

Fig. 1. Comparison of I_d–V_g characteristics for 25-nm bulk and FinFET devices. FinFET is designed with $N_a = 1 \times 10^{17}$ cm^{-3}, $L_{\rm eff} = 25$ nm, $W_{\rm fin} = 7$ nm, $H_{\rm fin} = 20$ nm, and EOT $= 0.65$ nm. Planar bulk device follows the prediction of 2007 International Technology Roadmap for Semiconductors with EOT $= 0.65$ nm.

In this paper, an analytical approach was employed to investigate the READ and WRITE static noise margin (RSNM and WSNM) for 6T FinFET SRAM operating in the subthreshold region. The remainder of this paper is organized as follows: Section II describes the subthreshold FinFET drain current model and the computational flow for subthreshold FinFET SRAM static noise margin (SNM) model, followed by validations with TCAD simulation results under various conditions. In Section III, the advantage of FinFET SRAM is further demonstrated by using TCAD atomistic Monte Carlo simulations considering random dopant fluctuation (RDF) and line edge roughness (LER) for bulk and FinFET cells, respectively. Furthermore, the temperature effect is also assessed. In Section IV, the proposed SNM model is used to analyze the stability of the standard 6T FinFET cell and several novel cells using independent-gate control techniques. In addition,

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The authors are with the National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: austin.ee95g@nctu.edu.tw; pinsu@faculty.nctu.edu.tw).

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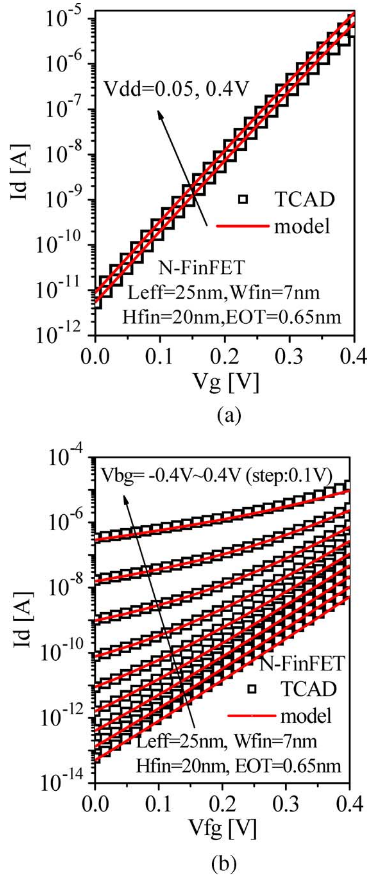

Fig. 2. Verification of the subthreshold current model with TCAD simulations for (a) tied-gate and (b) independent-gate FinFET device.

the impacts of device parameter variations on cell stability and write ability have also been assessed. Finally, the conclusions are presented in Section V.

II. Analytical Model for Subthreshold FinFET SRAM

A. Drain Current Model for Subthreshold FinFET

In this paper, the FinFET subthreshold drain current has been calculated using the following expression [6]:

$$I_{\mathrm{DS}} = \frac{q\mu_n\left(\frac{kT}{q}\right)\left(\frac{n_i^2}{N_a}\right)\left(\exp\left(\frac{-V_S}{kT/q}\right)-\exp\left(\frac{-V_D}{kT/q}\right)\right)}{\int_0^{L_{\mathrm{eff}}}\frac{dy}{\int_0^{H_{\mathrm{fin}}}\int_0^{W_{\mathrm{fin}}}\exp\left(\frac{q\phi(x,y,z)}{kT}\right)dxdz}} \tag{1}$$

where N_a is the doping concentration of the Si-fin body, W_{fin}, H_{fin}, and L_{eff} are the fin width, fin height, and channel length, respectively, V_D and V_S are the voltages for the drain and source terminals, respectively, and φ is the potential distribution inside the fully depleted Si fin, which can be obtained by solving 3-D Poisson's equation with adequate boundary conditions [7].

Note that in addition to the conventional tied-gate mode, the FinFET device has the flexibility to operate in independent-gate control mode. Fig. 2 compares the I_d–V_g characteristics of our subthreshold drain current model and TCAD simulations [8]. It can be seen that our model shows excellent agreement with TCAD results for both tied-gate and independent-gate FinFET current characteristics.

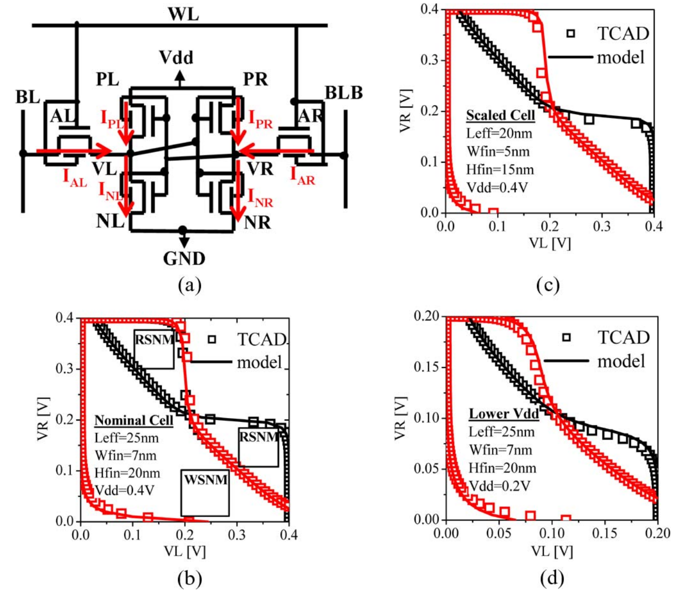

Fig. 3. (a) Conventional (tied-gate) 6T FinFET SRAM cell structure and the individual current components used in constructing butterfly curves. The SNM model verified with TCAD simulations for READ and WRITE of (b) nominal cell, (c) scaled cell, and (d) lower V_{dd} of 0.2 V.

B. SNM Model for Subthreshold FinFET SRAM

Using the subthreshold drain current model, SNM can be calculated by solving Kirchhoff's current law at the cell storage nodes VL and VR [Fig. 3(a)] [9]. The input voltage of the cross-coupled inverter (VL and VR) has been swept and iteratively solved to construct the butterfly curve. Fig. 3(b)–(d) demonstrates the accuracy and scalability of this model with various device parameters (i.e., with a nominal cell, a scaled cell, and a lowered V_{dd} of 0.2 V) for both READ and WRITE. With the butterfly curve, one can quantify the cell stability by RSNM and WSNM for READ and WRITE, respectively. As shown in Fig. 3(b), RSNM can be defined as the size of the maximum square that can fit inside the curves, and WSNM can be defined as the size of the minimum square that spans the curves [10]. When the value of RSNM or WSNM goes negative, the cell becomes unstable (for READ) or fails to write (for WRITE). The SNM computational flow described earlier is summarized in Fig. 4.

In this paper, the analysis is based on FinFET device designed with $N_a = 1\times10^{17}\ \mathrm{cm}^{-3}$, $L_{\mathrm{eff}} = 25$ nm, $W_{\mathrm{fin}} = 7$ nm, $H_{\mathrm{fin}} = 20$ nm, and equivalent oxide thickness (EOT) = 0.65 nm. The strengths of NMOS/PMOS are comparable with dual work functions (4.55/4.75 eV for NMOS/PMOS).

III. Comparison of Standard 6T FinFET and Bulk SRAM

With the established subthreshold SNM model, the nominal RSNM of a FinFET cell can be calculated and compared

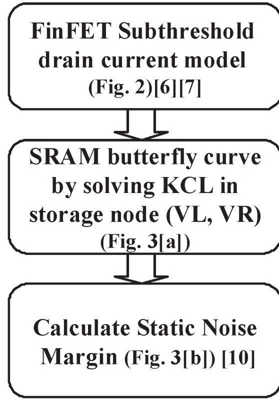

Fig. 4. Calculation flow of the subthreshold FinFET SRAM SNM model.

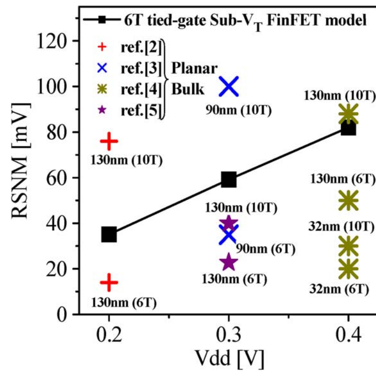

Fig. 5. Dependence of 25-nm FinFET 6T SRAM RSNM on $V_{\rm dd}$ and comparison with RSNM of the reported bulk SRAM cells.

with the published bulk cells, as shown in Fig. 5 [2]–[5]. The standard 6T FinFET tied-gate cell (with $L_{\rm eff} = 25$ nm) is found to exhibit better nominal RSNM than the bulk 6T cell and some 10T cell configurations (labeled 130- and 32-nm nodes). In Fig. 6, the impacts of device variations on bulk (considering RDF) and FinFET (considering fin LER) standard 6T cells have been investigated using TCAD atomistic Monte Carlo simulations [11], [12]. The FinFET cell offers adequate RSNM μ/σ ratio$(= 6.3)$ for the subthreshold operation at $V_{\rm dd} = 0.4$ V, whereas the bulk 6T cell SRAM produces an unacceptable RSNM μ/σ ratio$(= 2.9)$. The self-heating effect in thin Si film-based devices has long been a concern owing to the poor thermal conductivity of the surrounding oxide layers. By using calibrated thin-film thermal conductivity (κ) [13], we can simulate and compare the device temperature and RSNM with self-heating for bulk and FinFET silicon-on-insulator (SOI) 6T cells. As shown in Fig. 7(a), the device temperature rises with increasing $V_{\rm dd}$, and this effect is more severe for the FinFET SOI device. However, for subthreshold operation (e.g., at $V_{\rm dd} = 0.4$ V), the self-heating effect is negligible, and there is essentially no difference in device temperature between the FinFET SOI device and the bulk device. Fig. 7(b) shows the RSNM of FinFET SOI 6T cell and bulk 6T cell at $V_{\rm dd} = 0.4$ V versus temperature. As can be seen for the case at 300 °K, there is no difference in RSNM with and without self-heating. In addition, it can be observed that the FinFET SOI SRAM cell exhibits lesser sensitivity to temperature and offers better RSNM at 400 °K than the bulk cell operated

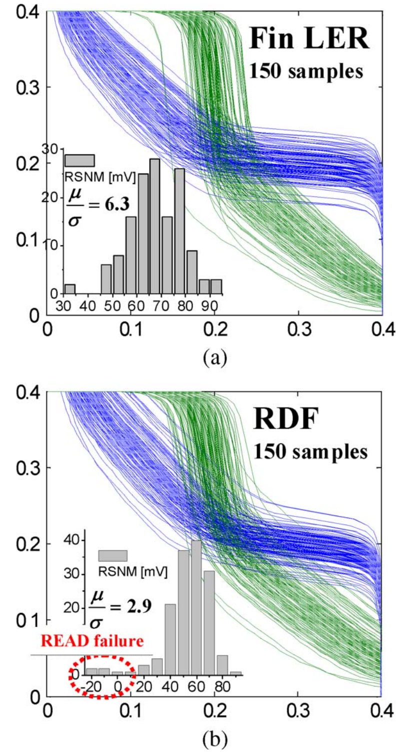

Fig. 6. RSNM characteristics for standard 6T (a) FinFET SRAM considering fin LER and (b) bulk SRAM with RDF.

at 250 °K. Thus, a subthreshold FinFET SRAM cell offers superior variation immunity and temperature sensitivity. In the following section, we will investigate the cell stability and write ability of subthreshold FinFET SRAM cells using the analytical approach.

IV. SNM of Subthreshold FinFET SRAM Cells

Examination of the impacts of transistor sizing and READ/WRITE word line (R/W WL) voltage control (as described in Table I) on FinFET SRAM cell stability and write ability (Fig. 8) shows that the use of double-fin pull-down N-type field effect transistor (NFET) to improve RSNM (or the use of double-fin access NFET to improve WSNM) amounts to about 25 mV of the WL voltage control. The results indicate that R/W WL voltage control is an efficient approach to improve subthreshold SRAM stability and write ability owing to the exponential dependence of drain current on gate voltage in the subthreshold regime.

Owing to the effectiveness of voltage control on FinFET SRAM, the stability and write ability of various novel SRAM cells exploiting the independent-gate control capability of FinFET merit further investigation. Fig. 9 illustrates several novel cell structures reported in the literature [14]–[17]. The Ying–Yang feedback cell [14], shown in Fig. 9(a), grounds the back gates of access transistors (AL, AR) to reduce their strength. A tied-gate pull-down NFET (NL, NR) has been used for increasing the strength of the pull-down NFET holding the "0" storage node to reduce the READ disturb voltage and for decreasing the strength of the pull-down NFET holding "1" storage node to increase the trip voltage of the corresponding

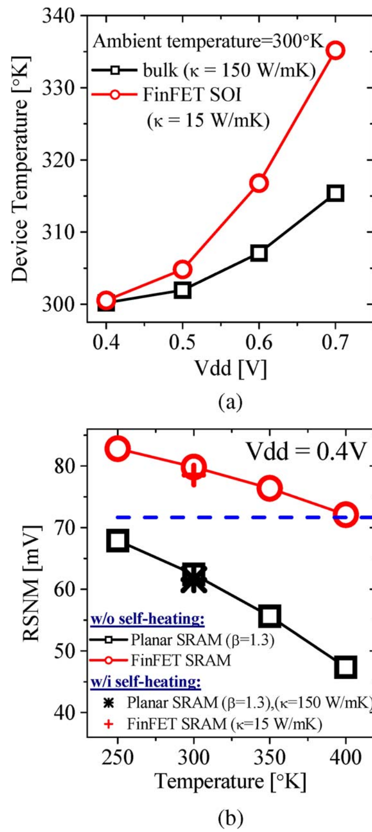

Fig. 7. (a) Impact of V_{dd} on the device temperature for bulk and FinFET SOI devices (ambient temperature was set to 300 °K). (b) Impact of temperature on RSNM for standard bulk and FinFET cells.

TABLE I
TECHNIQUES USED FOR R/W V_{WL} CONTROL AND TRANSISTOR SIZING

	R/W V_{WL} control	Transistor sizing
READ	lowered WL	double-fin NL (NR)
WRITE	boosted WL	double-fin AL (AR)

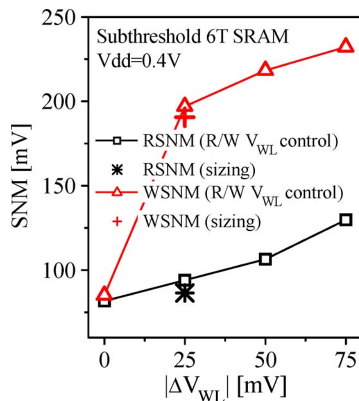

Fig. 8. Impacts of transistor sizing and R/W V_{WL} control on the subthreshold FinFET SRAM stability.

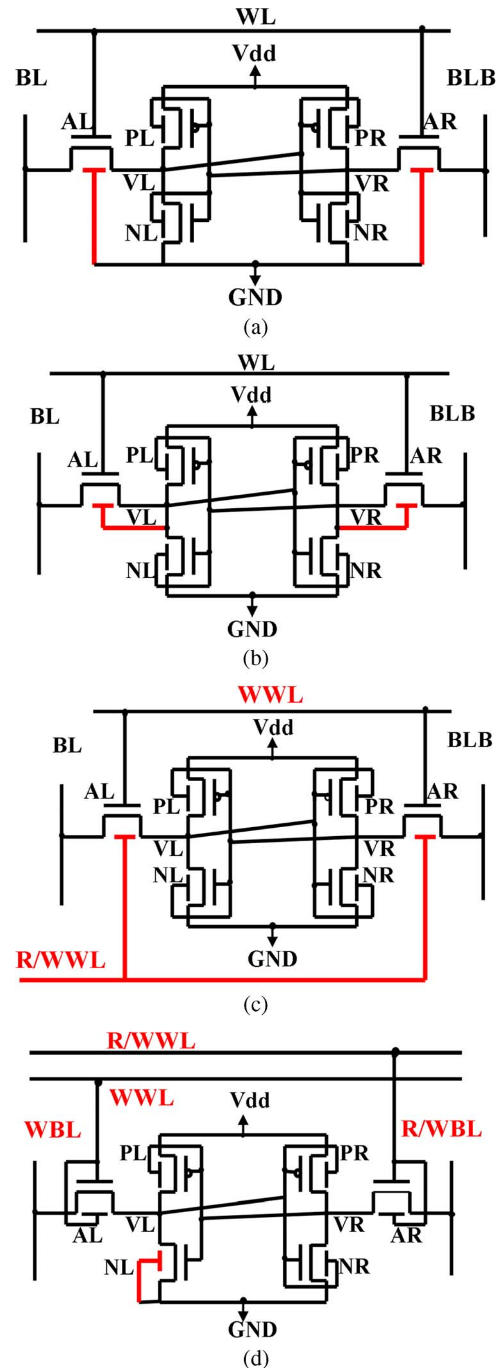

Fig. 9. Various 6T FinFET SRAM cells using independent-gate control technique. (a) Ying–Yang feedback [14]. (b) Improved Ying–Yang feedback [15]. (c) Double word line [16]. (d) Asymmetrical cell [17].

inverter, thus improving the RSNM. The improved Ying–Yang feedback cell [15] shown in Fig. 9(b) modifies the connection of the back gates of access transistors to the cell storage nodes. As such, the strength of the access transistor connected to “1” storage node has been increased to improve the WSNM (write ability) and WRITE performance. For the double word-line structure [Fig. 9(c)] [16], the strength of the access transistor is adaptively controlled by WWL and R/WWL. During the READ operation, only R/WWL turns on to improve RSNM. During the WRITE operation, both WWL and R/WWL turn on to enhance the WSNM and WRITE performance. The asymmetrical cell shown in Fig. 9(d) [17] employs a single-ended READ operation with the right-half cell (through R/WWL and R/WBL). Furthermore, the tied-gate configuration is used for NR to increase its strength and reduce the READ disturb voltage at the cell “0” storage node, whereas the back gate of NL is grounded

TABLE II
NOVEL INDEPENDENT-GATE CONTROL FinFET SRAM CELLS

(I)	Conventional tied-gate 6T
(II)	Ying-Yang feedback [14]
(III)	Improved Ying-Yang feedback [15]
(IV)	Double word-line structure [16]
(V)	Asymmetrical cell [17]

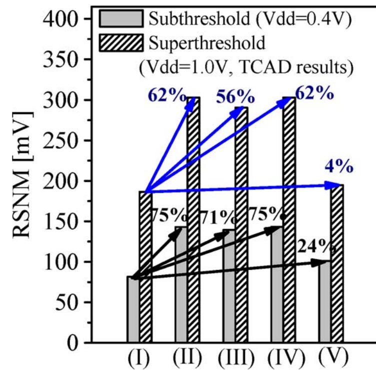

Fig. 10. Comparison of nominal RSNM of different FinFET cell structures listed in Table II.

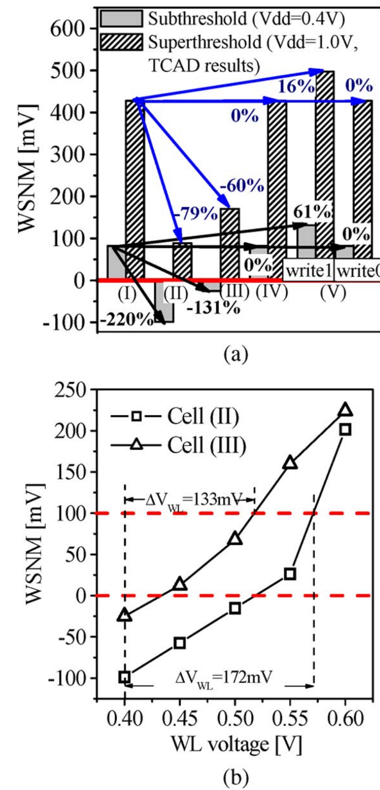

Fig. 11. (a) Comparison of nominal WSNM of different FinFET cell structures listed in Table II. (b) Impact of boosted WL on WSNM for cells (II) and (III).

to reduce its strength and increase the trip voltage of the cell left inverter, thus improving the RSNM.

These cells, in general, offer better RSNM or WSNM than that of the conventional tied-gate 6T cell in the superthreshold region. Subsequently, the RSNM and WSNM of these cells were analyzed in the subthreshold region, and the cases considered are summarized in Table II. In Fig. 10, the nominal RSNMs of different cells have been compared for subthreshold ($V_{\rm dd} = 0.4$ V) and superthreshold ($V_{\rm dd} = 1.0$ V) operations. The novel cells show significant improvement in nominal RSNM, particularly for cells (II), (III), and (IV). This is because the strength ratio of the access transistor (AL, AR) to the pull-down transistor (NL, NR) has been reduced during READ. One can also observe that the percentage improvement of RSNM for subthreshold operation is greater than that observed during superthreshold operation.

Fig. 11(a) compares the nominal WSNM of these cells under subthreshold and superthreshold conditions. Notice that owing to the asymmetrical structure of cell (V), the WSNMs for Write "1" and Write "0" are different. Furthermore, the impact of back-gate connection on WSNM is quite significant in the subthreshold region and is similar to that observed in the RSNM. However, their negative WSNM in the subthreshold region indicates that the degradation of the strength of the access transistor (AL, AR) to the pull-up "tied-gate" P-type field effect transistor (PFET) (PL, PR) may cause problems in WRITE for cells (II) and (III). In Fig. 11(b), the boosted WL has been applied to cells (II) and (III) to restore the strength of the access transistor (AL, AR). However, to achieve adequate WSNM (100 mV), the required boosted voltage is too large (172 and 133 mV for cells [II] and [III], respectively) to make this technique practical.

In Fig. 12(a), the RSNM variation (ΔRSNM) and the percentage change in RSNM have been used to assess the sensitivity of FinFET SRAM cells listed in Table II to process variations. ΔRSNM has been calculated from the RSNM difference between $\pm 20\%$ device parameter deviations (including $L_{\rm eff}$, $W_{\rm fin}$, $H_{\rm fin}$, and EOT), i.e., $\Delta\mathrm{RSNM} = |\mathrm{RSNM}(\mathrm{P} + 20\%) - \mathrm{RSNM}(\mathrm{P} - 20\%)|$. The percentage change in RSNM is defined as the ratio of ΔRSNM to the nominal RSNM. Fig. 12(a) shows that independent-gate-controlled FinFET SRAM cells (cells [II]–[V]) exhibit greater ΔRSNM than that obtained with cell (I). This is because the operation of FinFET in independent-gate mode has worse electrostatic integrity than that in tied gate mode [18], which degrades V_T and RSNM [shown in Fig. 12(b)] variations. However, owing to their significant improvements in nominal RSNM, cells (II)–(IV) still show lesser percentage change of RSNM than cell (I).

Fig. 13 compares the WSNM variation (ΔWSNM) and the percentage change in WSNM for cells (I), (IV), and (V). During WRITE operation, the ΔWSNMs of these cells are found comparable because of similarity in the configurations of access transistors (AL, AR) and pull-up transistors (PL, PR). Owing to its larger nominal WSNM, cell (V) of Write "1" shows $\sim$20% improvement in the percentage change of WSNM. Furthermore, a boosted word line (BWL) can also be used to minimize WSNM variation. When the WL was boosted to 0.42 V, significant suppression of WSNM variation (from $\sim$40 to $\sim$10 mV) and percentage change in WSNM (from $\sim$55% to $\sim$4%) were observed (Fig. 13).

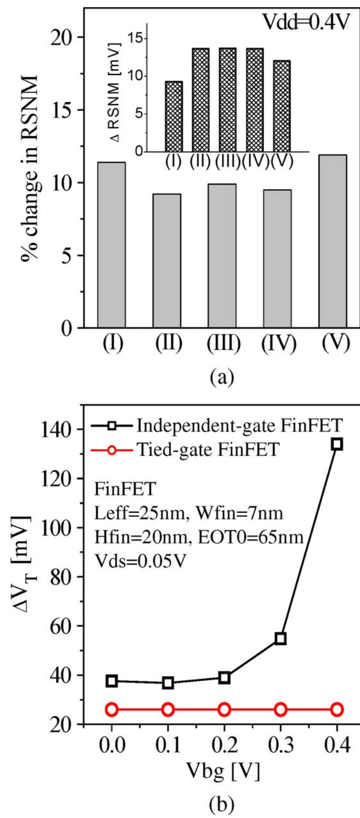

Fig. 12. (a) Comparison of different FinFET SRAM cells listed in Table II on RSNM variation and percentage change in RSNM. (b) Comparison of independent-gate and tied-gate FinFET on V_T variation. Variations in (a) and (b) result from $L_{\rm eff}$, $W_{\rm fin}$, $H_{\rm fin}$, and EOT dimension deviations (±20%).

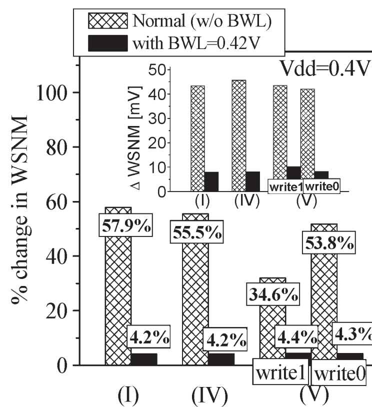

Fig. 13. Comparison of WSNM variation and percentage change in WSNM of different FinFET cell structures listed in Table II. $\Delta\text{WSNM} = [\text{WSNM}(\text{P} + 20\%) - \text{WSNM}(\text{P} - 20\%)]$, where P is the device parameter, such as $L_{\rm eff}$, $W_{\rm fin}$, $H_{\rm fin}$, and EOT.

V. Conclusion

In this paper, the stability and write ability of FinFET subthreshold SRAM have been investigated using an analytical solution of 3-D Poisson's equation. An analytical SNM model for FinFET subthreshold SRAM was demonstrated for the standard 6T cell and novel independent-gate-controlled 6T cells. The results indicate that the R/W WL voltage control technique is more efficient than transistor sizing for the subthreshold SRAM. Furthermore, significant nominal RSNM improvements were observed for the independent-gate-controlled cells. However, for cells (II) and (III), WSNM was severely degraded with the degradation of the strength ratio of the access transistor to the pull-up "tied-gate" PFET. In addition, the impacts of process-induced variations on the cell stability and write ability of various FinFET cells were also assessed. Owing to their better nominal RSNM, cells (II)–(IV) show superior immunity to variations (∼9% change in RSNM). It is found that WSNM is more susceptible than RSNM to process variation and can be effectively improved by boosting WL voltage. As opposed to the need to use 8T/10T cells for bulk subthreshold SRAMs, this paper has demonstrated the potential of 6T FinFET SRAM for subthreshold operation.

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Ming-Long Fan (S'09) was born in Taichung, Taiwan, in 1983. He received the B.S. and M.S. degrees in 2006 and 2008, respectively, from the National Chiao Tung University, Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree with the Institute of Electronics.

His current research interests include the design and modeling of subthreshold SRAM in scaled/exploratory technologies.

Yu-Sheng Wu (S'09) was born in Tainan, Taiwan, in 1982. He received the B.S. and M.S. degrees in electronics engineering in 2004 and 2006, respectively, from the National Chiao Tung University, Hsinchu, Taiwan, where he is currently working toward the Ph.D. degree with the Institute of Electronics.

His current research interests include design and modeling of advanced CMOS devices.

Vita Pi-Ho Hu (S'09) was born in Changhua, Taiwan, in 1982. She received the B.S. degree in 2004 from the National Chiao Tung University, Hsinchu, Taiwan, where she is currently working toward the Ph.D. degree with the Institute of Electronics.

Her research interests include the analysis and design of ultralow-power SRAMs in nanoscaled technologies.

Pin Su (S'98–M'02) received the B.S. and M.S. degrees in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, and the Ph.D. degree from the University of California, Berkeley.

From 1997 to 2003, he conducted his doctoral and postdoctoral research in silicon-on-insulator (SOI) devices the University of California, Berkeley. He was also one of the major contributors to the unified BSIMSOI model, the first industrial standard SOI MOSFET model for circuit design. Since August 2003, he has been with the Department of Electronics Engineering, National Chiao Tung University, where he is currently an Associate Professor. He is an author or coauthor of over 90 research papers in refereed journals and international conference proceedings. His research interests include silicon-based nanoelectronics, modeling and design for advanced CMOS devices, and device/circuit interactions in nano-CMOS.

Ching-Te Chuang (S'78–M'82–SM'91–F'94) received the B.S.E.E. degree from the National Taiwan University, Taipei, Taiwan, in 1975 and the Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1982.

From 1977 to 1982, he was a Research Assistant with the Electronics Research Laboratory, University of California, Berkeley, where he worked on bulk and surface acoustic wave devices. In 1982, he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY. From 1982 to 1986, he worked on scaled bipolar devices, technology, and circuits. He studied the scaling properties of epitaxial Schottky barrier diodes, did pioneering works on the perimeter effects of advanced double-poly self-aligned bipolar transistors, and designed the first subnanosecond 5-kb bipolar ECL SRAM. From 1986 to 1988, he was the Manager of the Bipolar VLSI Design Group and worked on low-power bipolar circuits, high-speed high-density bipolar SRAMs, multigigabit-per-second fiber-optic data-link circuits, and scaling issues for bipolar/BiCMOS devices and circuits. Since 1988, he has managed the High Performance Circuit Group, investigating high-performance logic and memory circuits. Since 1993, his group has primarily been responsible for the circuit design of IBM's high-performance CMOS microprocessors for enterprise servers, PowerPC workstations, and game/media processors. Since 1996, he has been leading the efforts in evaluating and exploring scaled/emerging technologies, such as PD/SOI, UT/SOI, strained-Si devices, hybrid orientation technology, and multigate/FinFET devices, for high-performance logic and SRAM applications. Since 1998, he has been responsible for the research VLSI technology circuit co-design strategy and execution. His group has also been very active and visible in leakage/variation/degradation tolerant circuit and SRAM design techniques. He took early retirement from IBM to join the National Chiao Tung University, Hsinchu, Taiwan, as a Chair Professor in the Department of Electronics Engineering in February 2008. He is currently the Director of the Intelligent Memory and SoC Laboratory at National Chiao Tung University.

Dr. Chuang has received one Outstanding Technical Achievement Award, one Research Division Outstanding Contribution Award, five Research Division Awards, and 12 Invention Achievement Awards from IBM. He received the Outstanding Scholar Award from Taiwan's Foundation for the Advancement of Outstanding Scholarship for 2008 to 2013. He served on the Device Technology Program Committee for IEDM in 1986 and 1987 and the Program Committee for Symposium on VLSI Circuits from 1992 to 2006. He was the Publication/Publicity Chairman for Symposium on VLSI Technology and Symposium on VLSI Circuits in 1993 and 1994, and the Best Student Paper Award Sub-Committee Chairman for Symposium on VLSI Circuits from 2004 to 2006. He was elected an IEEE Fellow in 1994 "For contributions to high-performance bipolar devices, circuits, and technology." He has authored many invited papers in international journals such as the *International Journal of High Speed Electronics*, PROCEEDINGS OF IEEE, IEEE CIRCUITS AND DEVICES MAGAZINE, and Microelectronics Journal. He has presented numerous plenary, invited, or tutorial papers/talks at international conferences such as the International Silicon on Insulator (SOI) Conference, Design Automation Conference (DAC), International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA), the International Solid-State Circuits Conference (ISSCC) Microprocessor Design Workshop, the Very Large Scale Integration (VLSI) Circuit Symposium Short Course, International Symposium on Quality Electronic Design (ISQED), International Conference on Computer-Aided Design (ICCAD), Asia-Pacific Microwave Conference (APMC), International Symposium on VLSI Design, Automation, and Test (VLSI-DAT), International Symposium on Circuits and Systems (ISCAS), International Workshop on Memory Technology, Design, and Testing (MTDT), WSEAS International Conference on Computational Intelligence, Man-Machine Systems and Cybernetics (WSEAS), VLSI Design/CAD Symposium, etc. He was the co-recipient of the Best Paper Award at the 2000 IEEE International SOI Conference. He is the holder of 31 U.S. patents with another 11 pending. He has authored or coauthored over 280 papers.