Design of 2×VDD-Tolerant Power-Rail ESD Clamp Circuit With Consideration of Gate Leakage Current in 65-nm CMOS Technology

Chang-Tzu Wang, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—A low-leakage 2×VDD-tolerant power-rail electrostatic discharge (ESD) clamp circuit composed of the silicon-controlled rectifier (SCR) device and new ESD detection circuit, realized with only thin-oxide 1× VDD devices, has been proposed with consideration of gate leakage current. By reducing the voltage across the gate oxides of the devices in the ESD detection circuit, the whole power-rail ESD clamp circuit can achieve an ultralow standby leakage current. The new proposed circuit has successfully been verified in a 1-V 65-nm CMOS process, which can achieve 6.5-kV human-body-model and 350-V machine-model ESD levels under ESD stresses, but only consumes a standby leakage current of 0.15 μA at room temperature under normal circuit operating conditions with 1.8-V bias.**

***Index Terms*—Electrostatic discharge (ESD), gate leakage, mixed-voltage input/output (I/O), silicon-controlled rectifier (SCR).**

I. Introduction

With the decrease of the power supply voltage for low-power applications, the thickness of the gate oxide has been scaled down in the nanometer CMOS technologies. In a complex microelectronic system, the I/O buffers of CMOS ICs may drive or receive high-voltage signals to communicate with other ICs. Several problems arise in these ICs with mixed-voltage interfaces, such as the gate-oxide reliability and the undesirable leakage current paths [1]–[3]. In addition, the thin gate oxide of only ∼2 nm in a 0.13-μm CMOS technology has been reported to result in a substantial leakage current in the on-chip power-rail electrostatic discharge (ESD) clamp circuit due to its gate leakage issue [4]. In 45-nm CMOS generation and beyond, the high-k metal gate technology is therefore applied to reduce the gate leakage current [5], [6]. Nevertheless, the gate leakage issue still exists in the 90- and 65-nm CMOS technologies, which are currently used in production without the high-k metal gate structure. Therefore, some works have been reported on how to reduce the gate leakage current for digital circuits in advanced CMOS processes [7], [8].

By using the stacked-MOS configuration and/or the high-voltage-tolerant ESD clamp circuit, some designs have been reported to solve ESD protection for the mixed-voltage I/O interfaces with consideration of gate-oxide reliability [9]–[11]. However, those prior designs did not consider the effect of gate leakage current if such circuits are further implemented in nanometer CMOS processes. New designs on the high-voltage-tolerant power-rail ESD clamp circuit need to be developed to further reduce the standby leakage current in nanometer CMOS processes.

In this paper, a low-leakage 2× VDD-tolerant power-rail ESD clamp circuit realized with only thin gate-oxide devices to protect mixed-voltage I/O buffers is proposed. By using the new proposed circuit solution with only thin gate-oxide devices, the standby leakage current of the proposed power-rail ESD clamp circuit can successfully be reduced under the normal circuit operating condition.

II. Review on the High-Voltage-Tolerant Power-Rail ESD Clamp Circuit

A. Gate Leakage Current in Nanoscale CMOS

The gate leakage current cannot be neglected when the gate-oxide thickness is scaled down to 3 nm and below. Based on the BSIM4 model [12] with device parameters provided from foundry, the simulated total gate current of the MOS capacitor with W/L of 5 μm/5 μm and 10 μm/10 μm in 65- and 90-nm CMOS processes are compared in Fig. 1. The gate current of a MOS capacitor is directly dependent on the polygate area. In addition, due to the thinner gate oxide, the gate leakage problem in the 65-nm CMOS process is more serious than that in the 90-nm CMOS process.

B. Gate Leakage Current in the Prior 2× VDD-Tolerant ESD Clamp Circuit

The prior work of the 2× VDD-tolerant ESD clamp circuit used to protect the mixed-voltage I/O buffers is redrawn and shown in Fig. 2 [11]. In the ESD detection circuit, the MOS capacitor with a gate oxide of large area will induce a large amount of gate current from node a to VDD under the normal

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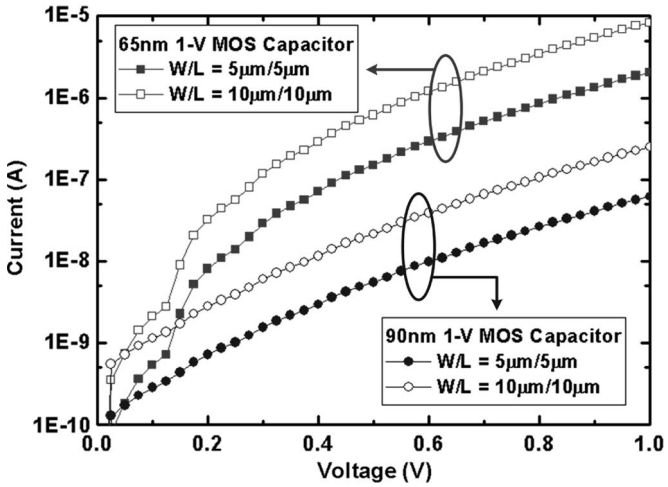

Fig. 1. Gate current of the MOS capacitor in 65- and 90-nm CMOS technologies.

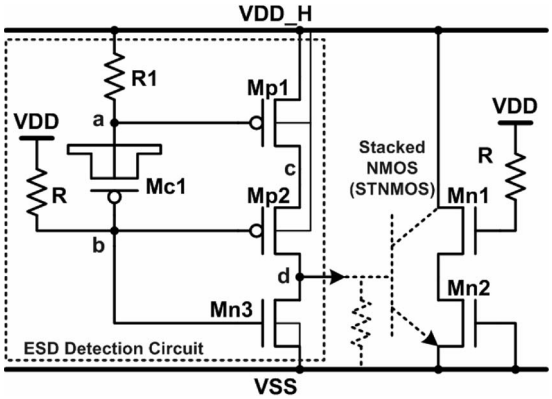

Fig. 2. Prior work of the 2×VDD-tolerant power-rail ESD clamp circuit used to protect the mixed-voltage I/O interfaces [11].

circuit operating condition. The stacked NMOS (STNMOS) in Fig. 2 with a large device size as the ESD clamp device also generates the gate leakage current from VDD_H to VDD via the gate of Mn1. The leakage current path exists from VDD_H through R1, Mc1, and R to VDD, which further causes a voltage drop across the resistor R1, and therefore, the PMOS Mp1 in the ESD detection circuit cannot completely be turned off. With a nonturned-off PMOS, node d could be charged up to some voltage level higher than VSS, which, in turn, provides some triggered current into the substrate of the STNMOS under the normal circuit operating condition. Both the ESD detection circuit and the STNMOS in this prior work suffer from the leakage current issue when this ESD clamp circuit is implemented in a nanoscale CMOS technology.

To overcome the gate leakage current in the MOSFET with a thin gate oxide, one solution is to use the thick gate-oxide device (realized with additional mask and process steps) to implement the MOS capacitor in the ESD detection circuit. In this paper, by using the new proposed circuit solution, the standby leakage current of the 2× VDD-tolerant power-rail ESD clamp circuit realized with only thin gate-oxide devices can successfully be reduced under the normal circuit operating condition.

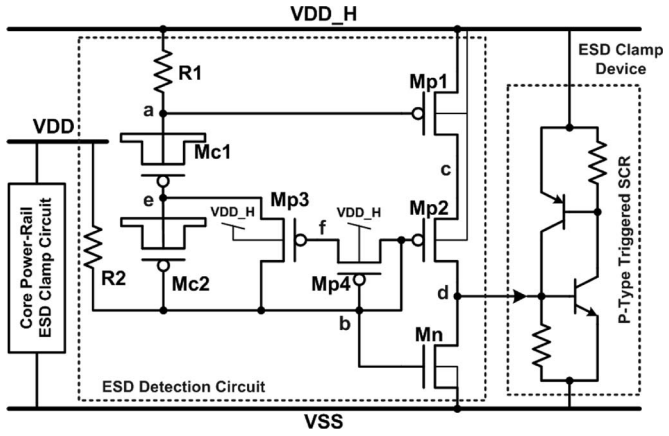

Fig. 3. Proposed low-leakage 2×VDD-tolerant power-rail ESD clamp circuit with a p-type substrate-triggered SCR device as the ESD clamp device, where the ESD detection circuit is designed with consideration of gate leakage current.

III. New Proposed Low-Leakage 2× VDD-Tolerant Power-Rail ESD Clamp Circuit With Consideration of Gate Leakage Current

The proposed low-leakage 2× VDD-tolerant power-rail ESD clamp circuit is shown in Fig. 3. The p-type substrate-triggered silicon-controlled rectifier (SCR) device is used as the main ESD clamp device [13]. The SCR device without a polygate structure is free from the gate leakage problem. The ESD detection circuit is used to improve the turn-on speed of the SCR device with a substrate-triggered mechanism. The new ESD detection circuit with only 1-V thin oxide devices is designed with consideration of gate current and gate-oxide reliability. By utilizing the gate current to bias the ESD detection circuit and optimizing the voltage difference across the gates of the MOS capacitors, the gate leakage current through the MOS capacitor under the normal circuit operating condition can be reduced. Therefore, the total standby leakage currents through the ESD clamp device (SCR) and the ESD detection circuit can be well controlled and minimized by this new proposed design.

In the proposed ESD detection circuit, the PMOS Mp1 and Mp2 are used as the substrate driver to generate the substrate-triggered current into the trigger node of the SCR device during the ESD stress event, but the substrate driver is kept off under the normal circuit operating condition. The NMOS Mn is used to keep the trigger node (node d in Fig. 3) at VSS; thus, the ESD clamp device (SCR) is guaranteed to be turned off during the normal circuit operating condition. The RC time constant from R1, Mc1, Mc2, and the parasitic gate capacitance of Mn is designed around the order of about microseconds to distinguish the ESD stress event from the normal power-on condition. The diode-connected Mp3 and Mp4 are acted as a start-up circuit with initial gate-to-bulk current from VDD_H into the ESD detection circuit and, in turn, conducted some gate current of Mc1 to bias the nodes e and f. After that, the voltage level at node e will be biased at a specified voltage level to reduce the voltage difference across the gate of Mc1 and to minimize the gate leakage current through the MOS capacitors.

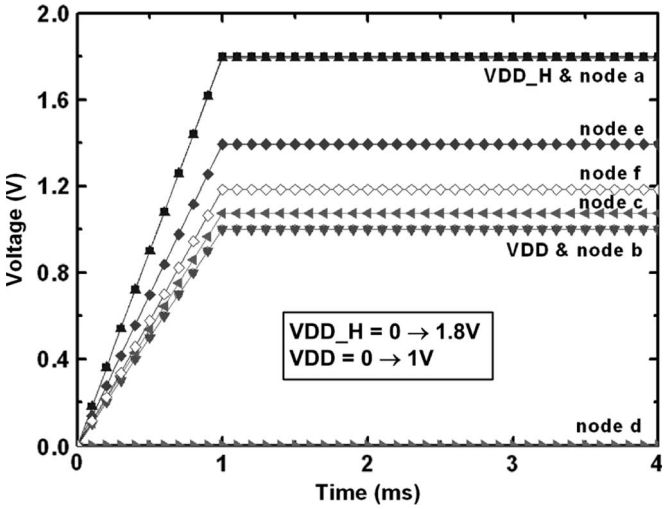

Fig. 4. HSPICE-simulated voltage on the nodes of the ESD detection circuit in a 65-nm CMOS process under the normal power-on condition with VDD_H of 1.8 V and VDD of 1 V.

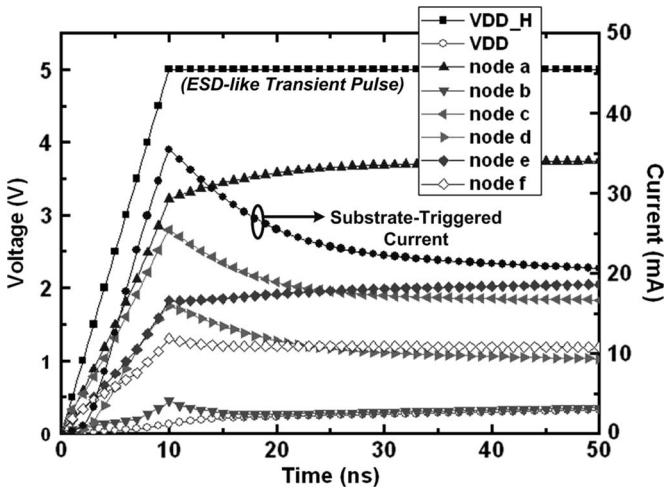

Fig. 5. HSPICE-simulated voltages on the nodes of the ESD detection circuit and the substrate-triggered current, which flows into the SCR device under the 0- to 5-V ESD-like transition on VDD_H.

A. Operation Under the Normal Circuit Operating Condition

During the normal circuit operating condition with VDD_H of 1.8 V, VDD of 1 V, and grounded VSS, the gate voltage (node a) of Mp1 is biased at around 1.8 V through the resistor R1 with a low gate current of the MOS capacitor Mc1 in the new proposed ESD detection circuit. Mp1 is kept off, and no trigger current is generated from the ESD detection circuit to the SCR device. In addition, node b is biased at 1 V through R2 of a 1-kΩ resistor to turn on Mn, which, in turn, keeps the trigger node (node d) of the SCR device grounded. With Mp1 in the OFF-state, no current flows from VDD_H through Mp1 and Mp2 to VSS. The source-to-gate voltage of Mp2 is less than the threshold voltage of a 1-V PMOS transistor, and therefore, node c is kept between 1 V and $(1\ \mathrm{V} + |\mathrm{Vtp}|)$. Node e is biased at ∼1.4 V, and node f is biased at some voltage level between that at node b (1 V) and node e (∼1.4 V). Under such a bias design, all 1-V devices in the proposed ESD detection circuit are free from the gate-oxide reliability issue under the normal circuit operating condition. By using the foundry-provided SPICE model, including the parameters of gate current, the simulated voltage waveforms at the nodes of the proposed ESD detection circuit during and after the normal power-on transition are shown in Fig. 4. VDD_H and VDD are powered on to 1.8 and 1 V, respectively, with a simultaneous rise time of 1 ms. From the simulation results, the voltage differences across the gate-to-drain, gate-to-source, and gate-to-bulk terminals of all devices in the proposed ESD detection circuit do not exceed the process limitation (1.1 V for 1-V devices in a 65-nm CMOS process). Therefore, the ESD detection circuit can be ensured against the gate-oxide reliability issue under the normal circuit operating condition.

B. Operation Under the ESD Transient Event

When a positive fast-transient ESD voltage is applied to VDD_H with VSS grounded and VDD floating (with an initial voltage level of ∼0 V), the RC delay keeps node a at a relatively low voltage level compared with the fast rising voltage level at VDD_H. Mp1 and Mp2, whose initial gate voltages are kept at relatively low voltage levels compared with their source voltages, can quickly be turned on to generate the substrate-triggered current into the trigger node of the SCR device. Finally, the SCR device can fully be turned on into holding state to discharge the ESD current from VDD_H to VSS. To simulate the fast transient voltage of the human-body-model (HBM) ESD event [14], a 0- to 5-V voltage pulse with a rise time of 10 ns is applied to VDD_H as the "ESD-like transient pulse" in HSPICE simulation. Fig. 5 shows the simulated transient voltage and the substrate-triggered current of the ESD detection circuit during the ESD transition. With a limited voltage height of 5 V in the voltage pulse, the voltage transition on each node in the ESD detection circuit can be simulated to check the desired circuit function before device breakdown.

IV. Experimental Results

The new proposed 2× VDD-tolerant power-rail ESD clamp circuit has been fabricated in a 65-nm 1-V fully silicided CMOS process. The widths of SCR devices in the ESD clamp circuit are varied with 30, 45, and 60 μm in the test chip to verify the corresponding ESD robustness. The prior work of Fig. 2 has also been fabricated in the same 65-nm CMOS process to compare standby leakage current and ESD performance.

A. Turn-On Verification

The turn-on behavior of the SCR device used as the ESD clamp device is an important index for ESD protection. To verify the turn-on efficiency of the proposed ESD clamp circuit, a square-type voltage pulse with a rise time of ∼10 ns and a pulse height of 5 V is used to simulate the rising edge of a positive-to-VSS HBM ESD pulse. When the positive voltage pulse is applied to VDD_H of the proposed 2× VDD-tolerant ESD clamp circuit with VSS grounded and VDD floating, the

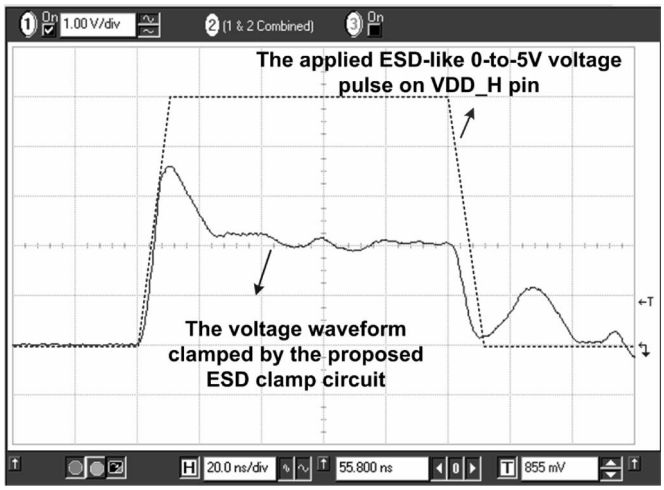

Fig. 6. Measured voltage waveforms clamped by the proposed 2×VDD-tolerant ESD clamp circuit by applying a 0- to 5-V voltage pulse to VDD_H of the proposed ESD clamp circuit with VSS grounded and VDD floating (Y-axis: 1 V/div; X-axis: 20 ns/div).

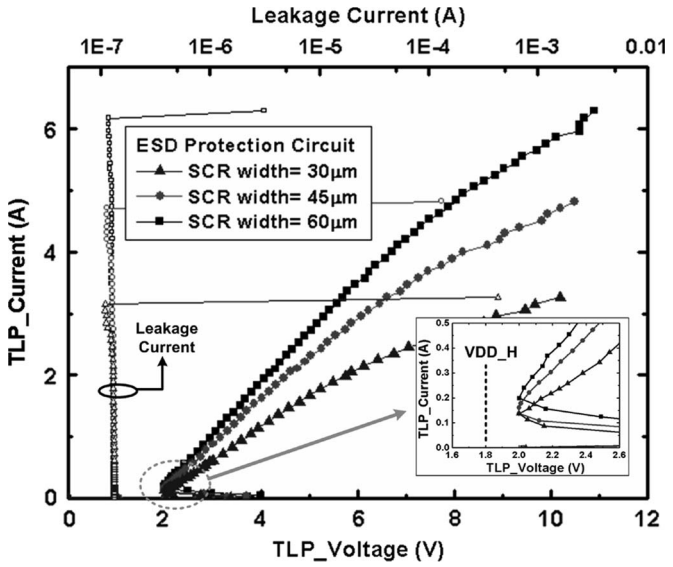

Fig. 7. TLP-measured I–V characteristics of the proposed power-rail ESD clamp circuit with SCR devices of different widths under a positive VDD_H-to-VSS ESD stress. The TLP pulse used in this measurement is with the pulsewidth of 100 ns and the rise time of 2 ns. (Inset) Room-in view on the snapback holding point, where the holding voltage is ∼2 V.

ESD-like voltage pulse will start the ESD detection circuit to trigger on the SCR device and, in turn, provide a low-impedance path from VDD_H to VSS. The voltage waveform on the VDD_H pin clamped by the ESD clamp circuit is shown in Fig. 6. The applied 5-V voltage pulse is quickly clamped down to a low voltage level (∼2 V) by the proposed ESD clamp circuit with an SCR device width of 45 μm. The turn-on time is ∼15 ns, as observed from the maximum voltage peak to the clamped low voltage level in Fig. 6. From the measured voltage waveform, the excellent turn-on efficiency of the proposed ESD clamp circuit during the ESD stress event has successfully been verified.

B. ESD Robustness

To investigate the protection performance against HBM ESD stresses, the transmission line pulse (TLP) generator with a pulsewidth of 100 ns and a rise time of ∼2 ns is used to measure the second breakdown current (It2) of the proposed 2× VDD-tolerant ESD clamp circuit. The TLP-measured I–V characteristics of the ESD clamp circuit with SCRs of different widths are shown in Fig. 7. The ESD clamp circuit with SCR widths of 45 μm can achieve an It2 value of 4.71 A. With the proposed ESD detection circuit in this paper, the trigger voltage of the SCR device is only around 3–4 V. Therefore, the low trigger voltage and high It2 value of the 2× VDD-tolerant ESD clamp circuit can ensure the effective ESD protection capability. The holding voltage of the 2× VDD-tolerant ESD clamp circuit is around 2 V. Such a holding voltage is higher than the voltage level of VDD_H (1.8 V) under the normal circuit operating condition. Therefore, the new proposed 2× VDD-tolerant power-rail ESD clamp circuit is free from the latchup issue in the circuit applications with VDD_H of 1.8 V. Once a higher holding voltage is needed for save guardband to prevent the latchup issue, the stacked diode structure can be added in series with the SCR to increase its overall holding voltage [13].

TABLE I
ESD ROBUSTNESS OF THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT WITH SCR DEVICES OF DIFFERENT WIDTHS

SCR Width	It2	HBM ESD Level	MM ESD Level
30μm	3.15A	4.25kV	225V
45μm	4.71A	6.5kV	350V
60μm	6.17A	> 8kV	450V

The HBM ESD levels and machine-model (MM) ESD levels of the proposed 2× VDD-tolerant power-rail ESD clamp circuit with SCRs of different widths under a positive VDD_H-to-VSS ESD stress are listed in Table I. The HBM (MM) ESD levels of the ESD clamp circuit with SCR widths of 30, 45, and 60 μm are 4.25, 6.5, and > 8 kV (225, 350, and 450 V), respectively, in a 65-nm CMOS process. The corresponding It2 measured by TLP is also listed in Table I.

C. Failure Analysis

The experimental results have shown that the turn-on speed of the SCR device can substantially be improved by the proposed ESD detection circuit. Failure analyses carried out by scanning electron microscopy [15] images provide the visual evidence for that the SCR device can uniformly be triggered on by the ESD detection circuit. Fig. 8 shows the ESD failure location of the proposed ESD clamp circuit with an SCR width of 45 μm after a 6.75-kV VDD_H-to-VSS HBM ESD stress. The failure spots were found at the anode-to-cathode path along the whole SCR device, indicating that the SCR device can uniformly be turned on by the proposed low-leakage ESD detection circuit.

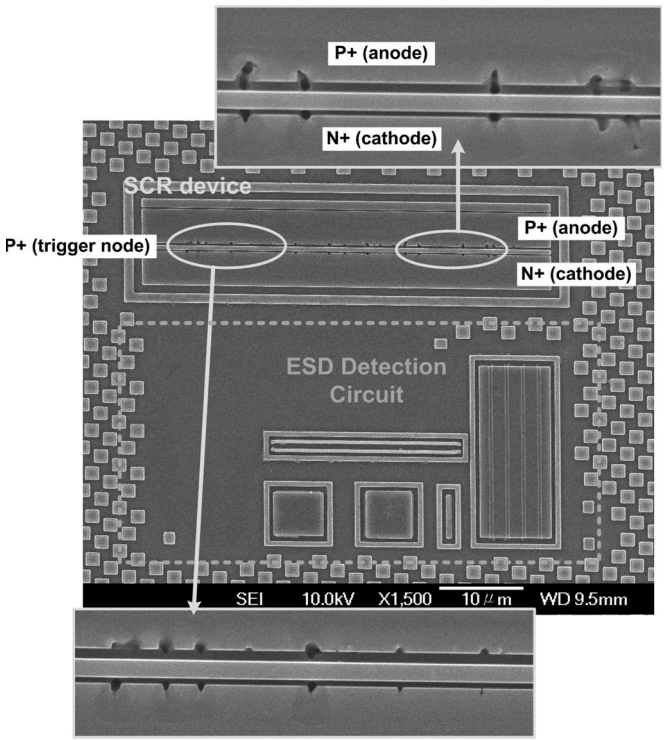

Fig. 8. After a 6.75-kV VDD_H-to-VSS HBM ESD stress, the failure spots were found at the anode-to-cathode path of the whole SCR device.

TABLE II
COMPARISON BETWEEN THE PROPOSED POWER-RAIL ESD CLAMP CIRCUIT AND THE PRIOR WORK

	Prior work (Fig. 2)		This work (Fig. 3)
	ESD Detection Circuit Only	With STNMOS W = 320μm L = 0.12μm	ESD Detection Circuit + SCR W_{SCR} = 45μm
Standby leakage current at 25°C	1.18μA	5.59μA	0.15μA
Standby leakage current at 125°C	12.6μA	66.6μA	1.71μA
HBM ESD Level	n/a	4kV	6.5kV
MM ESD Level	n/a	250V	350V

D. Discussion

The performance comparison between the prior work and the new proposed design of this work is shown in Table II. Although the STNMOS with the leaky polystructure is excluded, the standby leakage currents of the ESD detection circuit in the prior work under VDD_H of 1.8 V and VDD of 1 V at 25 °C and 125 °C are still as large as 1.18 and 12.6 μA, respectively. The standby leakage currents of the proposed ESD clamp circuit with an SCR width of 45 μm under VDD_H of 1.8 V and VDD of 1 V at 25 °C and 125 °C are only 0.15 and 1.71 μA, respectively. The HBM (MM) ESD level of the prior work with STNMOS of $W/L = 320\ \mu\text{m}/0.12\ \mu\text{m}$ is 4 kV (250 V), which is lower than the ESD levels of the proposed ESD clamp circuit. With consideration of ESD robustness and standby leakage current, the new proposed 2× VDD-tolerant ESD clamp circuit has provided an excellent ESD solution for mixed-voltage I/O interfaces in advanced nanoscale CMOS technologies.

V. CONCLUSION

A new 2× VDD-tolerant power-rail ESD clamp circuit with low standby leakage current and high robust ESD performance has successfully been verified in a 65-nm CMOS process, which is realized with only low-voltage (1× VDD) devices without suffering from the gate-oxide reliability issue. The proposed ESD detection circuit, which was designed with consideration of gate leakage current, has been verified with a very small standby leakage current of only 0.15 μA under 1.8-V bias at 25 °C, which is an excellent solution for on-chip ESD protection design for mixed-voltage I/O interfaces in nanometer CMOS technologies.

REFERENCES

[1] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P. J. Roussel, and G. Groeseneken, "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 500–506, Mar. 2002.

[2] Y. Luo, D. Nayak, D. Gitlin, M.-Y. Hao, C.-H. Kao, and C.-H. Wang, "Oxide reliability of drain engineered I/O NMOS from hot carrier injection," *IEEE Electron Device Lett.*, vol. 24, no. 11, pp. 686–688, Nov. 2003.

[3] S. Dabral and T. Maloney, *Basic ESD and I/O Design*. New York: Wiley, 1998.

[4] S. S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp.*, 2002, pp. 1–5.

[5] Z. Krivokapic, W. Maszara, K. Achutan, P. King, J. Gray, M. Sidorow, E. Zhao, J. Zhang, J. Chan, A. Marathe, and M.-R. Lin, "Nickel silicide metal gate FDSOI devices with improved gate oxide leakage," in *IEDM Tech. Dig.*, 2002, pp. 271–274.

[6] C.-H. Jan, P. Bai, S. Biswas, M. Buehler, Z.-P. Chen, G. Curello, S. Gannavaram, W. Hafez, J. He, J. Hicks, U. Jalan, N. Lazo, J. Lin, N. Lindert, C. Litteken, M. Jones, M. Kang, K. Komeyli, A. Mezhiba, S. Naskar, S. Olson, J. Park, R. Parker, L. Pei, I. Post, N. Pradhan, C. Prasad, M. Prince, J. Rizk, G. Sacks, H. Tashiro, D. Towner, C. Tsai, Y. Wang, L. Yang, J.-Y. Yeh, J. Yip, and K. Mistry, "A 45 nm low power system-on-chip technology with dual gate (logic and I/O) high- *k*/metal gate strained silicon transistors," in *IEDM Tech. Dig.*, 2008, pp. 637–640.

[7] K. Sathyaki and P. Paily, "Leakage reduction by modified stacking and optimum ISO input loading in CMOS devices," in *Proc. IEEE Int. Conf. Adv. Comput. Commun.*, 2007, pp. 220–225.

[8] M. Agarwal, P. Elakkumanan, and R. Sridhar, "Leakage reduction for domino circuits in sub-65-nm technologies," in *Proc. IEEE Int. SOC Conf.*, 2006, pp. 164–167.

[9] M.-D. Ker and K.-H. Lin, "Overview on electrostatic discharge protection designs for mixed-voltage I/O interfaces: Design concept and circuit implementations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 235–246, Feb. 2006.

[10] M.-D. Ker and C.-T. Wang, "Design of high-voltage-tolerant ESD protection circuit in low-voltage CMOS processes," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 1, pp. 49–58, Mar. 2009.

[11] M.-D. Ker and W.-J. Chang, "ESD protection design with on-chip ESD bus and high-voltage-tolerant ESD clamp circuit for mixed-voltage IO buffers," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1409–1416, Jun. 2008.

[12] *BSIM Model, Berkeley Short-Channel IGFET Model*. [Online]. Available: http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html

[13] M.-D. Ker and K.-C. Hsu, "Latchup-free ESD protection design with complementary substrate-triggered SCR devices," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1380–1392, Aug. 2003.

[14] For Electrostatic Discharge Sensitivity Testing—Human Body Model (HBM)—Component Level, ESD STM5.1-2001, 2001.

[15] J. Goldstein, D. E. Newbury, P. Echlin, C. E. Lyman, D. C. Joy, E. Lifshin, L. Sawyer, and J. R. Michael, *Scanning Electron Microscopy and X-ray Microanalysis,* 3rd ed. Berlin, Germany: Springer-Verlag, 2003.

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Prof. Ker has served as the Associate Editor for the IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION SYSTEMS. He has been selected as the Distinguished Lecturer in the IEEE Circuits and Systems Society from 2006 to 2007 and the IEEE Electron Devices Society from 2008 to 2010. He was the President of Foundation of the Taiwan ESD Association. He has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences. In 2008, he has been elevated as an IEEE Fellow "for his contributions to the electrostatic protection in integrated circuits and the performance optimization of VLSI Microsystems." He was the recipient as one of the top ten Distinguished Inventors in Taiwan and one of the top hundred Distinguished Inventors in China.