



Parameter extraction in polysilicon nanowire MOSFETs using new double integration-based procedure

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ABSTRACT

A new double integration-based method to extract model parameters is applied to experimental polysilicon nanowire MOSFETs. The threshold voltage and Subthreshold Slope factor are extracted from noisy measured current–voltage characteristics. It is shown that the present method offers advantages over previous extraction procedures regarding data noise reduction. In addition, the normalized mutual integral difference operator method is scrutinized and an improvement of the method is presented.

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1. Introduction

Some of the more promising devices, being considered as possible alternatives to conventional CMOS, are monocrystalline double- and surrounding-gate MOSFETs [1–5]. At the same time, amorphous silicon (a-Si) thin-film transistors (TFTs) have traditionally dominated display applications, but today there is a growing need for better performance than what a-Si technology can provide. Consequently, polycrystalline silicon (poly-Si) TFTs are also receiving a great deal of attention as alternatives for large-area, low cost displays, as well as for other 3-D and large-area electronics applications. However, the performance of conventional planar poly-Si TFTs is still significantly impaired by the abundance of grain boundary defects in the polysilicon film [6]. These defects disturb carrier transport and particularly give rise to high Subthreshold Slope factor and off-state leakage current.

Many polysilicon MOSFET applications require reducing the amount of defects present in the channel body in order to decrease their harmful impact on the device's performance. Several technologies have been proposed to increase the polysilicon film grain size. They include excimer laser annealing [7] and metal-induced lateral crystallization [8], among others.

An interesting alternative to increasing grain size is to reduce the influence of grain boundaries by significantly shrinking the channel body size. The use of polycrystalline nanowire (NW) channel structures seems to be an appealing course of action towards that objective, since the total number of defects decreases significantly when the NW cross section is decreased. In that line, several NW polysilicon MOSFETs have been reported [9–14]. Polycrystalline long-channel ultra-thin body surrounding-gate NW MOSFETs have been proposed and fabricated [15,16] for flexible macroelectronics, as well as for other unconventional applications such as highly sensitive biosensors [17,18].

Modeling the phenomenology specific to polysilicon MOSFETs has been a topic of research for the last three decades [19,20].

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Although the present dominating trends point towards continuous models and away from regional approximation-based models, regional parameters such as threshold voltage and Subthreshold Slope (SS) factor are still considered very important for quality and reliability assessment purposes [21–24].

In the present paper we present a new integration-based method to extract the threshold voltage and SS factor of MOSFETs. This method is applied to measured characteristics of experimental polysilicon nanowire MOSFETs. Other methods are also scrutinized in Section 8.

2. Current model

The transfer characteristics in the weak inversion or subthreshold region of most MOSFETs may be modeled by an exponential function of the gate voltage of the form [25]:

$$I_{Dw} = I_0 \exp\left(\frac{V_G}{n v_{th}}\right), \quad (1)$$

where I_0 is some global coefficient, $v_{th} = k_B T/q$ is the thermal voltage, V_G is the externally applied gate-to-source voltage, and n is the so-called subthreshold ideality factor. The subscript w in I_{Dw} refers to the drain current in the weak inversion region.

On the other hand, the strong inversion region at low drain voltage exhibits a super linear behavior with V_G and a linear behavior with V_D , that can be modeled by a power law, or monomial type, equation of the form [26]:

$$I_{Ds} = K(V_G - V_{Ts})^m V_D, \quad (2)$$

where V_D is the externally applied drain voltage, K is a global conduction coefficient, m is the monomial's order, usually around 2, which reflects the distribution of states in the conduction band tail, and V_{Ts} is the $I_{Ds} = 0$ intercept, which can be viewed as a "strong inversion region-defined" threshold voltage. In this case, the subscript s denotes that the equation is valid in the strong inversion region.

3. Previous method

An integration-based method was proposed in 2001 for extracting model parameters of non-crystalline MOSFETs biased in the saturation region [26]. Its mathematical nature lessens the effect of data noise, in contrast to traditional derivative-based procedures which inherently worsen the data noise problem. The auxiliary function used in that method had been originally proposed in 1999 by our group to extract the model parameters of PN junctions at very low forward voltages [27]. The auxiliary function has the form:

$$H_1(V_G, I_D) = \frac{\int_{V_{Glow}}^{V_G} I_D(V_G) dV_G}{I_D - I_{low}}, \quad (3)$$

where $I_{low} = I_D(V_G = V_{Glow})$, and V_{Glow} is the lower limit of integration. The value of V_{Glow} must be selected such that Eq. (1) is valid at this point; i.e., the current is exponentially dependent on gate bias.

Substituting (1) into (3) and performing the indicated integration we get for the weak inversion, or subthreshold, region:

$$H_{1w}(V_G, I_D) = \frac{n v_{th} I_0 \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right]}{I_0 \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right]} = n v_{th}, \quad (4)$$

which is a constant value that we will refer to as H_{weak} from now on.

Substituting (2) into (3) and performing the indicated integration we get for the strong inversion region:

$$H_{1s}(V_G, I_D) = \frac{V_G - V_{Ts}}{m + 1}, \quad (5)$$

which is a linear equation on V_G with a reciprocal slope of $m + 1$.

This auxiliary function H_1 defined in (3), which can be obtained by numerical integration of the $I_D - V_G$ transfer data measured at a small constant V_D , may be used to readily extract parameters I_0 , n , m , and V_{Ts} by means of (4) and (5). The use of H_1 already is an improvement over derivative-based methods regarding data noise reduction. However, because H_1 still contains the possibly noisy raw current data in the denominator of (3), we propose the use of another auxiliary function to further improve the noise immunity of the procedure.

4. The new auxiliary function

The idea suggested by (3) may be taken one step further with the purpose of reducing even more the effect of data noise. To that end, let us define another function, H_2 , based on successive double integration, to be used as an alternative to (3):

$$\begin{aligned} H_2(V_G, I_D) &\equiv \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G) dV_G dV_G}{\int_{V_{Glow}}^{V_G} I_D(V_G) dV_G - \int_{V_{Glow}}^{V_G} I_D(V_G = V_{Glow}) dV_G} \\ &= \frac{\int_{V_{Glow}}^{V_G} \int_{V_{Glow}}^{V_G} I_D(V_G) dV_G dV_G}{\int_{V_{Glow}}^{V_G} I_D(V_G) dV_G - I_{low} V_G}. \end{aligned} \quad (6)$$

Replacing (1) into (6) and solving the integral yields for the subthreshold region:

$$H_{2w}(V_G, I_D) = \frac{n v_{th} I_{low} \left\{ n v_{th} \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right] - V_G \right\}}{n v_{th} I_{low} \left[\exp\left(\frac{V_G}{n v_{th}}\right) - 1 \right] - I_{low} V_G} = n v_{th}, \quad (7)$$

which is the exact same result obtained in (4) using H_1 . However, as will be confirmed later, the use of H_2 provides better noise immunity than H_1 .

Replacing the strong inversion transfer Eq. (2) into (6) and solving the integral yields:

$$H_{2s}(V_G, I_D) = \frac{V_G - V_{Ts}}{m + 2}, \quad (8)$$

which is a linear equation on V_G with a reciprocal slope of $m + 2$, in a similar fashion as H_{1s} in (5), except that in this case the reciprocal slope is $m + 2$.

5. Extraction procedure

The procedural sequence used to extract the parameter values proceeds as follows:

- 1) Numerically calculate the first and second integrals versus V_G of the measured $I_D(V_G)$ at low V_D . With these calculate function H_2 using (6).
- 2) Select an appropriate linear range of V_G in the strong inversion region to fit equation H_{2s} in (8) to the calculated H_2 data.
 - a) Extract the values of m and V_{Ts} from the linear fit.
 - b) Calculate K with (2) using the two extracted values of m and V_{Ts} .
- 3) Determine H_{weak} as the value of H_2 in a range of the weak inversion region where it remains approximately constant.
- 4) Calculate the phenomenological V_T as the value of V_G corresponding to the intersection of H_{weak} and H_{2s} .

6. Parameter extraction

This new extraction procedure was applied to experimental data of polycrystalline silicon nanowire *n*-channel MOSFETs, as shown in Figs. 1 and 2, fabricated at the Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, using a process similar to that reported in Ref. [28]. In order to avoid very long or narrow devices, they were designed using a layout of multi-nanowire and multi-finger source and drain, as is shown in Fig 3. The devices were later measured at the University of Central Florida, Orlando, FL, USA.

Three devices with the following makeup were used: undoped poly-Si NW body with a rectangular cross section of 60 nm × 18 nm, channel lengths of 0.4, 1.0, and 2.0 μm, *n*⁺ polysilicon gate with 10²¹ cm⁻³ doping, gate SiO₂ oxide thickness of 20 nm, and *S/D* doping density of 5 × 10²⁰ cm⁻³.

The measured transfer and output characteristics of three transistors with different mask channel lengths are presented in Fig. 4 at *V_D* = 10 mV and *V_G* = 2.5 V respectively.

The first step in the parameter extraction procedure is to calculate the auxiliary function *H*₂ from the measured transfer characteristics using (6). The result for *L_m* = 0.4 μm at *V_D* = 10 mV, with *V_{Glow}* = 0, has been plotted in Fig. 5a. The auxiliary function *H*₁ is

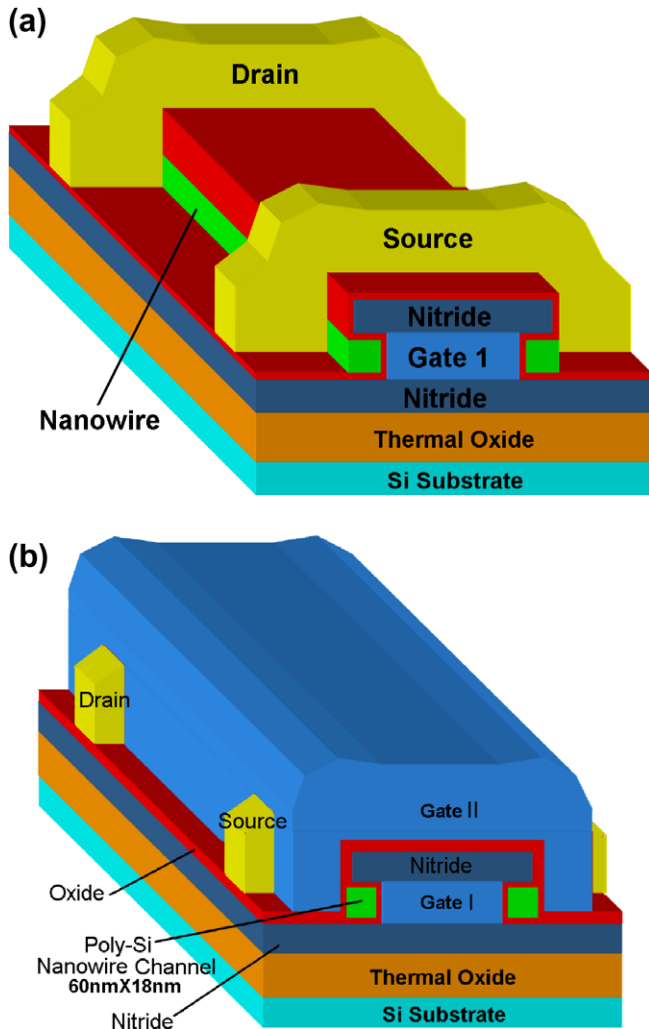


Fig. 1. Geometrical schematic of the poly-Si NW MOSFETs before (a) and after (b) second gate (top gate) and dielectric deposition.

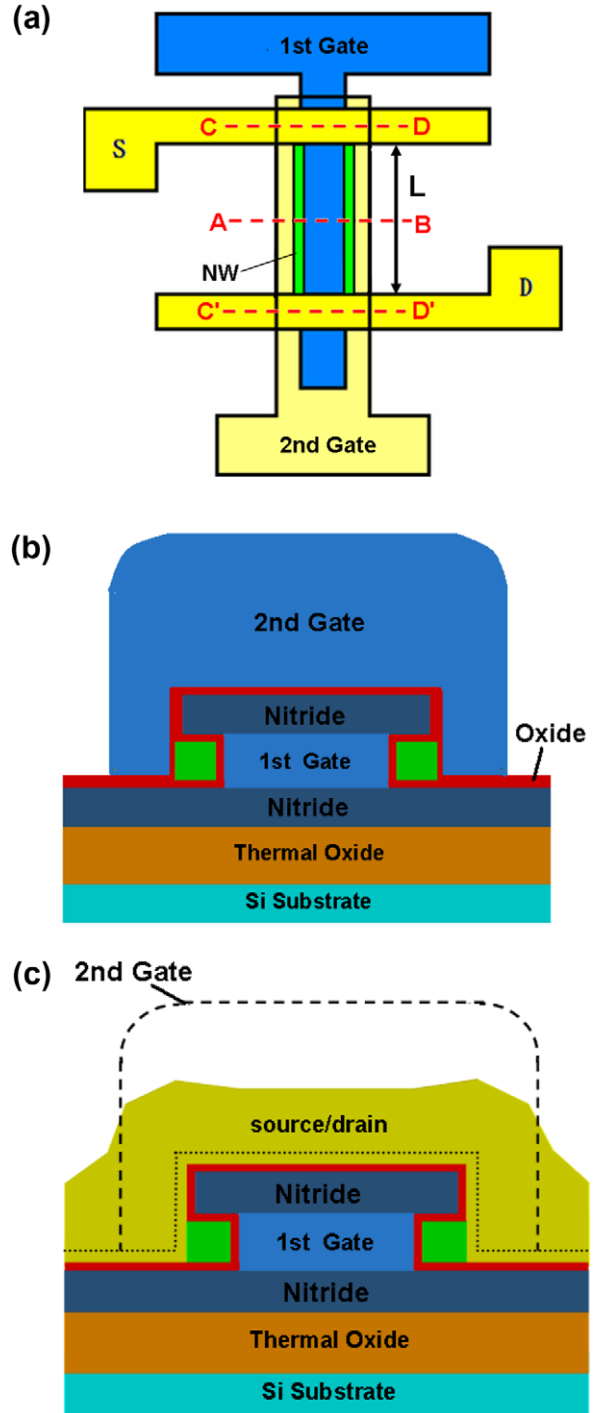


Fig. 2. Top view (a) and cross-section views along red dashed line A-B (b), C-D (c) and C'-D' (c) of the poly-Si NW MOSFETs. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

also shown to illustrate the advantage of using the double-integral auxiliary function regarding noise reduction.

Notice in Fig. 5a that in weak inversion below threshold, *H*_{1W} and *H*_{2W} have approximately the same value, as expected from (4) and (7), although the curve corresponding to *H*₂ is less noisy. However, in the strong inversion region above-threshold, despite *H*_{1S} and *H*_{2S} having the same shape, they differ in slope, in agreement with the expected *m* + 1 and *m* + 2 reciprocal slope behaviors as indicated in (5) and (8). The curve corresponding to *H*_{2S} is also obviously less noisy.

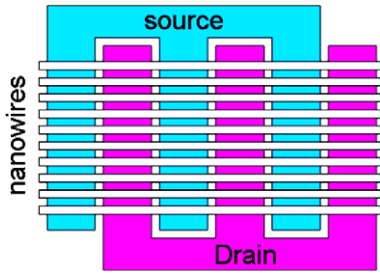


Fig. 3. Layout of the device using multi-nanowire and multi-finger source and drain.

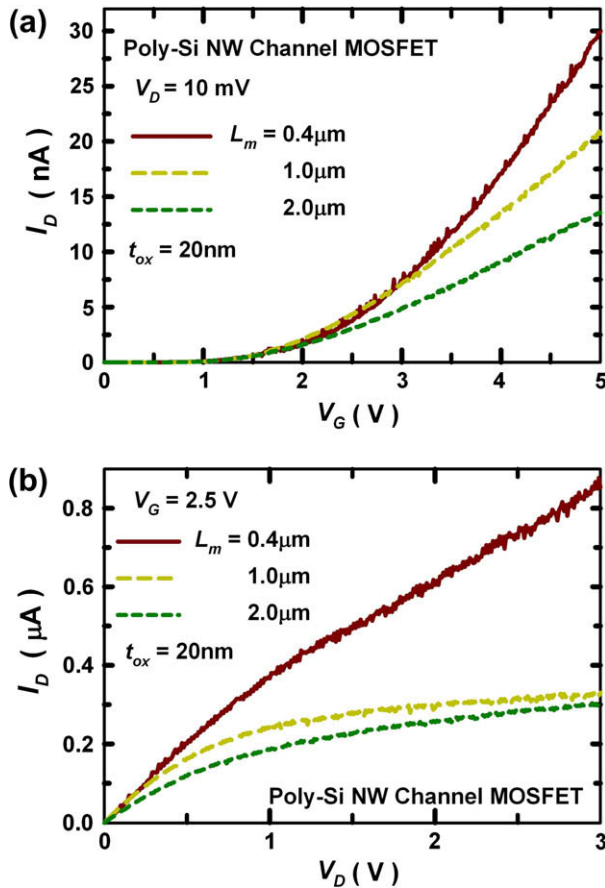


Fig. 4. Transfer (a) and output (b) characteristics of the experimental poly-Si nanowire n -channel MOSFETs, with $L_m = 0.4, 1.0$ and $2.0 \mu\text{m}$ gate lengths.

Next, an appropriate V_G range is selected in the strong inversion region to extract the parameters m and V_{T_S} by fitting equation (8) to the corresponding segment of H_{2S} . This function is plotted in Fig. 5b together with the linear extrapolation of its strong inversion region. The values extracted from the straight line are $m = 2.1023$, and $V_{T_S} = 0.9171 \text{ V}$.

The value of K was then calculated using (2) in the same range, with the extracted values of m and V_{T_S} . The result is shown in Fig. 6. We point out that K looks fairly constant at a mean value of $K = 158.78 \text{ nA/V}^{(m+1)}$, for the chosen V_G range.

As a confirmation of the procedure's effectiveness, Fig. 7 presents the measured transfer characteristic together with the model playback, calculated with (2) using the extracted values of m , V_{T_S} and K , for the device of $L_m = 0.4 \mu\text{m}$ at $V_D = 10 \text{ mV}$.

We recall that V_{T_S} is the $I_{D_S} = 0$ intercept, which we have referred to as the “strong inversion region-defined” threshold voltage.

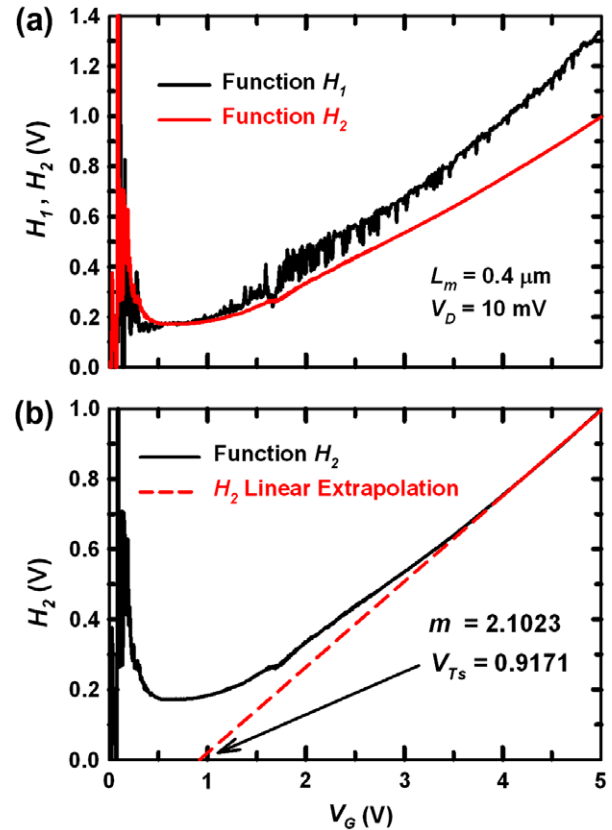


Fig. 5. (a) Plot of both H_1 and H_2 functions vs V_G , to illustrate the noise reduction effect obtained by using H_2 . (b) Plot of H_2 vs V_G for device with $L_m = 0.4 \mu\text{m}$ and $V_D = 10 \text{ mV}$, and its linear extrapolation (red dashed line) used to determine the value of V_{T_S} as the intersection with the V_G -axis. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

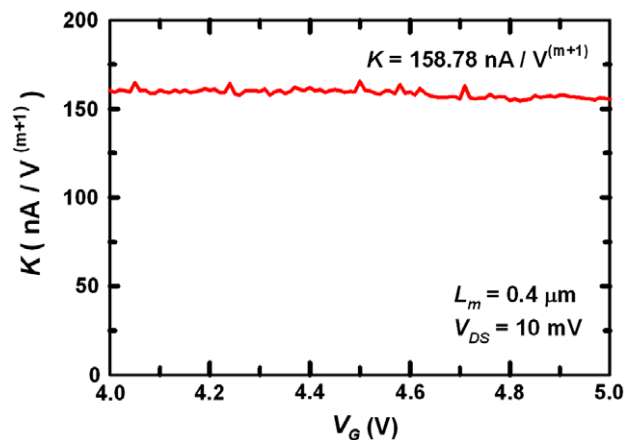


Fig. 6. Plot of K vs. V_G as calculated from (2), using the extracted values of m and V_{T_S} for the device with $L_m = 0.4 \mu\text{m}$ at $V_D = 10 \text{ mV}$. The value of K shown corresponds to the mean value of the curve.

However, we propose that a more phenomenological definition of threshold voltage, V_T , for these devices would be the weak inversion-to-strong inversion transition gate voltage. In order to find it, we need to know the value of the subthreshold H_{weak} . Fig. 8 shows a close up view of H_2 in a range of low V_G . We see that function H_2 is approximately constant from $V_G = 0.6 \text{ V}$ to 0.8 V , and has a mean value of $H_{weak} = 0.1727$.

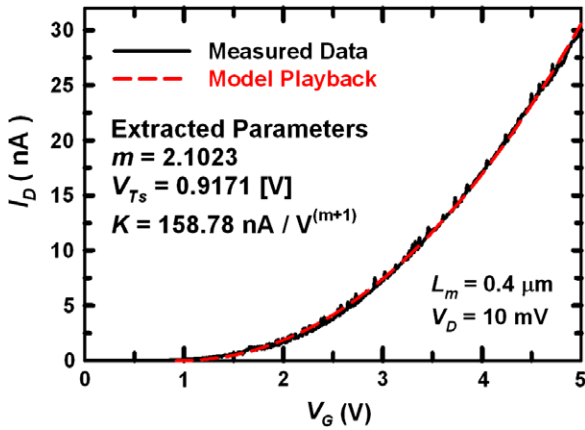


Fig. 7. Measured transfer characteristic and model playback (red dashed line) resulting from the extracted parameters. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

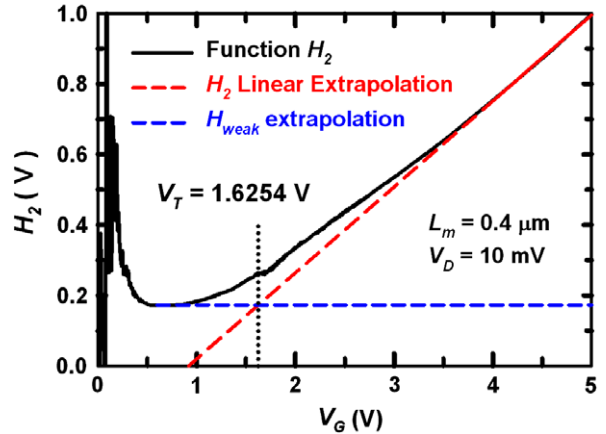


Fig. 9. H_2 vs. V_G and its two asymptotic linear extrapolations: strong (oblique straight red dashed line) and weak (horizontal blue dashed line) regions. The value of V_G at which the intersection occurs, corresponds to V_T . (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

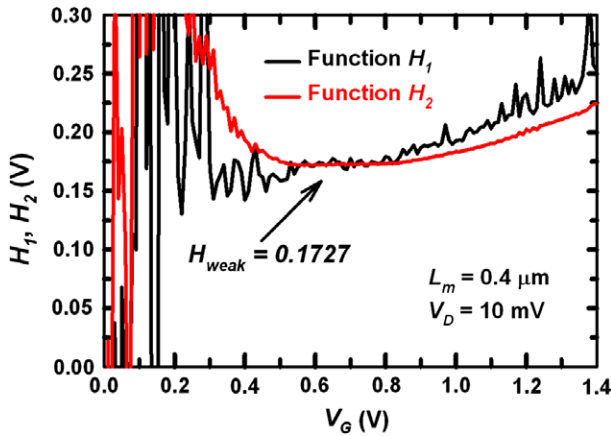


Fig. 8. Close up view of the subthreshold H_1 and H_2 functions. From this region, a mean value of $H_{weak} = 0.1727$ is found.

Finally, the phenomenological threshold voltage V_T is obtained as the value of V_G where H_{weak} intersects the linear extrapolation of the strong inversion region of H_2 (H_{2S}). A value of $V_T = 1.6254$ V is the result for the device with $L_m = 0.4 \mu\text{m}$ at $V_D = 10$ mV. Fig. 9 presents this last step of the procedure. It is important to point out that V_{Ts} (the threshold voltage for strong conduction) fits well the $I_D(V_G)$ characteristic for strong conduction but not for weak conduction. On the other hand, the phenomenological V_T is defined using the asymptotic behavior of both regions.

7. Extraction results

In what follows we present all the results obtained for the rest of the devices at three values of $V_D = 10, 20,$ and 50 mV. The extracted values are presented in Table 1.

The value of the Subthreshold Slope factor (volts of gate voltage change per decade of drain current change) can be readily calculated from function H_2 in the weak inversion or subthreshold region (H_{weak}) using the following formula:

$$SS = \ln(10)n v_{th} = \ln(10)H_{weak} = 2.3H_{weak}. \quad (9)$$

For the case of the $0.4 \mu\text{m}$ channel length device, H_2 approximately has a mean value of $H_{weak} = 0.1727$, which corresponds to an $SS = 397$ mV/decade. The extracted values of SS are plotted versus channel length in Fig. 10 for three small drain voltages.

Table 1

Results obtained using the double integration-based parameter extraction method, for all transistors available.

Device	L_m (nm)	V_D (mV)	m	V_{Tl} (V)	K (nA/ $V^{(m+1)}$)	H_{2weak} (V)	V_T (V)
Poly-Si NW MOSFET parameter extraction results							
DB1	400	10	2.10	0.92	159	0.17	1.63
		20	1.93	1.07	216	0.16	1.71
		50	1.79	1.20	274	0.16	1.80
DB3	1000	10	1.45	1.19	302	0.15	1.70
		20	1.46	1.19	299	0.15	1.71
		50	1.45	1.21	304	0.14	1.71
DB4	2000	10	1.46	1.07	187	0.15	1.60
		20	1.41	1.13	201	0.14	1.63
		50	1.42	1.13	195	0.14	1.60

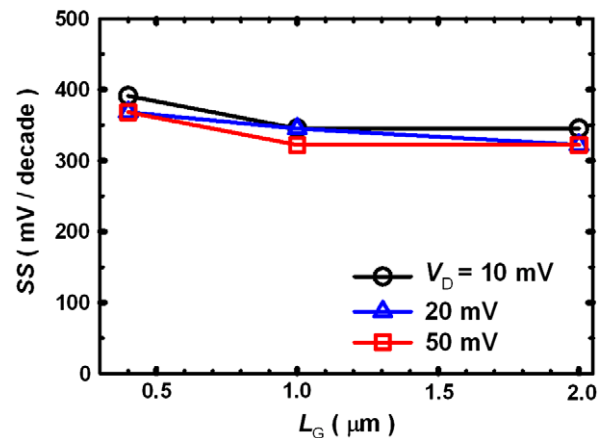


Fig. 10. Extracted Subthreshold Slope factor vs. channel length.

8. Comparison and improvements of previous methods

In order to show the advantages of the present method, we will test some previous methods using the same experimental data. We

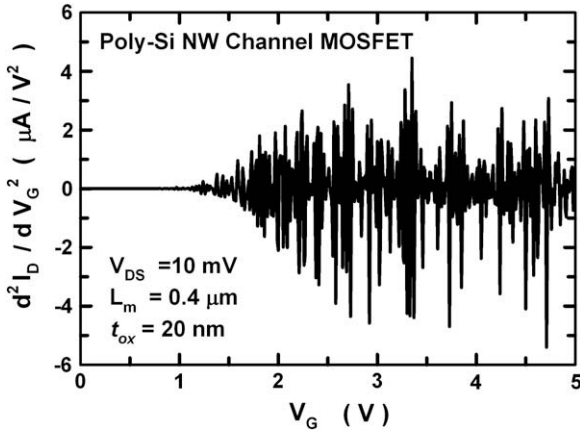


Fig. 11. Second-derivative method [29] for extracting the threshold voltage. This method fails because of the experimental noise; i.e., it is not possible to evaluate the point at which the maximum occurs.

start with the second-derivative method [29], which determines V_T as the gate voltage at which the derivative of the transconductance (i.e., $dg_m/dV_G = d^2 I_D = dV_G^2$) is maximum. Fig. 11 shows that this method fails when it is applied to the present experimental data because of the noise; i.e., it is not possible to evaluate the point at which the maximum occurs.

We will now test the transition method [30], which uses the sub-threshold-to-strong inversion transition region of MOSFETs to extract the threshold voltage. It is based on an auxiliary operator that involves integration of the drain current as a function of gate voltage. The following function G_1 is numerically calculated from the measured data.

$$G_1(V_G, I_D) = V_G - 2 \frac{\int_0^{V_G} I_D(V_G) dV_G}{I_D} \quad (10)$$

A plot of G_1 versus $\ln(I_D)$ should be a straight line below threshold where the current is dominated by diffusion and consequently it is predominantly exponential. As soon as V_G is greater than the inflexion point of the plot $I_D(V_G)$, function G_1 drops abruptly. Therefore, the maximum value of G_1 corresponds to the threshold voltage of the device. This method fails with the present data because the plot $I_D(V_G)$ does not have an inflexion point; therefore, function G_1 does not present a maximum value.

We will now test the normalized mutual integral difference operator method [31,32] to extract the threshold voltage. This method is based on a normalized version of the transition method, with the normalized mutual integral difference operator expressed as follows:

$$P(V_G, I_D) = \frac{G_1(V_G, I_D)}{V_G} = 1 - 2 \frac{\int_0^{V_G} I_D(V_G) dV_G}{V_G I_D} \quad (11)$$

According to this method, V_T is the value of V_G at the maximum value of P . Fig. 12 shows that this method is sensitive to the noise when it is applied to the present experimental data. This is due to the fact that the denominator of (11) does not contain integration.

An improvement of the normalized mutual integral difference operator method could be obtained by using successive integration. In order to do so, we need to explain the origin of this method, which can be understood by analyzing the following ideal case of a MOSFET modeled with a simple level = 1 SPICE model, where $I_D = 0$ for $V_G < V_T$ and I_D is proportional to V_G for $V_G > V_T$. Using the previous simplifying assumption, V_T is the point that joins two different linear behavior of $I_D(V_G)$; therefore, the function is nonlinear at this point.

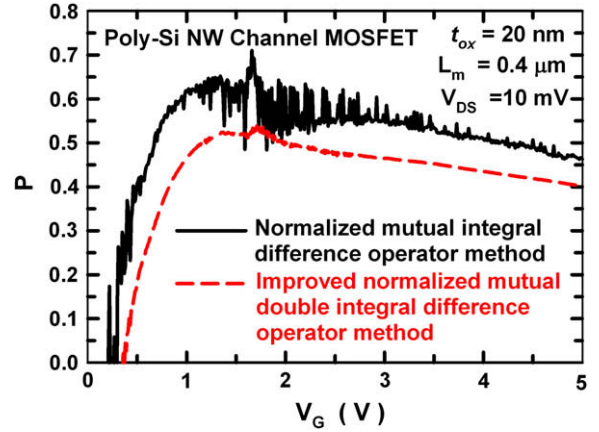


Fig. 12. Normalized mutual integral difference operator method [30,31] and improved normalized mutual double-integral difference operator method.

On the other hand, the operator D ,

$$\begin{aligned} D(V_G, I_D) &= \int_0^{I_D} V_G(I_D) dI_D - \int_0^{V_G} I_D(V_G) dV_G \\ &= V_G I_D - 2 \int_0^{V_G} I_D(V_G) dV_G, \end{aligned} \quad (12)$$

which was proposed in 1996 [33], has the property of eliminating the linear term and is a measurement of nonlinearity. This operator presents sensitivity to noise because the term $V_G I_D$ does not contain integration. Following the ideas about successive integration in distortion analysis [34], the following operator also eliminates the linear term:

$$D_2(V_G, I_D) = V_G \int_0^{V_G} I_D(V_G) dV_G - 3 \int_0^{V_G} \int_0^{V_G} I_D(V_G) dV_G dV_G. \quad (13)$$

Normalizing the previous equation, we obtain the improved normalized mutual double-integral difference operator method

$$\begin{aligned} P_2(V_G, I_D) &= \frac{D_2(V_G, I_D)}{V_G \int_0^{V_G} I_D(V_G) dV_G} \\ &= 1 - 3 \frac{\int_0^{V_G} \int_0^{V_G} I_D(V_G) dV_G dV_G}{V_G \int_0^{V_G} I_D(V_G) dV_G}. \end{aligned} \quad (14)$$

A plot of P_2 is also presented in Fig. 12 and we see how the effects of experimental noise are reduced. The value of V_T is about 1.5 V, which is in agreement with the results presented in Section 7. We observe that this method is not very precise because the maximum value is very broad.

9. Conclusions

We have presented a new method to extract MOSFET regional model parameters based on the first and second integrals of the transfer characteristics. The method has proved capable of extracting the key parameters of polysilicon nanowire MOSFETs regional models, in the subthreshold region, as well as in the strong inversion region, where the drain current of these devices exhibits a power law behavior with respect to the gate voltage. However, the procedure is equally applicable to other devices with linear-like or super linear above-threshold transfer characteristics. The method has been tested on a batch of experimental polysilicon NW MOSFETs of several gate lengths whose model parameters have been extracted. The proposed new method has demonstrated that it offers advantages over traditional extraction procedures regarding data noise reduction and ease of application. The

normalized mutual integral difference operator method [31,32] is scrutinized and an improvement, based on successive integration, is presented.

References

- [1] Ortiz-Conde A, García Sánchez FJ, Muci J, Malobabic S, Liou JJ. A Review of core compact models for undoped double-gate SOI MOSFETs. *IEEE Trans Electron Dev* 2007;54(1):131–40.
- [2] Song J, Yu B, Yuan Y, Taur Y. A review on compact modeling of multiple-gate MOSFETs. *IEEE Trans Circ Syst I* 2009;56(8):1858–69.
- [3] Jiménez D, Iñiguez B, Suñé J, Marsal LF, Pallarès J, Roig J, et al. Continuous analytic current–voltage model for surrounding gate MOSFETs. *IEEE Electron Dev Lett* 2004;25(8):571–3.
- [4] Liu F, He J, Zhang L, Zhang J, Hu J, Ma C, et al. A charge-based model for long-channel cylindrical surrounding-gate MOSFETs from intrinsic channel to heavily doped body. *IEEE Trans Electron Dev* 2008;55(8):2187–94.
- [5] Yang J, He J, Liu F, Zhang L, Liu F, Zhang X, et al. A compact model of silicon-based nanowire MOSFETs for circuit simulation and design. *IEEE Trans Electron Dev* 2008;55(11):2898–906.
- [6] Fossum JG, Ortiz-Conde A. Effects of grain boundaries on the channel conductance of SOI MOSFETs. *IEEE Trans Electron Dev* 1983;30(8):933–40.
- [7] Giust GK, Sigmon TW. High-performance thin-film transistors fabricated using excimer laser processing and grain engineering. *IEEE Trans Electron Dev* 1998;45(4):925–32.
- [8] Lee SW, Ihn TH, Joo SK. Fabrication of high-mobility p-channel poly-Si thin film transistors by self-aligned metal-induced lateral crystallization. *IEEE Electron Dev Lett* 1996;17(8):407–9.
- [9] Im M, Han J-W, Lee H, Yu L-E, Kim S, Jeon SC, et al. Multiple-gate CMOS thin-film transistor with polysilicon nanowire. *IEEE Electron Dev Lett* 2008;29(1):102–5.
- [10] Lin HC, Lee MH, Su CJ, Huang TY, Lee CC, Yang YS. A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel. *IEEE Electron Dev Lett* 2005;26(9):643–5.
- [11] Lin HC, Lee MH, Su CJ, Shen SW. Fabrication and characterization of nanowire transistors with solid-phase crystallized poly-Si channels. *IEEE Trans Electron Dev* 2006;53(10):2471–7.
- [12] Lin HC, Hsu HH, Su CJ, Huang TY. A novel multiple-gate polycrystalline silicon nanowire transistor featuring an inverse-T gate. *IEEE Electron Dev Lett* 2008;29(7):718–20.
- [13] Hsu HH, Liu TW, Chan L, Lin CD, Huang TY, Lin H-C. Fabrication and characterization of multiple-gated poly-si nanowire thin-film transistors and impacts of multiple-gate structures on device fluctuations. *IEEE Trans Electron Dev* 2008;55(11):3063–9.
- [14] Hsu HH, Lin HC, Chan L, Huang TY. Threshold-voltage fluctuation of double-gated poly-Si nanowire field-effect transistor. *IEEE Electron Dev Lett* 2009;30(3):243–5.
- [15] Chen W-C, Lin C-D, Lin H-C, Huang T-Y. Fabrication of novel nanowire field effect transistors. 21st international microprocesses and nanotechnology conference (MNC), October 27–30; 2008. <<http://imnc.jp/2008/>>.
- [16] Lin H-C, Chen W-C, Huang T-Y, Lin C-D. Performance enhancement in double-gated poly-Si nanowire transistors with reduced nanowire channel thickness. *IEEE Electron Dev Lett* 2009;30(6):644–6.
- [17] Lin Y-C, Lu K-C, Wu W-W, Lih JB, Chen J, Tu N, et al. Single crystalline PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures and nanodevices. *Nano Lett* 2008;8(3):913–8.
- [18] Lin C-H, Hung C-H, Hsiao C-Y, Lin H-C, Ko F-H, Yang Y-S. Poly-silicon nanowire field-effect transistor for ultrasensitive and label-free detection of pathogenic avian influenza DNA. *Biosens Bioelectron* 2009;24(10):3019–24.
- [19] Ortiz-Conde A, Fossum JG. Subthreshold behavior of thin-film small-grain polysilicon MOSFETs. *IEEE Trans Electron Dev* 1986;33(10):1563–71.
- [20] Chen R, Zheng X, Deng W, Wu Z. A physics-based analytical solution to the surface potential of polysilicon thin film transistors using the Lambert W function. *Solid-State Electron* 2007;51(6):975–81.
- [21] Ortiz-Conde A, García Sánchez FJ, Liou JJ, Cerdeira A, Estrada M, Yue Y. A review of recent MOSFET threshold voltage extraction methods (invited). *Microelectron Reliab* 2002;42(5):583–96.
- [22] Schneider MC, Galup-Montoro C, Machado MB, Cunha AIA. About the concept of threshold in MOS transistors. In: *Proceedings electrochemical society*, PV 2005-08; 2005. p. 447–54.
- [23] Schneider MC, Galup-Montoro C, Machado MB, Cunha AIA. Interrelations between threshold voltage definitions and extraction methods. In: *NSTI nanotech 2006 technical proceedings*, vol. 3; 2006. p. 868–71.
- [24] de Andrade MGC, Martino JA. Threshold voltages of SOI MuGFETs. *Solid-State Electron* 2008;52(12):1877–83.
- [25] Liou JJ, Shireen R, Ortiz-Conde A, García-Sánchez FJ, Cerdeira A, Gao X, et al. Influence of polysilicon-gate depletion on the subthreshold behavior of submicron MOSFETs. *Microelectron Reliab* 2002;42(3):343–7.
- [26] Ortiz-Conde A, Cerdeira A, Estrada M, García-Sánchez FJ, Quintero R. A simple procedure to extract the threshold voltage of amorphous thin film MOSFETs in the saturation region. *Solid-State Electron* 2001;45(5):663–7.
- [27] Ranuarez JC, García-Sánchez FJ, Ortiz-Conde A. Procedure for determining diode parameters at very low forward voltage. *Solid-State Electron* 1999;43(12):2129–33.
- [28] Hsu H-H, Liu T-W, Chan L, Lin C-D, Huang T-Y, Lin H-C. Fabrication and characterization of multiple-gated poly-Si nanowire thin-film transistors and impacts of multiple-gate structures on device fluctuations. *IEEE Trans Electron Dev* 2008;55(11):3063–9.
- [29] Wong HS, White MH, Kruttsick TJ, Booth RV. Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFETs. *Solid-State Electron* 1987;30(9):953–68.
- [30] García Sánchez FJ, Ortiz-Conde A, Mercado GD, Salcedo JA, Liou JJ, Yue Y. New simple procedure to determine the threshold voltage of MOSFETs. *Solid-State Electron* 2000;44(4):673–5.
- [31] He J, Xi X, Chan M, Cao K, Hu C, Li Y, et al. Normalized mutual integral difference method to extract threshold voltage of MOSFETs. *IEEE Electron Dev Lett* 2002;23(7):428–30.
- [32] He J, Zhang X, Wang Y, Xi X, Chan M, Hu C. Normalized mutual integral difference operator: a novel experimental method for extracting threshold voltage of MOSFETs. *Microelectron J* 2002;33(8):667–70.
- [33] García Sánchez FJ, Ortiz-Conde A, Liou JJ. A parasitic series resistance-independent method for device-model parameter extraction. *IEE Proc Circ Dev Syst* 1996;143(1):68–70.
- [34] Salazar R, Ortiz-Conde A, García Sánchez FJ, Ho C-S, Liou JJ. Evaluating MOSFET harmonic distortion by successive integration of the I – V characteristics. *Solid-State Electron* 2008;52(7):1092–8.