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Investigation on NMOS-based power-rail ESD clamp circuits with gate-driven mechanism in a 0.13-μm CMOS technology

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ABSTRACT

NMOS-based power-rail ESD clamp circuits with gate-driven mechanism have been widely used to obtain the desired ESD protection capability. All of them are usually based on a similar circuit scheme with multiple-stage inverters to drive the main ESD clamp NMOS transistor with large device dimension. In this work, the designs with 3-stage inverter and 1-stage inverter controlling circuits have been studied to verify the optimal circuit schemes in the NMOS-based power-rail ESD clamp circuits. Besides, the circuit performances among the main ESD clamp NMOS transistors drawn in different layout styles cooperated with the controlling circuit of 3-stage inverters or 1-stage inverter are compared. Among the NMOS-based power-rail ESD clamp circuits, an abnormal latch-on event has been observed under the EFT test and fast power-on condition. The root cause of this latch-on failure mechanism has been clearly explained by the emission microscope with InGaAs FPA detector.

1. Introduction

Electro static Discharge (ESD) protection has become a troublesome task on the reliability of CMOS integrated circuits fabricated in the advanced nanoscale CMOS technology. The power-rail ESD clamp circuit is an efficient design to achieve whole-chip ESD protection in IC products [1–3]. It not only can improve ESD robustness of VDD-to-VSS ESD stress, but also can significantly enhance ESD robustness of input/output-to-VDD/VSS and pin-to-pin ESD stresses [2]. Furthermore, to efficiently protect the core circuits realized with much thinner gate oxide in nanoscale CMOS technology, some studies had reported the efficient power-rail ESD clamp circuits with modified circuit designs [3–6]. All of them were based on the power-rail ESD clamp circuits with gate-driven mechanism which was basically implemented by the RC-based ESD-transient detection circuit with a controlling circuit [1–6], as illustrated in Fig. 1. Besides, those previous works also adopted the power-rail ESD clamp NMOS transistor with no snapback operations to obtain excellent turn-on efficiency. The snapback phenomenon usually occurs in NMOS transistors, npn bipolar transistors, or silicon controlled rectifiers (SCRs) under higher voltage and current stress conditions. No snapback means that the huge ESD current was discharged by the channel current of NMOS transistors. Therefore, those NMOS transistors in the power-rail ESD clamp circuits were traditionally drawn with huge channel width of several-thousand micrometer to achieve the required ESD robustness under no snapback operation. They were often called as Big FET (BFET) in some previous literatures [3–6].

The RC-based ESD-transient detection circuits were used to distinguish ESD-stress conditions from normal circuit operation conditions due to the difference in the rise time between these two conditions [1,2]. Then, 3-stage inverters, which were adopted as a function of tapered buffer [7–11], usually performed the controlling circuit to efficiently turn on or turn off the BFET, which has large capacitive load from the NMOS transistor with a huge channel width in power-rail ESD clamp circuit, as shown in Fig. 1. The tapered buffer, which is the multiple inverter stages with cascaded arrangement, is constantly applied to drive the large loading capacitance under a desirable propagation delay and power consumption [7–9]. However, such design concerns are not always appropriate to the function of the controlling circuits in the power-rail ESD clamp circuits because of two main reasons. First, the controlling circuits are only required to propagate a unity signal, such as logical high or logical low, in order to turn on the main ESD clamp devices under ESD-stress conditions, but they are not required to propagate a dynamic signal or alternating logic under normal circuit operation conditions. Second, the controlling circuits are always biased at the static off state under the normal circuit operation conditions in the power-rail ESD clamp circuits.

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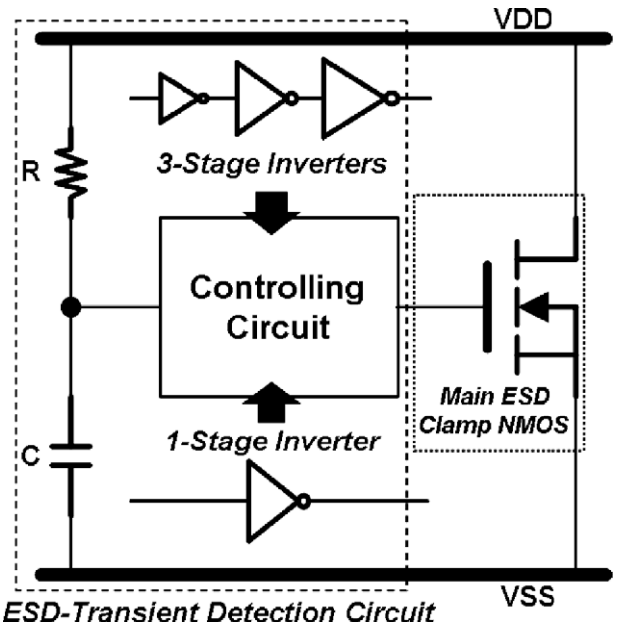

Fig. 1. Typical design scheme for NMOS-based power-rail ESD clamp circuit with RC-based ESD-transient detection circuit.

Some basic circuit performances, such as short-circuit dissipation and propagation delay, would not be improved by the controlling circuits with the tapered buffer arrangement. Therefore, the controlling circuits with tapered buffer concepts should be unnecessary and even be unsuitable for power-rail ESD clamp circuits.

The comparison between 1-stage and 3-stage inverters in the controlling circuits has been studied in this work. The circuit performances of both controlling circuits in power-rail ESD clamp circuits are measured and compared under ESD-stress conditions and normal circuit operation conditions. On the other hand, the drain-contact-to-poly-gate spacing (D) of the main ESD clamp NMOS transistor has been also split from 0.25 μm to 2.0 μm in order to investigate the influence of this spacing on the ESD protection capability. Through the arranged combinations of different controlling circuits and main ESD clamp NMOS transistors in different layout styles, the influence can be thoroughly investigated from the characteristic and performance of each power-rail ESD clamp circuit in silicon. Moreover, the impact of the fast power-on application [5,6] or the transient noise on power/ground lines [12,13] on the power-rail ESD clamp circuits has been also discussed in this work. According to these experimentally measured results, the optimized circuit scheme for controlling circuits and layout style for the main ESD clamp NMOS transistors can be suggested for using in the power-rail ESD clamp circuits.

2. Power-rail ESD clamp circuits with different controlling circuits and layout styles on main ESD clamp NMOS

It has been studied and reported that the RC-time constants of the RC-based ESD-transient detection circuits made an impact on the ESD robustness of the power-rail ESD clamp circuits. In a previous work [14], all main ESD clamp NMOS transistors were drawn as the BFETs with the drain-contact-to-poly-gate spacings from 0.22 μm to 0.44 μm and no silicide blocking on the diffusions. The total channel widths of those BFETs were identically 2000 μm; however, they occupied different silicon areas. According to the measured results in that previous work, the ESD robustness were not significantly improved or enhanced by increasing the RC-time constant from 0.1 μs to 1.0 μs. More specifically, the longest RC-time constant of 1.0 μs could slightly induce some degradation on ESD robustness of the power-rail ESD clamp circuit. Based on these related measured results in previous research [14], the RC-time constant has been fixed at 0.2 μs in this work to reduce the occupied silicon area of the resistance and capacitance in this testchip.

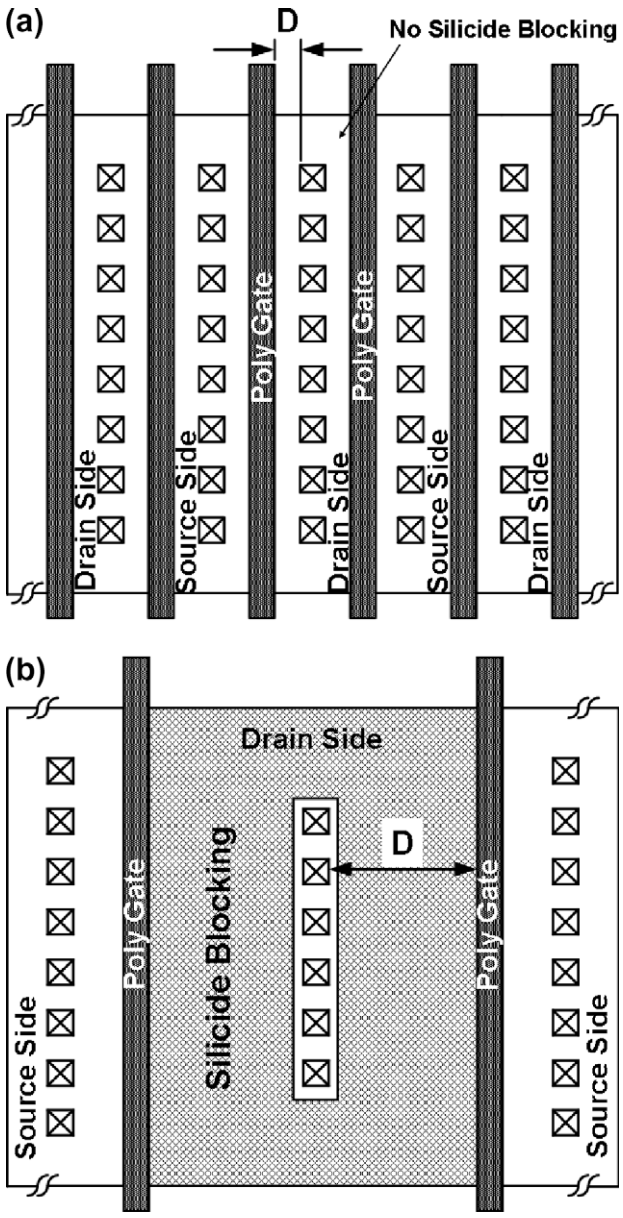

Fig. 2. The main ESD clamp NMOS transistor has (a) the BFET layout style with the drain-contact-to-poly-gate spacing (D) of 0.25 μm and no silicide blocking (SB) on its diffusions, and (b) the standard layout style with the drain-contact-to-poly-gate spacing (D) of 2.0 μm and silicide blocking (SB) on its drain-side diffusions.

Both controlling circuits, which are the 1-stage inverter and the 3-stage inverters, are respectively arranged to command the main ESD clamp NMOS transistors with different drain-contact-to-poly-gate spacings. One of the main ESD clamp NMOS transistors has the layout style with minimized drain-contact-to-poly-gate spacing (D) and no silicide blocking (SB) on its diffusion, as shown in Fig. 2a. This NMOS transistor, which is the Big FET (BFET), will be expected to have no snapback operation. However, another one has a totally different layout style with extended drain-contact-to-poly-gate spacing (D) and silicide blocking (SB) on its diffusion,

Table 1
Eight designs of the power-rail ESD clamp circuits verified in this work.

Design	Controlling circuit	Main ESD clamp NMOS	
		Drain-contact-to-poly-gate spacing (D) and total channel width (W)	Silicide blocking (SB)
Standard1	1-Stage inverter	D = 2.0 μm and W = 624 μm	Yes
Standard2	3-Stage inverters	D = 2.0 μm and W = 624 μm	Yes
Modified1	1-Stage inverter	D = 0.75 μm and W = 1144 μm	No
Modified2	1-Stage inverter	D = 0.75 μm and W = 1144 μm	Yes
Modified3	3-Stage inverters	D = 0.75 μm and W = 1144 μm	No
Modified4	3-Stage inverters	D = 0.75 μm and W = 1144 μm	Yes
BFET1	1-Stage inverter	D = 0.25 μm and W = 2600 μm	No
BFET2	3-Stage inverters	D = 0.25 μm and W = 2600 μm	No

as shown in Fig. 2b. It is a standard ESD clamp NMOS transistor with snapback operation. It has been proven that the parasitic npn bipolar transistor was turned on induce the snapback operation in such ESD clamp NMOS transistor [15,16]. The drain-contact-to-poly-gate spacings of the BFET and standard ESD clamp NMOS transistors are 0.25 μm and 2.0 μm, respectively. Besides, another different layout style, called as modified design in this work, has been also implemented in this testchip. The modified designs have the main ESD clamp NMOS transistor with a drain-contact-to-poly-gate spacing of 0.75 μm. Moreover, there are two different main ESD clamp NMOS transistors with or without silicide blocking on their drain-side diffusion in modified designs. Through such splits in layout, the influences of the drain-side equivalent resistance on circuit performance and ESD robustness can be used to judge the optimal layout style for the main ESD clamp NMOS transistor.

Totally, eight designs of power-rail ESD clamp circuits from the combinations of the main ESD clamp NMOS transistor in different layout styles and the controlling circuit with different inverter stages have been drawn in the testchip for comparison, as shown in Table 1 For comparison purpose, the layout areas of the main ESD clamp NMOS transistors among those eight designs are kept the same in layout. Therefore, the total channel width of the standard main ESD clamp NMOS transistor is 624 μm, whereas that of the BFET is about 2600 μm. For all modified designs, the main ESD clamp NMOS transistors have a total channel width of 1144 μm. Then, the two type controlling circuits implemented by 3-stage inverters and 1-stage inverter also occupied similar layout areas. The device sizes (W/L) of PMOS and NMOS transistors are 444/0.18 μm and 62/0.18 μm in the design with 1-stage inverter, respectively. They are 14/0.18 μm (70/0.18 μm and 360/0.18 μm) and 2/0.18 μm (10/0.18 μm and 50/0.18 μm) in 1st-stage inverter (2nd-stage and 3rd-stage inverters) of the design with 3-stage inverters, respectively. This testchip has been fabricated in a 0.13-μm 1.2-V CMOS process.

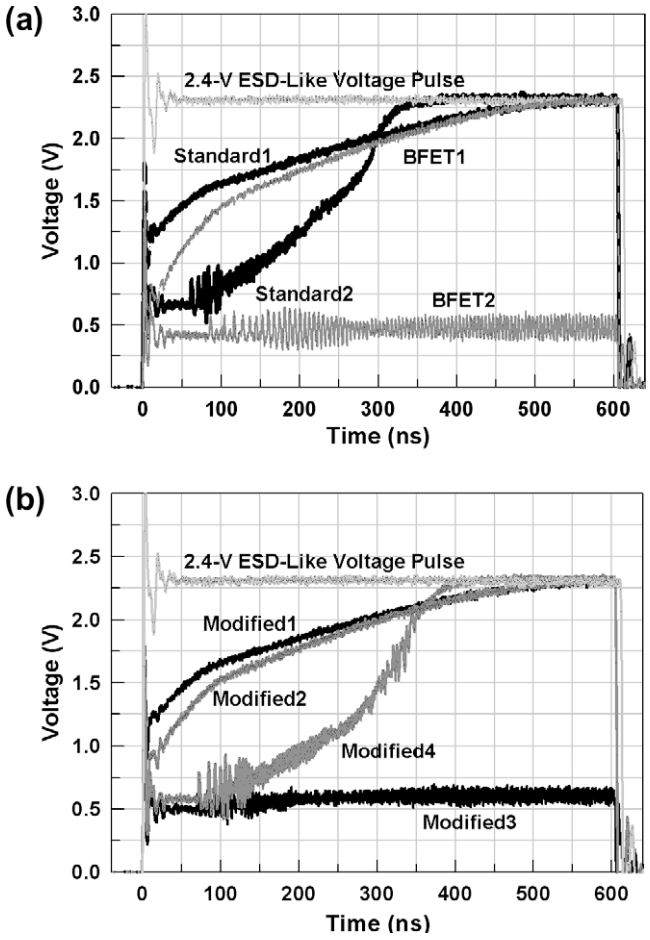

Fig. 3. The measured voltage waveforms of (a) Standard1, Standard2, BFET1, and BFET2, and of (b) Modified1, Modified2, Modified3, and Modified4, under 2.4-V ESD-like voltage pulses with 2-ns rise time.

3. Experimental results in component-level tests

3.1. Turn-on verification under ESD-like stress condition

To observe the turn-on efficiency among the different power-rail ESD clamp circuits, a 2.4-V ESD-like voltage pulse with 2-nano-seconds (ns) rise time is applied on the VDD terminal with VSS terminal grounded in each circuit. The voltage pulse with a rise time of 2 ns and duration of 600 ns generated from a pulse generator is used to simulate the fast rising edge of HBM ESD event [17]. The sharp-rising edge of the ESD-like voltage pulse will be detected by the RC-based ESD-transient detection circuit and then to turn on the main ESD clamp NMOS transistor. When the main ESD clamp NMOS is turned on, the voltage waveform on VDD node will be clamped as the measured results shown in Fig. 3a and b. Standard1 and BFET1, both of which have 1-stage inverter in the controlling circuits, presented similar voltage waveforms under 2.4-V ESD-like voltage pulses. Besides, Standard2 clamped the overshoot voltage pulses to a lower voltage level during the first 300 ns of the ESD-like voltage pulses. However, the BFET2 performs an excellent ability to clamp the overshoot voltage pulse to a much lower voltage level, as shown in Fig. 3a. On the other hand, the influences of drain-side silicide blacking on turn-on behaviors of the power-rail ESD clamp circuits have been measured in Fig. 3b. Under the same drain-contact-to-poly-gate spacings of 0.75 μm, Modified3 exhibits the best turn-on efficiency among other designs. Besides, the turn-on efficiency of Modified4 is higher than that of Modified1 and Modified2 during the first 350-ns pulse duration. According to the measured results, the controlling circuit with 3-stage inverters seems to be an optimal

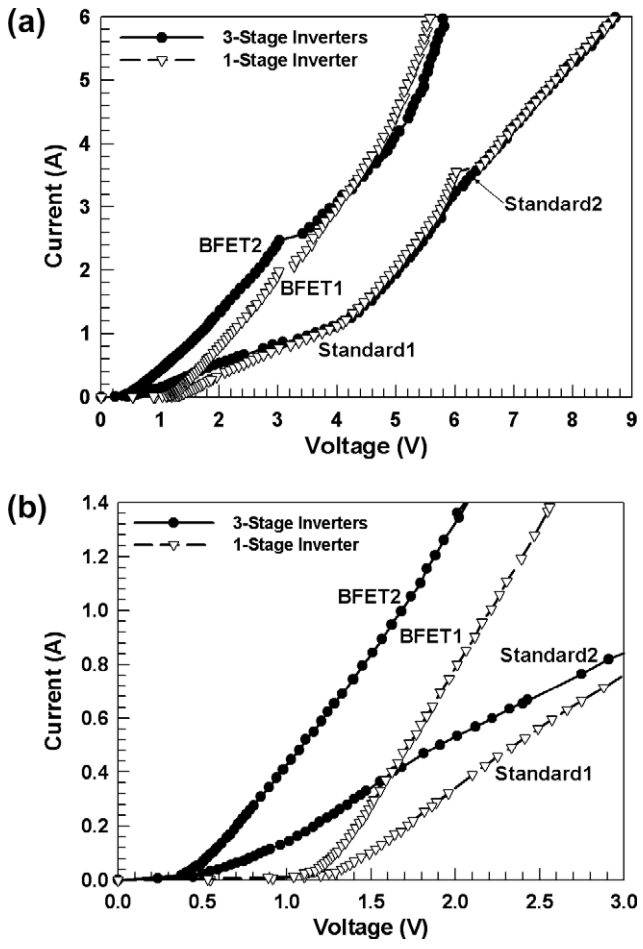

Fig. 4. (a) The TLP *I–V* curves of Standard1, Standard2, BFET1, and BFET2. (b) The zoomed-in view of (a) around the low-current region.

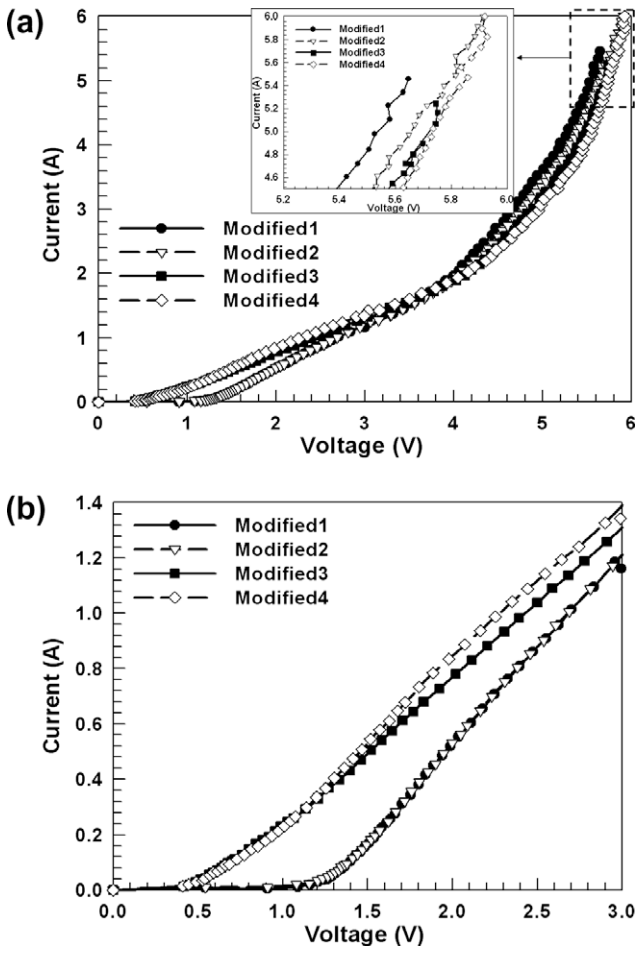

Fig. 5. (a) The TLP *I–V* curves of Modified1, Modified2, Modified3, and Modified4. (b) The zoomed-in view of (a) around the low-current region.

candidate to implement the main ESD clamp NMOS transistor with BFET layout style in the power-rail ESD clamp circuit. The controlling circuit would hold a dominant factor on the turn-on behaviors of the power-rail ESD clamp circuit.

3.2. TLP I–V characteristics and HBM ESD robustness

The Transmission Line Pulse (TLP) [18] measured *I–V* characteristics of the power-rail ESD clamp circuits are shown in Figs. 4a, b and 5a, b. This TLP system has a 100-ns pulse width and 10-ns rise time. In Fig. 4a, the TLP *I–V* curves can be simply discriminated between the main ESD clamp NMOS transistors with standard or BFET layout styles. Although the second breakdown currents (It2) of these four designs can achieve over 6 A, the difference of on resistance (Ron) clearly distinguished the designs with standard main ESD clamp NMOS transistor from those with BFET. Due to smaller total channel widths in Standard1 and Standard2, their clamp voltage (Vclamp) and Ron are signification higher than those of BFET1 and BFET2. Higher Vclamp and Ron in Standard1 and Standard2 easily induced some damages to the internal circuits. In addition, the TLP *I–V* curves of Standard1 and Standard2 presented obvious two-stage Ron in Fig. 4a. The phenomenon of two-stage Ron can be attributed to the changes of the discharging paths. The currents were conducted through the channel of the main ESD clamp NMOS transistor under the low-current region, and they would be discharged by the parasitic npn bipolar transistor of the main ESD clamp NMOS transistor [19].

Moreover, the controlling circuits with 3-stage inverters can enhance the turn-on efficiency, such as lower trigger voltage (Vt1) and smaller on resistance, especially under the low-current region in both standard and BFET designs, as shown in Fig. 4b. It was ever reported that the higher Vt1 and insufficient turn-on duration in the ESD devices will induce some damages to interface circuits [20]. The enhancement of the turn-on efficiency is more emphasized on the design with the controlling circuit of 3-stage inverter cooperated with BFET. However, the influence of the different controlling circuits with 3-stage inverters and 1-stage inverter on the turn-on efficiency is gradually indistinct under the high current region. When the measured current is over ~2.5 A, no obvious difference of Vclamp between BFET1 and BFET2, both of which have the total channel widths of 2600 μm, is observed in Fig. 4a. The phenomenon can be also attributed to the changes of the discharging paths. Under such high current region, the huge current can not be totally discharged by the channel of the main ESD clamp NMOS transistor. The parasitic npn bipolar transistor would be triggered on discharge huge current. Therefore, the gate-driven enhancement by the 3-stage inverters will disappear under the high current region. The similar measured results also can be observed in Modified1, Modified2, Modified3, and Modified4. Fig. 5a and b present the TLP *I–V* curves of these modified designs. These four TLP *I–V* curves have the similar trends, especially in the high current range. The trigger voltages of Modified3 and Modified4 are lower than those of Modified1 and Modified2. The second breakdown currents (It2) of the modified designs with silicide blocking (Modified2 and Modified4) are higher than those without silicide

blocking (Modified1 and Modified3), as shown in the insert of Fig. 5a. The influence of the drain-side silicide blocking on the Ron and Vclamp is not obvious, as illustrated in Fig. 5a and b. According to the TLP measured results, the design scheme of controlling circuit would affect the trigger voltage of the power-rail ESD clamp circuit. However, the on resistance and Vclamp would be dominated by the drain-side layout style in the main ESD clamp NMOS transistor.

The second breakdown currents and HBM ESD robustness of the eight different power-rail ESD clamp circuits are listed in Table 2. The power-rail ESD clamp circuit with design of BFET2 sustains the highest HBM ESD stress of 7 kV. However, the ESD robustness of Standard2 is below 6 kV. The four modified designs have the similar ESD robustness from 5.5 kV to 6.0 kV. The ESD robustness of these four designs do not have significant enhancement by depositing silicide blocking oxide layer on their drain-side diffusions of the main ESD clamp NMOS transistors or by adopting 3-stage inverters in the controlling circuit. A faint relation between the ESD robustness and the controlling circuits (or the layout style of the main ESD clamp NMOS transistor) is summarized in Table 2. The 3-stage inverters in controlling circuit could be suitable for the main ESD clamp NMOS transistor without silicide blocking on its diffusion. Such NMOS transistor has a lower parasitic resistance on its surface channel. But, the controlling circuit with 3-stage inverters would induce some degradation on ESD robustness of the designs with drain-side silicide blocking in the main ESD clamp NMOS transistor. Therefore, based on the measured results of the TLP *I–V* characteristics and HBM ESD robustness, the 3-stage inverters in controlling circuit did not have obvious improvement for the power-rail ESD clamp circuits in nanoscale CMOS technology.

3.3. Power-on condition and normal circuit operation condition

In general, the normal VDD power-on voltage waveform of CMOS ICs has a rise time in the order of milli-second (ms). Due to such a slow rise time in normal power-on conditions, the ESD-transient detection circuit with a RC-time constant of ~μs can distinguish the power-on signal to keep the main ESD clamp NMOS transistor off. All of the power-rail ESD clamp circuits studied in this work can successfully achieve this desired task under normal power-on conditions. However, the power-rail ESD clamp circuits with RC-based ESD-transient detection circuits were easily mis-triggered to cause themselves into a "latch-on" state, which the potential on VDD node will be continuously clamped at a lower voltage, under some abnormal fast power-on conditions [5,6] or transient noise on VDD power lines [12,13]. In this work, the eight different power-rail ESD clamp circuits were verified by a 1.2-V voltage pulse with 100-ns rise time, which is used to simulate the abnormal fast power-on condition, to investigate their immunities from the mis-trigger and latch-on state. The measured results are respectively shown in Figs. 6 and 7.

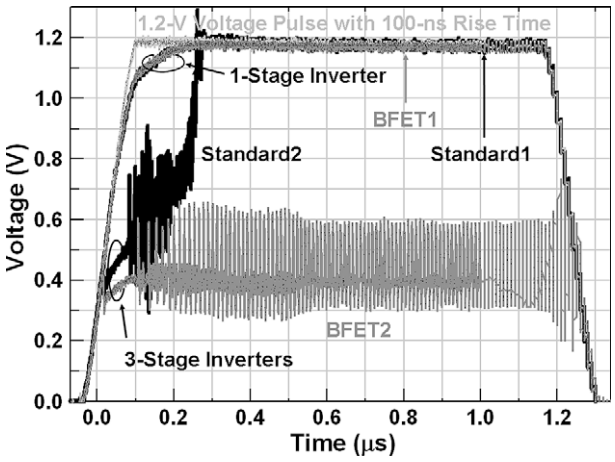

Fig. 6. The measured voltage waveforms of Standard1, Standard2, BFET1, and BFET2 under the 1.2-V fast power-on condition with 100-ns rise time.

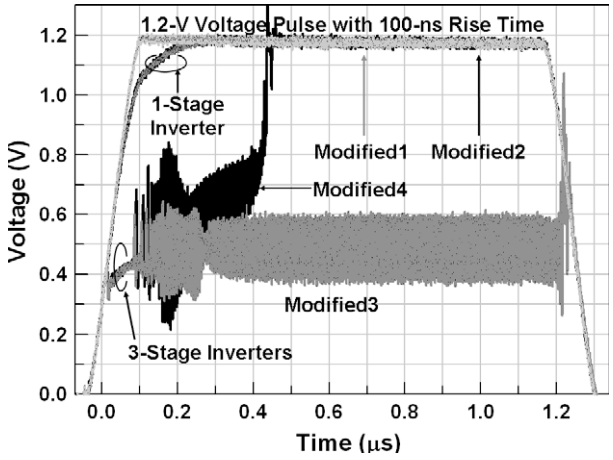

Fig. 7. The measured voltage waveforms of Modified1, Modified2, Modified3, and Modified4 under the 1.2-V fast power-on condition with 100-ns rise time.

Unfortunately, the power-rail ESD clamp circuits with 3-stage inverters in controlling circuit present the worse immunity against mis-trigger under the 1.2-V fast power-on test conditions. BFET2 will be mis-triggered on enter latch-on state under the 1.2-V fast power-on test condition. The voltage waveform is clamped at a very low voltage level around 0.3–0.6 V, as illustrated in Fig. 6. Such phenomenon is much harmful for the applications of the power-rail ESD clamp circuits in real IC products. Besides, Modified3 also presents a similar measured result to that of BFET2. Standard2 and Modified4, both of which have the silicide blocking on their drain sides, will be mis-triggered at the first 250 ns and first

Table 2
HBM ESD robustness of the eight power-rail ESD clamp circuits.

Designs	HBM		Second breakdown current (It2) (A)
	Positive (kV)	Negative (kV)	
Standard1	6.5	>8.0	>6
Standard2	5.5	>8.0	>6
Modified1	5.5	>8.0	5.4
Modified2	6.0	>8.0	>6
Modified3	6.0	>8.0	5.2
Modified4	5.5	>8.0	>6
BFET1	6.5	>8.0	>6
BFET2	7.0	>8.0	>6

420 ns, respectively, under the 1.2-V fast power-on test condition with 100-ns rise time. However, all of designs with 1-stage inverter in the controlling circuit, such as Standard1, BFET1, Modified1, and Modified2, exhibit the higher mis-trigger immunity under this 1.2-V fast power-on test condition. Their voltage waveforms can follow up with the fast power-on voltage waveforms, as presented in Figs. 6 and 7. Although the 3-stage inverters for controlling circuit would enhance the gate-driven ability to slightly increase the ESD robustness and decrease Vclamp (and Ron), they will dramatically degrade the immunity against mis-trigger and latch-on issues under the fast power-on condition. Based on the aforementioned results, the controlling circuits with 1-stage inverter should be the optimal choice among the power-rail ESD clamp circuits with RC-based ESD-transient detection circuit.

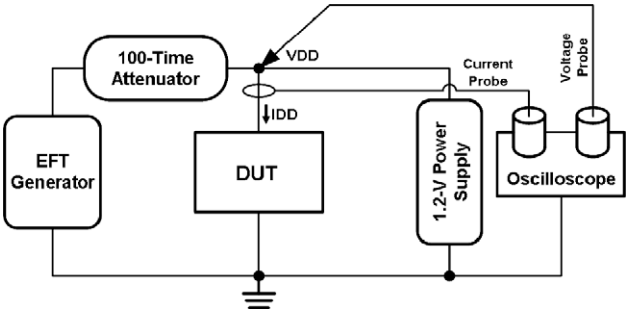

Fig. 9. Measurement setup for electrical fast transient (EFT) test on the DUT with the VDD bias of 1.2 V.

4. Experimental results in system-level test

The reliability of microelectronic products has been put more emphasis on the electromagnetic compatibility (EMC). In order to avoid the occurrence of the malfunction and mis-trigger during normal system operation conditions, the on-chip ESD protection circuits also has been required to meet the EMC regulation. For power-rail ESD clamp circuits, the impact of the transient noise coupled from microelectronic system on the power (or ground) line has attracted more attentions. The transient noise could induce some power-rail ESD clamp circuits into serious latch-on failure according to the previous studies [12,13]. In this work, the electrical fast transient (EFT) test [21] has been applied on the eight different power-rail ESD clamp circuits to judge their immunities against fast transient noise on their power lines. The EFT voltage waveforms consist of many bursts with 15-ms duration and these bursts are repeated every 300 ms, as shown in Fig. 8a. Besides, each voltage pulse in the burst has a rise time of 5 ns and a pulse width of 50 ns, as illustrated in Fig. 8b. Moreover, because the minimum EFT voltage waveforms of 200 V provided by EFT generator would easily destroy the on-chip devices in nanoscale CMOS technology, the EFT voltage waveforms were decayed by a 100-time attenuator before they were directly applied to the VDD terminals of the power-rail ESD clamp circuits. The measurement setup for the EFT test was demonstrated in Fig. 9. Besides monitoring the influence of voltage waveforms on the VDD terminals, the abnormal variations in currents from VDD to VSS also have been observed through the current probe.

Fig. 10a shows the measured results of BFET1 and BFET2 under the 4-V EFT test on the VDD terminals. The overshooting voltages on the VDD nodes can be effectively clamped by these two power-rail ESD clamp circuits. BFET1 exhibits a smooth waveform, only decaying the voltage amplitude on the VDD terminal, whereas BFET2 presents a rough waveform during the period of the EFT execution. Besides, the measured results of Standard1 and Standard2 have been illustrated in Fig. 10b. The overshooting voltage on the VDD nodes also can be clamped by the designs with the standard ESD clamp NMOS transistor (D = 2.0 μm with SB). Standard1 and Standard2 show similar waveforms and the clamp voltage of Standard2 is slightly lower than that of Standard1. In addition, the cur-

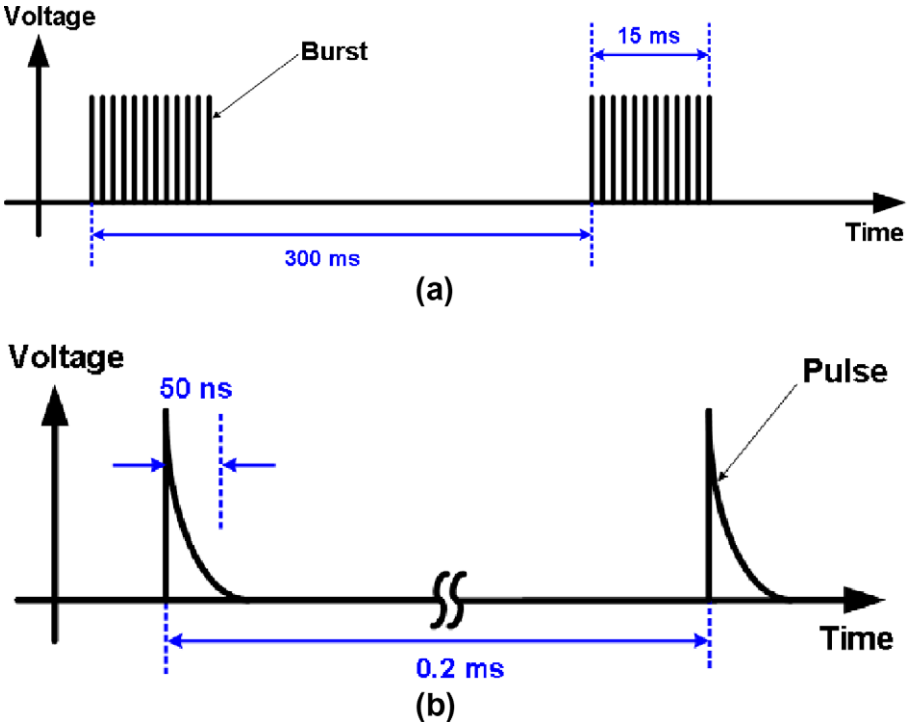

Fig. 8. Specified electrical fast transient (EFT) waveforms of (a) burst, and (b) single pulse, with a repetition frequency of 5 kHz.

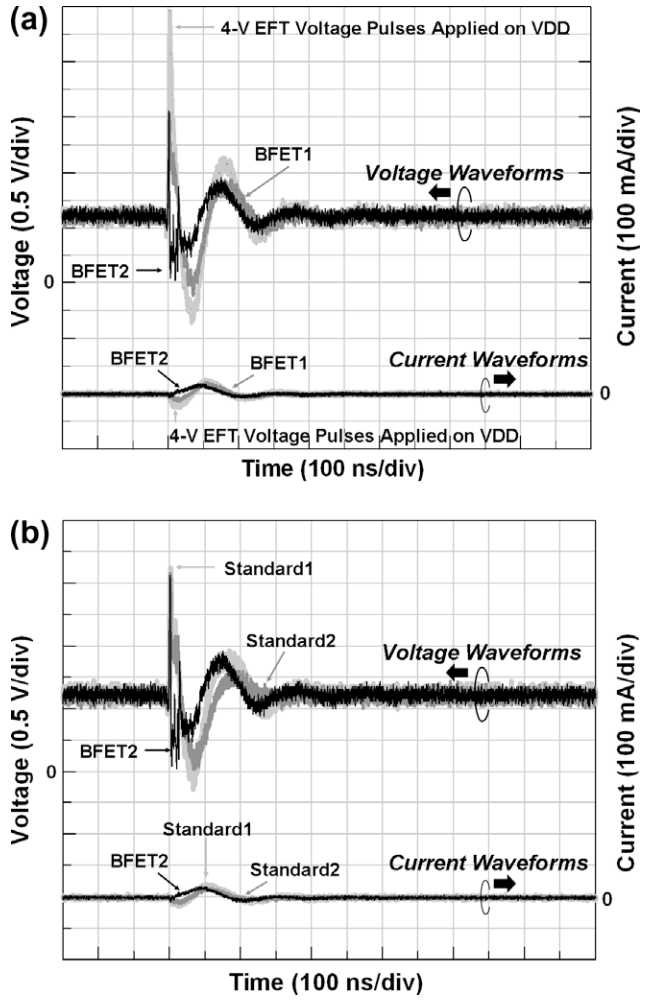

Fig. 10. Under the 4-V EFT voltage pulse, the measured voltage waveforms of (a) BFET1 and BFET2, and (b) Standard1 and Standard2.

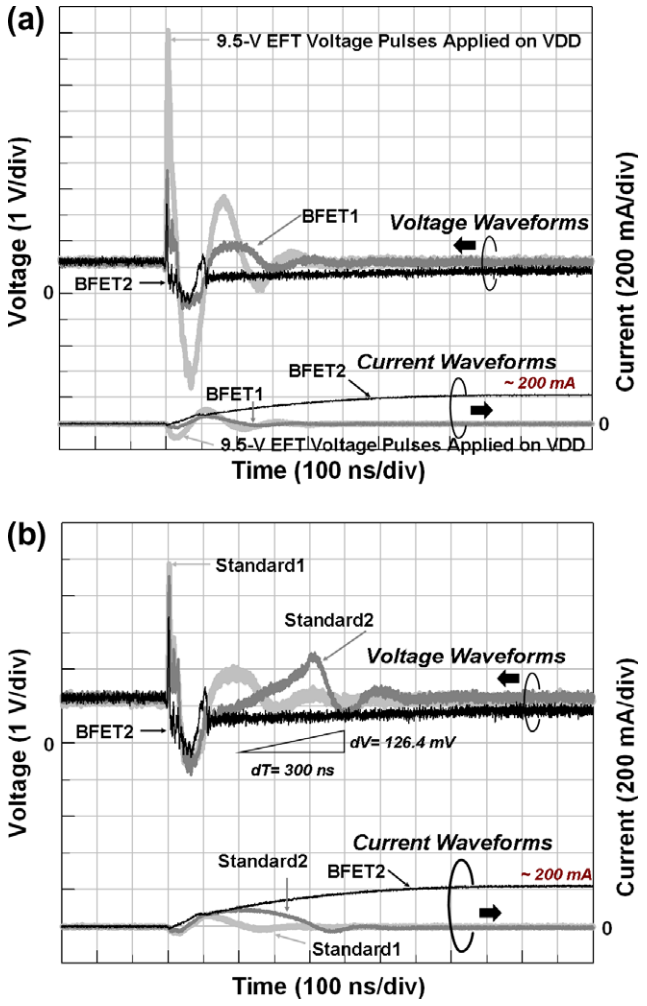

Fig. 11. Under the 9.5-V EFT voltage pulse, the measured voltage waveforms of (a) BFET1 and BFET2, and (b) Standard1 and Standard2.

rent waveforms of these four designs only vibrated during the period of the EFT execution. No abnormal current from VDD to VSS was observed after the 4-V EFT stresses. With the 9.5-V EFT voltage stress on the VDD terminals, the measured results are presented in Fig. 11a and b. All of the designs still can efficiently clamp the overshooting voltage pulses on the VDD nodes during the EFT stresses. However, after the duration of the EFT voltage pulse, the voltage potential on VDD terminal is not successfully recovered to the normal operation voltage of 1.2 V in BFET2, as clearly shown in Fig. 11b. Moreover, the current waveform of the BFET2 will drastically rise and finally hold at around 200 mA. Such phenomenon could be attributed to the main ESD clamp NMOS transistor is still kept at on state after 9.5-V EFT stress, which is the occurrence of latch-on event. The further explanation of this latch-on mechanism will be analyzed and discussed in the next paragraphs. In contrast, the voltage waveforms of other designs can be quickly recovered to 1.2 V after the duration of the EFT voltage pulse and no abnormal current from VDD to VSS was observed after 9.5-V EFT stress. According to the measured results in Fig. 11b, the recovery period of Standard2 is larger than that of Standard1. Standard2 would induce an irregular overshooting voltage pulse at the end of the duration of the EFT voltage pulse. Its current waveform also manifests the irregular transient under this duration. In a nutshell, the RC-based ESD-transient detection circuit with the controlling circuit of 3-stage inverters and the main ESD clamp NMOS transistor with BFET (D = 0.25 μm without SB) layout style are unreliable to be used as the power-rail ESD clamp circuit due to the mis-trigger and latch-on concern.

5. Failure analysis and latch-on mechanism

5.1. Failure analysis

According to the measured results of the EFT test and fast power-on condition, BFET2 would induce the latch-on phenomenon if the fast transient noises applied on the VDD terminal. The potential on the VDD node will be clamped into a lower voltage level or the huge conducting current from VDD to VSS will be observed, as shown in Figs. 6 and 11a,b. However, such power-rail ESD clamp circuit with RC-based ESD-transient detection circuit should maintain in a high impedance state from VDD to VSS after the turn-on duration of main ESD clamp NMOS transistor. Standard2 clearly presents this characteristic, as shown in Fig. 6. But, the voltage waveforms of BFET2 are always clamped to a lower voltage potential under the fast power-on condition. There is an abnormal mechanism to contribute a positive feedback path that in turn triggers the occurrence of the latch-on event. In order to observe the root cause of this latch-on mechanism, the failure analysis has been executed by the emission microscope with InGaAs focal plane arrays (FPA) detector [22], which has an excellent capability to capture the photon emission of wavelength range from

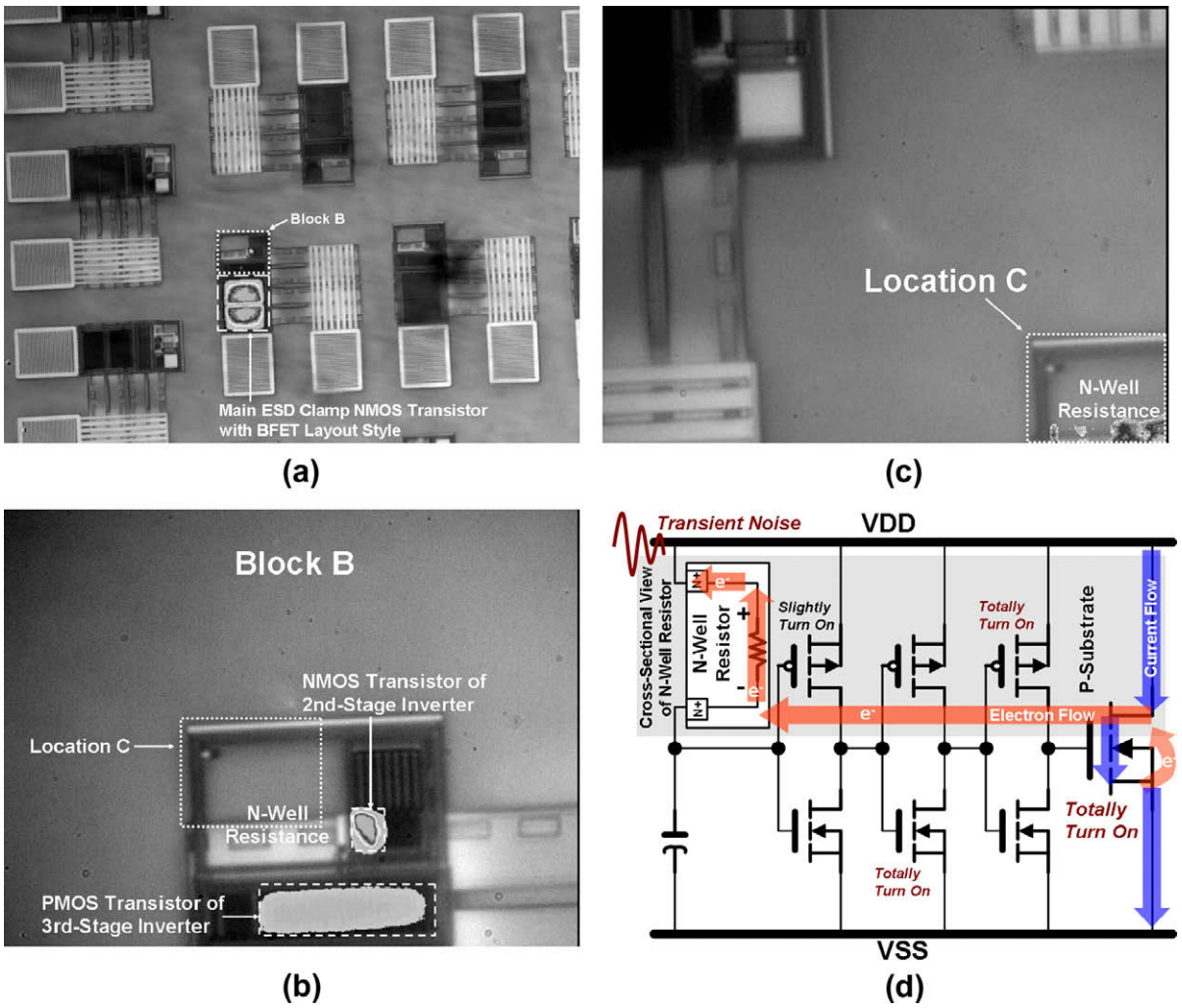

Fig. 12. Through the emission microscope with InGaAs FPA detector. (a) The abnormal emission spots after the EFT test are located at the NMOS transistor of the 2-stage inverter, the PMOS transistor of the 3-stage inverter, and main ESD clamp NMOS transistor. (b) The zoomed-in view around the controlling circuit and the RC-based ESD-transient detection circuit. (c) The emission image is only located at the n-well resistance of the RC-based ESD-transient detection circuit. (d) The failure mechanism of this latch-on event.

800 nm to 1700 nm. This failure analysis equipment is suitable for the abnormal location with very slight photon emissions [22–24] because of the higher quantum efficiency.

Fig. 12a–c illustrated the results of the failure analysis after the EFT test. According to the images in Fig. 12a and b, the main ESD clamp NMOS transistor with BFET layout style is turned on into the latch-on status after the 9.5-V EFT voltage stress because the PMOS transistor in the 3rd-stage inverter and the NMOS transistor in the 2nd-stage inverter are also in the on state. The PMOS transistor in the 3rd-stage inverter and the NMOS transistor in the 2nd-stage inverter kept in the on state could be attributed to voltage drop across the n-well resistance of the RC-based ESD-transient detection circuit. The failure mechanism of this latch-on event was illustrated in Fig. 12d. In general, the n-well resistance is usually regarded as a common choice in such RC-based ESD-transient detection circuit to obtain an adequate resistance and a sufficient RC-time delay. However, based on the previous studies [25,26], a few electrons would be captured by this n-well resistance since this n-well resistance could be performed as the guard ring of the minority to capture the minority carriers (electrons) in the p-substrate, as shown in Fig. 12d. The slight hot spots on the n-well resistance have been observed in Fig. 12c. In the layout, although the n-well resistance has been surrounded by the N+/n-well minority guard rings connected to VDD, some escaped electrons still were captured by the n-well resistance. It induces some voltage drop across the n-well resistance because the electrons were captured and conducted by this n-well resistance. Due to the slight voltage drop across the n-well resistance, the PMOS transistor in 1st-stage inverter can be slightly turned on. Then, through the amplification of the 1st-stage inverter, the NMOS transistor in the 2nd-stage inverter and the PMOS transistor in the 3rd-stage inverter are thoroughly in the on state, as shown in Fig. 12b with bright hot spots.

5.2. Discussion on the latch-on mechanism

According to the measured results in the power-on and FET tests, this latch-on event of BFET2 relied on a mis-trigger status of the main ESD clamp NMOS transistor which was induced by a sufficient transient noise (or power-on signal). For example, the latch-on event was not observed under the power-on condition with ms-order rise time and under the 4-V EFT stress. Under the sufficient transient noise (or power-on signal), such as 9.5-V EFT test (or 100-ns power-on signal), the main ESD clamp NMOS transistor was initially into on state and conducted huge current from VDD to VSS. Then, a few escaped electrons were captured by the

n-well resistance to induce the voltage drop across the n-well resistance. Through the amplification gain of the 3-stage inverters, the main ESD clamp NMOS transistor was kept at the further on state. Such on state main ESD clamp NMOS transistor would also conduct huge current and unavoidably induce the voltage drop across the n-well resistance. Finally, the main ESD clamp NMOS transistor in BFET2 was continuously held at the latch-on state. Therefore, the latch-on mechanism consists of three essential steps which are initial mis-trigger of main ESD clamp NMOS transistor, inducement of voltage drop across the n-well resistance, and amplification gain of 3-stage inverters.

The latch-on phenomenon was not observed in the designs with 1-stage inverter, such as BFET1 and Standard1, since they have the higher immunities against mis-trigger to avoid the main ESD clamp NMOS transistor entering into on state. More importantly, they lack the amplification gain of multi-stage inverters. Even though their main ESD clamp NMOS transistors were mis-triggered and into a short-period on state under large transient stresses, they still could not be held at latch-on state. On the other hand, because Standard2 with the standard ESD clamp NMOS transistor ($D = 2.0\,\mu m$ with SB) has a smaller channel width to generate less channel conduction current and substrate injection current, the deficient electrons can not induce adequate voltage drop across the n-well resistance. Although it suffered from the mis-trigger and possessed the amplification gain of 3-stage inverter, the insufficient voltage drop could not hold itself into the latch-on state. For the power-rail ESD clamp circuits in modified designs, the latch-on event can be only observed in Modified3 since it can exactly satisfy the three essential steps of the latch-on mechanism. However, the latch-on event was not observed in Modified1, Modified2, and Modified4. According to the further measured results, besides BFET2 and Modified3, the latch-on phenomenon was not observed in the other designs under the 44-V EFT stresses (44 V is the maximum value in the EFT measurement setup shown in Fig. 9).

In addition, the latch-on event in BFET2 or Modified3 would vanish by some modifications of layout style and n-well resistance. Consequently in layout, the width of N+/n-well minority guard rings connected to VDD and the distance between the n-well resistance and the main ESD clamp NMOS transistor should be further enlarged to prevent the threat of latch-on event under the EFT test and fast power-on condition. However, such adjustments would extend some layout areas of the power-rail ESD clamp circuit in the standard I/O cell library. Another approach is to replace the n-well resistance by poly resistance. Since the poly resistance is thoroughly separated from the silicon substrate, the poly resistance would not capture the escaped electrons to induce the voltage drop across itself. This approach would successfully conquer the latch-on failure in the BFET2 and Modified3. However, based on the related studies on the power-rail ESD clamp circuits, the 3-stage inverters in controlling circuit would be susceptible to the transient signal on VDD node. Although such design could enhance the turn-on efficiency of main ESD clamp NMOS transistor under ESD stresses, it would also suffer from the mis-trigger under the transient noise (or power-on signal). More specifically, the immunity level against mis-trigger in the design with 1-stage inverter is far higher than that in the design with multi-stage inverters. Most importantly, the power-rail ESD clamp circuit with 1-stage inverter also possesses acceptable turn-on efficiency, clamp ability, and ESD robustness.

6. Conclusion

The designs with controlling circuits of 3-stage inverters and 1-stage inverter have been studied to verify the optimal circuit schemes in NMOS-based power-rail ESD clamp circuits. In addition, the circuit performance among the four different main ESD clamp NMOS transistors drawn with different drain-contact-to-poly-gate spacings and co-designed with different inverter stages in the controlling circuits are compared. According to the experiments and analyses, the 3-stage inverters for controlling circuit and BFET layout style for the main ESD clamp NMOS transistor can slightly increase the ESD robustness, but they will dramatically degrade the immunity against mis-trigger and latch-on issues under the EFT test and fast power-on condition. The 1-stage inverter should be an appropriate and reliable candidate for the controlling circuit in the power-rail ESD clamp circuits. Finally, the latch-on phenomenon has been successfully observed by the emission microscope with InGaAs FPA detector. The root cause to induce such failure can be attributed to the abnormal mechanism of the voltage drop across the n-well resistance after the EFT test.

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References

[1] Merrill R, Issaq E. ESD design methodology. In: Proceedings of EOS/ESD symposium; 1993. p. 233–7.
[2] Ker M-D. Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp circuits for submicron CMOS VLSI. IEEE Trans Electron Dev 1999;46:173–83.
[3] Worley E, Gupta R, Jones B, Kjar R, Nguyen C, Tennyson M. Sub-micron chip ESD protection schemes which avoid avalanching junction. In: Proceedings of EOS/ESD symposium; 1995. p. 13–20.
[4] Stockinger M, Miller J, Khazhinsky M, Torres C, Weldon J, Preble B, et al. Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies. In: Proceedings of EOS/ESD symposium; 2003. p. 17–26.
[5] Li J-J, Gauthier R, Rosenbaum E. A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection. In: Proceedings of EOS/ESD symposium; 2004. p. 273–9.
[6] Li J-J, Gauthier R, Mitra S, Putnam C, Chatty K, Halbach R, et al. Design and characterization of a multi-RC-triggered MOSFET-based power clamp for on-chip ESD protection. In: Proceedings of EOS/ESD symposium; 2006. p. 179–85.
[7] Lin H-C, Linholm L. An optimized output stage for MOS integrated circuits. IEEE J Solid-State Circ 1975;10:106–9.
[8] Nemes M. Driving large capacitances in MOS LSI systems. IEEE J Solid-State Circ 1984;19:159–61.
[9] Veendrick H. Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits. IEEE J Solid-State Circ 1984;19:468–73.
[10] Li N-C, Haviland G, Tuszynski A. CMOS tapered buffer. IEEE J Solid-State Circ 1990;25:1005–8.
[11] Prunty C, Gal L. Optimal tapered buffer. IEEE J Solid-State Circ 1992;27:118–9.
[12] Yen C-C, Ker M-D. Failure of on-chip power-rail ESD clamp circuits during system-level ESD test. In: Proceedings of IEEE international reliability physics; 2007. p. 598–9.
[13] Ker M-D, Yen C-C. Unexpected failure in power-rail ESD clamp circuits of CMOS integrated circuits in microelectronics systems during electrical fast transient (EFT) test and the re-design solution. In: Proceedings of IEEE international Zurich symposium on electromagnetic compatibility; 2007. p. 69–72.
[14] Yeh C-T, Liang Y-C, Ker M-D. The impact of BIGFET clamp device layout on ESD protection circuit robustness. In: Proceedings of international ESD workshop; 2008. p. 414–25.
[15] Voldman S. ESD physics and devices. England: John Wiley & Sons; 2004.
[16] Amerasekera A, Duvvury C. ESD in silicon integrated circuits. England: John Wiley & Sons; 2002.
[17] Electrostatic discharge sensitivity testing – human body model (HBM) – component level. ESD Association Standard. Test Method ESD STM5.1-2001; 2001.
[18] Maloney T, Khurana N. Transmission line pulsing techniques for circuit modeling of ESD phenomena. In: Proceedings of EOS/ESD symposium; 1985. p. 49–54.
[19] Smith J, Boselli G. A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies. In: Proceedings of EOS/ESD symposium; 2003. p. 8–16.
[20] Vashchenko V, Scholz M, Jansen P, Petersen R, Natarajan M, Tremouilles D, et al. Turn-off characteristics of the CMOS snapback ESD protection devices – new insights and its implications. In: Proceedings of EOS/ESD symposium; 2006. p. 39–45.

[21] Testing and measurement techniques – electrostatic fast transient/burst immunity test. IEC 61000-4-4 International Standard. EMC-Part 4-4; 2004.
[22] Phang C-H, Chan S-H, Tan S-L, Len W-B, Yim K-H, Koh L-S, et al. A review of near infrared photon emission microscope and spectroscopy. In: Proceedings of international symposium on physical failure analysis of integrated circuits; 2005. p. 275–81.
[23] Tan S-L, Yim K-H, Chan S-H, Phang C-H, Zhou Y, Balk L-J, et al. Detectivity optimization of InGaAs photon emission microscope systems. In: Proceedings of international symposium on physical failure analysis of integrated circuits; 2006. p. 315–9.
[24] Tan S-L, Toh K-H, Phang C-H, Chan S-H, Chua C-M, Koh L-S. A near-infrared, continuous wavelength, in-lens spectroscopic photon emission microscope system. In: Proceedings of international symposium on physical failure analysis of integrated circuits; 2007. p. 240–4.
[25] Lin I-C, Huang C-Y, Chao C-J, Ker M-D. Anomalous latchup failure induced by on-chip ESD protection circuit in a high-voltage CMOS IC product. Microelectron Reliab 2003;43:1295–301.
[26] Tong C-F, Chen W, Jiang H-C, Hui J, Xu P-P, Liu Z-Q. Active ESD shunt with transistor feedback to reduce latch-up susceptibility of false triggering. In: Proceedings of international symposium on physical failure analysis of integrated circuits; 2004. p. 89–92.