國立交通大學

電子工程學系電子研究所

博士論文

高性能時序交錯管線式類比至數位轉換器設計

Design of High-Performance Time-Interleaved Pipelined Analog-to-Digital Converters

研究生 ： 李瑞梅

指導教授 ： 吳介琮

中華民國九十六年六月

高性能時序交錯管線式類比至數位轉換器設計

Design of High-Performance Time-Interleaved Pipelined Analog-to-Digital Converters

研究生 ： 李瑞梅　　Student ： Zwei-Mei Lee

指導教授 ： 吳介琮　　Advisor ： Jieh-Tsorng Wu

國立交通大學

電機學院　　電子工程學系　　電子研究所

博士論文

A Dissertation

Submitted to Department of Electronics Engineering
and Institute of Electronics
College of Electrical Engineering
National Chiao-Tung University
in partial Fulfillment of the Requirements
for the Degree of
Doctor of Philosophy
in
Electronics Engineering
June 2007
Hsin-Chu, Taiwan, Republic of China

中華民國九十六年六月

高性能時序交錯管線式類比至數位轉換器設計

學生 ： 李瑞梅　　指導教授 ： 吳介琮

國立交通大學

電機學院　電子工程學系　電子研究所

摘要

高速高解析度之奈奎斯特率類比至數位轉換器在設計上主要採用管線式的架構來實現，通常高增益具線性回授之運算放大器被用於確保內部取樣並保持電路與管線級的線性度，為了達到高於十四位元的解析度，其中的運算放大器必須有高於 90 dB 的直流電壓增益，在如此高的直流增益需求下，運算放大器的設計難以達到高速的需求。時序交錯多個慢速但高解析度的管線式類比至數位轉換器因而被提出，用於增加整體的取樣速度，然而，這樣的架構卻會因為各個類比至數位轉換器間的增益、偏移量以及取樣信號相位上不匹配的誤差而使得整體的轉換線性度變差。因此，為了降低這樣的不匹配誤差以維持轉換的線性度，發展校準的技術是必需的。

本論文主要探討時序交錯管線式類比至數位轉換器之設計、改善管線式類比至數位轉換器線性度的方法，以及降低時序交錯之各個類比至數位轉換通道間增益與電壓偏移不匹配誤差的方法。同時，也說明我們所提出之緩衝器預先充電取樣並保持電路，被放置於轉換器最前端來取樣輸入信號藉以改善各個轉換通道間取樣時序不匹配的影響。

最後，一個 15 位元每秒 125 百萬取樣之時序交錯管線式類比至數位轉換器之設計原型被實現以驗證本研究所提出之方法，這個轉換器採用 0.18 微米之 CMOS 製程製造完成，在輸入信號之頻率為 9.99 百萬赫茲時，可達 91.9 dB 的無雜散信

號動態範圍 (SFDR) 及 69.9 dB 的信號對雜訊與失真比 (SNDR) 。此類比至數位轉換器採用單一一個緩衝器預先充電之取樣並保持放大器藉以降低取樣信號之相位不匹配所造成的誤差，同時也採用數位背景校準的方法來維持單一轉換器通道的線性度及校正通道間增益與偏移量不匹配所造成的誤差。不包含輸入/輸出之緩衝器電路，此轉換器的面積為 $4.3 \times 4.3\ mm^2$ ，功率消耗為 909 mW 。

Design of High-Performance Time-Interleaved Pipelined Analog-to-Digital Converters

Student : Zwei-Mei Lee Advisor : Jieh-Tsorng Wu

Department of Electronics Engineering
and Institute of Electronics
National Chiao-Tung University

Abstract

High-speed high-resolution Nyquist-rate analog-to-digital converters (ADCs) have been predominantly realized using the pipeline architecture. High-gain opamps with linear feedback are often used to ensure the linearity of sample-and-hold amplifiers (SHAs) and pipeline stages. To achieve more than 14-bit resolution, the opamps are required to have a voltage gain of more than 90 dB, which results in reduced speed.

Time-interleaving slow high-resolution pipelined A/D channels is therefore used to increase the effective sampling speed. However, gain, offset and sampling phase mismatch errors among the A/D channels degrade the overall A/D linearity. Thus, calibration is necessary for reducing the mismatch errors to maintain the A/D conversion linearity.

This thesis presents a time-interleaved pipelined ADC design. Methodologies for reducing the mismatch errors and improving the A/D linearity of a single channel are investigated and discussed. The proposed buffered-precharged SHA used to reduce the sampling time skew errors among A/D channels is also discussed.

Finally, A 15-bit 125-MS/s two-channel time-interleaved pipelined ADC's prototype is described. This ADC is fabricated in a 0.18 μm CMOS technology, and achieves 91.9 dB SFDR, 69.9 dB SNDR for a 9.99 MHz input. The ADC uses a single buffered-precharged sample-and-hold amplifier to avoid sampling phase error. Digital background calibration is employed to maintain the conversion linearity of each A/D channel and also correct both gain and offset mismatches between the two channels. Excluding I/O buffers, the chip occupies an area of 4.3 × 4.3 mm^2 and dissipates 909 mW from a 1.8 V supply.

Acknowledgements

First of all, I would like to express my appreciation to Prof. Jieh-Tsorng Wu for his support and patient guidance in my research. I was truely very fortunate to have the opportunity to work under him as a student. Whenever I encounter the difficulties or problems, he is always patient to give me the direction and encouragement.

I would also like to express my appreciation to the other students in Prof. Jieh-Tsorng Wu's group, to the students in Prof. Jing-Yang Jou's group, and to the other members in ED307 lab at NCTU. They provided a comfortable environment to work in, and peopele were very accepting. Without their help, my Ph. D work never be done well.

I especially appreciate Mr. Hung-Chih Liu for his guidence during my time here at National Chaio-Tong University. I worked with him on his pipelined ADC and through working with him learned a great deal about circuit design.

I would like express my greatest appreciation to Mr. Cheng-Yeh Wang, for his patient encouragement. In addition to being a valuable resource, he provided a great deal support to me through all the phases of my research work. He also took care of me when I was sick and damp.

Finally, I would like to express my appreciation to my mother, and other members of my family for their unconditional support and encouragement.

ZWEI-MEI LEE

National Chiao-Tung University

2007, June

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

Nyquist-rate analog-to-digital converters (ADCs) of more than 12-bit resolution have been predominantly realized using the pipelined analog-to-digital conversion (A/D) architecture as shown in Fig. 1.1, which is a survey of CMOS Nyquist-rate ADCs published from 1997 to 2006. As a pipelined ADC is required high sample rate, time-interleaving technique is applied. Therefore, this work addresses on the design of time-interleaved pipelined ADCs.

In switched-capacitor pipelined ADCs, the linearities of sample-and-hold amplifiers and pipeline stages are ensured by using high-gain opamps with capacitor feedback. Pipelined ADCs of more than 14-bit resolution can be achieved by incorporating digital calibration (either foreground or background) to mitigate the requirements for device matching and opamps' dc gain [3] [4] [5]. The maximum sampling rate of a pipelined ADC is mainly determined by the achievable operating speed of its internal high-gain opamps.

The time-interleaved (TI) architecture which contains more than one A/D channels to share the conversion operations can overcome the speed limitation imposed by their internal circuit blocks [6]. However, the overall accuracy of a TI-ADC can be degraded by the gain, offset, and sampling phase mismatches among its A/D channels. Many calibration techniques have been developed to correct the A/D errors caused by these mismatches.

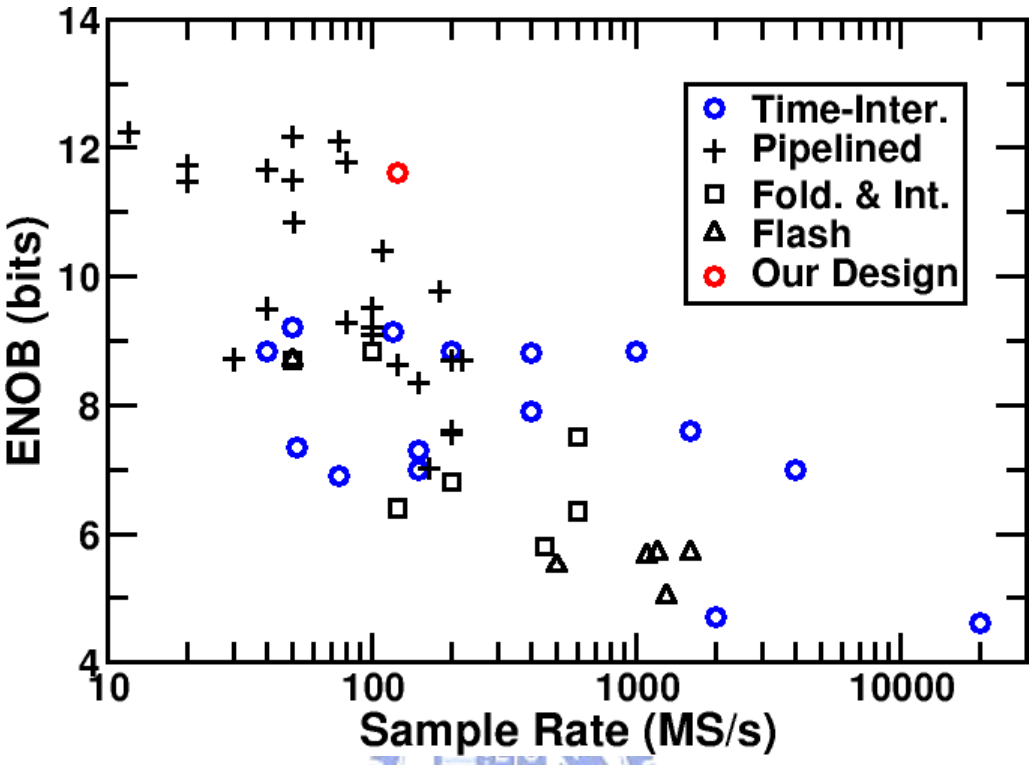


Figure 1.1: CMOS Nyquist ADC survey.

To take advantage of low-cost digital circuits in scaled CMOS technologies, there are calibration schemes that execute the calibration procedures continuously in the background, while requiring no external reference signals or extra A/D channels [7] [8]. These schemes are able to extract mismatch information directly from the ADC's digital outputs. These techniques usually involve complicated signal processing in the digital domain. They also impose certain requirements on the ADC's input signal, e.g., it must be bandlimited and asynchronous with the ADC's sampling clock.

In this work, we designed a 15-bit 125-MS/s CMOS TI-ADC which consists of two pipelined A/D channels. This ADC incorporates a single sample-and-hold amplifier (SHA) to avoid sampling phase mismatch. The SHA uses a precharged circuit configuration to mitigate the performance requirements for its opamp which has to operate at a maximum clock rate of 125 MHz. Digital background calibration is employed to maintain the conversion linearity of each A/D channel and also correct both gain and offset mismatches between the two channels. The calibration is proceeded continuously in the background

without interrupting the normal A/D operations. The calibration schemes incorporated in this ADC are robust since they do not rely on input signal condition. The ADC chip was fabricated in a 0.18 μm 1P6M CMOS technology with MIM capacitors, and operates under a single 1.8 V supply.

1.2 Organization of Thesis

This thesis is organized into eight chapters. Chapter 1 gives the introduction of the thesis from high resolution, high speed ADCs. Chapter 2 examines the switch-capacitor based pipelined ADC with its error sources, and the linearity enhancement techniques are presented in chapter 3. Chapter 4 overviews the time-interleaved ADC, and the degradation of linearity caused by mismatches among A/D channels. Then, the mismatch error correction methods are briefly reviewed in chapter 5. Chapter 6 discusses the topology of the sample-and-hold amplifiers with their essential parameters. Factors limiting the resolution and sampling rate of sample-and-hold amplifier are analyzed and summarized. In chapter 7, the prototyping ADC's implementation is described, including the opamp, comparator, and digital function blocks for calibration, as well as the experimental measurements. Finally, conclusions and future works are drawn in chapter 8.


E
S
A
1896

Chapter 2

Pipelined Analog-to-Digital Converters

2.1 Introduction

Pipelined A/D architecture is widely used for implementing high performance ADCs due to its high throughput rate. In addition, it exhibits linear growth in hardware as resolution increases. However, it can achieves only 8-10 bits of linearity in most IC processing technologies without the use of component trimming or calibration. In this chapter, an overview of pipeline ADCs is presented, and nonidealities in pipeline ADCs are examined. Moreover, switched-capacitor (SC) implementations are discussed.

Fig. 2.1 shows the block diagram of a pipelined ADC [9]. It consists of P identical pipeline stages. A pipeline stage comprises a sub-ADC, a sub-DAC, a subtractor, and a gain amplifier. Its block diagram is shown in Fig. 2.2. The input signal V_j to the j-th stage

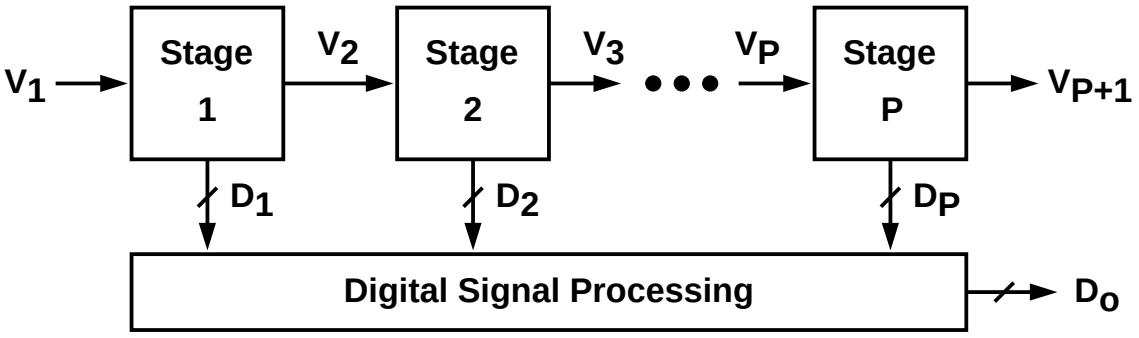


Figure 2.1: A pipelined ADC.

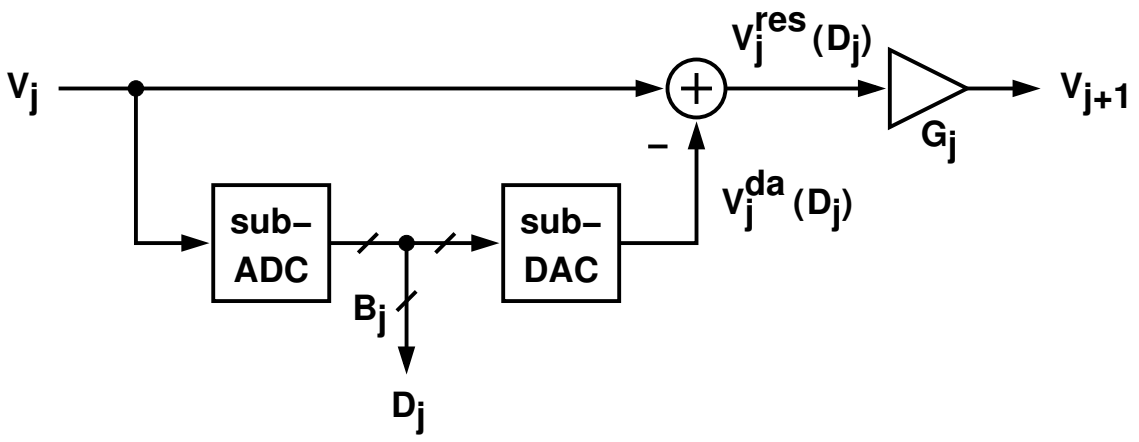


Figure 2.2: A pipeline stage.

is quantized by the sub-ADC to produce B_j bits digital code, D_j. The sub-ADC typically consists of a bank of $2^{B_j} - 1$ comparators, $j \in \{1, 2, \cdots, P\}$. Then, the digital code, D_j, drives the B_j-bit sub-DAC to produce $V_j^{\mathrm{da}}(D_j)$, which is a quantized analog estimate of the V_j input signal. This sub-DAC output, $V_j^{\mathrm{da}}(D_j)$, is then subtracted from the stage input to give an analog residue, $V_j^{\mathrm{res}}(D_j)$. Finally, $V_j^{\mathrm{res}}(D_j)$ is amplified by an amount of G_j and transferred to the next stage. In typically, B_j is ranged from 2 to 5 bits, and G_j usually equals to 2^{B_j}.

The static transfer characteristics of a B_j-bit pipeline stage is shown in Fig. 2.3. Its V_j input has a full-scale range from $-V_r$ to $+V_r$. That means the minimum range of resolution corresponding to the B_j bits digital code equals to $[(+V_r) - (-V_r)]/2^{B_j}$, denoted as r_j. The plot of V_j^{da} versus V_j exhibits a staircase. Note that the threshold levels in the V_j-axis ideally are uniformly spaced. The V_j^{da} represents the approximation of V_j corresponding to D_j. Thus, the difference of V_j and V_j^{da} can be plotted as the middle curve of Fig. 2.3, named V_j^{res} versus V_j. This difference is gained up by G_j, and then the stage analog output, V_{j+1}, is obtained. The curve of V_{j+1} versus V_j is shown in the most underlying frame, where the slope of each sawtooth-like shape equals to $G_j = 2^{B_j}$.

The mathematical description for the ideal relationship of the stage input, V_j, and the amplified residue, V_{j+1}, is given by

$$V_{j+1} = G_j \times \left[V_j - V_j^{\mathrm{da}}(D_j)\right] \tag{2.1}$$

where the parameters of a pipeline stage referred to (2.1) are listed in Table 2.1.

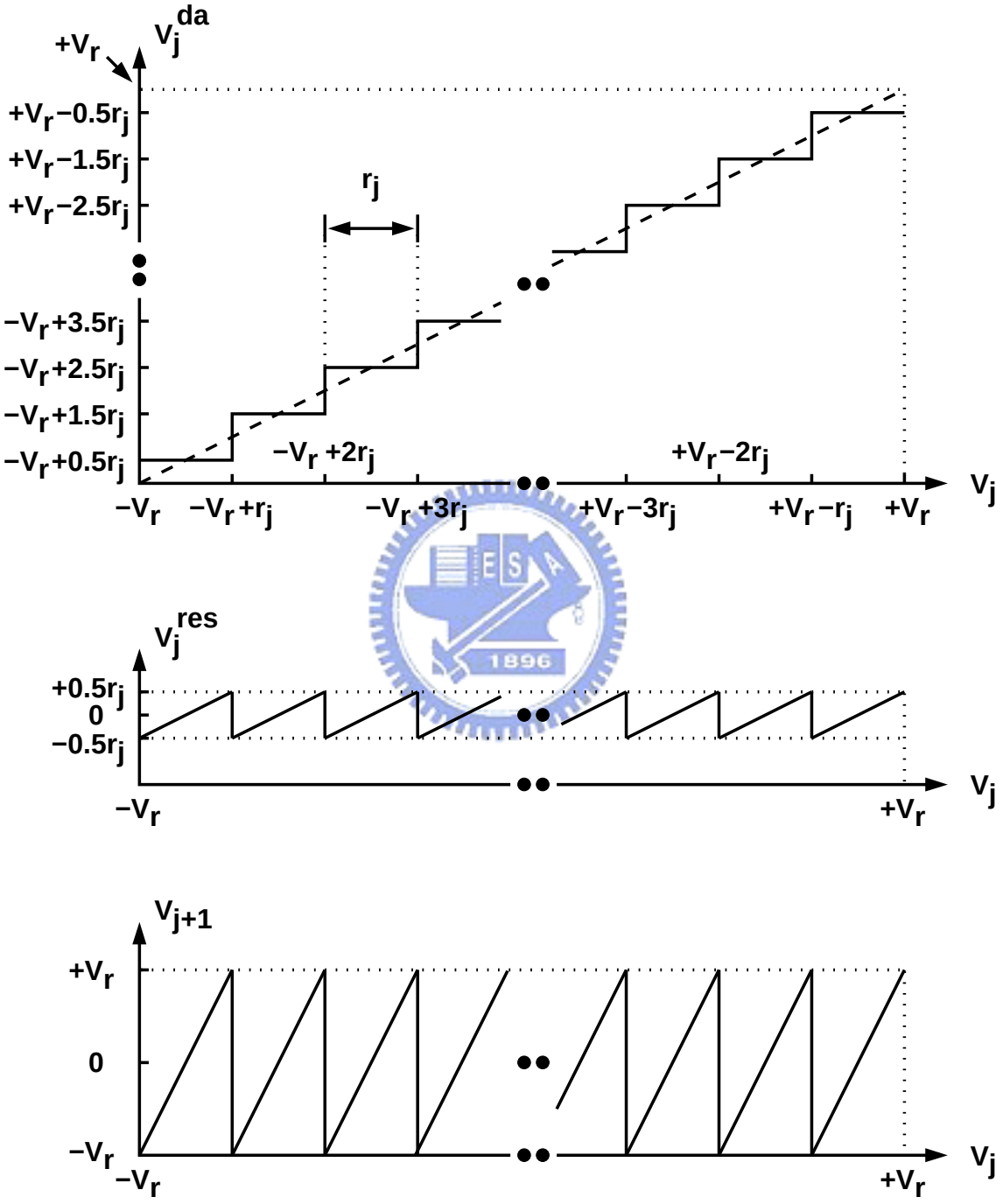


Figure 2.3: Transfer characteristics of a stage.

Table 2.1: Parameters of a B_j-bit pipeline stage.

Range of V_j	$\{-V_r, +V_r\}$
Thresholds of sub-ADC	$\pm(V_r - r_j), \pm(V_r - 2r_j), \cdots, \pm 2r_j, \pm r_j$
Digital codes (D_j)	$0, 1, 2, \cdots, 2^{B_j} - 1$
Reference levels (V_j^{da})	$\pm(V_r - 0.5r_j), \pm(V_r - 1.5r_j), \cdots, \pm 1.5r_j, \pm 0.5r_j$

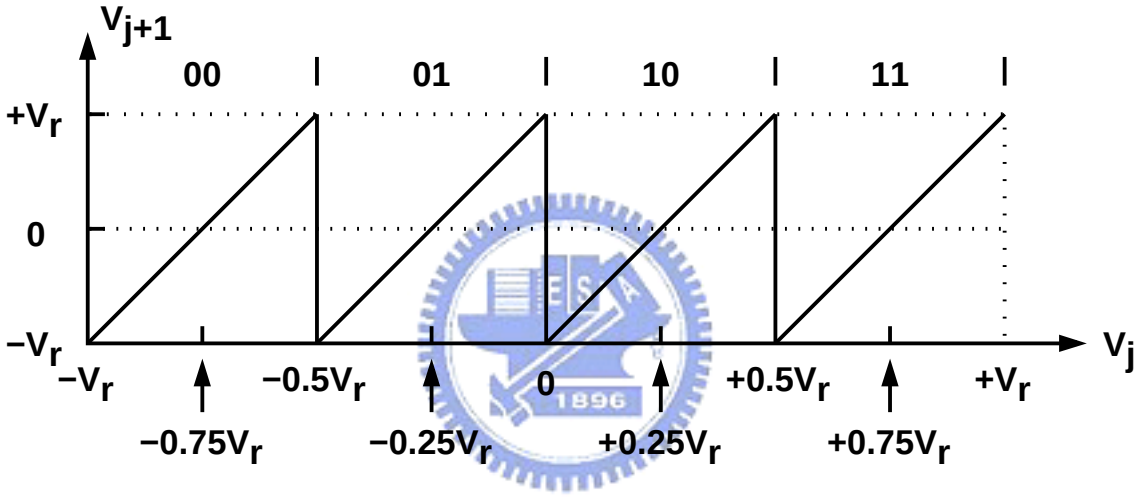


Figure 2.4: Ideal transfer curve of a 2-bit stage.

Furthermore, the overall ADC's input can be iteratively derived according to (2.1) from the 1-st stage to the last P-th stage. It is obtained by:

$$V_1 = V_1^{\mathrm{da}}(D_1) + \frac{V_2^{\mathrm{da}}(D_2)}{G_1} + \frac{V_3^{\mathrm{da}}(D_3)}{G_1 G_2} + \cdots + \frac{V_P^{\mathrm{da}}(D_P)}{G_1 G_2 \cdots G_{P-1}} + \frac{V_{P+1}}{G_1 G_2 \cdots G_P} \tag{2.2}$$

where the last term, $V_{P+1}/G_1 G_2 \cdots G_P$, is the typical quantization error.

So far, it has been assumed that each stage has ideal transfer characteristics as well as the whole pipelined ADC. However, there will be errors incurred due to the imperfections of circuit implementations.

Table 2.2: Parameters of a 2-bit pipeline stage.

Range of V_j	$\{-V_r, +V_r\}$
Thresholds of sub-ADC	$-0.5V_r, 0, +0.5V_r$
Four digital codes (D_j)	$0, 1, 2, 3$
Four reference levels (V_j^{da})	$-0.75V_r, -0.25V_r, +0.25V_r, +0.75V_r$

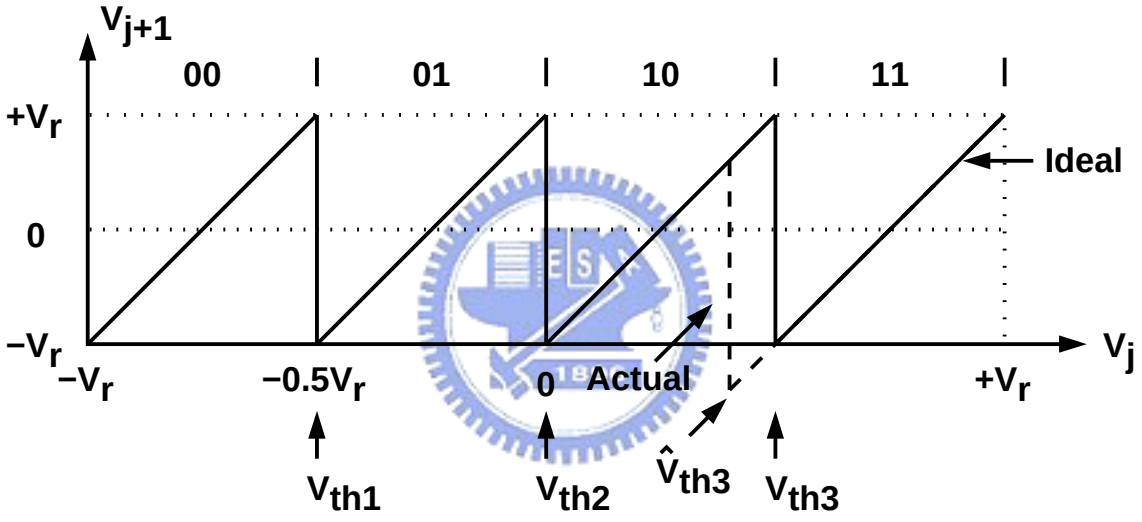


Figure 2.5: Transfer curve of a 2-bit stage with sub-ADC offsets.

2.2 Nonidealities in Pipelined ADCs

In this section, the linear errors of a pipelined ADC are discussed by illustrating with a 2-bit pipeline stage, i.e. $B_j = 2$. Its ideal transfer curve is shown in Fig. 2.4 and the corresponding parameters are shown in Table 2.2, where $r_j = 0.5V_r$. Here, three major error sources are examined. They are offset errors, sub-DAC reference errors and inter-stage gain errors. As shown in Fig. 2.2, the sub-ADC, the subtractor and gain amplifier can result in offset errors in a pipelined ADC.

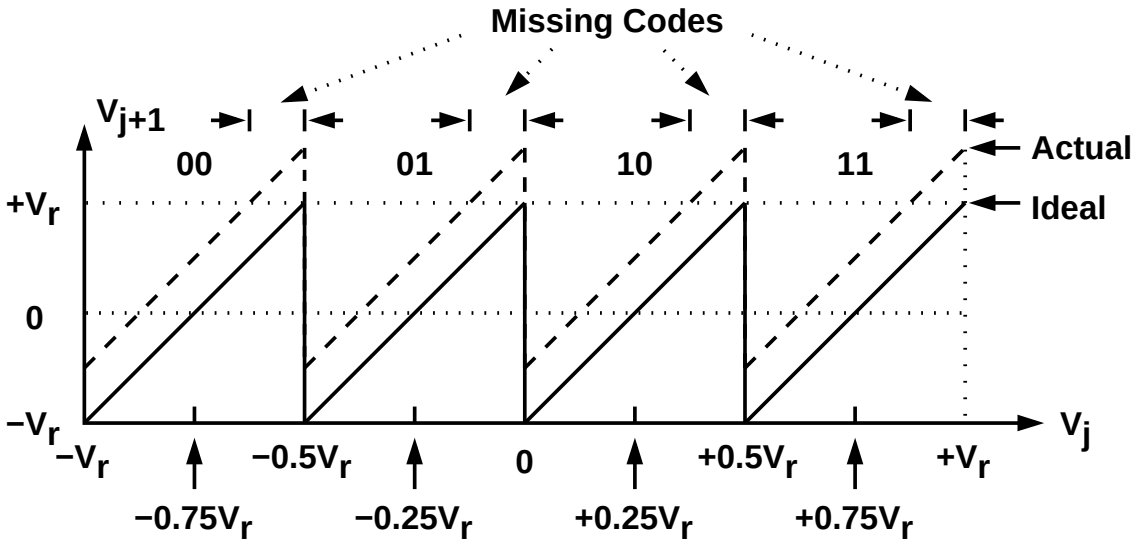


Figure 2.6: Transfer curve of a 2-bit stage with offsets in the subtractor and gain amplifier.

2.2.1 Offset Errors

The behavior of the 2-bit stage with an offset in one of the thresholds is illustrated in Fig. 2.5. Assume that only the nonideal threshold levels are discussed in this subsection unless extra being stated. If there has an offset in the threshold level, the actual transfer curve is shown as the dash line in Fig. 2.5. The threshold level of V_{th3} is broken by an offset and becomes as $\hat{V}_{th3}$. Due to the changed level, the stage output, V_{j+1}, is more negative than $-V_r$, and thus out of the input range of the next stage. Furthermore, errors in the overall A/D transfer characteristics will be incurred, especially in missing digital codes. This means that if V_{j+1} is less than $-V_r$, D_j becomes too large, i.e. $10 \rightarrow 11$, and should be made more negative. On the other hand, if V_{j+1} is greater than $+V_r$, D_j is too small, and should be made more positive.

The transfer characteristics due to the offsets in the subtractor and the gain amplifier are shown in Fig. 2.6. These offsets result in a repeated pattern, whereas those of sub-ADC cause errors only in the neighborhood of the thresholds. The transfer relations of the stage can be expressed in mathematical description as:

$$V_{j+1} = G_j \times \left[V_j - V_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}}\right] \tag{2.3}$$

The overall amplified output V_{j+1} is shifted by the offset with amount of $-G_j \times V_j^{\mathrm{os}}$. This

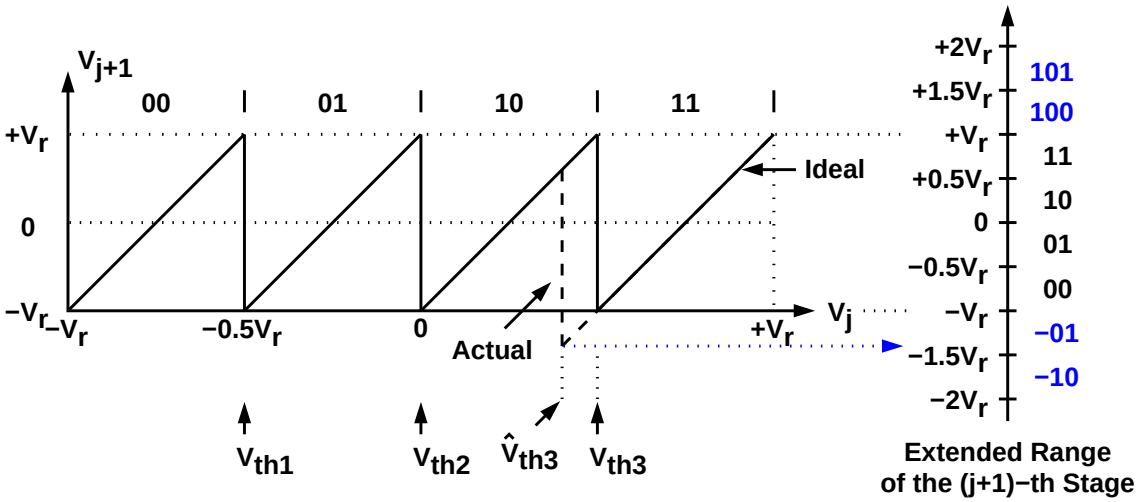


Figure 2.7: Transfer curve of a 2-bit j-th stage with the extended range of the $(j+1)$-th stage.

means that a repeated pattern of missing codes appears at the whole A/D digital output.

Two techniques are used to alleviate the offset effects resulted from the sub-ADC, the subtractor, and the gain amplifier. One is to expand the range to be more than $\pm V_r$ of the following stage to allow the amplified residue output with some amount of being more than $\pm V_r$. The other is to reduce the interstage gain, and thus to use the less range than $\pm V_r$ to guarantee that the offsets do not result in overrange. Both the two schemes here are discussed.

Consider an example of 2-bit j-th stage following by the $(j+1)$-th stage with the extended range shown in Fig. 2.7. The threshold levels of the $(j+1)$-th stage and its corresponding codes are shown on the right-side of the figure. The extended range is 2 times of the normal range. If there have threshold offsets in the j-th stage, the V_{j+1} will not be overrange while the $(j+1)$-th stage accommodates it to vary from $-2V_r$ to $+2V_r$.

Reducing gain scheme with shifting the sub-ADC thresholds and the sub-DAC levels is also helpful for avoiding the overrange of V_{j+1}. In a 2-bit case shown in Fig. 2.8, its dc parameters are listed in Table 2.3. Due to the reduced interstage gain, the redundancy is introduced to alleviate the offset requirement. Then, this redundancy is removed after the output digital coding. After digital correction [9] [10], the final effective number of bits equals to 1 bit.

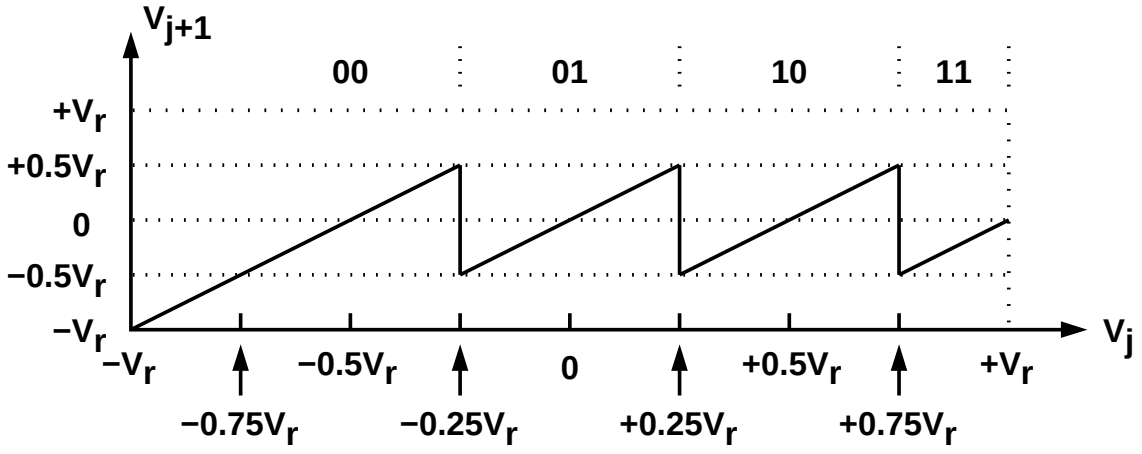


Figure 2.8: Transfer curve of a 2-bit stage with interstage gain=2.

Table 2.3: Parameters of a 2-bit pipeline stage with reduced gain.

Range of V_j	$\{-V_r, +V_r\}$
Thresholds of sub-ADC	$-0.25V_r, +0.25V_r, +0.75V_r$
Four digital codes (D_j)	$0, 1, 2, 3$
Four reference levels (V_j^{da})	$-0.5V_r, 0, +0.5V_r, +V_r$

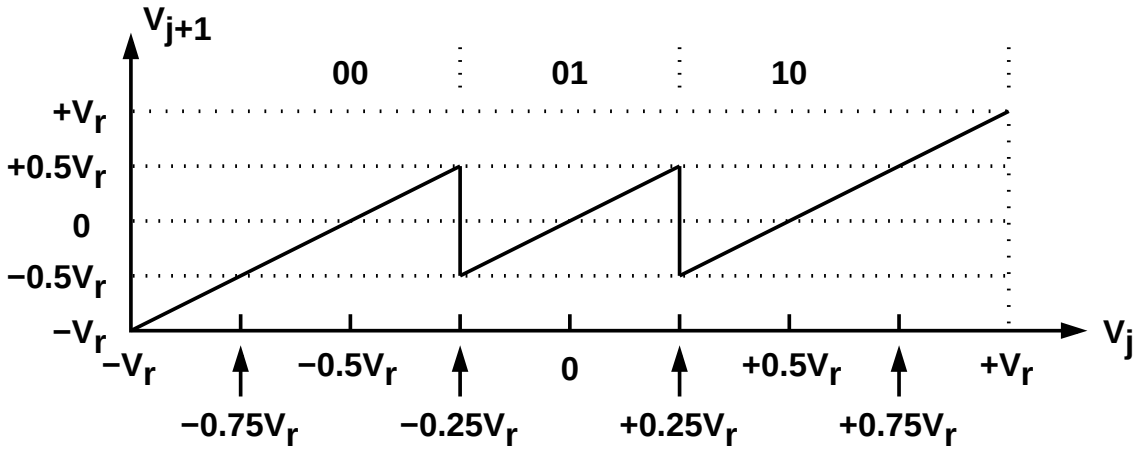


Figure 2.9: Transfer curve of a 1.5-bit stage with interstage gain=2.

Table 2.4: Parameters of an alternative of 2-bit pipeline stage with reduced gain.

Range of V_j	$\{-V_r, +V_r\}$
Thresholds of sub-ADC	$-0.25V_r, +0.25V_r$
Four digital codes (D_j)	$0, 1, 2$
Four reference levels (V_j^{da})	$-0.5V_r, 0, +0.5V_r$

At this point, in a pipelined ADC, reduced interstage gain permits large allowable offsets and thus leads to a robust implementation. The maximum allowable offsets are defined by the requirement that V_{j+1} must be within the range of the following $(j+1)$-th stage. Therefore, the accuracy of the thresholds is independent of the overall A/D accuracy.

An alternative with 1 effective bit which is most widely used in pipelined ADC's implementations [2] [11] [3] [12] is 1.5 bits per stage. Its corresponding transfer characteristics are shown in Fig. 2.9, and its dc parameters are presented in Table 2.4. While the characteristics of this alternative is widely employed and is easily extend to implement multibit per stage, it is furthermore discussed in the following sections. In particular, it is used to investigated the switched-capacitor implementation of a pipelined ADC.

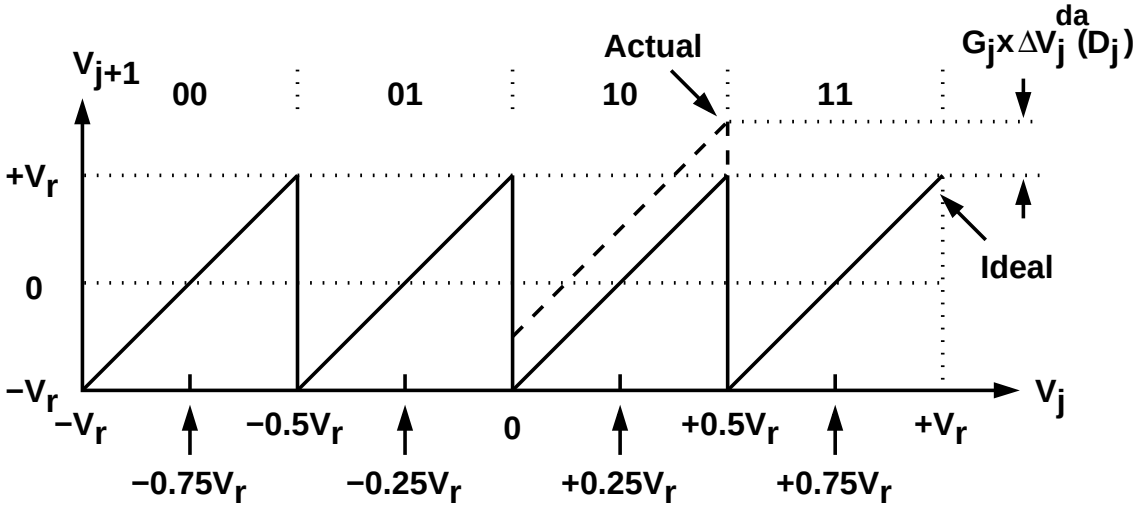


Figure 2.10: Transfer curve of a 2-bit stage with sub-DAC reference errors.

2.2.2 Sub-DAC and Interstage Gain Error

The effect on transfer characteristics of an individual stage due to errors in a sub-DAC reference level is examined here. Its corresponding transfer curve is depicted in Fig. 2.10. It can be observed that an error $\Delta V_j^{\mathrm{da}}(D_j)$ in the sub-DAC reference level will result in an error in the final amplified residue output with a value of $G_j \times \Delta V_j^{\mathrm{da}}(D_j)$. Due to this sub-DAC error, the stage transfer function is rewritten as:

$$V_{j+1} = G_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j)\right] \tag{2.4}$$

where $\hat{V}_j^{\mathrm{da}}(D_j) = V_j^{\mathrm{da}}(D_j) - \Delta V_j^{\mathrm{da}}(D_j)$. In order to maintain the overall ADC's accuracy, this error amount is required to be less than x LSB of the remaining stages and this is expressed as

$$G_j \times \Delta V_j^{\mathrm{da}} < x \cdot \frac{2V_r}{2^{\left(\sum_{p=j+1}^{P} B_p\right)}} \tag{2.5}$$

which yields the relative sub-DAC accuracy as

$$\frac{\Delta V_j^{\mathrm{da}}(D_j)}{2V_r} < \frac{x}{2^{\left(\sum_{p=j+1}^{P} B_p\right)}} \cdot \frac{1}{G_j} = \frac{x}{2^{\left(\sum_{p=j}^{P} B_p\right)}} \tag{2.6}$$

Typically, x is chosen as $1/2$, and $G_j = 2^{B_j}$.

It is obvious that any errors in the sub-DAC will directly degrade the accuracy of the stage input since V_j^{da} is subtracted directly from the input. It is also clear to be examined

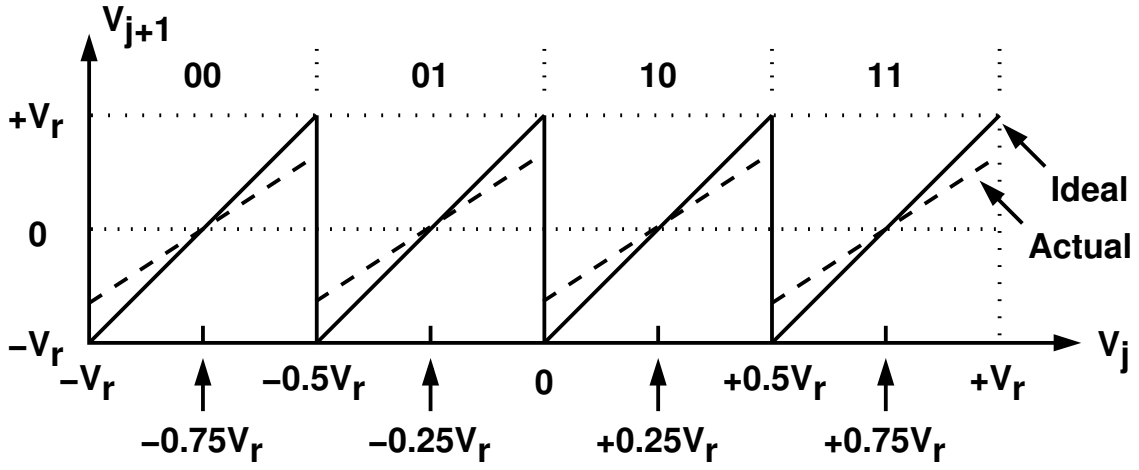


Figure 2.11: Transfer curve of a 2-bit stage with residue gain errors.

from (2.2) that the kind of errors directly degrades the overall A/D accuracy of the whole ADC. Therefore, the sub-DAC relative accuracy, $\Delta V_j^{\mathrm{da}}(D_j)/2V_r$ should be considered to be consistent with the corresponding resolution of the pipeline stages from the j-th to the last one.

The effects of nonideal interstage gain are now examined, as depicted in Fig. 2.11. For a 2-bit stage using simple coding with no redundancy, its nominal gain is $G_j = 4$. However, if there appears gain error, denoted by ε_G, the actual gain becomes as $\hat{G}_j = G_j(1-\varepsilon_G)$. Hence, the actual transfer curve shown as the dash line in Fig. 2.11 indicates to have the slope of $4(1-\varepsilon_G)$. This causes that the maximum residue output is reduced from V_r to $V_r(1-\varepsilon_G)$, and the stage's analog I/O transfer function is given by

$$V_{j+1} = \hat{G}_j \times \left[V_j - V_j^{\mathrm{da}}(D_j)\right] = G_j\,(1-\varepsilon_G) \times \left[V_j - V_j^{\mathrm{da}}(D_j)\right] \tag{2.7}$$

The error, $G_j \times \varepsilon_G \times [V_j - V_j^{\mathrm{da}}(D_j)]$, of the residue output due to the interstage gain error will be passed down the pipeline. In order to maintain the ADC's resolution, this error is therefore limited to be less than x LSB of the resolution in the remaining stages. This

Table 2.5: Parameters of a B_j-bit SC stage.

Range of V_j	$\{-V_r, +V_r\}$
$(2^{B_j}-2)$ thresholds of sub-ADC	$\pm(N_s-0.5)r_j, \pm(N_s-1.5)r_j, \cdots, \pm 0.5r_j$
$(2^{B_j}-1)$ digital codes (D_j)	$0, \pm1, \pm2, \cdots, \pm(N_s-1), \pm(N_s)$
$(2^{B_j}-1)$ reference levels (V_j^{da})	$\pm N_s r_j, \pm(N_s-1)r_j, \cdots, \pm r_j, 0$
N_s intermediate codes $D_{j,y}$	$-1, 0, +1$

implies that

$$
\begin{aligned}
& G_j \times \varepsilon_G \times [V_j - V_j^{\mathrm{da}}(D_j)] < x \cdot \frac{2V_r}{2^{\left(\sum_{p=j+1}^{P} B_p\right)}} \\
\Rightarrow \quad & \varepsilon_G < \frac{x}{2^{\left(\sum_{p=j}^{P} B_p\right)}} \times \frac{2V_r}{\left[V_j - V_j^{\mathrm{da}}(D_j)\right]} \\
\Rightarrow \quad & \varepsilon_G < \frac{x}{2^{\left(\sum_{p=j}^{P} B_p\right)-1}}
\end{aligned}
\tag{2.8}
$$

Equation 2.8 holds if $max\{V_j - V_j^{\mathrm{da}}(D_j)\} = V_r$. To avoid missing codes, x corresponds to 1 and thus $\varepsilon_G < \left[1/2^{\left(\sum_{p=j}^{P} B_p\right)-1}\right]$.

In the practical design, the error contributions of settling time errors and matching errors in the gain amplifier are also considered. Therefore, x in (2.8) is typically required to be less than $1/4$.

2.3 Switched-Capacitor Implementations

A general B_j-bit SC stage in the single-ended configuration with reduced G_j to alleviate offset effects is illustrated here to examine its operating principles and nonidealities.

A general switched-capacitor (SC) configuration for a B_j-bit stage with the reduced G_j is shown in Fig. 2.12. Since it is to emphasize the essence of what is happening with respect to the pipelined A/D conversion function, the peripheral details such as output reset are therefore omitted. The sub-ADC consists of a bank of $2N_s$ comparators. The

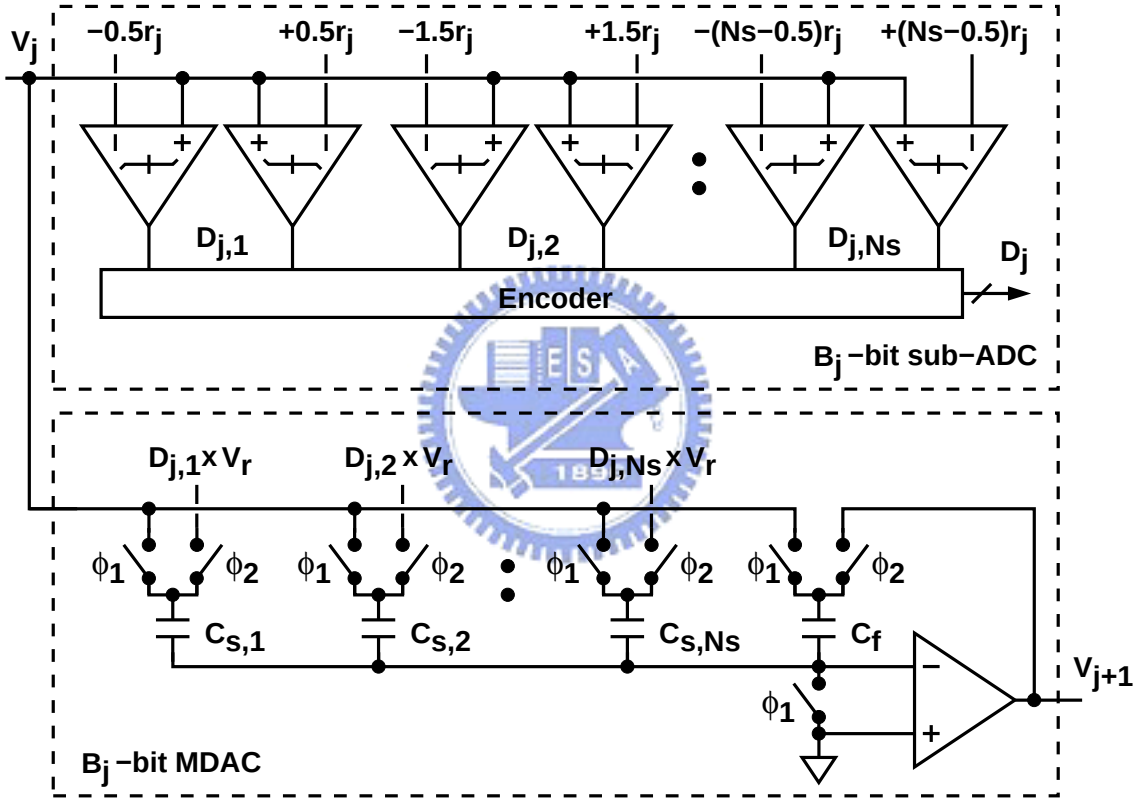


Figure 2.12: A B_j-bit SC pipeline stage with the reduced interstage gain.

Table 2.6: Parameters of a 3-bit SC stage.

Range of V_j	$\{-V_r, +V_r\}$
6 thresholds of sub-ADC	$\pm 5V_r/8, \pm 3V_r/8, \pm V_r/8$
7 digital codes D_j	$-3, -2, -1, 0, +1, +2, +3$
7 reference levels V_j^{da}	$\pm 6V_r/8, \pm 4V_r/8, \pm 2V_r/8, 0$

multiplying digital-to-analog converter (MDAC) is used to implemented the sub-DAC, the subtractor, and the gain amplifier shown in Fig. 2.2, and comprises a bank of switched-capacitors, and an opamp. Its corresponding parameters are listed in Table 2.5, where N_s is defined as the minimum number of required sampling capacitors while employing the reduced interstage gain technique with sharing the C_f feedback capacitor, and its value related to B_j is given by

$$N_s = 2^{B_j - 1} - 1 \tag{2.9}$$

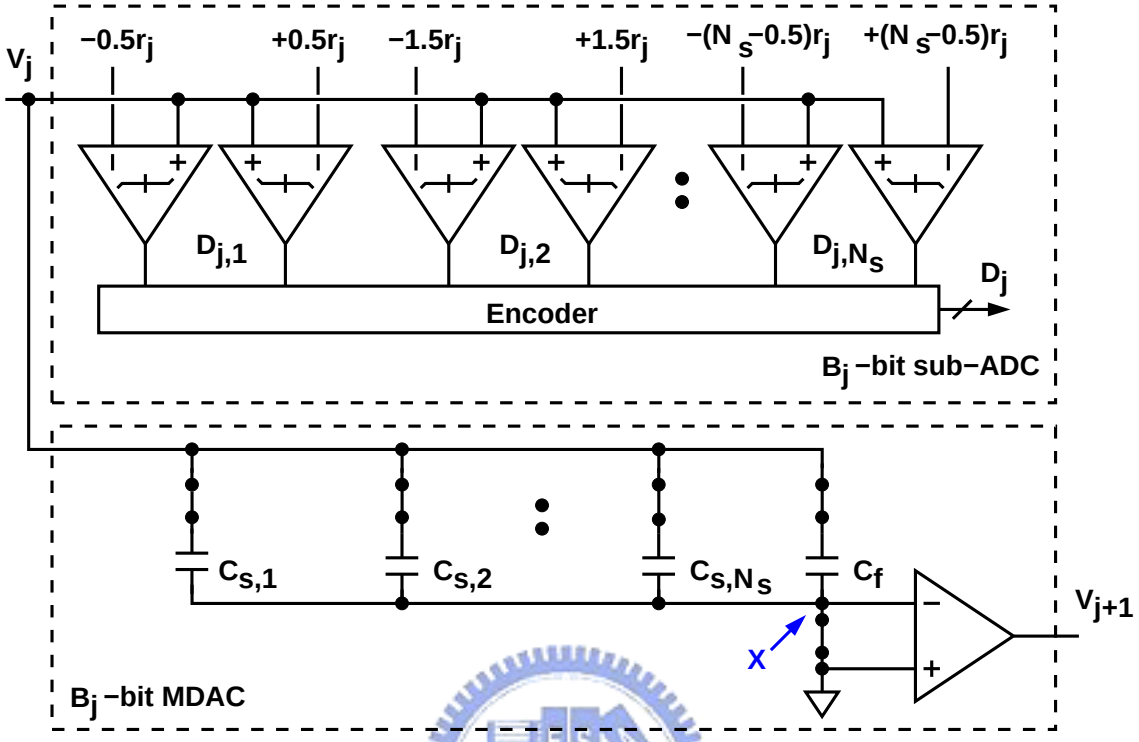
The intermediate code, $D_{j,y}$, is produced by the two comparators which have thresholds with the same value but opposite sign, and its corresponding values are within $\{-1, 0, +1\}$. The D_j output code is obtained by adding the $D_{j,y}$'s, and is expressed as

$$D_j = \sum_{y=1}^{N_s} D_{j,y} \tag{2.10}$$

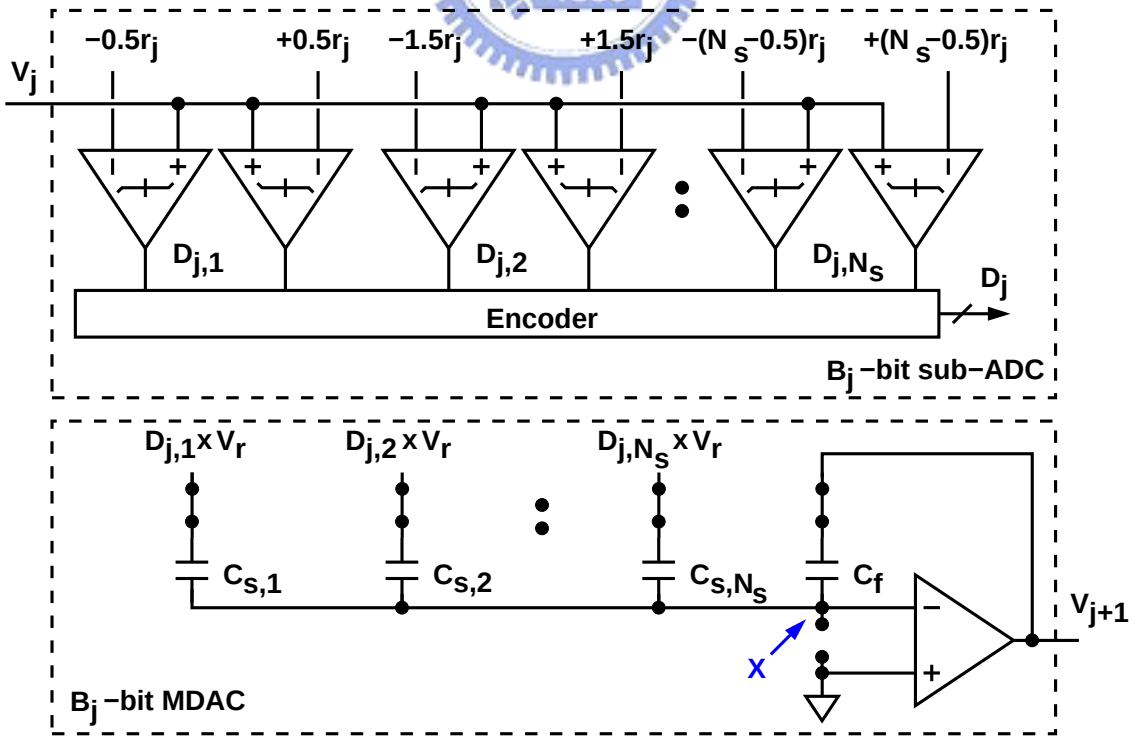
For example, a 3-bit SC stage sharing the feedback capacitor has $N_s = 3$ sampling capacitors and its has the dc parameters shown in Table 2.6.

The SC schematic shown in Fig. 2.12 has two operating phases which is shown in Fig. 2.13. It is assumed that the operational amplifier (opamp) is ideal as well as the switches and capacitors. The nonideal effects are considered later.

During the sample phase ($\phi_1 = 1$), as shown in Fig. 2.13(a), the V_j input is acquired on sampling capacitors, $C_{s,y}$, for all $y \in \{1, 2, \cdots, N_s\}$, and the shared feedback capacitor, C_f. The input is also acquired by the comparators in the sub-ADC for comparing to the thresholds. At the end of the sampling phase which is defined as the sampling instant, the



(a) Sample phase.



(b) Hold phase.

Figure 2.13: Two phase operations of a B_j-bit SC stage.

sampling switches are opened, and the stored charge at the node X is given by

$$Q_{X,s} = -\left(C_f V_j + \sum_{y=1}^{N_s} C_{s,y} V_j \right) \tag{2.11}$$

During the hold phase ($\phi_2 = 1$), as shown in Fig. 2.13(b), the digital code produced by the sub-ADC determines which references are connected to the capacitors, $C_{s,y}$, to perform the sub-DAC function. At the same phase, the opamp goes into closed-loop configuration with the feedback capacitor, C_f, and the sampled charge, $Q_{X,s}$, is redistributed over $C_{s,y}$ and C_f, to generate the stage's output, V_{j+1}. Then, this output is acquired by the next pipeline stage. At the end of the hold phase, the charge at node X is given by

$$Q_{X,h} = -\left(C_f \times V_{j+1} + \sum_{y=1}^{N_s} C_{s,y} \times D_{j,y} V_r \right) \tag{2.12}$$

According to the charge conservation theorem, $Q_{X,h}$ equals to $Q_{X,s}$. Therefore, equating (2.11) and (2.12) yields

$$-\left(C_f V_j + \sum_{y=1}^{N_s} C_{s,y} V_j \right) = -\left(C_f \times V_{j+1} + \sum_{y=1}^{N_s} C_{s,y} \times D_{j,y} V_r \right) \tag{2.13}$$

which can be solved to given V_{j+1},

$$V_{j+1} = \left(1 + \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} \right) \times V_j - \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} \times D_{j,y} V_r \tag{2.14}$$

Let the notation C_t is denoted the total capacitance used for acquiring the input at phase 1, thus it is given by

$$C_t = C_f + \sum_{y=1}^{N_s} C_{s,y} \tag{2.15}$$

Then, (2.14) can be rewritten as

$$V_{j+1} = \frac{C_t}{C_f} \left(V_j - \frac{\sum_{y=1}^{N_s} C_{s,y} \cdot D_{j,y}}{C_t} \times V_r \right) \tag{2.16}$$

Furthermore, we can compare (2.16) to (2.1) and obtain that

$$G_j = \frac{C_t}{C_f} = 1 + \frac{\sum_{y=1}^{N_s} C_{s,y}}{C_f} \tag{2.17}$$

$$V_j^{\mathrm{da}}(D_j) = \frac{\sum_{y=1}^{N_s} C_{s,y} \cdot D_{j,y}}{C_t} \times V_r \tag{2.18}$$

From (2.2), it appears that G_j and V_j^{da} directly affect the accuracy of the whole pipelined A/D conversion. Moreover, both (2.17) and (2.18) indicate that they are closely related to the ratio of the sampling capacitors, $C_{s,y}$, and the feedback capacitor, C_f. This implies that the capacitor ratio dominates the accuracy of the conversion in an SC pipelined ADC.

In the following, the major nonidealities presented in the SC implementation of a pipelined ADC are discussed. Assume that the digital correction scheme has been employed in the pipelined ADC's design. Therefore, the thresholds offsets of the sub-ADC here are not further discussed. The investigation is focused on the imperfections of the SC MDAC which is assumed to be implemented with sharing the feedback capacitor.

Since the feedback capacitor, C_f, is shared to be used for acquiring the input signal during the sample phase, the closed-loop gain of the pipeline stage during the hold phase is given by

$$G_j = \frac{C_{s,1} + C_{s,2} + \cdot + C_{s,N_s} + C_f}{C_f} = 1 + \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} \tag{2.19}$$

Assume that the $C_{s,y}$'s and C_f capacitors are independent and identically distributed (i.i.d) random variables, the variance of G_j therefore can be obtained by

$$Var(G_j) = Var\left(1 + \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f}\right) = 0 + \sum_{y=1}^{N_s} \sigma^2_{\Delta C_{s,y}/C_f} \tag{2.20}$$

where $\sigma_{\Delta C_{s,y}/C_f}$ is the standard deviation of the capacitor relative mismatches, and they have typical values from 0.1% to 0.025% for a 1 pF capacitor implemented in a CMOS technology using metal-insulator-metal (MIM) structure.

The operating configurations of MDAC in a pipeline stage here are duplicated in Fig. 2.14. Its operation is similar to that shown in Fig. 2.13, except including the effects of the opamp's finite gain and offset.

During the sample phase, the sampling switch, $S0$, is closed, and thus the inputs of opamp are shorted. The charge at node X therefore is given by (2.11). The parasitic capacitor, C_{pi}, of the opamp's input stores no charge due to the shorted $S0$. During the hold phase, the $Q_{X,s}$ is redistributed. and the charge at node X becomes as

$$Q_{X,h} = \left[\sum_{y=1}^{N_s} C_{s,y}\left(V_X - D_{j,y} \cdot V_r\right)\right] + C_{pi}V_X + C_f(V_X - V_{j+1}) \tag{2.21}$$

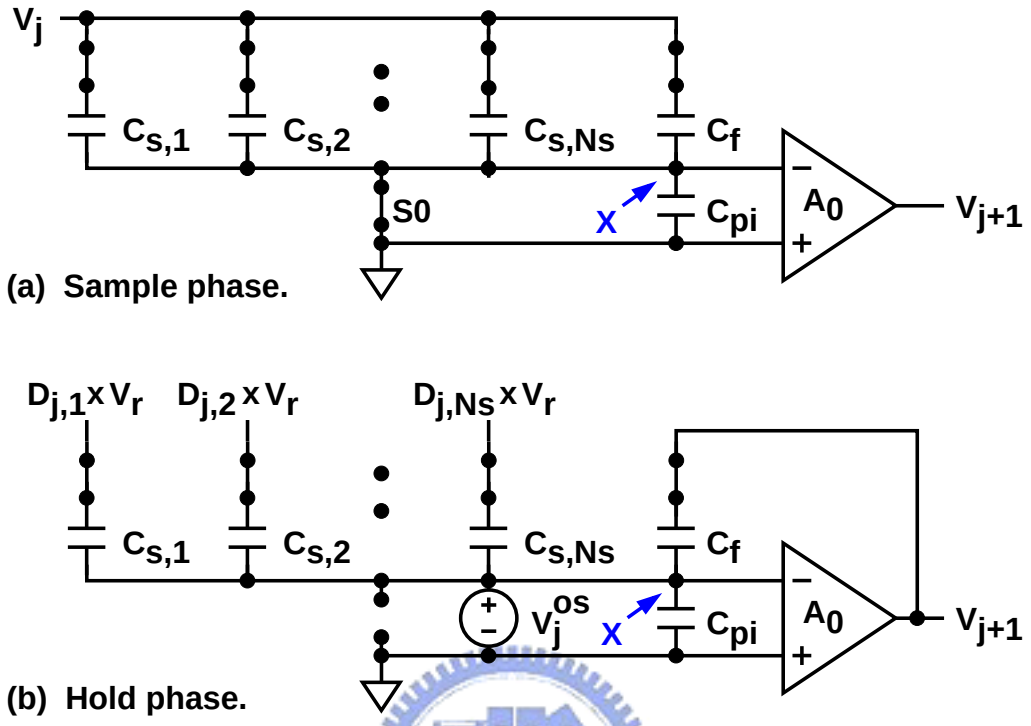


Figure 2.14: Two phase operations of MDAC.

Typically, the I/O relation of the opamp with the finite DC gain A_0 and offset V_{os} is given by

$$V_{j+1} = A_0 \times (0 - V_{os} - V_X) \tag{2.22}$$

thus, the voltage at node X is obtained by

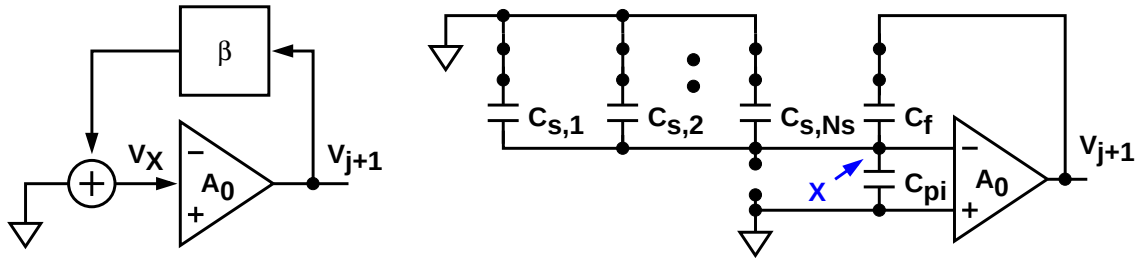
$$V_X = -\left(\frac{V_{j+1}}{A_0} + V_{os}\right) \tag{2.23}$$

Again, according to the charge conservation theorem, equating the expressions (2.21) and (2.11) yields

$$\left[\sum_{y=1}^{N_s} C_{s,y}\left(V_X - D_{j,y} \cdot V_r\right)\right] + C_{pi}V_X + C_f(V_X - V_{j+1}) = -\left(C_f V_j + \sum_{y=1}^{N_s} C_{s,y}V_j\right) \tag{2.24}$$

which gives

$$C_f V_{j+1} = \left(C_f + \sum_{y=1}^{N_s} C_{s,y}\right)V_j - \sum_{y=1}^{N_s} C_{s,y}D_{j,y}V_r + \left(C_{pi} + C_f + \sum_{y=1}^{N_s} C_{s,y}\right)V_X \tag{2.25}$$



(a) A simple feedback system. **(b) Circuit for feedback factor calculation.**

Figure 2.15: Relevant block diagram and circuit for feedback factor calculation.

Then, replacing V_X with (2.23) yields

$$C_f V_{j+1} = \left(C_f + \sum_{y=1}^{N_s} C_{s,y} \right) V_j - \sum_{y=1}^{N_s} C_{s,y} D_{j,y} V_r + \left(C_{pi} + C_f + \sum_{y=1}^{N_s} C_{s,y} \right) \left(-\frac{V_{j+1}}{A_0} - V_{os} \right) \tag{2.26}$$

and solving this for V_{j+1} obtains

$$V_{j+1} = \left(\frac{1}{1+\varepsilon_G} \right) \times \left[\left(1 + \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} \right) V_j - \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} D_{j,y} V_r - (A_0 \times \varepsilon_G) V_{os} \right] \tag{2.27}$$

with

$$\varepsilon_G = \frac{1}{A_0} \cdot \left(\frac{C_{pi} + C_f + \sum_{y=1}^{N_s} C_{s,y}}{C_f} \right) \tag{2.28}$$

which is regarded as the gain error of the pipeline stage caused by the opamp's finite dc gain.

Since the MDAC output feeds back to node X during the hold phase configuration, its relevant block diagram is shown in Fig. 2.15(a) as well as the circuit shown in Fig. 2.15(b). The feedback amount is quantized by the feedback factor β and is given by

$$\beta = \frac{V_X}{V_{j+1}} = \frac{C_f}{C_{pi} + C_f + \sum_{y=1}^{N_s} C_{s,y}} \tag{2.29}$$

Note that the feedback factor is the ratio of the feedback capacitance C_f to the total capacitance at node X, $\left(C_{pi} + C_f + \sum_{y=1}^{N_s} C_{s,y} \right)$, during the hold phase.

Replacing (2.29) into the expression of the gain error of (2.28) yields

$$\varepsilon_G = \frac{1}{A_0 \times \beta} \tag{2.30}$$

and also substituting this for the expression of (2.27) gives

$$V_{j+1} = \left(\frac{1}{1+\varepsilon_G}\right) \times \left[\left(1 + \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f}\right) V_j - \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} D_{j,y} V_r - \frac{V_{os}}{\beta}\right] \tag{2.31}$$

Clearly, the gain accuracy of a stage is closely related to the dc loop gain $A \cdot \beta$ in its closed-loop configuration. Therefore, to maintain the gain accuracy, both the opamp's open-loop dc gain and the feedback factor are considered.

In addition to the finite dc gain, the opamp's finite settling speed also causes error imposed on V_{j+1}. If only the settling error ε_τ is considered, the stage's analog output V_{j+1} of (2.14) is modified as

$$V_{j+1} = (1-\varepsilon_\tau) \times \left[\left(1 + \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f}\right) \times V_j - \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} \times D_{j,y} V_r\right] \tag{2.32}$$

If only consider the exponential settling, the settling error ε_τ at the end of the hold phase is given by

$$\varepsilon_\tau = e^{-\omega_{-3dB} \times T_{on}} \tag{2.33}$$

where T_{on} is the time for exponential settling, and ω_{-3dB} is the -3dB corner frequency of MDAC. Typically, T_{on} is one third of the sampling clock period. The settling error is time-dependent, and thus causes signal-dependent errors. The signal-dependent errors are difficult to be cancelled or calibrated. Therefore, the opamp's speed actually limits the sampling speed of an SC pipelined ADC, and its settling behavior needs be particularly considered.

Thermal noise is also particularly considered in the SC implementations of ADCs required the resolutions higher than 10 bits. Two major error sources result in thermal noises. One is the kT/C noise caused by the sampling switches, and the other are resulted from the opamp's transistors. Here, only kT/C noise is discussed.

The thermal noise from the sampling switch is stored on the sampling capacitors and results in a noise power of

$$n_{kT/C}^2 = \frac{kT}{C_f + \sum_{y=1}^{N_s} C_{s,y}} \tag{2.34}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann's constant, and T is the absolute temperature. If only the kT/C noise is considered, for a sinusoidal signal with an amplitude of $V_{FS}/2$,

the signal-to-noise ratio (SNR) of an SC MDAC is given by

$$SNR_{kT/C} = \frac{V_{FS}^2/8}{n_{kT/C}^2} = \frac{V_{FS}^2\left(C_f + \sum_{y=1}^{N_s} C_{s,y}\right)}{8kT} \tag{2.35}$$

This indicates that the minimum size of the capacitors is determined by the total contribution of kT/C noise which does not degrade the SNR below that resulted from the quantization noise.

2.4 Summary

In this chapter, the operating principles of a pipelined ADC is presented, as well as the corresponding mathematical derivation. The general error sources of a pipeline stage are also examined. Then, the most often used SC implementations and their nonidealities are investigated. Finally, the general mathematical description is given to indicate the limitations of SC pipelined ADC's designs.

For a pipeline stage as shown in Fig. 2.2, the actual transfer function combining with offsets of the subtractor and gain amplifier, sub-DAC errors, and interstage gain errors can be written as

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}}\right] \tag{2.36}$$

with

$$\hat{G}_j = G_j \times (1 - \varepsilon_G) \tag{2.37}$$

$$\hat{V}_j^{\mathrm{da}}(D_j) = V_j^{\mathrm{da}}(D_j) - \Delta V_j^{\mathrm{da}}(D_j) \tag{2.38}$$

whereas the threshold level offsets of the sub-ADC are not included in this equation, since it is difficult to precisely described in mathematics.

For an SC pipeline stage, assume the finite dc gain error ε_G and the settling error ε_τ are considered uncorrelated, as well as the opamp's offset V_{os}. The effect of these errors can be superimposed on the stage's analog output V_{j+1}, and the expression of V_{j+1} is given by

$$V_{j+1} = (1 - \varepsilon_\tau)\left(\frac{1}{1+\varepsilon_G}\right)\left[\left(1 + \sum_{y=1}^{N_s}\frac{C_{s,y}}{C_f}\right)V_j - \sum_{y=1}^{N_s}\frac{C_{s,y}}{C_f}D_{j,y}V_r - \frac{V_{os}}{\beta}\right] \tag{2.39}$$

which is a basis of designing an SC MDAC. Compare (2.39) to (2.36), and hence we have

$$\hat{G}_j = (1-\varepsilon_\tau)\left(\frac{1}{1+\varepsilon_G}\right) \times \left(1+\sum_{y=1}^{N_s}\frac{C_{s,y}}{C_f}\right) \tag{2.40}$$

and

$$\hat{V}_j^{\mathrm{da}}(D_j) = \sum_{y=1}^{N_s} D_{j,y} \cdot \frac{C_{s,y}}{C_f} \times V_r \tag{2.41}$$

Chapter 3

Techniques for Linearity Enhancement

3.1 Introduction

Since ADC's performance is degraded due to the imperfections of the circuit components, lots of techniques have been developed for compensating such degradations. In this chapter, the published methods for improving the linearity of SC pipelined ADCs are investigated and summarized, as well as the proposed technique. Three natures are discussed. They are capacitor error averaging, foreground digital self-calibration, and digital background calibration.

As capacitor mismatch in a SC pipelined ADC is the most important error source of nonlinearity, capacitor error averaging (CEA) techniques have been developed for reducing this error effect. Active CEA (ACEA) can realize excellent linearity with poorly matched capacitors, but requires an extra opamp, capacitors and additional clock phases [13]. More power consumption and circuit complexity are hence added. Passive CEA (PCEA) was presented achieving good linearity without an extra opamp but still requires additional clock phases [1] [14]. Therefore, PCEA techniques conduct low power consumption, but sacrifice little speed due to adding additional clock phases. An alternative technique, DAC and feedback capacitor averaging (DFCA), was presented resulting in high SFDR by simultaneously shuffling the DAC and the feedback capacitors. The DFCA technique requires little analog circuits and no additional clock phases, but requires extra digital hardware [15] [16].

Foreground digital self-calibration techniques are presented to relieve the accuracy requirements of analog circuits by injecting a calibration signal. This kind of technique requires interrupting normal A/D conversion for measuring calibration parameters, and hence is so-called foreground or off-line calibration. DC signals, the white gaussian noise and ramp signals have been presented as the calibration signal to measure calibration parameters. DC signal is the most frequently used [17] [18], especially the threshold levels of a pipeline stage [19] [20] [21] [22] [23]. The reference levels of pipeline stages are also employed as the calibration signal sometimes [24]. White gaussian noise presented in [25] was indicated highly improving ADC's linearity using Matlab simulation, but required an additional white gaussian noise generator. Literature [26] presented a on-chip ramp signal as a calibration signal. Therefore, the design of [26] required to implement a highly accurate ramp signal generator.

Background calibration is developed for considering the reliability for the long term of a pipelined ADC. It can be performed continuously without interrupting normal A/D conversion. Two digital background calibration methods are investigated. They are the equalization-based [27] [28] [29] and correlation-based background calibration [30] [5] [31].

3.2 Capacitor Error Averaging

This section addresses the PCEA technique. Fig. 3.1 presents the schematic and the corresponding timing diagram of a radix-2 1.5-b SC stage employing PCEA. Fig. 3.2 illustrates the operations of the pipeline stage together with the next stage. Four operating phases are required for performing the PCEA. At sampling phase 1, $\phi_1 = 1$ and $\phi_{11} = 1$, the stage first input, $V_{j,1}$, is sampled by C_1. At sampling phase 2, $\phi_1 = 1$ and $\phi_{12} = 1$, the second input, $V_{j,2}$, is sampled by C_2. During hold phase 1, $\phi_{21} = 1$, C_1 is connected in the feedback loop and the first residue output, $V_{j+1,1}$, is generated and sampled by the following stage's sampling capacitor, C_3. During hold phase 2, $\phi_{22} = 1$, C_1 and C_2 are swapped; the second residue output, $V_{j+1,2}$, is produced and sampled by C_4.

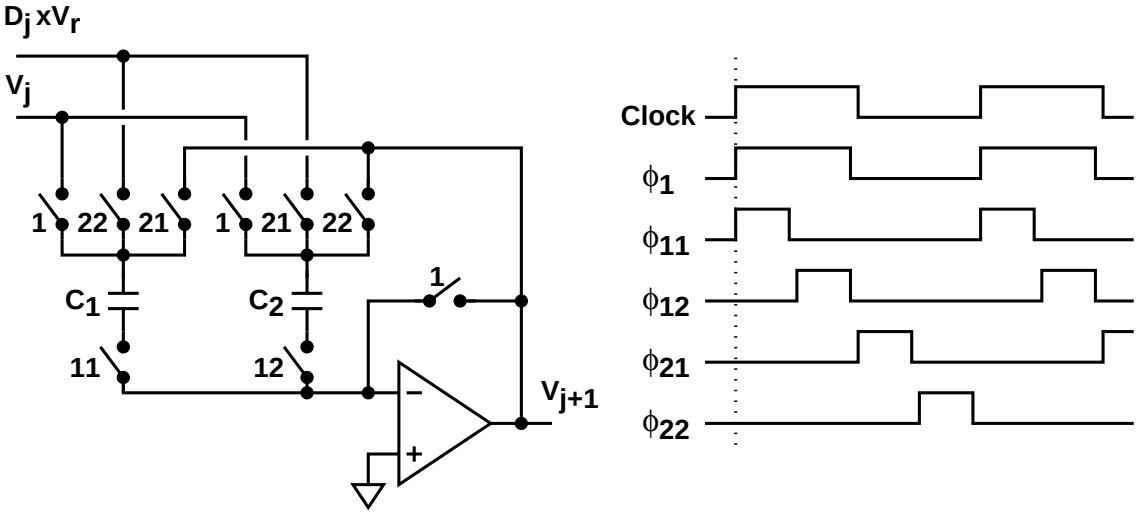


Figure 3.1: A radix-2 1.5-b SC stage with PCEA [1].

Furthermore, $V_{j+1,1}$ and $V_{j+1,2}$ are derived mathematically as follows. First, assume

$$\begin{aligned} C_1 &= C \times (1+\delta_1) \qquad C_2 = C \times (1+\delta_2) \\ C_3 &= C \times (1+\delta_3) \qquad C_4 = C \times (1+\delta_4) \\ V_{j,1} &= V - \Delta V/2 \qquad V_{j,2} = V + \Delta V/2 \end{aligned} \tag{3.1}$$

where δ_1, δ_2, δ_3, and δ_4 are independent random variables with zero mean and variance, σ^2; ΔV is difference of $V_{j,1}$ and $V_{j,2}$; and V is average of $V_{j,1}$ and $V_{j,2}$. According to the charge reservation at the summing node X, we have

$$\begin{aligned} &\text{Hold phase 1:} \quad C_1 \times V_{j,1} + C_2 \times V_{j,2} = C_2(D_j \cdot V_r) + C_1 \times V_{j+1,1} \\ &\text{Hold phase 2:} \quad C_1 \times V_{j,1} + C_2 \times V_{j,2} = C_1(D_j \cdot V_r) + C_2 \times V_{j+1,2} \end{aligned} \tag{3.2}$$

Substituting (3.1) into (3.2) and rearranging the equation of (3.2) obtains

$$\begin{aligned} V_{j+1,1} &\approx (2V - D_j \times V_r) + (\delta_2 - \delta_1)(V - D_j \times V_r) \\ &\quad +\delta_1(\delta_1 - \delta_2)(V - D_j \times V_r) + (\delta_1 - \delta_2)\frac{\Delta V}{2} \\ V_{j+1,2} &\approx (2V - D_j \times V_r) - (\delta_2 - \delta_1)(V - D_j \times V_r) \\ &\quad +\delta_2(\delta_2 - \delta_1)(V - D_j \times V_r) + (\delta_2 - \delta_1)\frac{\Delta V}{2} \end{aligned} \tag{3.3}$$

Furthermore, assume $V_{j,1} = V_{j,2} = V_j$, then, the averaged residue output sampled on C_3

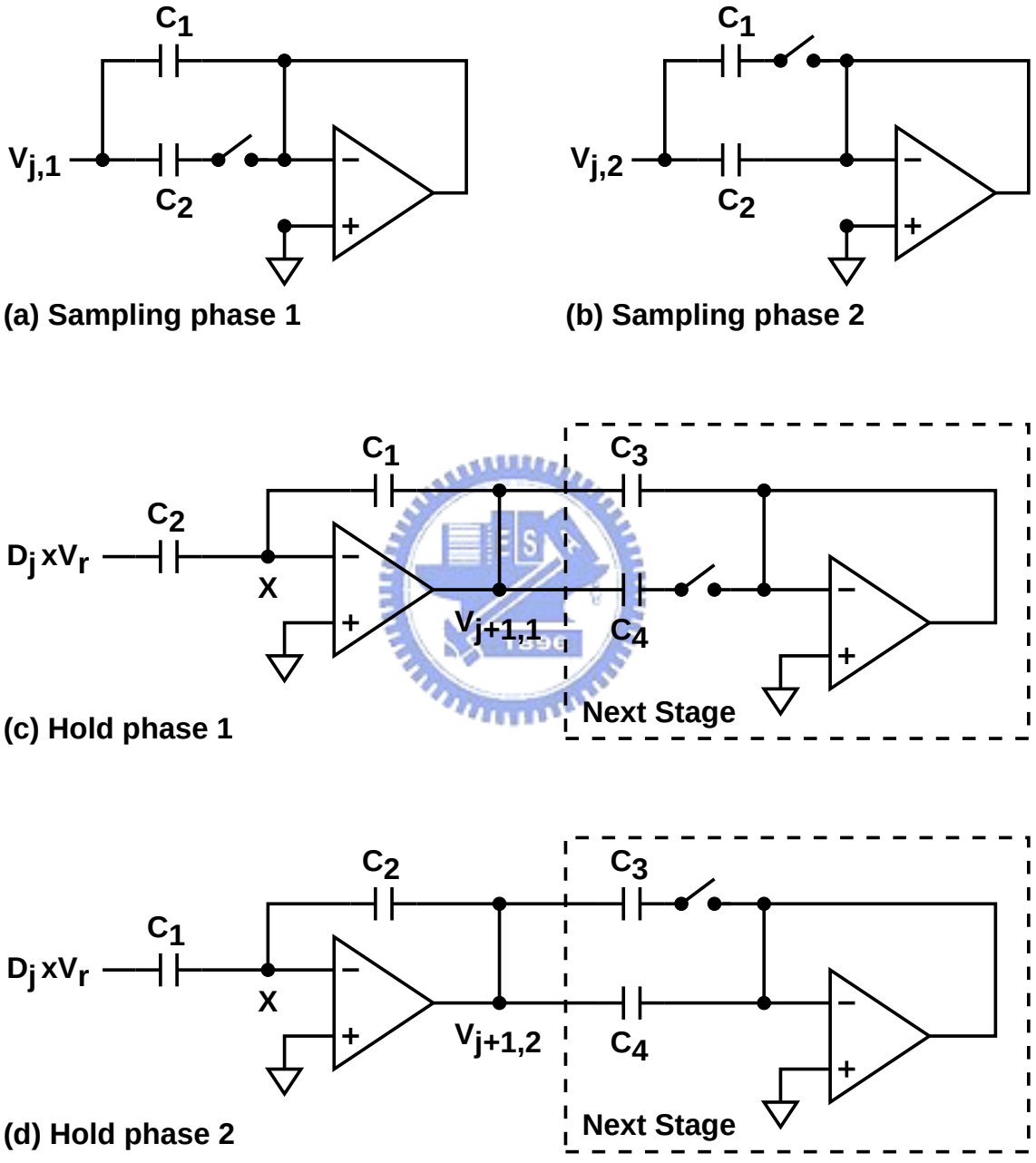


Figure 3.2: Operations of a radix-2 1.5-b SC stage with PCEA [1].

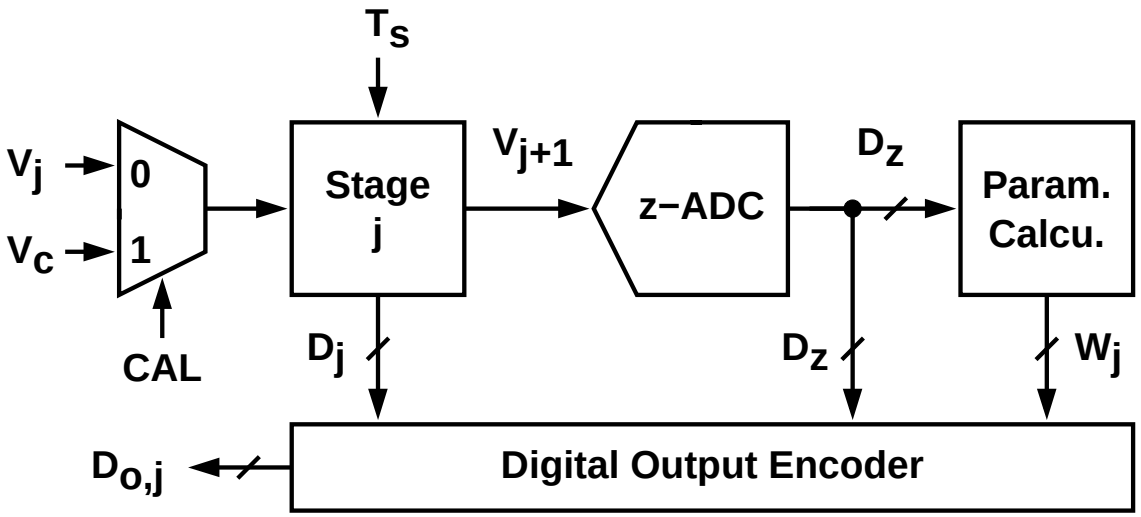


Figure 3.3: Block diagram of foreground digital self-calibration.

and C_4 after charge sharing is given by

$$V_{j+1} = \frac{C_3 V_{j+1,1} + C_4 V_{j+1,2}}{C_3 + C_4} = (2 + \varepsilon_j)V_j - (1 + \varepsilon_j)D_j \times V_r \tag{3.4}$$

where

$$\varepsilon_j = \frac{1}{2}(\delta_1 - \delta_2)(\delta_1 - \delta_2 - \delta_3 + \delta_4)$$

with

$$\begin{cases} E\{\varepsilon_j\} = \sigma^2 \\ \text{var}\{\varepsilon_j\} = 3\sigma^4 \end{cases}$$

It shows that the first order error in the input signal is suppressed to the second order; and hence, employing PECA technique enhances linearity.

3.3 Foreground Digital Calibration

Fig. 3.3 shows the block diagram of foreground digital self-calibration for a pipelined ADC. During calibration phase ($CAL = 1$), the normal A/D conversion is interrupted. During sample phase, the V_c signal is applied to the input of the stage under calibration. During hold phase, the digital test signal, T_s, is applied to the sub-DAC of the stage generate the V_{j+1} output. Then, the V_{j+1} signal is digitized by the following stages named

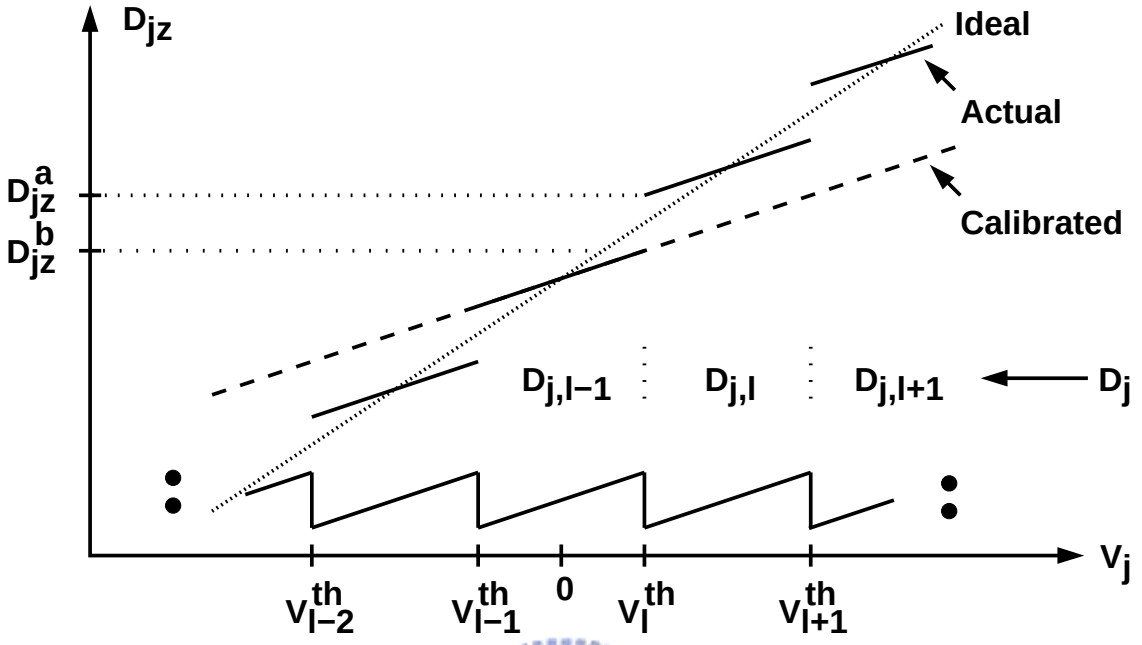


Figure 3.4: Transfer curve of (j+z)-ADC.

as z-ADC, and generates D_z digital output. According to (2.36), the relationship of D_z and V_{j+1} is given by

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}}\right] = \frac{G_z}{\hat{G}_z} D_z + O_z + Q_z \tag{3.5}$$

where $G_z/\hat{G}_z$ is the gain error of z-ADC, O_z is the digital offset, and Q_z is the quantization error of z-ADC. Hence, we have

$$V_{j+1} = \hat{G}_j \times \left[V_c - \hat{V}_j^{\mathrm{da}}(T_s) - V_j^{\mathrm{os}}\right] = \frac{G_z}{\hat{G}_z} D_z + O_z + Q_z \tag{3.6}$$

To evaluate the calibration parameters, the transfer curve of the V_j signal versus its corresponding digital output D_{jz} is shown in Fig. 3.4 as an illustration. When the V_c calibration signal is set as the V_l^{th} threshold level, and T_s is set as the successive decision codes, $D_{j,l-1}$ and $D_{j,l}$ respectively, we have

$$V_{j+1}(D_{j,l-1}) = \hat{G}_j \times [V_l^{\mathrm{th}} - \hat{V}_j^{\mathrm{da}}(D_{j,l-1}) - V_j^{\mathrm{os}}] \tag{3.7}$$

$$V_{j+1}(D_{j,l}) = \hat{G}_j \times [V_l^{\mathrm{th}} - \hat{V}_j^{\mathrm{da}}(D_{j,l}) - V_j^{\mathrm{os}}] \tag{3.8}$$

where $V_{j+1}(D_{j,l-1})$ and $V_{j+1}(D_{j,l})$ represent the stage analog output corresponding to $T_s =$

$D_{j,l-1}$ and $T_s = D_{j,l}$. By subtracting (3.7) from (3.8), we have

$$\left[\hat{V}_j^{\mathrm{da}}(D_{j,l}) - \hat{V}_j^{\mathrm{da}}(D_{j,l-1})\right] + \frac{V_{j+1}(D_{j,l}) - V_{j+1}(D_{j,l-1})}{\hat{G}_j} = 0 \tag{3.9}$$

Rearranging (3.9) obtains the transition height when code $D_{j,l-1}$ transfers to code $D_{j,l}$; the transition height is expressed as

$$\hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_{j,l}) - \hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_{j,l-1}) = V_{j+1}(D_{j,l-1}) - V_{j+1}(D_{j,l}) \tag{3.10}$$

As V_{j+1} is digitized by z-ADC, the transition height can be given in digital form as

$$\hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_{j,l}) - \hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_{j,l-1}) = \frac{G_z}{\hat{G}_z}(D_{z,l-1} - D_{z,l}) + (O_{z,l-1} - O_{z,l}) + (Q_{z,l-1} - Q_{z,l}) \tag{3.11}$$

In reality, the evaluation for a transition height will be iteratively performed hundred of times which are typical power of 2. The digital output codes of these evaluations are accumulated and averaged to obtain the data which are immune of the influence of random noise. Here, define the digital calibration parameter of the j-th stage as $W_j(D_{j,l})$, for all l, and is given by

$$W_j(D_{j,l}) \equiv E\left\{\hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_{j,l})\right\} \tag{3.12}$$

According to (3.11), we have

$$W_j(D_{j,l}) = W_j(D_{j,l-1}) + E\left\{\frac{G_z}{\hat{G}_z}(D_{z,l-1} - D_{z,l}) + (O_{z,l-1} - O_{z,l}) + (Q_{z,l-1} - Q_{z,l})\right\} \tag{3.13}$$

where $E\{\}$ is the evaluation operation of expected value. Evaluating all the calibration parameters, $W_j(D_{j,l})$, for all l, and assume $W_j(0) = 0$ without loosing generality. Then, the calibrated transfer curve of the (j+z)-ADC can be constructed shown as the dash line in Fig. 3.4. Employing this calibrated curve for (j+z)-ADC achieves the digital output, D_{jz}, without the first order errors.

From (3.5), we have

$$V_j = \hat{V}_j^{\mathrm{da}}(D_j) + \frac{V_{j+1}}{\hat{G}_j} + V_j^{\mathrm{os}} = \frac{G_{jz}}{\hat{G}_{jz}} D_{jz} + O_{jz} + Q_{jz} \tag{3.14}$$

With calibration, V_j can be rewritten as

$$V_j = \frac{G_{jz}}{\hat{G}_{jz}}\left[\frac{W_j(D_j) + D_z}{G_j}\right] + O_{jz} + Q_{jz} \tag{3.15}$$

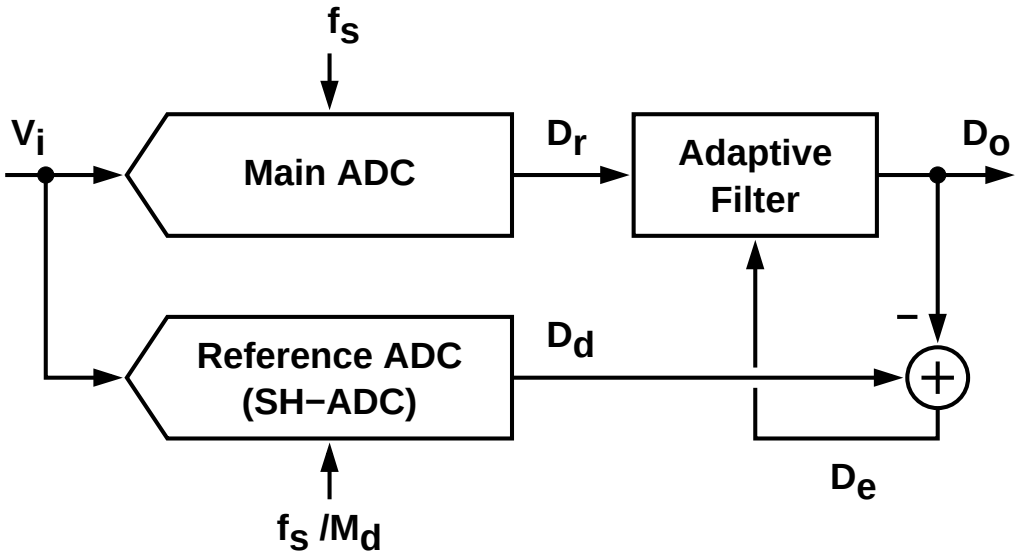


Figure 3.5: Block diagram of equalization-based digital background calibration.

with the gain error

$$\frac{G_{jz}}{\hat{G}_{jz}} = \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \tag{3.16}$$

and O_{jz} is (j+z)-ADC's digital offset; Q_{jz} is quantization error. Furthermore, (j+z)-ADC is used for calibrating the (j-1)-th stage. Calibration is performed toward the front-end pipeline stage until finishing the first stage calibration, and the calibration cycle is completed. All the calibration parameters are stored in memories and used for combining with D_z to generate the final ADC's digital output as the ADC performs normal A/D conversion.

3.4 Background Digital Calibration

The equalization-based (EB) method based on least-mean-square (LMS) algorithm for estimating calibration parameters is discussed here. When an LMS approach is applied for calibration, a desired signal needs to be addressed to adaptively adjust calibration parameters. A slow, high-resolution ADC (SH-ADC) is therefore employed for generating the desired signal.

Fig. 3.5 shows the block diagram of the EB digital background calibration. The input is applied into the main ADC operating at the sample rate of f_s, as well as the reference

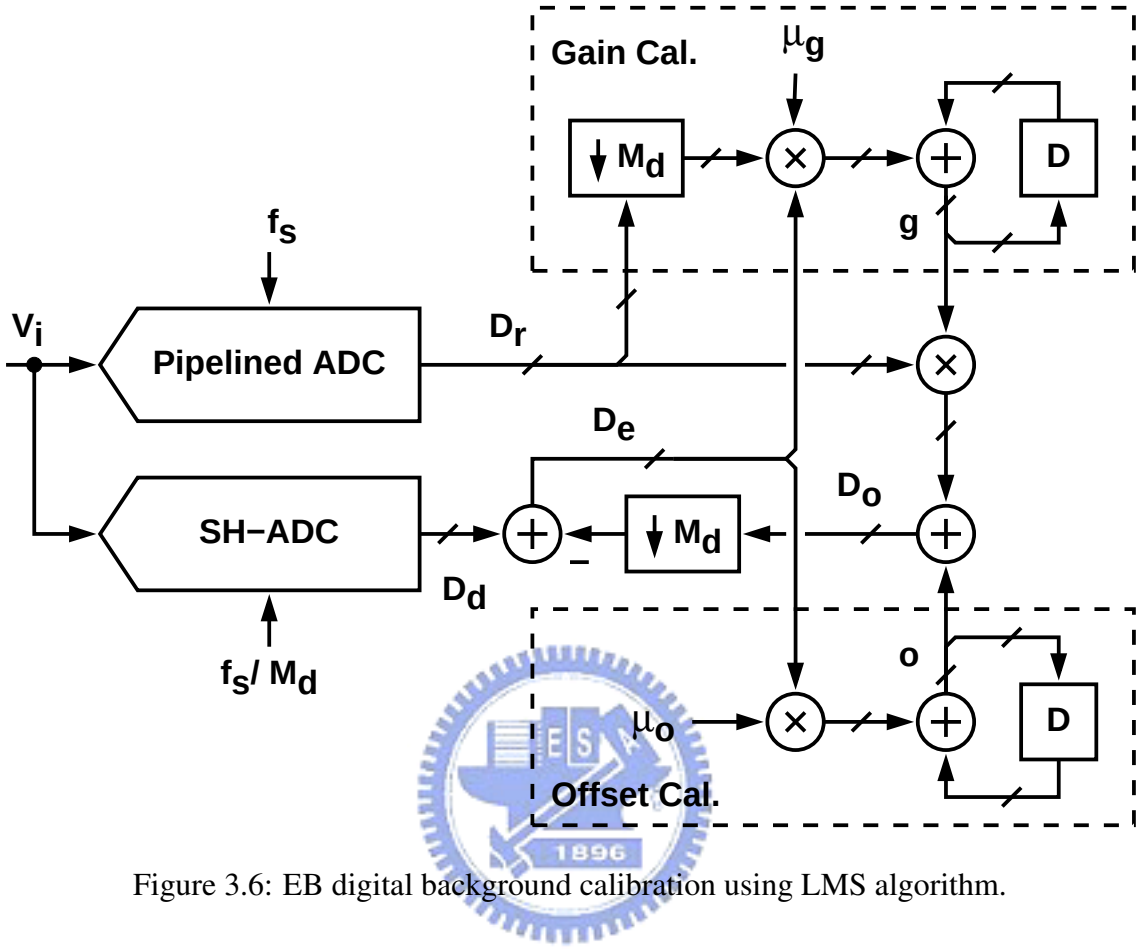


Figure 3.6: EB digital background calibration using LMS algorithm.

ADC operating at much lower sample rate, f_s/M_d. The D_o output is subtracted from the D_d desired output to produce the D_e error signal. This error signal is then fed into the adaptive filter to adjust its parameters to minimize D_e.

Fig. 3.6 shows the block diagram of the EB background calibration using the LMS algorithm. The V_j stage input not only applies into the normal A/D pipes, but also injects to the SH-ADC every M_d clock cycles. The SH-ADC digitizes the stage input and generates the D_d digital desired signal as a reference for the LMS algorithm. Assume the D_r raw digital output is corrected by gain g, and offset error o, and the corrected digital output is obtained by

$$D_o = g \times D_r + o \tag{3.17}$$

where g and o are the calibration parameters determined by LMS adaptive mechanism. The LMS algorithm employed in the adaptive mechanism is summarized below:

1. Initialize the parameters, $(g[0], o[0])$.

2. Calculate error:

$$D_e[n'] = D_d[n'] - D_o[n'] \tag{3.18}$$

3. Adjust parameter $g[n']$ and $o[n']$ as:

$$g[n'] = g[n'-1] + \mu_g \times D_e[n'] \times D_r[n'] \tag{3.19}$$

$$o[n'] = o[n'-1] + \mu_o \times D_e[n'] \tag{3.20}$$

where n' indicates the time index downsampling by M_d; μ_g is the updating step size for gain, and μ_o is the updating step size for offset. When the adjustment is convergent, the LMS algorithm gives a unique desired solution for the parameters g and o. Therefore, the final digital output, D_o, is corrected according to (3.17). A trade-off exists between convergent time and step size for the LMS algorithm. As the convergent time depends on the updating step size, small step size makes long convergent time.

Employing the EB calibration produces the drawbacks that this calibration scheme requires an additional SH-ADC. Therefore,the complexity of analog circuits increases, and so is analog hardware, as well as analog power consumption. In addition, as the SH-ADC is binded at the input, large input loading capacitance appears such that increases the required input driving capability.

Digital background calibration using correlation-based (CB) method is used to improve the entire A/D linearity by applying a test signal, T_s, to the stage under calibration, as shown in Fig. 3.7. The T_s signal is included in the V_{j+1} stage output which is quantized by the backend stages (z-ADC). A digital random sequence which is uncorrelated with the input signal, and has zero mean is typically used as the test signal to dither calibration parameter in analog domain and extract the calibration parameter in digital domain. A simplified model of the stage usder CB calibration is shown in Fig. 3.8. As the q random signal dithers the R_c calibration parameter of the j-th stage, the stage's analog output, V_{j+1}, is given by

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) + V_j^{\mathrm{os}}\right] + q \times R_c \tag{3.21}$$

where assume q is zero mean and is uncorrelated with the input. The widely used dithering signal is the binary-valued pseudo-random sequence, i.e. $q = \{-1, +1\}$.

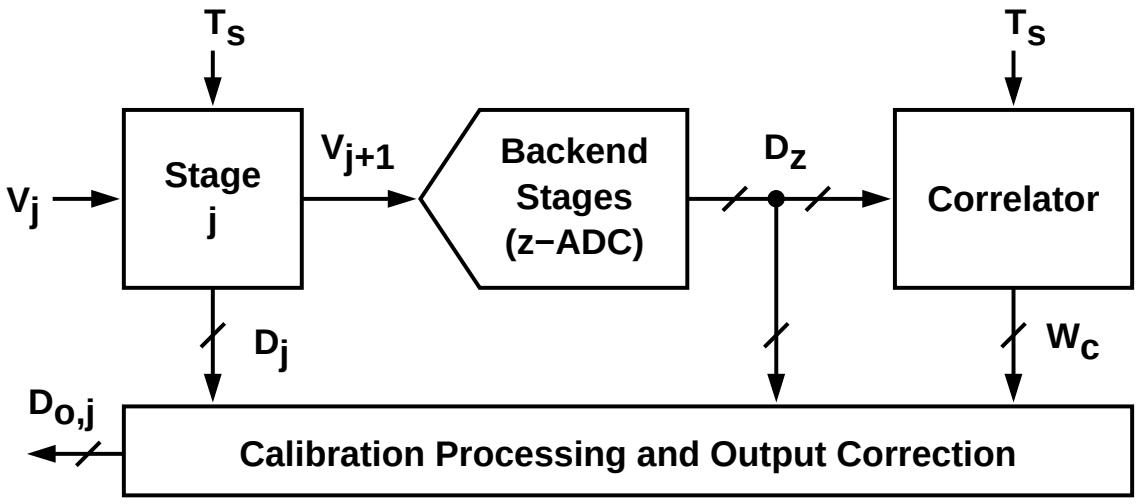


Figure 3.7: Block diagram of calibration employing CB method.

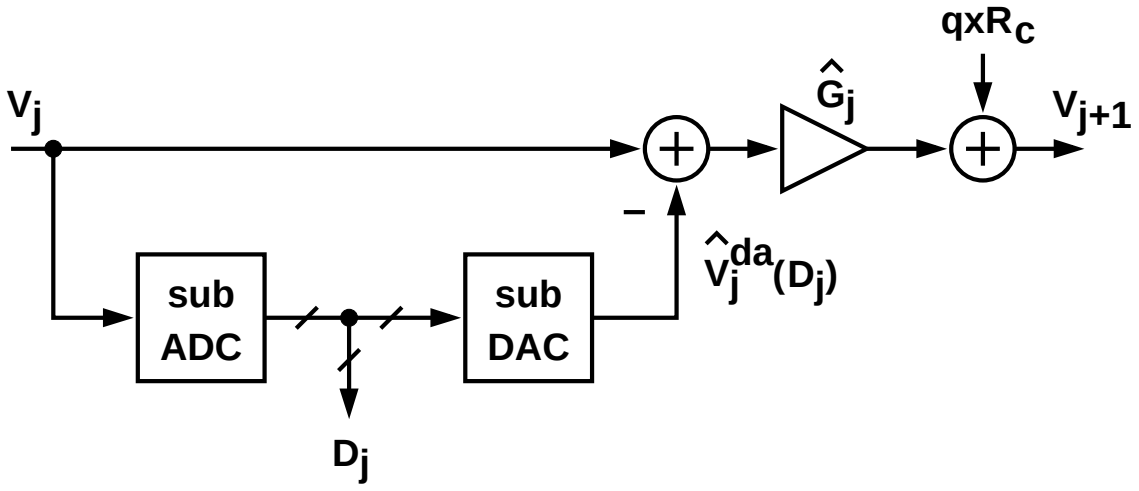


Figure 3.8: Model for the stage under calibration using CB method.

The dithered V_{j+1} is then digitized by the following z-ADC, and generates the digital output, D_z. According to (3.5), the D_z output is given by

$$D_z = \frac{\hat{G}_z}{G_z} \times (V_{j+1} - O_z - Q_z) \tag{3.22}$$

Furthermore, the calibration parameter R_c is extracted based on evaluating the correlation between q and D_z by using a correlation filter. The extracted digital calibration parameter named W_j, is obtained by

$$W_j = E\{q \times D_z\} = E\left\{q \times \left[\frac{\hat{G}_z}{G_z}(V_{j+1} - O_z - Q_z)\right]\right\} = \frac{\hat{G}_z}{G_z}R_c + \text{var}\{W_j\} \tag{3.23}$$

Only $q \times R_c$ shown in (3.21) correlated with q survives after passing the correlation filter. However, since q is pseudo random sequence, variance of W_j appears, and it is denoted as $\text{var}\{W_j\}$ in (3.23). The obtained W_j is used to generate D_{jz}. Then, calibration procedure is performed for (j-1)-th stage; the calibration works toward the first pipeline stage and then iterated from the j-th stage. Finally, calibration parameter for each stage under calibration is obtained, and the entire ADC's digital output is corrected in digital domain.

The major drawback of CB calibration is long calibration time. The calibration time is determined by the resolution requirement of W_j. To achieve a resolution of N_j bits, the extracted W_j needs to satisfy the following condition:

$$10\log_{10}\frac{(\hat{G}_z/G_z) \times R_c}{\text{var}\{W_j\}} \geq 6.02 \times N_j + 1.76 \tag{3.24}$$

where $(6.02 \times N_j + 1.76)$ is the required signal-to-quantization noise ratio (SNR) for achieving N_j-bit resolution. Because of the long calibration time, a pipelined ADC with CB calibration is unsuitable for real-time systems. Therefore, reducing uncorrelated components before extracting W_j was presented that significantly reduced the calibration time by employing the "split-ADC" A/D architecture [30] [32].

3.5 Proposed Background Digital Calibration

A correlation-based method using a binary-valued pseudorandom sequence to dither calibration parameters for an SC pipelined ADC is proposed [4]. This technique requires

only little modification of the analog circuit and simple digital signal processing. It can perform continuously without interrupting normal A/D conversion and achieve significant improvement of the A/D linearity.

To perform the correlation-based calibration, a B_j-bit SC pipeline stage is modified as shown in Fig. 3.9. Comparing the schematic of Fig. 3.9 to the normal B_j-bit SC pipeline stage of Fig. 2.12, the difference is each sampling capacitor, $C_{s,y}$, is split into N small segments, where $C_{s,y} = C_{s,y1} + C_{s,y2} + \cdots + C_{s,yN}$, and the injection of the q pseudo random signal.

The split-capacitor SC configuration also has the two operating phases as the normal case. During sampling phase ($\phi_1 = 1$), its operation is similar to the normal case, and all capacitors sample the V_j input signal. During hold phase ($\phi_2 = 1$), all sampling capacitors are connected to the $D_{j,y} \times V_r$ voltage except that the $C_{s,yi}$ capacitor is connected to the $q \times V_r$ voltage. The stage's analog output of (2.39) therefore becomes as

$$V_{j+1} = (1-\varepsilon_\tau)\left(\frac{1}{1+\varepsilon_G}\right)\left[\left(1+\sum_{y=1}^{N_s}\frac{C_{s,y}}{C_f}\right)V_j - \sum_{y=1}^{N_s}\frac{C_{s,y}}{C_f}D_{j,y}V_r - \frac{V_{os}}{\beta}\right] + D_{j,y}\cdot R_{j,yi} - q\cdot R_{j,yi} \tag{3.25}$$

with

$$R_{j,yi} = (1-\varepsilon_\tau)\left(\frac{1}{1+\varepsilon_G}\right)\times\frac{C_{s,yi}}{C_f}\times V_r \tag{3.26}$$

Calibration of the j-th stage is to measure

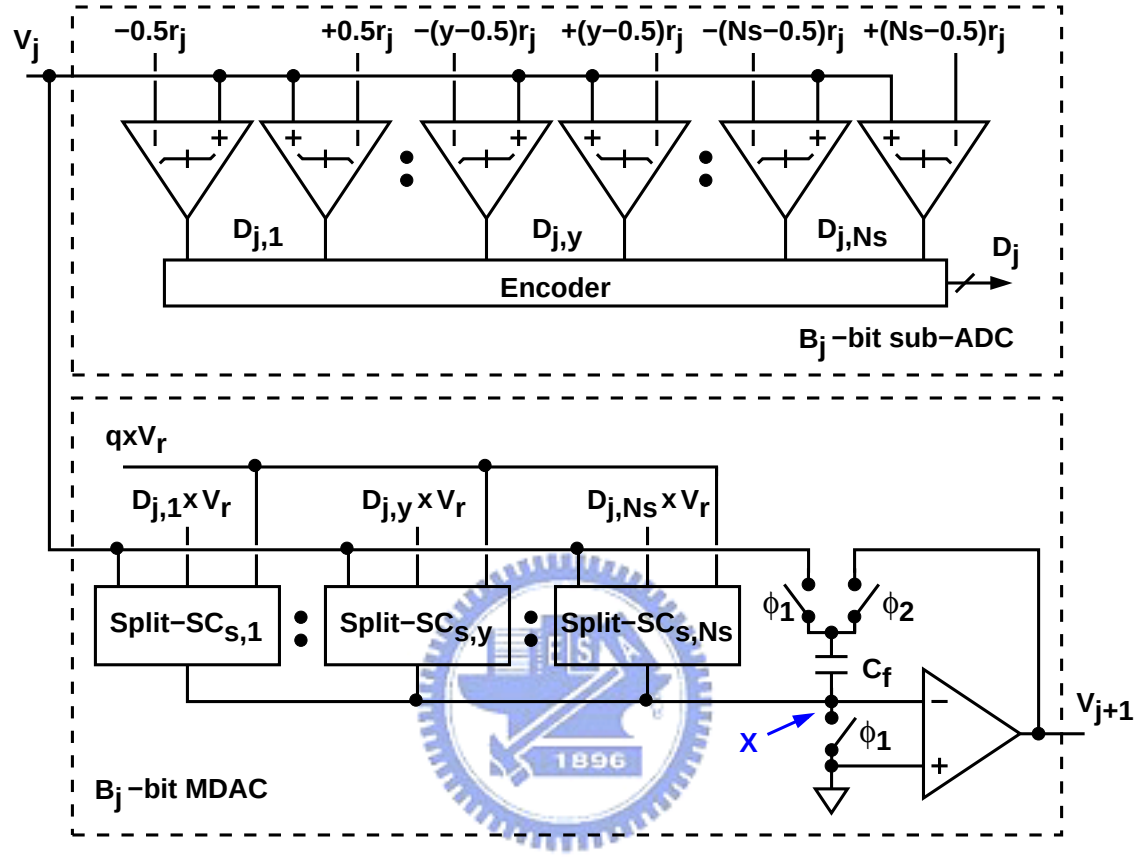
$$R_{j,y}(D_{c,y}) = (1-\varepsilon_\tau)\left(\frac{1}{1+\varepsilon_G}\right)D_{c,y}\cdot\frac{C_{s,y}}{C_f}\times V_r = \sum_{i=1}^{N} D_{c,y}\cdot R_{j,yi} \tag{3.27}$$

where $D_{c,y} \in \{-1, 0, +1\}$. Then

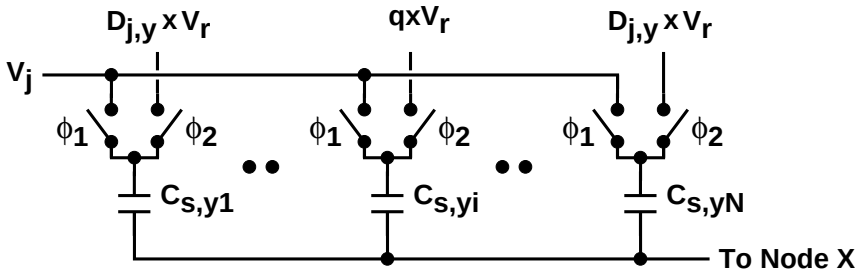
$$R_j(D_c) = \sum_{y=1}^{N_s} R_{j,y}(D_{c,y}) = \sum_{y=1}^{N_s}\left(\sum_{i=1}^{N} D_{c,y}\cdot R_{j,yi}\right) \tag{3.28}$$

where $D_c \in \{-N_s, -(N_s-1), \cdots, 1, 0, +1, \cdots, +(N_s-1), +N_s\}$. This q injection procedure is applied to all $C_{s,yi}$'s capacitors in turn to support the calibration to obtain all $R_{j,yi}$'s, $R_{j,y}$'s and R_j's, for all i and y. To measure $R_{j,y}(+1)$, the value of q alternates between $+1$ and 0. To measure $R_{j,y}(-1)$, q alternates between -1 and 0.

The procedure will be proceeded from the LSB stage to the MSB stage to finish a calibration cycle, and then restart the procedure from the LSB stage. The number of split



(a) SC pipeline stage.



(b) Split−capacitor array of C_Y .

Figure 3.9: A B_j-bit split-capacitor SC pipeline stage.

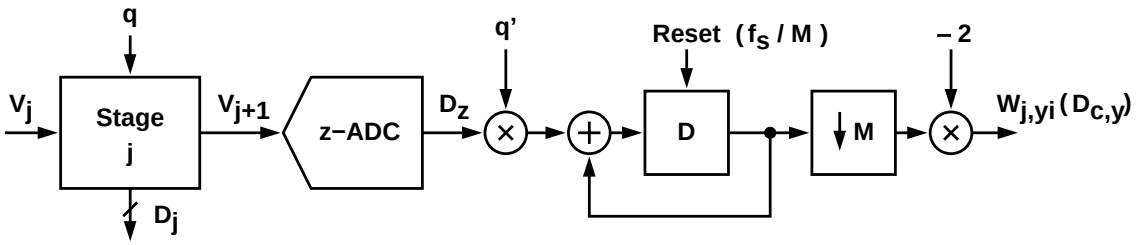


Figure 3.10: Correlation-based parameter extraction.

segments, N, is chosen so that the variation of $q \cdot R_{j,yi}$ of V_{j+1} does not exceed the bounds of the redundant range of the digital correction.

As described in the preceding paragraphs, the injection of the q random signal is done at the input of the SC MDAC to produce the dithered V_{j+1} analog output. The V_{j+1} is then digitized by the following pipeline stages named as z-ADC to generate the D_z digital code as shown in Fig. 3.10. After digitizing, we have

$$V_{j+1} = \frac{G_z}{\hat{G}_z} D_z + O_z + Q_z \tag{3.29}$$

and, hence

$$D_z = \frac{\hat{G}_z}{G_z}(V_{j+1} - O_z - Q_z) \tag{3.30}$$

The D_z code is then correlated with the q random signal. The correlated signal is integrated and then dumped after integrating M samples, where M equals to the length of the q pseudo random sequence. During the correlation, the signal expressed in (3.25) is considered as noise except the $q \cdot R_{j,yi}$ term. (3.25) is therefore rewritten as

$$V_{j+1} = S_j - q \cdot R_{j,yi} \tag{3.31}$$

with

$$S_j = (1 - \varepsilon_\tau)\left(\frac{1}{1+\varepsilon_G}\right)\left[\left(1 + \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f}\right) V_j - \sum_{y=1}^{N_s} \frac{C_{s,y}}{C_f} D_{j,y} V_r - \frac{V_{os}}{\beta}\right] + D_{j,y} \cdot R_{j,yi} \tag{3.32}$$

After the integration and dump, the digital representation corresponding to $R_{j,yi}$ is extracted, named $W_{j,yi}(D_{c,y})$, which is given by

$$W_{j,yi}(D_{c,y}) = \frac{1}{M} \times \sum^{M} \left[q \cdot D_z\right] = \frac{\hat{G}_z}{G_z} R_{j,yi} + \mathrm{var}\{W_{j,yi}\} \tag{3.33}$$

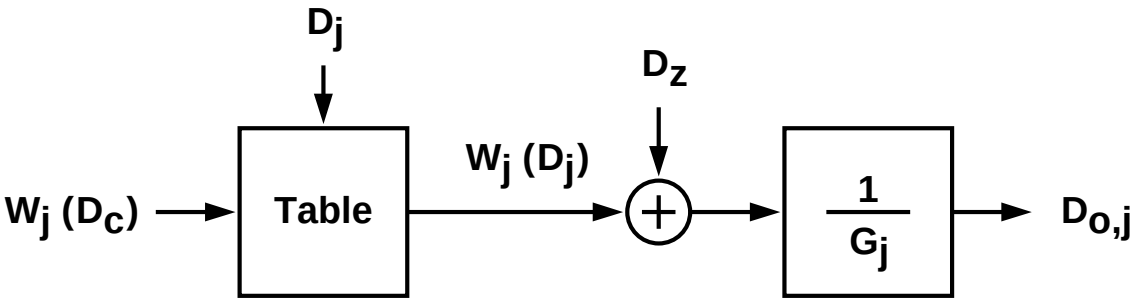


Figure 3.11: $(j+z)$-ADC output encoding.

where

$$\mathrm{var}\{W_{j,yi}\} = \frac{1}{M}\sum^{M}\left[q\cdot\frac{\hat{G}_z}{G_z}\times(S_j - O_z - Q_z)\right] \tag{3.34}$$

which interferes in the extraction of $R_{j,yi}$, and hence makes it less accurate. The $\mathrm{var}\{W_{j,yi}\}$ can be minimized by increasing the value of M. However, increasing M makes a slow extraction.

By summing the $W_{j,yi}(D_{c,y})$'s according to the $D_{c,y}$'s code, the digital weight corresponding to each possible value of D_j digital output can be obtained, and is given by

$$W_j(D_c) = W_j(0) + \sum_{y=1}^{N_s}\sum_{i=1}^{N} W_{j,yi}(D_{c,y}) \tag{3.35}$$

If ignore offset and the $\mathrm{var}\{W_{j,yi}\}$ variance, and the $W_j(0)$ is assumed as 0, then, we have

$$W_j(D_c) = \sum_{y=1}^{N_s}\sum_{i=1}^{N} W_{j,yi} = \frac{\hat{G}_z}{G_z}R_j(D_c) \tag{3.36}$$

which is used for correcting the pipelined ADC's digital output.

After the j-th stage is calibrated, the obtained $W_j(D_c)$, for all D_c, are stored in registers, and are used to correct the digital output corresponding to V_j. Fig. 3.11 shows the digital output encoder of the stage under calibration. The D_j output is used to as an index to extract the corresponding digital weight $W_j(D_j)$ for combining with the D_z code to give the D_{jz} code which is given by

$$D_{jz} = \frac{W_j(D_j) + D_z}{G_j} \tag{3.37}$$

Then, the $(j-1)$-th stage is calibrated, and D_{jz} is used for the extraction of the $W_{j-1}(D_c)$ weight. The calibration is performed from the K-th stage to the first stage

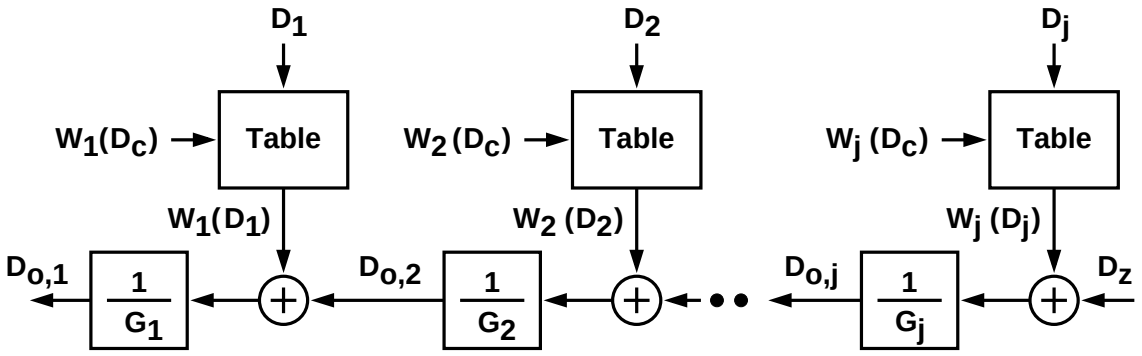


Figure 3.12: ADC's output encoding.

to find all $W_K(D_c)$ weights, for $K = j, j-1, \cdots, 1$. After the calibration of the first stage is finished, next calibration cycle is restarted from $K = j$-th stage, and the obtained $W_K(D_c)$ weights are stored in registers. Then, these weights are used to correct the entire ADC's output code, D_o, as shown in Fig. 3.12, and the D_o output is obtained as

$$D_o = D_{o,1} = \frac{W_1(D_1)}{G_1} + \frac{W_2(D_2)}{G_1G_2} + \cdots + \frac{W_{j-1}(D_{j-1})}{G_1G_2\cdots G_{j-1}} + \frac{W_j(D_j) + D_z}{G_1G_2\cdots G_{j-1}G_j} \tag{3.38}$$

For the pipelined ADC with P stages as shown in Fig. 2.1, the ADC's input, V_1, can be derived from (2.39) and (3.28), and is expressed using R_j as

$$\begin{aligned} V_1 &= \frac{R_1(D_1)}{\hat{G}_1} + \frac{R_2(D_2)}{\hat{G}_1\hat{G}_2} + \cdots + \frac{R_P(D_P)}{\hat{G}_1\hat{G}_2\cdots\hat{G}_{P-1}\hat{G}_P} + \frac{V_{P+1}}{\hat{G}_1\hat{G}_2\cdots\hat{G}_{P-1}\hat{G}_P} \\ &= \sum_{j=1}^{P} \frac{R_j(D_j)}{\hat{G}_1\hat{G}_2\cdots\hat{G}_{j-1}\hat{G}_j} + \frac{V_{P+1}}{\hat{G}_1\hat{G}_2\cdots\hat{G}_{P-1}\hat{G}_P} \end{aligned} \tag{3.39}$$

If the calibration is performed from the LSB stage to the MSB stage of the pipelined ADC, the D_o output is rewritten as

$$\begin{aligned} D_o &= \frac{W_1(D_1)}{G_1} + \frac{W_2(D_2)}{G_1G_2} + \cdots + \frac{W_P(D_P)}{G_1G_2\cdots G_{P-1}G_P} \\ &= \sum_{j=1}^{P} \frac{W_j(D_j)}{G_1G_2\cdots G_{j-1}G_j} \end{aligned} \tag{3.40}$$

According to (3.36), the D_o and V_1 have the relationship as

$$V_1 = \frac{G_1G_2\cdots G_{P-1}G_P}{\hat{G}_1\hat{G}_2\cdots\hat{G}_{P-1}\hat{G}_P} \times D_o + \frac{V_{P+1}}{\hat{G}_1\hat{G}_2\cdots\hat{G}_{P-1}\hat{G}_P} \tag{3.41}$$

Table 3.1: Summary of methods for linearity enhancement

Method	Advantage	Disadvantage
Foreground	• Simple	• Interrupt normal A/D conversion
Capacitor Error Averaging	• Simple • Continuous calibration	• Require extra clock phase • Increase the complexity of MDAC realization • Sensitive to amplifier nonidealities and charge injection
Equalization Based	• Continuous calibration • Fast convergence	• Increase analog design complexity • Create significant analog overhead
Correlation Based	• Simple • Continuous calibration	• Signal range is reduced • Slow calibration

where

$$g_e = \frac{G_1 G_2 \cdots G_{P-1} G_P}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_{P-1} \hat{G}_P} \tag{3.42}$$

is the conversion gain error of the pipelined ADC, and

$$\frac{V_{P+1}}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_{P-1} \hat{G}_P} \tag{3.43}$$

is the overall quantization error. So far, the D_o output is free of the linear errors, and the entire A/D conversion linearity is improved.

3.6 Summary

The characteristics of the calibration methods described in the preceding sections are summarized in Table 3.1. This table can be used as a simple indication, since in most cases the choice of calibration method is application specific. Many applications will not tolerate

data loss, and foreground calibration can not be acceptable. Extra clock phase lowers the ADC's speed, and hence capacitor error averaging technique is unsuitable for high-speed applications. The correlation-based method requires long calibration time, and this problem can be solved by upon start-up initializing a separate foreground calibration routine, and then switch to the correlation-based background calibration as the start-up routine is completed. The proposed calibration method is obviously correlation-based. If neither pauses in normal A/D conversion or long calibration time is acceptable, the equalization-based method is the good alternative.


E
S
A
1896

Chapter 4

Time-Interleaved Analog-to-Digital Converters

4.1 Introduction

This chapter presents an overview of a time-interleaved ADC (TI-ADC), including the concept of time-interleaved sampling, and mismatch error sources. As described in Chapter 2, the sampling speed of SC pipelined ADCs is usually limited by the opamp's performance. Time-interleaving an array of slow ADCs can increase the effective sampling rate [6]. However, the entire A/D conversion linearity will be degraded if there exist mismatches among these ADCs.

A TI-ADC has two primary properties due to the time-interleaving operation. One is that time-interleaved sampling can increase the sampling rate, but not increase the individual ADC's clock rate. This allows for high data rate without increasing each ADC's processing speed. The other is that using time-interleaving A/D architecture makes the ADC's output data easy to be parallel processed, since each ADC can provide its own data stream.

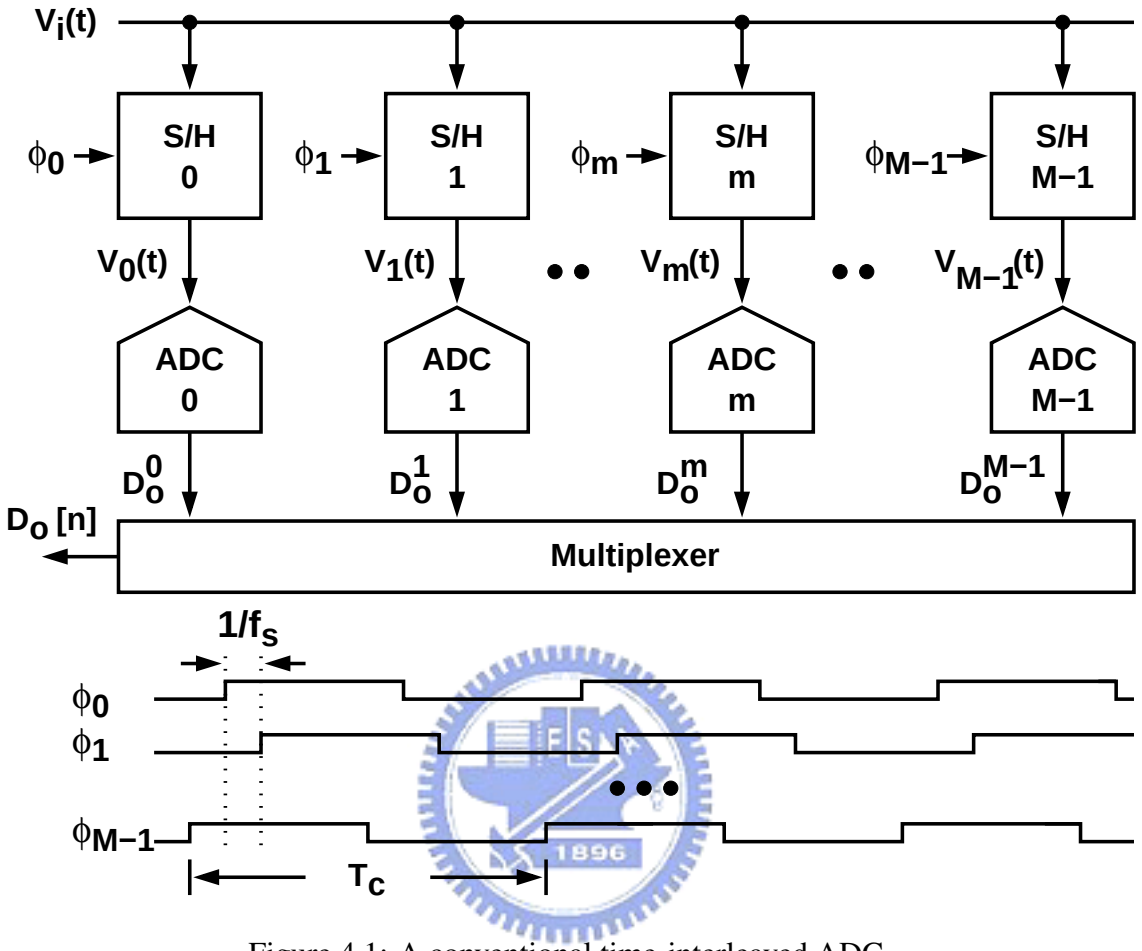


Figure 4.1: A conventional time-interleaved ADC.

4.2 Overview of Time-Interleaved ADCs

A conventional TI-ADC along with its timing diagram is shown in Fig. 4.1, where T_c is the clock period of the individual A/D channel, and its corresponding clock frequency is given by $f_c = 1/T_c$. This TI-ADC consists of M low-speed A/D channels, and hence has an effective sampling rate of $f_s = M \times f_c$. Each channel comprises a sample-and-hold (S/H) circuit and an ADC. In each channel, the analog input, $V_i(t)$, is sampled by the front-end S/H. The sampled signal, $V_m(t)$, is then quantized by the following ADC to produce the digital output, $D_o^m[n]$. The final digital output, $D_o[n]$, of the TI-ADC is obtained by multiplexing $D_o^m[n]$'s. In this figure, t means the continuous-time index, and n means the discrete-time index.

The operation of the front-end S/H is typically modeled as that the $V_i(t)$ input mul-

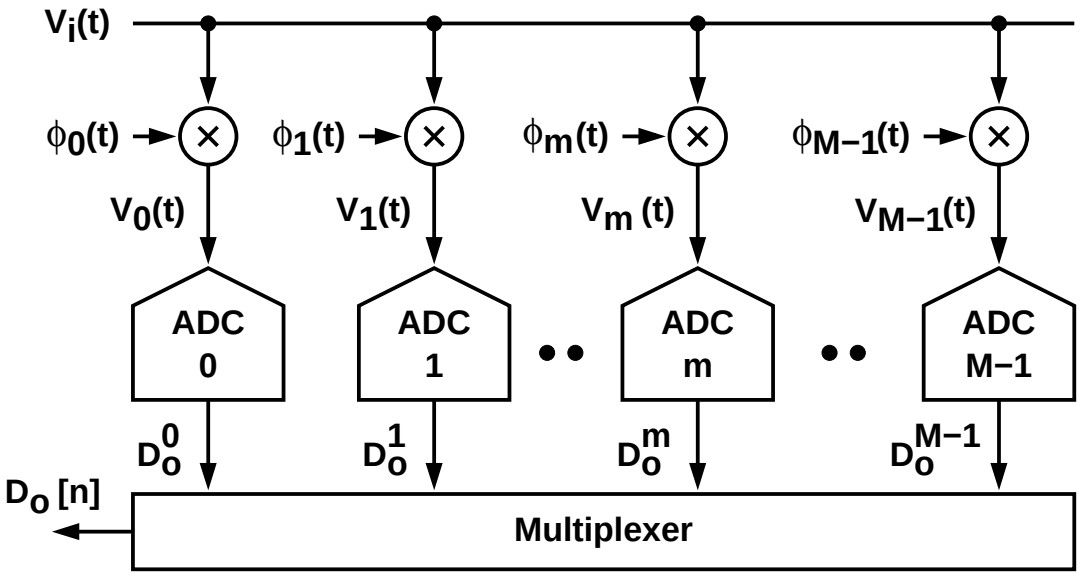


Figure 4.2: The behavioral model of S/H in a TI-ADC.

tiplies with the channel's sampling clock, $\phi_m(t)$, and then produces the discrete output, $V_m(t)$. The model is as shown in Fig. 4.2. The $\phi_m(t)$ sampling signal can be expressed using the delta function, $\delta(t)$, with the sampling period of $T_c = M \times T_s$, where $T_s = 1/f_s$ is the TI-ADC's sampling period. The $\phi_m(t)$ is hence written as

$$\phi_m(t) = \sum_{n=-\infty}^{+\infty} \delta(t - (nM + m)T_s) \tag{4.1}$$

where $m = 0, 1, \cdots, M-1$. Then, the SHA's output, $V_m(t)$, for each m, is therefore given by

$$V_m(t) = V_i(t) \times \phi_m(t) = V_i(t) \times \sum_{n=-\infty}^{+\infty} \delta(t - (nM + m)T_s) \tag{4.2}$$

whose corresponding Fourier transformation (FT) is obtained by

$$\tilde{\mathbf{V}}_m(f) = \tilde{\mathbf{V}}_i(f) * \tilde{\mathbf{\Phi}}_m(f) = \frac{1}{MT_s} \sum_{k=-\infty}^{+\infty} \tilde{\mathbf{V}}_i\left(f - \frac{k}{MT_s}\right) \cdot e^{-j\frac{2\pi km}{M}} \tag{4.3}$$

where $*$ means the convolution operation, $\tilde{\mathbf{V}}_i(f)$ is the FT of $V_i(t)$, and $\tilde{\mathbf{\Phi}}_m(f)$ is the FT of $\phi_m(t)$. If the TI-ADC is a linear system, the overall output spectrum, $\tilde{\mathbf{D}}_o(f)$, can be obtained by linearly adding each channel's output spectrum, $\tilde{\mathbf{D}}_m(f)$, and is given by

$$\tilde{\mathbf{D}}_o(f) = \sum_{m=0}^{M-1} \tilde{\mathbf{D}}_m(f) \tag{4.4}$$

Assume these ADCs are ideal, for all m. Then, the $\tilde{\mathbf{D}}_m(f)$ can be replaced by $\tilde{\mathbf{V}}_m(f)$, and (4.4) can be rewritten as

$$\tilde{\mathbf{D}}_o(f) = \sum_{m=0}^{M-1} \tilde{\mathbf{V}}_m(f) = \sum_{m=0}^{M-1} \left[\frac{1}{MT_s} \sum_{k=-\infty}^{+\infty} \tilde{\mathbf{V}}_i \left(f - \frac{k}{MT_s} \right) \cdot e^{-j\frac{2\pi km}{M}} \right] \tag{4.5}$$

Fig. 4.3 shows the conceptual spectra of a 4-channel TI-ADC. According to the sampling theorem, there are no aliasing as long as the frequency of $V_i(t)$ input is equal or less than half of the fs sampling frequency, and the output spectrum, $\tilde{\mathbf{D}}_o(f)$, periodically repeats the input spectrum, $\tilde{\mathbf{V}}_i(f)$, at the multiplicative frequency of f_s. All channels' spectra have the same magnitude but different phases except those at the multiplicative frequency of f_s. These spectra are shown as the $\tilde{\mathbf{V}}_0(f)$ to $\tilde{\mathbf{V}}_3(f)$ in Fig. 4.3. Ideally, as they are combined into the output, the $\tilde{\mathbf{D}}_o(f)$ output spectrum can exactly repeat the input spectrum at the frequencies of the integral multiples of f_s.

4.3 Nonidealities in Time-Interleaved ADCs

The use of the time-interleaved A/D architecture introduces errors in the sampled signals, which would not appear in a single A/D channel. Sampling time skew, gain and offset mismatches among A/D channels are three major error sources which will distort a TI-ADC's output [33]. In this section, the errors caused by timing mismatch, gain and offset mismatches are discussed by assuming the TI-ADC's sampling rate is f_s, and M channels are time-interleaved. Moreover, a 4-channel TI-ADC is illustrated to describe the mismatch effects on the final ADC's output spectrum.

4.3.1 Timing Mismatch

Timing accuracy of the front-end S/H circuit in each channel is required more crucial than its following ADC, since the S/H circuit proceeds the full bandwidth of the input signal whereas the ADC proceeds the slowly held signal. However, this accuracy is degraded due to the imperfections of the clock generator network in the TI-ADC, the actual turn-off time of the switches in the S/H circuit, and the thermal noise of devices. These imperfections can be categorized into systematic errors and random errors. Systematic errors result

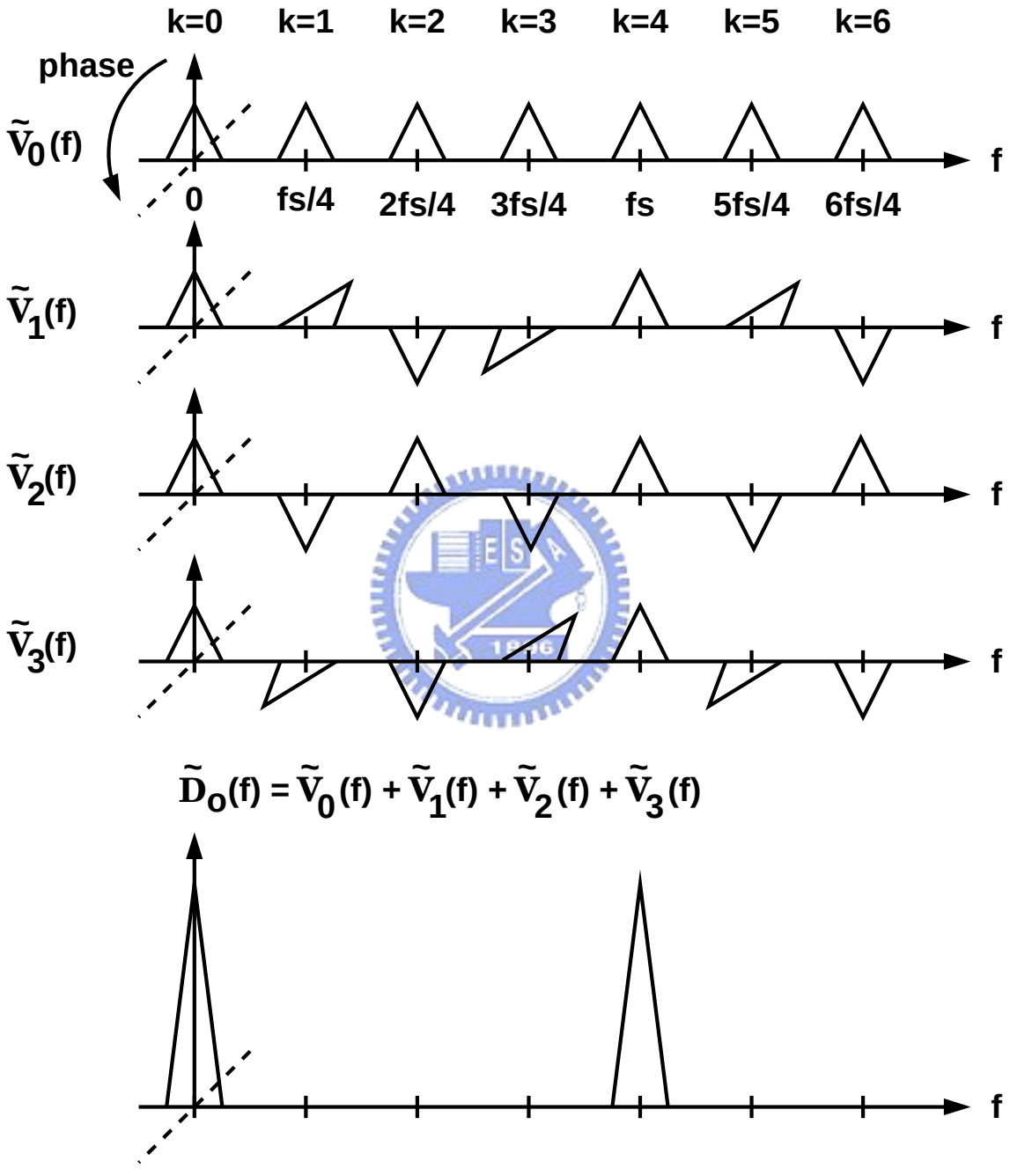


Figure 4.3: Conceptual spectra of a 4-channel TI-ADC.

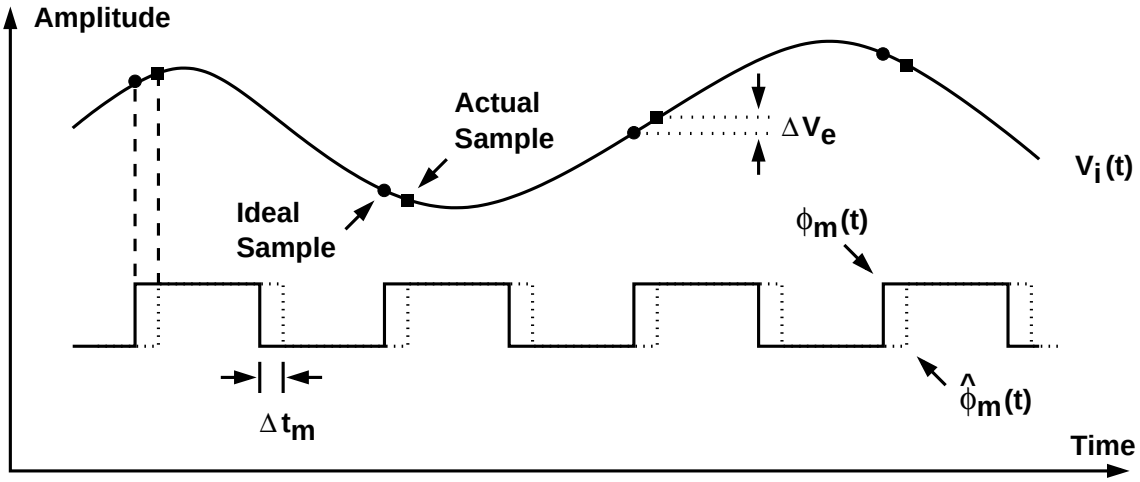


Figure 4.4: Illustration of timing skew effect on the sampled signal.

in frequency dependent distortion in the output spectrum. Random errors resulted from clock jitter and thermal noise can be viewed as the white noise added to the output signal. The random errors cannot be avoided in any circuits, and they are not further discussed in this section.

Systematic timing errors resulted from the clock skews among the A/D channels can be modeled as a time delay Δt_m in the $\phi_m(t)$ sampling function. This mismatch effect on the sampled signal of the m-th ADC can be illustrated as shown in Fig. 4.4. The ideal ϕ_m(t) sampling function shown as the square wave with solid line, and can be rewritten with the skew effect as

$$\hat{\phi}_m(t) = \sum_{n=-\infty}^{+\infty} \delta(t - [(nM + m)T_s + \Delta t_m]) \tag{4.6}$$

represented with the dot-lined square wave, where using $\hat{\phi}$ represents the nonideal case. When $\hat{\phi}$ is used to sample the $V_i(t)$ input, the sampled data will be incurred with the time skew errors, and is shown as the square symbol in Fig. 4.4. The mathematical expression of the sampled data is therefore given by

$$V_{m,\Delta t}(t) = V_i(t) \times \hat{\phi}_m(t) = V_i(t) \times \sum_{n=-\infty}^{+\infty} \delta(t - [(nM + m)T_s + \Delta t_m]) \tag{4.7}$$

Furthermore, we have the output spectrum of the TI-ADC affected by the time skew given

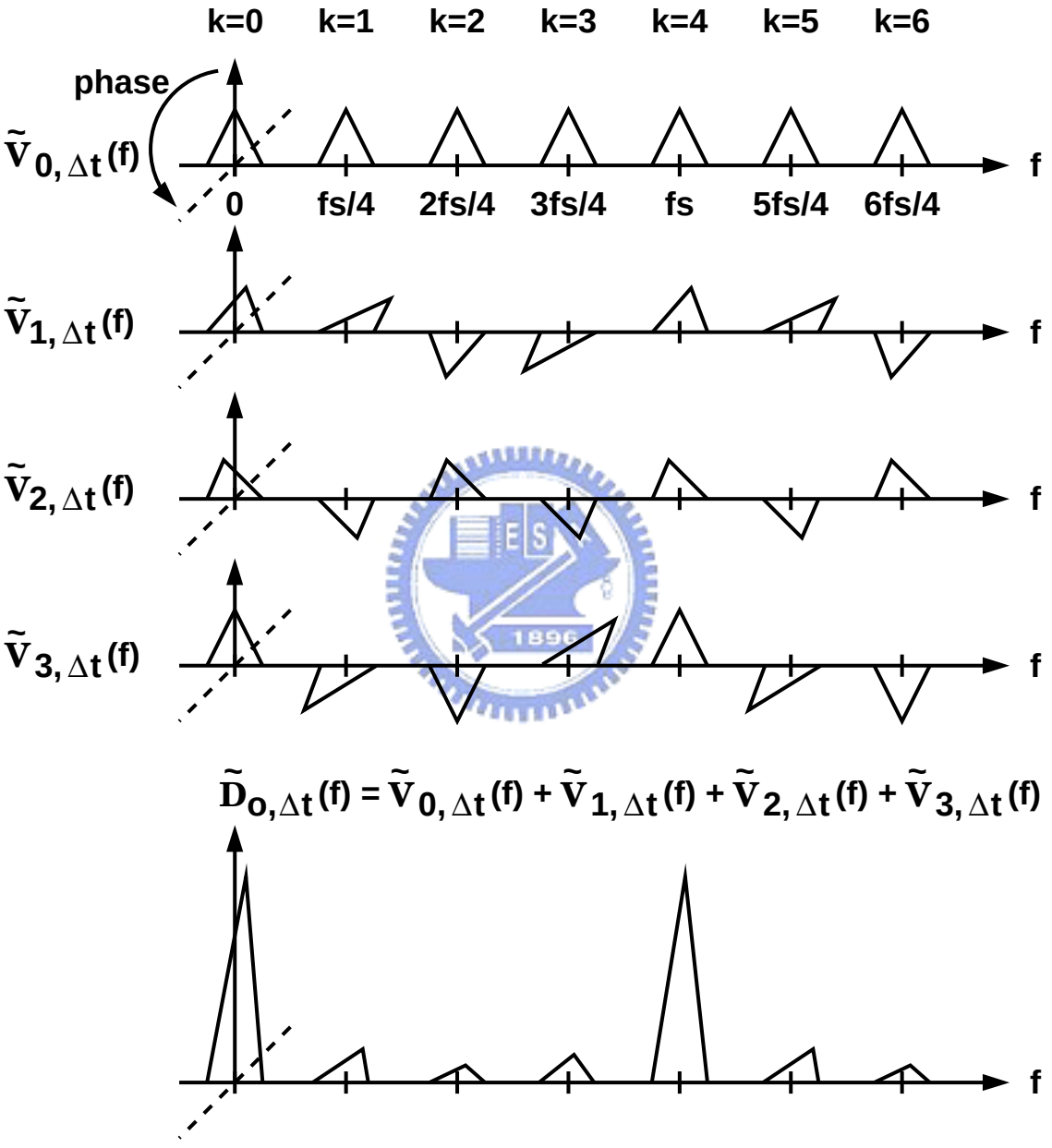


Figure 4.5: Conceptual spectra of a 4-channel TI-ADC with sampling skew mismatch.

as:

$$\tilde{\mathbf{D}}_{o,\Delta t}(f) = \sum_{m=0}^{M-1} \tilde{\mathbf{V}}_{m,\Delta t}(f) = \sum_{m=0}^{M-1} \left[\frac{1}{MT_s} \sum_{k=-\infty}^{+\infty} \tilde{\mathbf{V}}_i \left(f - \frac{k}{MT_s} \right) \cdot e^{-j\frac{2\pi k(mT_s+\Delta t_m)}{MT_s}} \right] \tag{4.8}$$

Comparison of (4.8) and (4.5) shows that the first one has an extra term of $e^{\left(-j\frac{2\pi k \Delta t_m}{MT_s}\right)}$. If the Δt_m time skew is a constant, it causes an effective gain error in the sampled signal of the individual A/D channel. If there exist mismatches in Δt_m's, they cause distortions at the frequency locations of k_t/MT_s in the TI-ADC's output spectrum except the multiples of $1/T_s$, where k_t is an integer.

The conceptual spectra of a 4-channel TI-ADC interfered with sampling time skew in A/D channels are sketched in Fig. 4.5. If the 2nd and the 3rd A/D channels have sampling time skew, their output spectra incur phase errors. When they are combined into the final ADC's output, these errors will reflect on the output spectrum. Finally, they result in the gain error of magnitude and the phase shift in the output spectrum, $\tilde{\mathbf{D}}_{o,\Delta t}(f)$.

4.3.2 Gain Mismatch

The gain effect of the m-th channel in a TI-ADC can be modeled as a multiplication of the input signal $V_i(t)$ with a gain factor of g_m, for all $m = 0, 1, \cdots, M-1$, as shown in Fig. 4.6. A multiplier added in the front of the S/H circuit in each channel is used to model the gain factor. Ideally, $g_0 = g_1 = \cdots = g_{M-1} = 1$.

Assume the linear gain factor is only considered. The sampled signal of the S/H output is therefore modified as

$$V_{m,g}(t) = g_m \times V_i(t) \times \phi_m(t) = g_m \times V_i(t) \times \sum_{n=-\infty}^{+\infty} \delta(t - (nM + m)T_s) \tag{4.9}$$

for all $m = 0, 1, \cdots, M-1$. In this model, the S/H of the m-th channel samples $g_m \times V_i(t)$ rather than $V_i(t)$. Fig. 4.7 shows an illustration of gain error influenced on the sampled signal. Due to the gain error, the sampled data have ΔV_e different from the nominal case as shown in the figure. This will result in insufficient D_o^m output codes, and missing codes will appear in the final digital output.

In the frequency domain, the nonideal gain will distort the final output spectrum. Assume g_m is constant, for all m. The mathematical expression of the final output spectrum

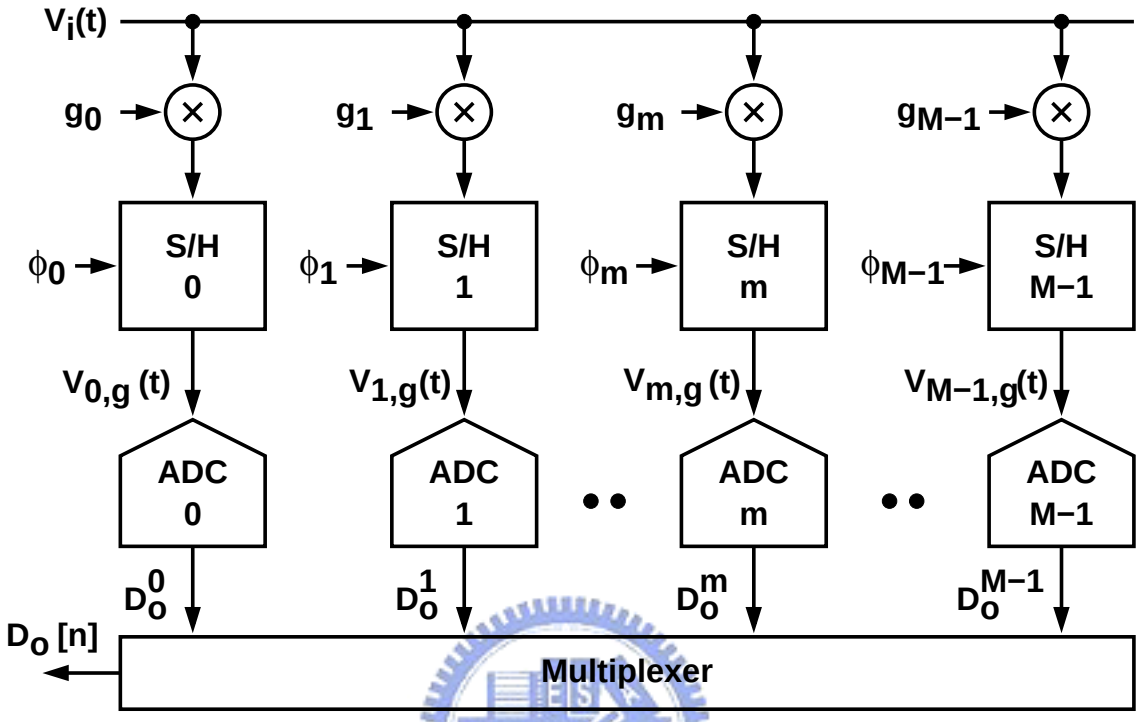


Figure 4.6: Model of A/D channel's gain factor in a TI-ADC.

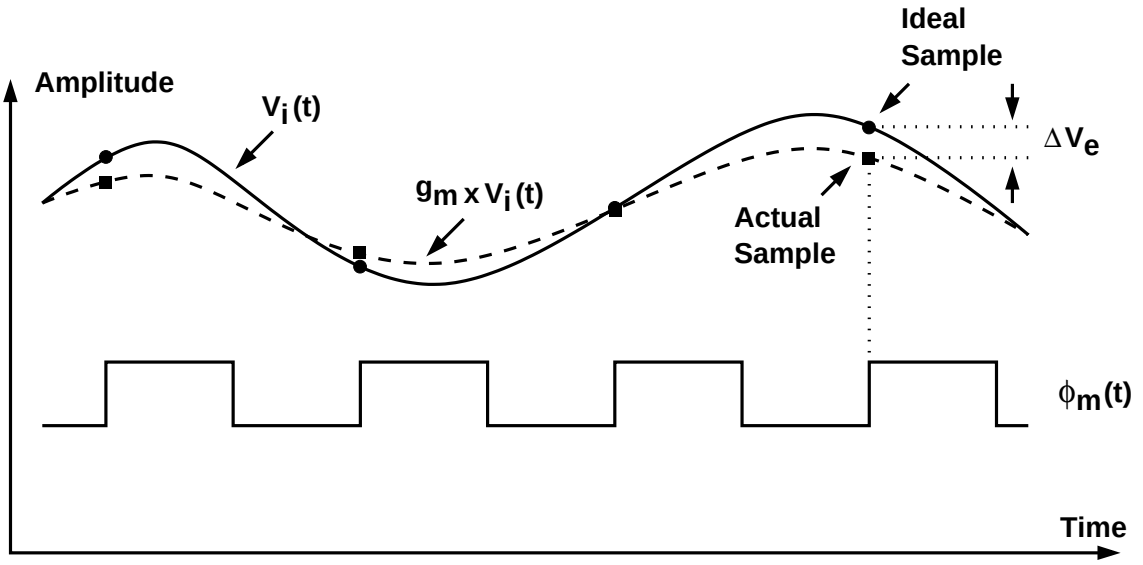


Figure 4.7: Illustration of gain error effect on the sampled data.

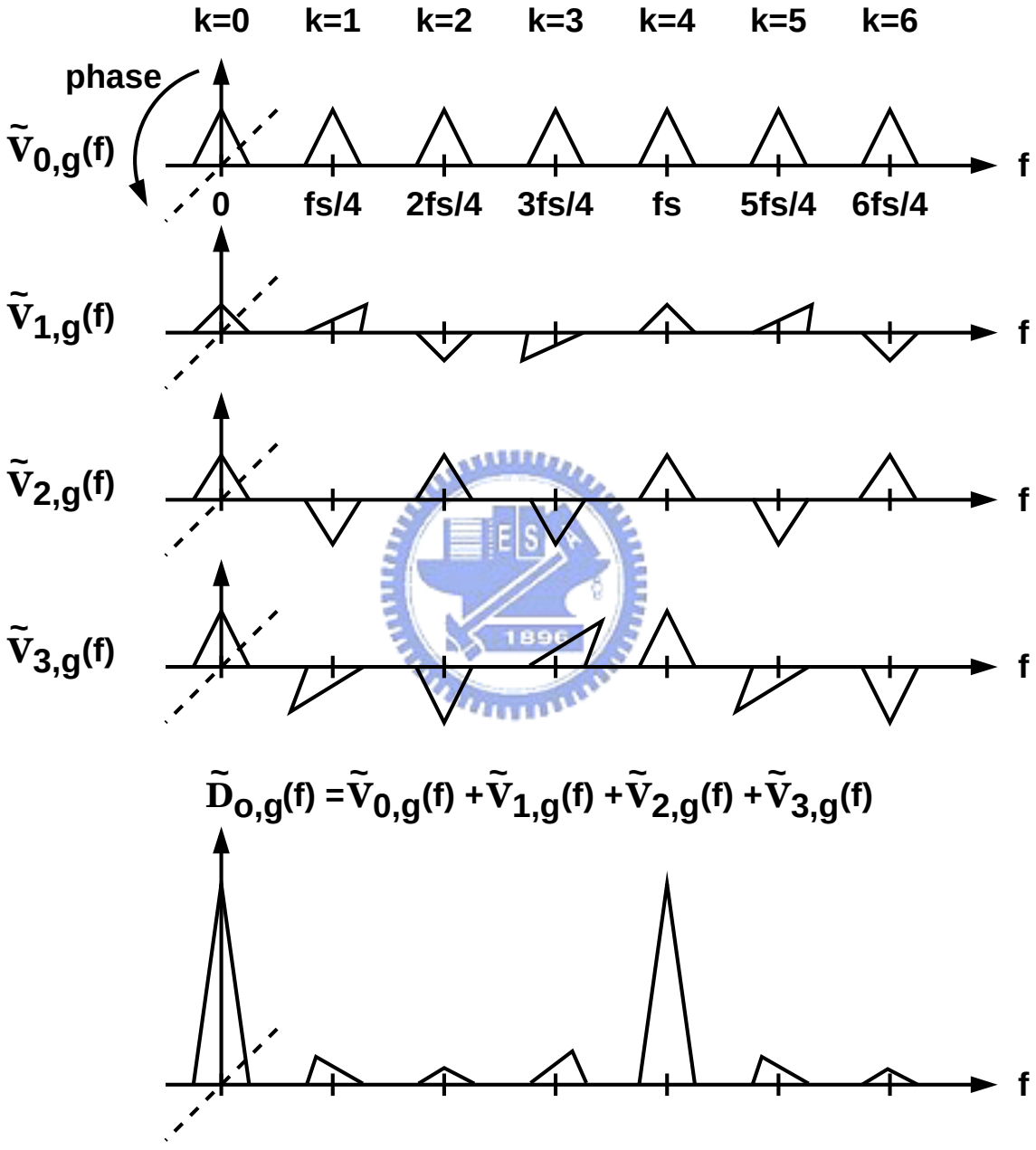


Figure 4.8: Conceptual spectra of a 4-channel TI-ADC with gain effect.

with nonideal gain is therefore given by

$$\tilde{\mathbf{D}}_{o,g}(f) = \sum_{m=0}^{M-1} \tilde{\mathbf{V}}_{m,g}(f) = \sum_{m=0}^{M-1} \left[\frac{g_m}{MT_s} \sum_{k=-\infty}^{+\infty} \tilde{\mathbf{V}}_i \left(f - \frac{k}{MT_s} \right) \cdot e^{-j\frac{2\pi k m T_s}{MT_s}} \right] \tag{4.10}$$

Compare (4.10) to (4.5), an additional g_m factor appears in the spectrum. The spectral magnitude is scaled by g_m. If there are mismatches among g_m's, the spectral images of the D_o output can not be completely eliminated. Hence, spurious distortions will appear at the same frequency locations as the spurs resulted from the sampling time skew. A 4-channel TI-ADC is used as an example to illustrate this influence.

The conceptual spectra of a 4-channel TI-ADC is drawn in Fig. 4.8. If the 2nd and the 3rd channels have gain error, the magnitude of their spectrum, $\tilde{\mathbf{V}}_{1,g}(f)$ and $\tilde{\mathbf{V}}_{2,g}(f)$, are scaled down with their gain factor respectively. This makes the $\tilde{\mathbf{D}}_{o,g}(f)$ output spectrum has spurs at the frequencies of $k_g \times f_s/M$ excluding those of multiples of f_s, where k_g is an integer. The overall A/D linearity is therefore degraded.

4.3.3 Offset Mismatch

Offset effects on a TI-ADC are investigated here by modeling it as a constant signal, o_m, added into the input signal at the front of the S/H circuit. Since other non-ideal effects are not considered, this model is shown in Fig. 4.9. The S/H samples the $V_i(t) + o_m$ signal. Its output is therefore given by

$$V_{m,os}(t) = [V_i(t) + o_m] \times \phi_m(t) = [V_i(t) + o_m] \times \sum_{n=-\infty}^{+\infty} \delta(t - (nM + m)T_s) \tag{4.11}$$

for all $m = 0, 1, \cdots, M-1$. Equation 4.11 indicates that the S/H samples not only the input signal $V_i(t)$, but also the offset o_m. Fig. 4.10 illustrates the offset effects on the sampled data. Due to the offset, the actual sampled data compared to the ideal case have errors with a constant amount of $\Delta V_e = o_m$. This also causes insufficient D_o^m codes of the m-th channel output, and hence, results in missing codes in the final digital output.

The TI-ADC's output spectrum incurred by offset becomes as

$$\tilde{\mathbf{D}}_{o,os}(f) = \sum_{m=0}^{M-1} \left\{ \frac{1}{MT_s} \sum_{k=-\infty}^{+\infty} \left[\tilde{\mathbf{V}}_i \left(f - \frac{k}{MT_s} \right) + o_m \times \delta \left(f - \frac{k}{MT_s} \right) \right] \cdot e^{-j\frac{2\pi k m T_s}{MT_s}} \right\} \tag{4.12}$$

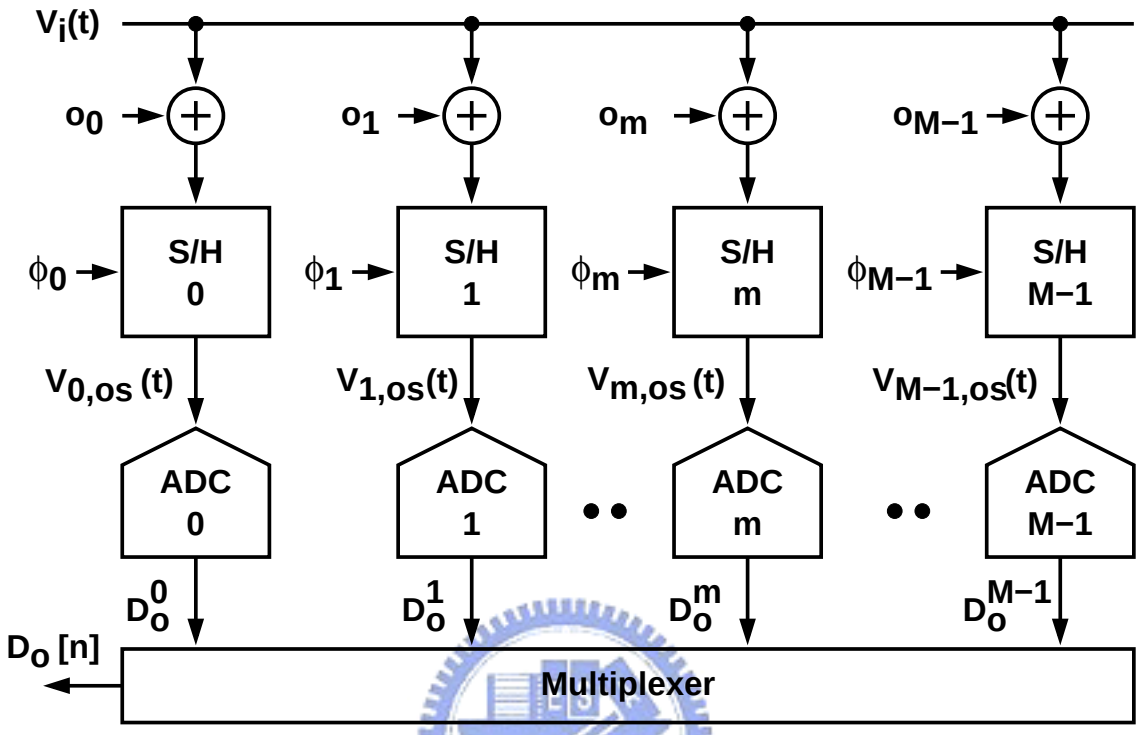


Figure 4.9: Model of offset in a TI-ADC.

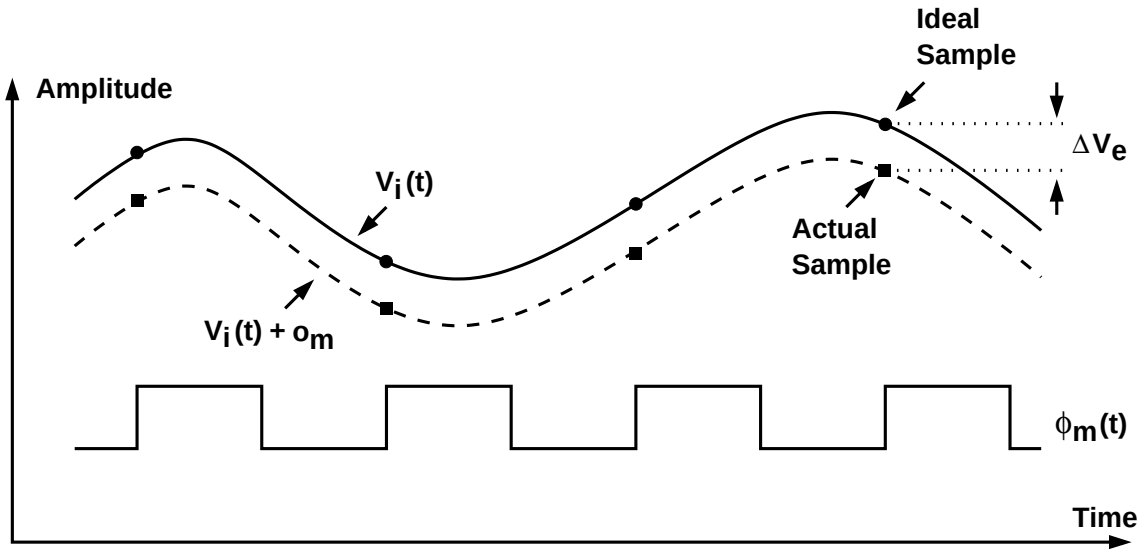


Figure 4.10: Illustration of offset error effect on the sampled data.

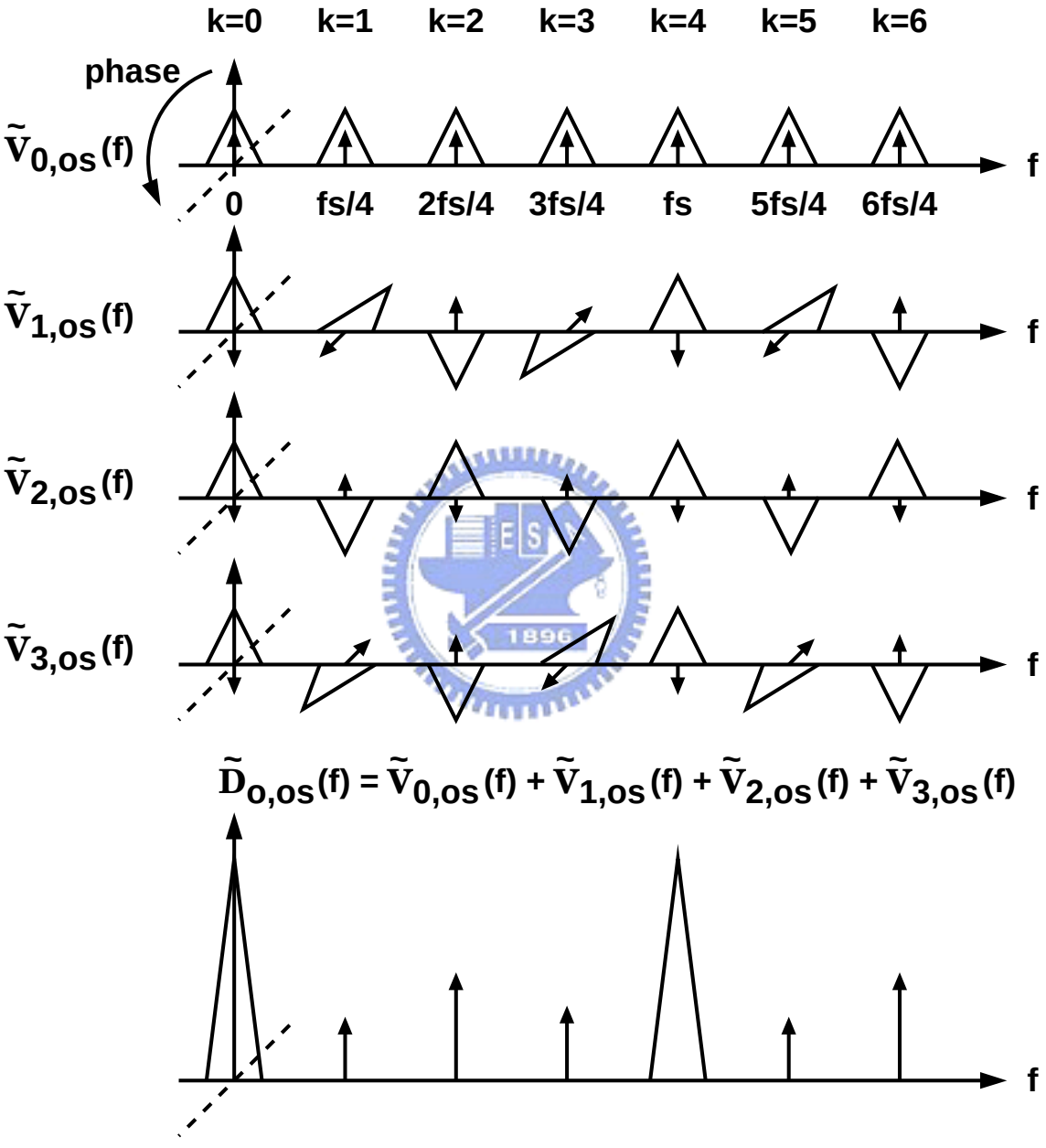


Figure 4.11: Conceptual spectra of a 4-channel TI-ADC with offset.

The offset of each channel causes a constant impulse spectrum independent of the input signal exactly at the frequencies of k_o/MT_s which interferes the signal spectrum at the same frequencies, where k_o is an integer. If there exist offset mismatches among the channels, the final TI-ADC's output spectrum will be disturbed with the spectrum of the offset. This is illustrated with the conceptual spectrum of a 4-channel TI-ADC as shown in Fig. 4.11. These mismatches result in incomplete cancellation of the spurs in the TI-ADC's output spectrum at these frequencies of $k_o \times f_s/4$ except the multiples of f_s, and can cause dramatic degradation in the overall A/D linearity.

4.4 Summary

Using time-interleaving technique can increase the effective sampling rate, but timing, gain and offset mismatches among the interleaved channels result in dynamic degradation. This chapter overviews the time-interleaved A/D architecture, and discusses these mismatch effects. The mathematical expressions of the operation principles of the time-interleaved A/D conversion are also drawn.

As described in the preceding section, the timing and gain mismatch errors contribute to the image spurs distorted the final output signal spectrum at the same frequency locations. The offset spurs generated by the offset mismatches among A/D channels are independent of the input signal. Therefore, for a given offset mismatch, the offset spurs will always at the same level.

To design a TI-ADC, channel-to-channel matching requirements at high-resolution levels (> 12 bits) are not easily achievable. Hence, many approaches were proposed to reduce these mismatch errors. In particular, the digital background calibration techniques are flexible in their implementation. A variety of techniques for reducing time-interleaving mismatch error will be discussed in the following chapter.

Chapter 5

Techniques for Reducing Time-Interleaving Mismatch Errors

5.1 Introduction

Time-interleaved pipelined A/D architecture can achieve high resolution and sampling rate. However, the unavoidable channel mismatches discussed in Section 4.3 indeed degrade the performance of A/D conversion. If the mismatch errors are systematic, they can be reduced by employing calibration techniques, and hence improve the entire A/D linearity. In this chapter, four techniques for reducing the spurious distortions will be discussed. According to their natures, they are categorized into foreground calibration, equalization-based calibration, the randomly time-interleaving, and the developed calibration method.

5.2 Foreground Calibration

The block diagram of a M-channel TI-ADC with the foreground calibration is shown in Fig. 5.1, where D_{ro}^{m} is the offset, and G_{c}^{m} is the gain correction factor in digital domain. The calibration operation is similar to the foreground method for pipelined ADCs described in Section 3.3. It also requires an extra calibration phase controlled by the CAL signal, and will take the TI-ADC out of the normal A/D conversion as starting calibration. Therefore, the foreground calibration typically is enabled at the power-on. During the calibration

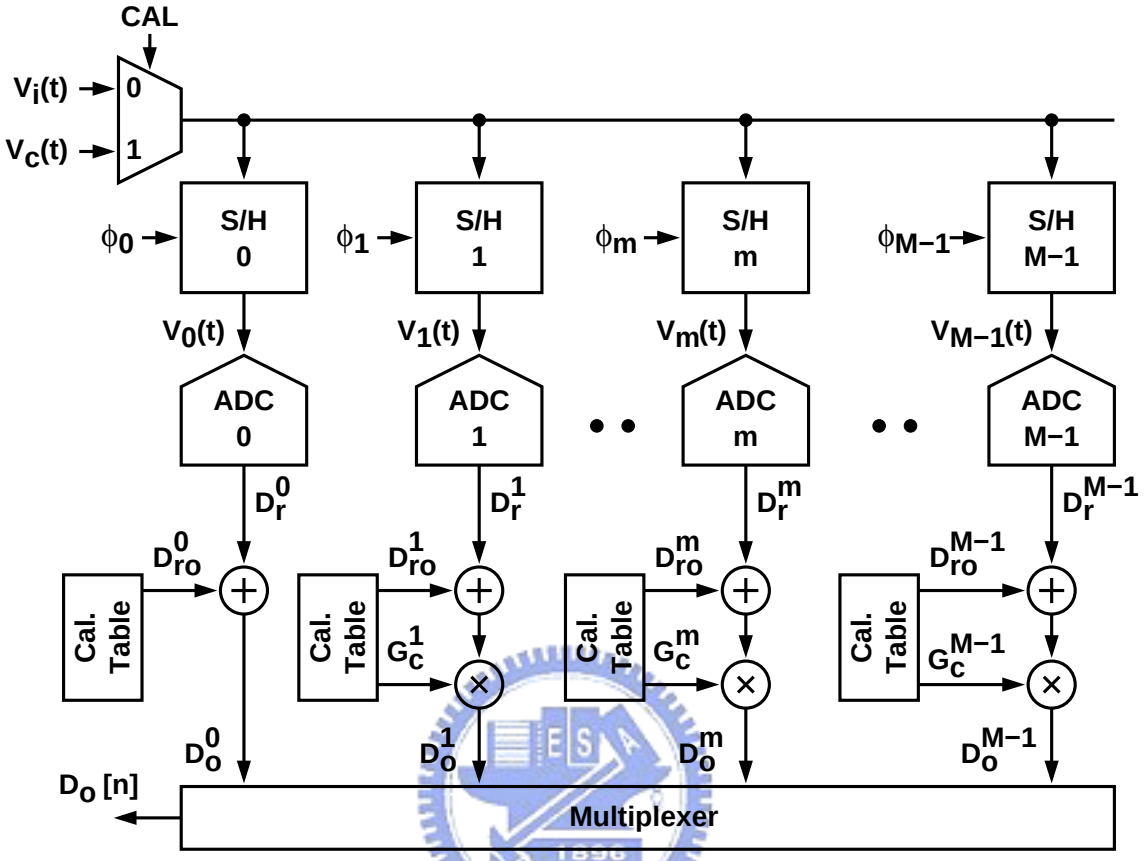


Figure 5.1: Block diagram of a TI-ADC with foreground calibration.

phase ($CAL = 1$), the TI-ADC's input is connected to the calibration signal, $V_c(t)$. The $V_c(t)$ signal is $\pm V_r$ for gain calibration, and 0 for offset calibration. After calibration (CAL= 0), the normal input signal, $V_i(t)$, is applied to the ADC's input, and the TI-ADC performs normal conversion.

Assume g_m is the conversion gain of the m-th channel, and o_m is the offset. Then, the transfer function can be expressed as

$$D_r^m = g_m \times V_i(t) + o_m \tag{5.1}$$

where $m = 0, 1, \cdots, M-1$. During the calibration phase, the input is connected to 0, so that the offset, o_m, for all m, can be obtained in digital domain; its mathematical expression is given by

$$D_r^m = g_m \times 0 + o_m = o_m \equiv D_{ro}^m \tag{5.2}$$

To calculate the channel's conversion gain, the input is firstly connected to $+V_r$, and the maximum digital output code, $D^m_{r,max}$, can be obtained, and is given by

$$D^m_{r,max} = g_m \times (+V_r) + o_m \tag{5.3}$$

Then, the $-V_r$ signal is applied to the ADC's input, and the minimum digital code, $D^m_{r,min}$, can be obtained, and is expressed as

$$D^m_{r,min} = g_m \times (-V_r) + o_m \tag{5.4}$$

Furthermore, the conversion gain of the m-th channel can be obtained by subtracting (5.4) from (5.3), for all m. The g_m gain is therefore given by

$$g_m = \frac{D^m_{r,max} - D^m_{r,min}}{+V_r - (-V_r)} \tag{5.5}$$

To equalize the conversion gains of A/D channels, one channel is chosen as the reference. For instance, if the 1-st channel ($m = 0$) is the reference, the gain correction factors of other channels can be obtained by

$$G^m_c = \frac{g_0}{g_m} = \frac{D^0_{r,max} - D^0_{r,min}}{D^m_{r,max} - D^m_{r,min}} \tag{5.6}$$

The gain correction factor G^m_c is then multiplied by the output code which is offset-compensated to equalize the conversion gain to the reference channel. The final output D_o is obtained by multiplexing A/D channel output, D^m_o, for all m, which are offset-compensated and gain-equalized.

5.3 Equalization-Based Calibration

This section overviews equalization-based calibration which is similar to that presented in Section 3.4. To perform calibration, a reference ADC is required to produce desired data for equalization. This reference ADC can be one of the interleaved ADCs or an additional ADC. Using one of the interleaved ADCs as the reference requires fairly complicated digital signal processing indicated as blind calibration [8] [34] [35]. Since the blind calibration is so complicated, little implementations are presented. Therefore, it is not further

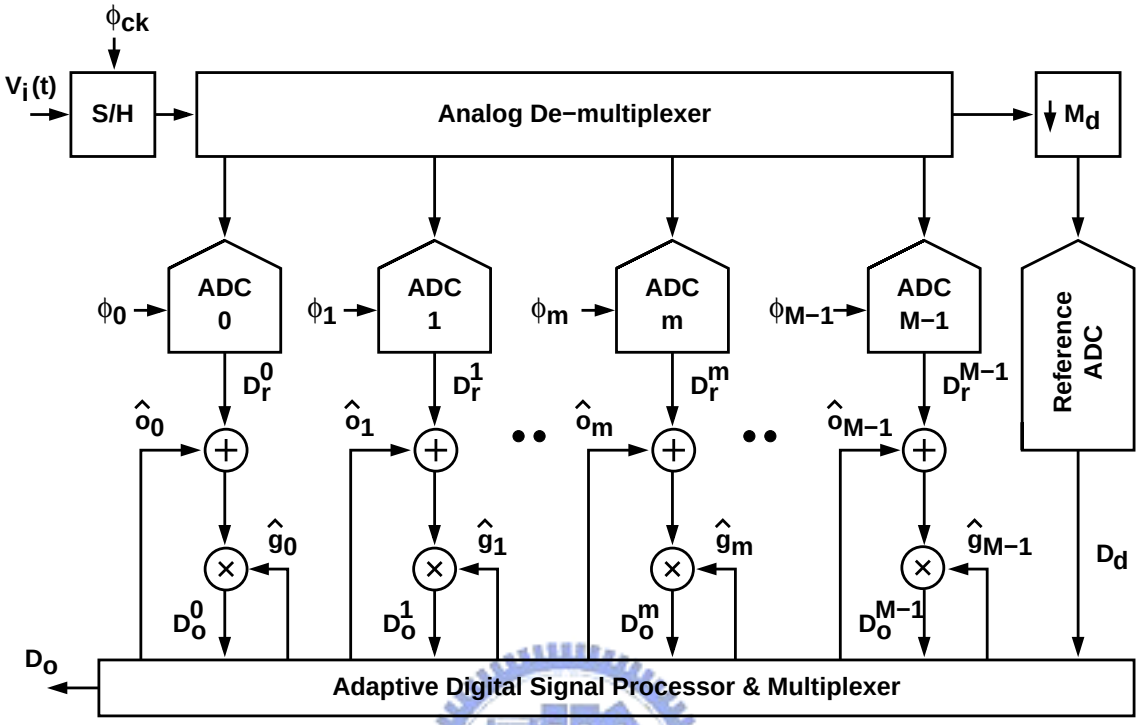


Figure 5.2: Block diagram of a TI-ADC with equalization-based calibration.

discussed here. Conversely, adding an additional slow, high-resolution ADC (SH-ADC) as the reference is straight-forward to employ the LMS algorithm to perform equalization [36].

Fig. 5.2 shows the block diagram of a TI-ADC employing equalization-based calibration. The TI-ADC uses a single front-end S/H to avoid time skew errors among A/D channels. The reference ADC is a SH-ADC generating a desired digital output D_d every M_d clock cycles. Assume the ADC's raw output, D_r^m, has nonideal conversion gain, g_m, and offset, o_m, and is modeled by

$$D_r^m = g_m \times V_i + o_m \tag{5.7}$$

for all $m = 0, 1, \cdots, M-1$. The corrected digital code, D_o^m, is given by

$$D_o^m = \hat{g}_m \times \left[D_r^m + \hat{o}_m\right] = \hat{g}_m g_m \times V_i + \hat{g}_m \left[o_m + \hat{o}_m\right] \tag{5.8}$$

where $\hat{g}_m$ is the gain correction factor the m-th channel, and $\hat{o}_m$ is the offset compensation factor. Ideally, $D_o^m = V_i = D_d$, where the D_d desired signal can be regarded as the ideal

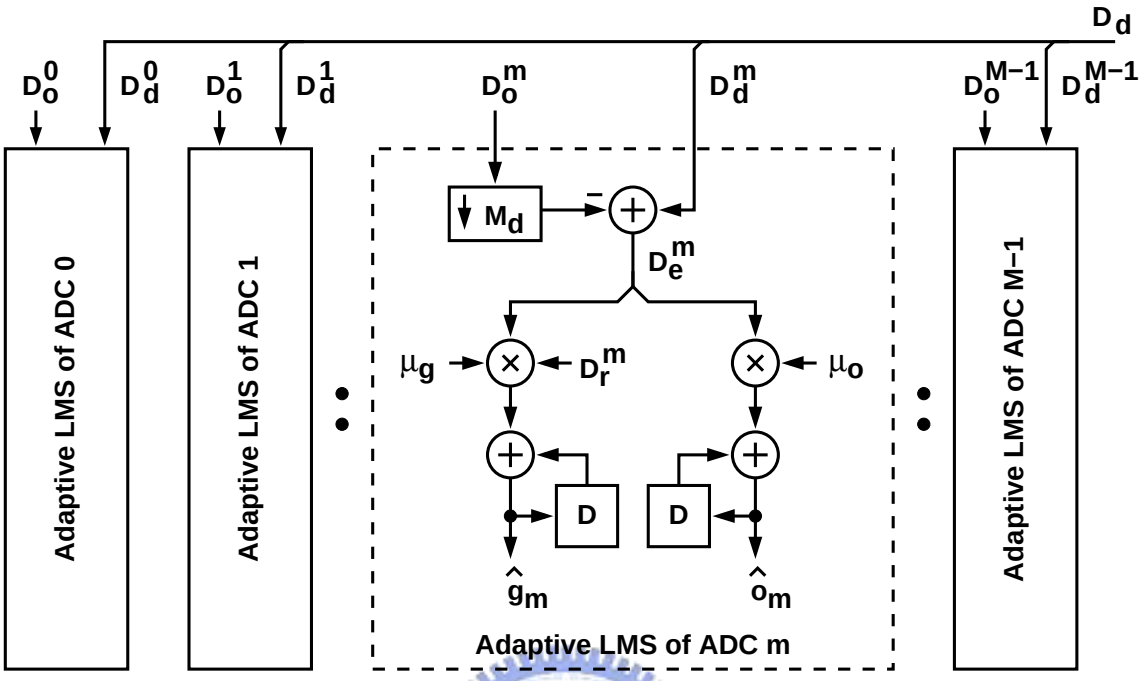


Figure 5.3: Block diagram of the adaptive signal processing.

digitized code of V_i. Hence, ideally, after the equalization to the reference ADC, we have

$$\hat{g}_m = \frac{1}{g_m} \tag{5.9}$$

$$\hat{o}_m = -o_m \tag{5.10}$$

Fig. 5.3 shows the gain and offset estimations based on LMS algorithm similar to those of Section 3.4. The estimations have three steps summarized as follows.

1. Initialize the parameters, $(\hat{g}_m[0], \hat{o}_m[0])$.

2. Calculate error:

$$D_e^m[n'] = D_d^m[n'] - D_o^m[n'] \tag{5.11}$$

3. Adjust parameters $\hat{g}_m[n']$ and $\hat{o}_m[n']$ as:

$$\hat{g}_m[n'] = \hat{g}_m[n'-1] + \mu_g \times D_e^m[n'] \times D_r^m[n'] \tag{5.12}$$

$$\hat{o}_m[n'] = \hat{o}_m[n'-1] + \mu_o \times D_e^m[n'] \tag{5.13}$$

where μ_g is the step size of gain adaptation, μ_o is that of offset adaptation, and $n' = M_d \times n$ is the time index with downsampling. When the error D_e^m is minimized, i.e. $D_e^m \to 0$,

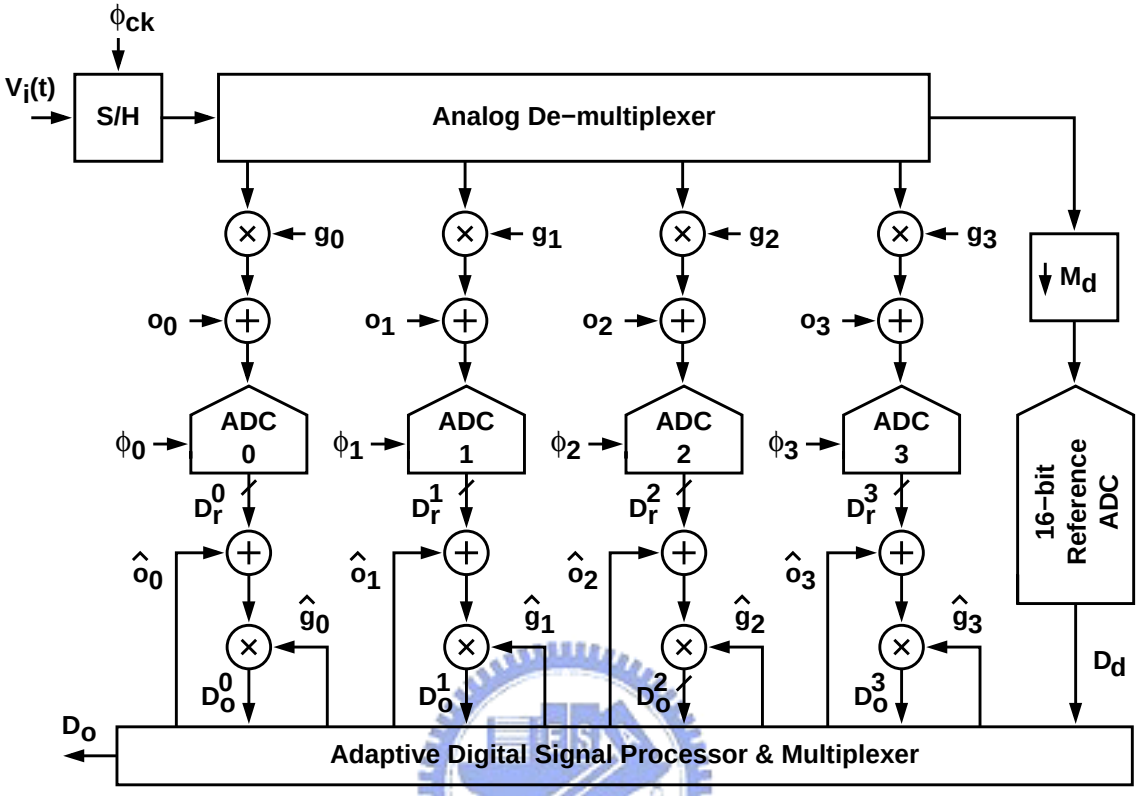


Figure 5.4: Block diagram of a 4-channel TI-ADC with equalization-based calibration.

the gain and offset of the m-th channel are equalized to the reference. The equalization is proceeded for each channel. When each channel is equalized to the reference. The mismatch errors among the A/D channels are corrected.

A 4-channel TI-ADC with a SH-ADC shown in Fig. 5.4 as an example to illustrate the feasibility of equalization-based calibration. A C-code model is built for simulation by assuming the gain and offset mismatches between the four A/D channels are modeled as

$$\text{Gain} \Rightarrow \begin{cases} \text{Channel 0:} & g_0 = g \times (1 - \varepsilon_g/4) \\ \text{Channel 1:} & g_1 = g \times (1 + \varepsilon_g/4) \\ \text{Channel 2:} & g_2 = g \times (1 - \varepsilon_g/2) \\ \text{Channel 3:} & g_3 = g \times (1 + \varepsilon_g/2) \end{cases} \quad \text{Offset} \Rightarrow \begin{cases} \text{Channel 0:} & o_0 = +\varepsilon_{os}/4 \\ \text{Channel 1:} & o_1 = -\varepsilon_{os}/4 \\ \text{Channel 2:} & o_2 = +\varepsilon_{os}/2 \\ \text{Channel 3:} & o_3 = -\varepsilon_{os}/2 \end{cases}$$

where g is the nominal conversion gain, and has a typical value of 1, ε_g and ε_o are modeled the gain error and offset error respectively. Assume only the gain error and offset are con-

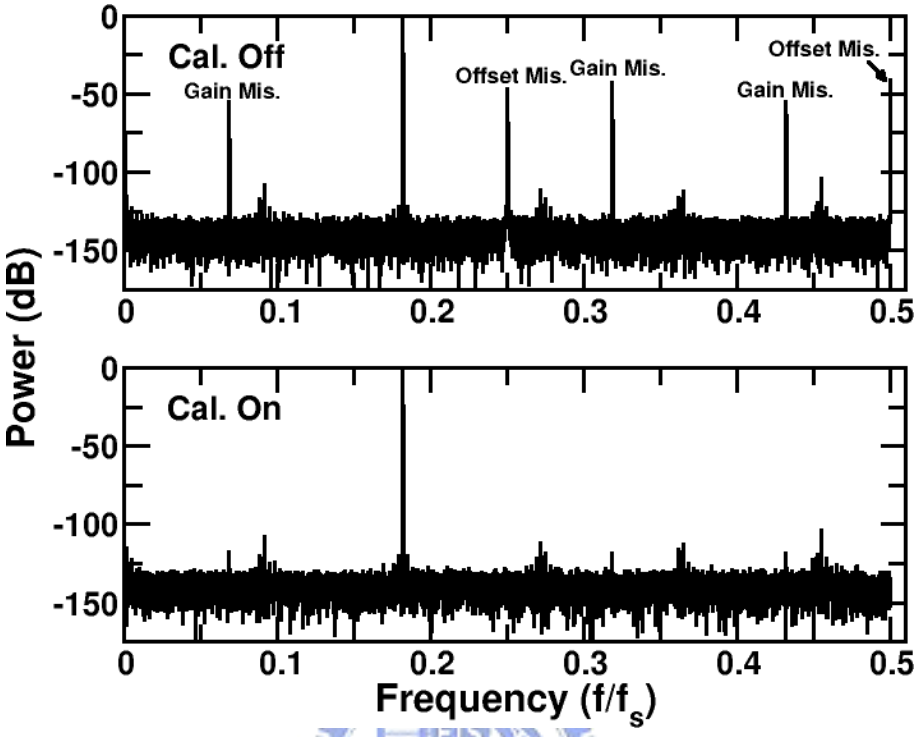


Figure 5.5: Simulated power spectrum at f_{in} = 18.17 MHz and f_s = 100 MHz.

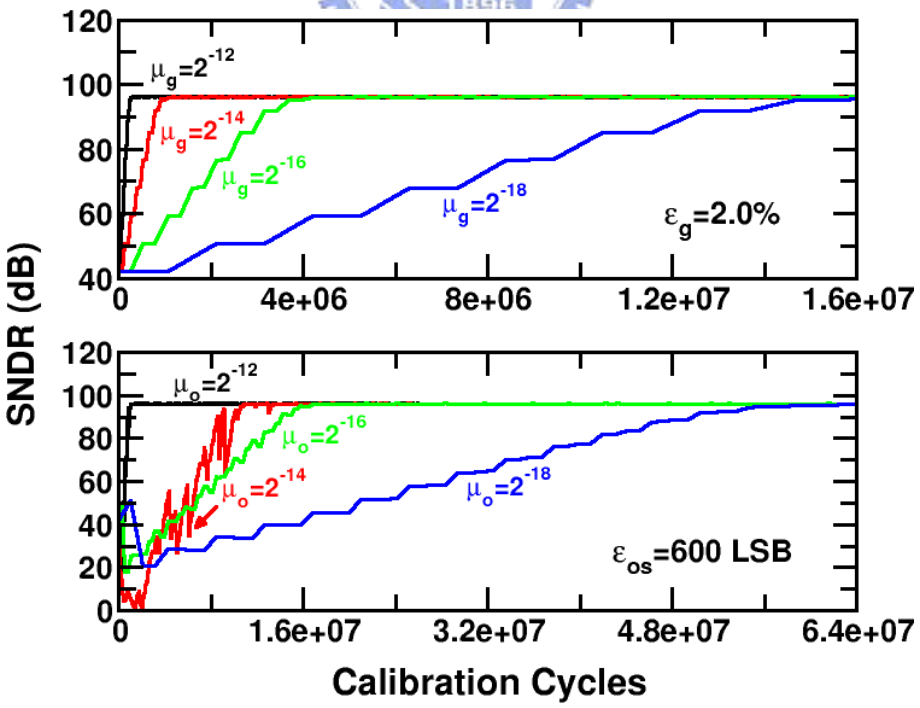


Figure 5.6: Output SNDR versus calibration cycles.

sidered, and choose $\varepsilon_g = 2.0\%$ and $\varepsilon_{os} = 600$ LSB as the simulation parameters, where 1 LSB= 2^{-15}. To speedy up the simulation process, M_d is chosen as 1. In reality, M_d typically is chosen as a value of power of 2, according to the sampling rate of the reference ADC which is an ideal 16-bit ADC. Fig. 5.5 shows the simulated FFT power spectrum with a step size $\mu_g = \mu_o = 2^{-12}$. It indicates that the equalization-based technique indeed corrects the gain/offset mismatch errors between A/D channels and significantly improves the entire A/D linearity. Fig. 5.6 shows the ADC's output SNDR with variant step sizes versus the calibration cycles, where the horizontal axis presents the start point of collecting samples for analyzing SNDR. The top penal shows the output SNDR of ADC with gain error $\varepsilon_g = 2\%$ and zero offset, whereas, the bottom penal shows that of ADC with offset error $\varepsilon_{os} = 600$ LSB and zero gain error. The simulation results demonstrate that smaller step size for equalization requires longer calibration time.

5.4 Randomly Time-Interleaving Method

The randomly time-interleaving technique is used to improve the SFDR of a TI-ADC by whitening its spurious components caused by the mismatches among channels. This randomly-controlled sampling concept was investigated in [37] to remove the spurs caused by the offset mismatches. It was extended to overcome not only the offset mismatch errors but also the gain and timing mismatch erros [38] [39] [40].

A general randomly TI-ADC requires one or more extra A/D channels to support the randomization of the channels. The architecture of a randomly TI-ADC with K extra channels is shown in Fig. 5.7. There are total $(M + K)$ A/D channels, but only M times improvement of the sampling rate can be achieved. The normal M sampling clock signals, ϕ_0 to ϕ_{M-1}, are gated by the randomly interleaving selector controlled by a positive integer pseudo-random generator (PSR) to generate $(M + K)$ randomized controlling signals,$\phi'_m(t)$. The PSR generates random values altering from 0 to K. The controlling signals $\phi'_m(t)$'s are used to control the sampling and quantizing of input signal, $V_i(t)$. Finally, the mismatch-whitened digital output is obtained.

To analyze the efficiency of randomization in reducing the influence of mismatches among A/D channels, each channel now is linearly modeled as shown in Fig. 5.8, where

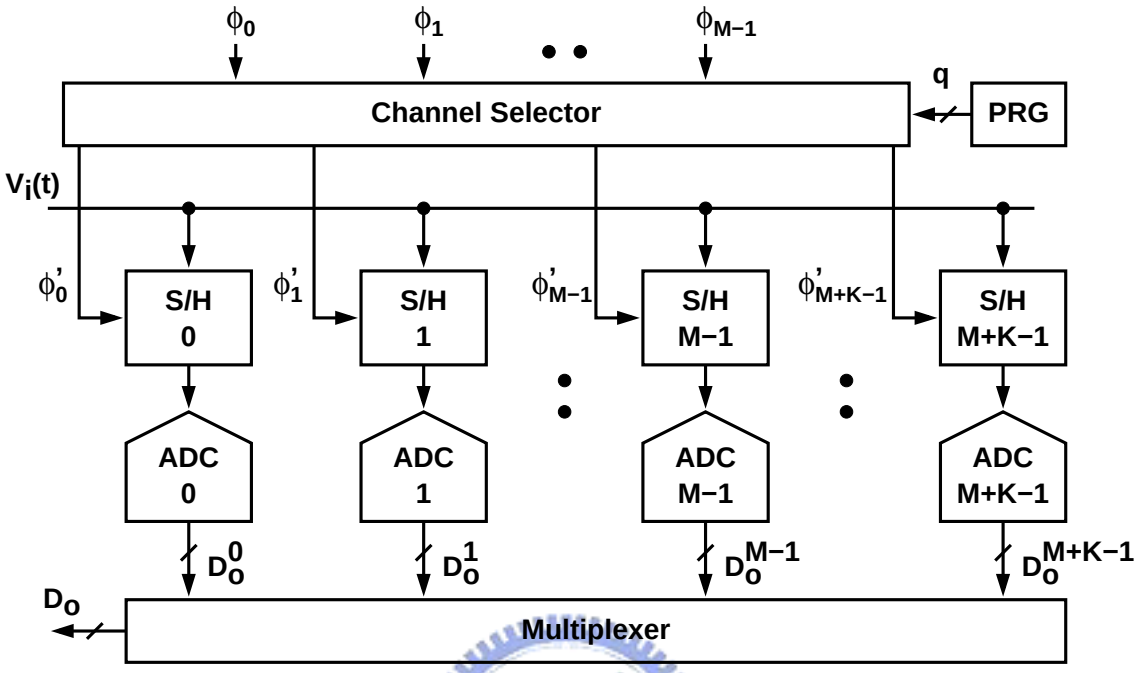


Figure 5.7: A randomly time-interleaved ADC.

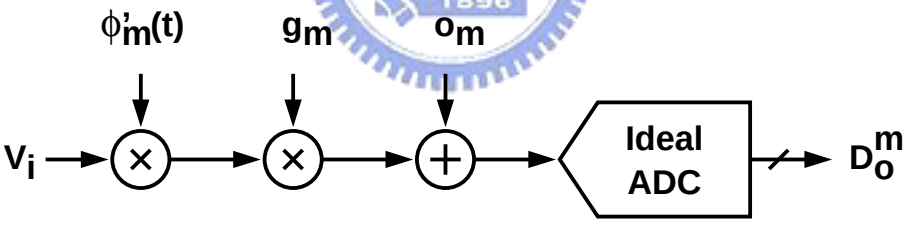


Figure 5.8: The model of single channel in a randomly TI-ADC.

Table 5.1: Simulated Parameters

Channel Index	0	1	2	3	4
Gain Factor, g_m (%)	-0.1	-0.2	+0.1	-0.3	-0.2
Sampling Skew ($\Delta t_m/T_s$)	0.02	0.015	0.01	0.03	0.012
Offset, o_m (LSB)	100	220	175	200	155

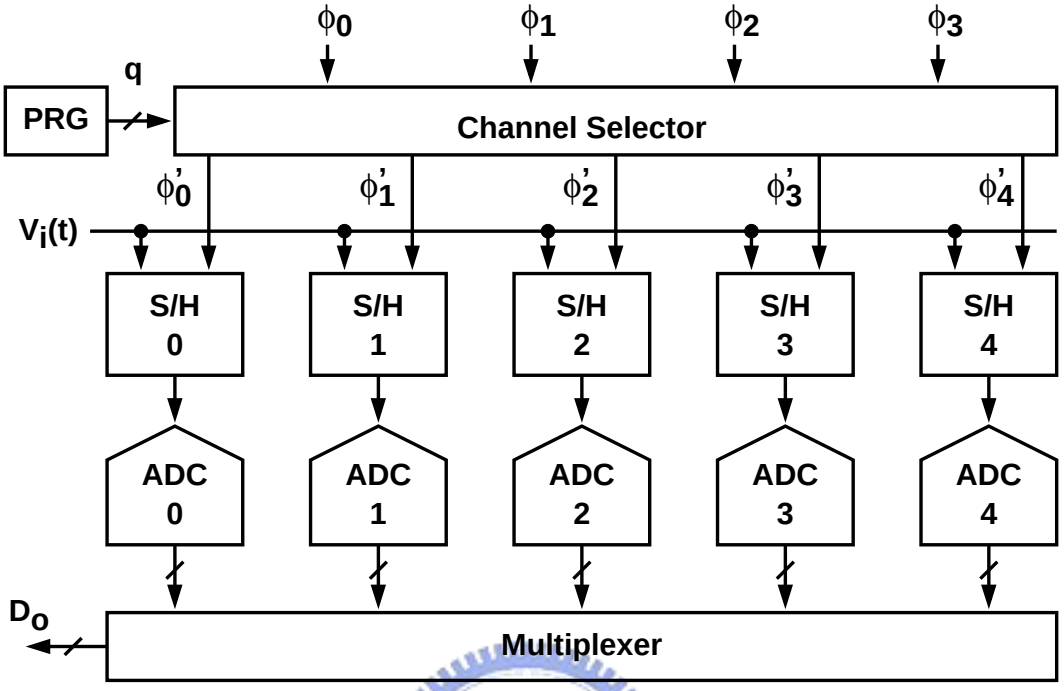


Figure 5.9: A $(4+1)$-channel randomly TI-ADC.

$m \in \{0, 1, \cdots, M+K-1\}$. g_m is the m-th channel's conversion gain factor, and o_m is the dc offset.

A $(4+1)$-channel randomly TI-ADC, i.e. $M = 4$ and $K = 1$, is used to illustrate the randomizing operation in the following paradigm. The architecture is shown in Fig. 5.9. In generally, only 4 channels are needed to achieve the 4 times improvement of effective sampling rate of a TI-ADC. The corresponding sampling of each channel of a normal 4-channel TI-ADC is shown as ϕ_m, $m \in \{0, \cdots, 3\}$, in Fig. 5.10. However, in order to activate the randomly interleaving mechanism, ϕ_m's are encoded based on the randomized principles. The waveform of ϕ_m' signals, for $m \in \{0, \cdots, 4\}$ are also shown in Fig. 5.10. $\phi_m^{'}$'s are used to control which channel to sample the input signal at each cycle of the system sampling clock (f_s). Fig. 5.11 shows the principles of randomization describing that each sampling cycle, one of the two candidates of channels excluding those used in the preceded three cycles is decided to sample the input based on the random signal q. The simulation of the $(4+1)$-channel TI-ADC was done based on these parameters described in Table 5.1 to verify the randomizing method.

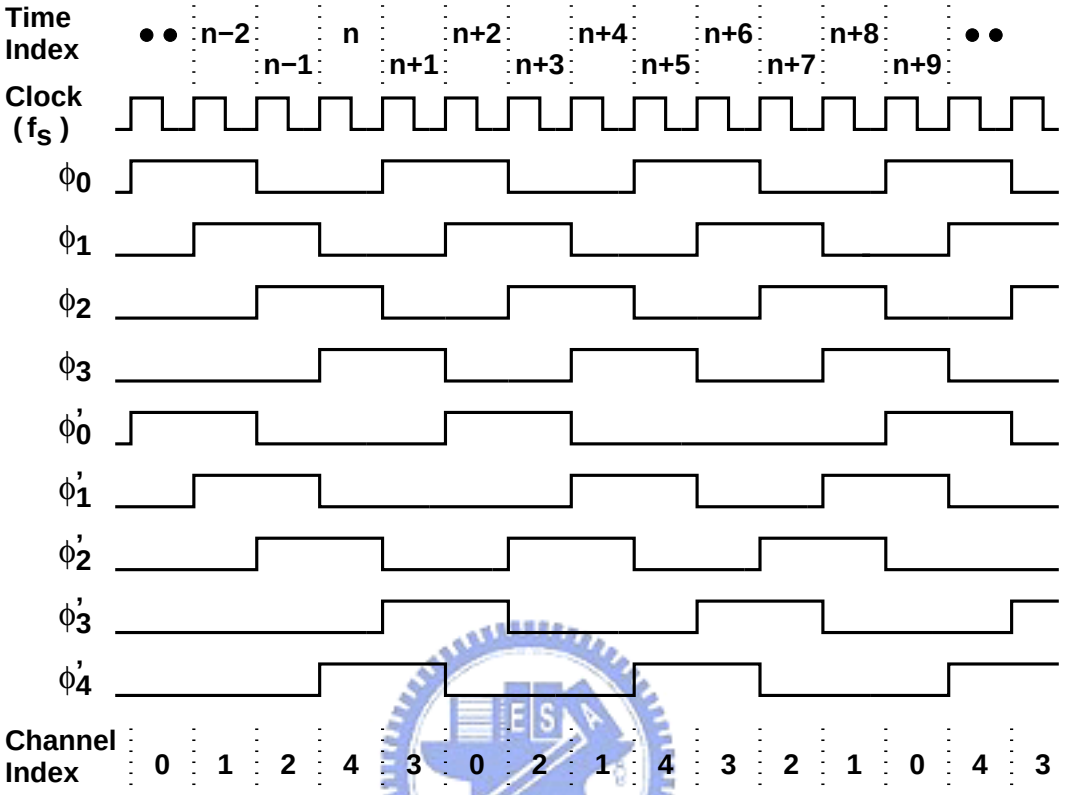


Figure 5.10: A diagram of randomly controlling signals in a (4+1) TI-ADC.

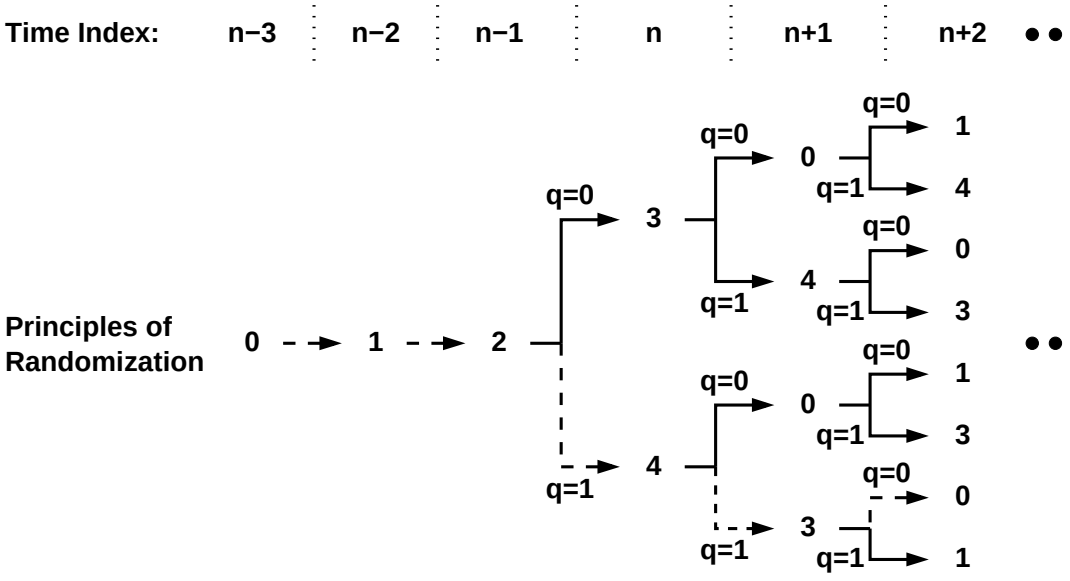


Figure 5.11: Principles of randomization.

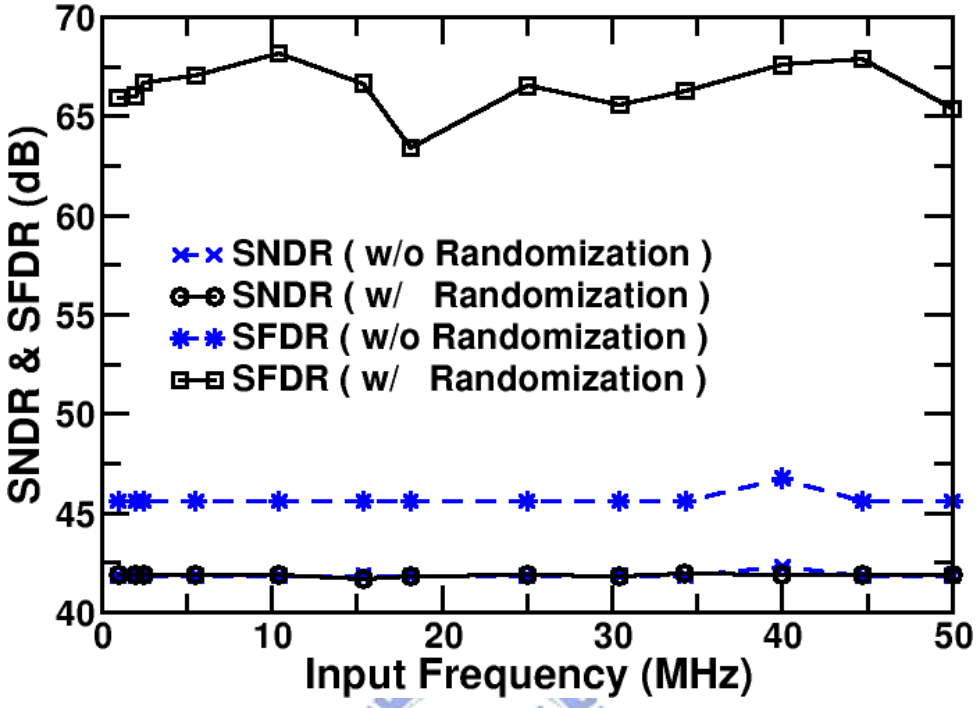


Figure 5.12: Simulated SNDR and SFDR versus input frequency of a (4 + 1) TI-ADC.

Fig. 5.12 shows the simulated SNDR and SFDR versus variant input frequencies. The SNDR never improves when the randomization is applied. This is because the randomization only spreads the distortion tones over frequencies, rather than removes them. Hence, the randomization method can only be used in the applications that SNDR is not a considered issue.

5.5 Proposed Mismatch Correction Technique

The proposed calibration technique here is addressed only for the gain and offset mismatches of a TI-ADC. The timing skew calibration is not necessary when employ a single SHA in the front of the A/D architecture. The gain correction is conducted from the digital calibration scheme mentioned in Section 3.5. The offset calibration is similar to the scheme employed in [41] and [7].

Fig. 5.13 shows the block diagram of a TI-ADC with the proposed gain and offset mismatch correction schemes. Since the gain correction technique is based on the digi-

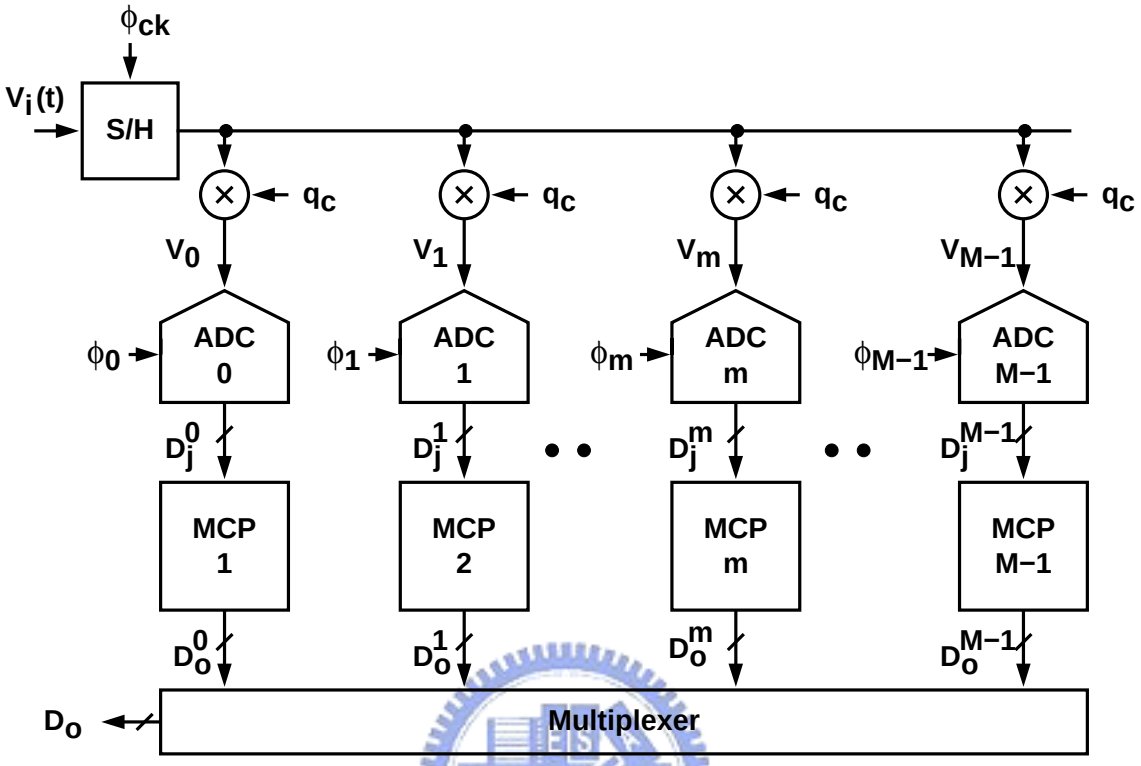


Figure 5.13: A TI-ADC with the proposed mismatch correction.

tal calibration of Section 3.5. All ADCs here employ the pipelined A/D configuration to maintain the gain mismatch correction scheme. When the offset calibration is activated, the channel input is randomly chopped by a random sequence q_c. Each channel has an individual mismatch correction processor (MCP) including gain and offset mismatches correction. After the MCP, mismatch-interfered digital output code is corrected and generates the output D_o^m. Then, D_o^m's, for all m, pass through a multiplexer to generate the final digital output code (D_o).

Fig. 5.14 shows the block diagram of the MCP including the digital output encoding and correction for the A/D channel. The calibration processor (CP) executes the calibration procedures described in Section 3.5, and updates the $W_j(D_c)$ calibration data constantly, where D_c means each possible digital output code of the j-th stage of the pipelined ADC. The channel encoder calculates the raw A/D output, D_{r1}, based on (3.38) by using the pipeline stages' output codes, D_j^m, for all j, as pointers to the $W_j(D_c)$ table. From

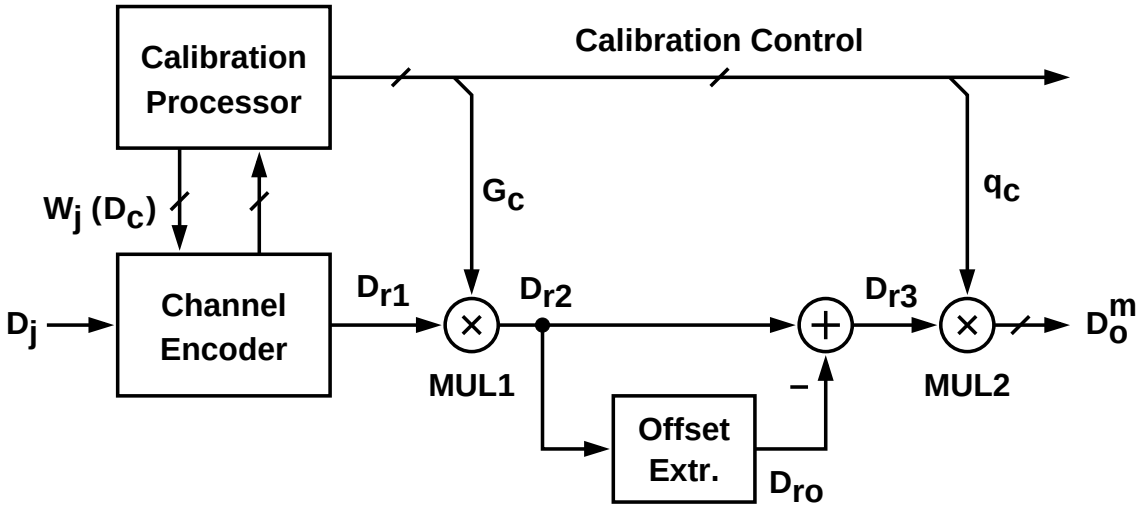


Figure 5.14: A mismatch correction processor.

(3.41), we have

$$V_1 = \frac{G_1 G_2 \cdots G_P}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} \times D_{r1} + \frac{V_{P+1}}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} \tag{5.14}$$

with

$$D_{r1} = \sum_{j=1}^{P} \frac{W_j(D_j^m)}{G_1 G_2 \cdots G_j} \tag{5.15}$$

The CP also calculates the G_c gain correction factor by using only the $W_j(D_c)$ calibration data. The normalized D_{r2} signal is obtained by multiplying D_{r1} with G_c. The V_1-to-D_{r2} conversion gain for all A/D channels are then equalized. The overall dc offset of the A/D channel, D_{ro}, is extracted from D_{r2} by using a LPF. The D_{r3} signal is the D_{r2} signal with its dc offset removed. Finally, the individual channel output, D_o^m, where $m \in \{0, 1, \cdots, M-1\}$, is obtained by unscrambling D_{r3} with the q_c sequence.

To examine the gain correction scheme for a M-channel TI-ADC, and each channel employs the pipelining A/D architecture with P stages. All pipeline stages are assumed having the same configuration as shown in Fig. 3.9, and each stage has a resolution of B_j bits. The stages are also assumed sharing the identical V_r reference. From (2.39), (2.36), (3.27) and (3.28), we have

$$\hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_j) = (1 - \varepsilon_\tau) \left(\frac{1}{1 + \varepsilon_G} \right) \sum_{y=1}^{N_s} D_{j,y} \cdot \frac{C_{s,y}}{C_f} \times V_r = R_j(D_j) \tag{5.16}$$

Then, according to (2.40), the $R_j(D_j)$ parameter can be rewritten as

$$R_j(D_j) = V_r \times \frac{D_j}{N_s} \times \left(\hat{G}_j - \frac{1-\varepsilon_\tau}{1+\varepsilon_G} \right) \tag{5.17}$$

$$\approx V_r \times \frac{D_j}{N_s} \times (\hat{G}_j - 1 + \varepsilon_\tau + \varepsilon_G) \tag{5.18}$$

Assume only the linear settling is considered, and let $\mu_j = \varepsilon_\tau + \varepsilon_G$. The $R_j(D_j)$ parameter is rewritten as

$$R_j(D_j) \approx V_r \times \frac{D_j}{N_s} \times (\hat{G}_j - 1 + \mu_j) \tag{5.19}$$

Neglecting the quantization error, and assuming D_j, for all j, have the same value, i.e., $D_j = D_s$. From (5.14), (5.15), and (5.19), the channel's input signal is given by

$$V_m = \sum_{j=1}^{P} \frac{R_j(D_s)}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j} \tag{5.20}$$

$$= V_r \times \frac{D_s}{N_s} \times \left(1 - \frac{1}{\hat{G}_1 \hat{G}_2 \cdot \hat{G}_P} + \sum_{j=1}^{P} \frac{\mu_j}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j} \right) \tag{5.21}$$

which indicates that if (5.15) is used to encode the digital output, then the corresponding analog input V_m approximates $+V_r$ if $D_j = +N_s$ for all j, amd the corresponding analog input V_m approximates $-V_r$ if $D_j = -N_s$ for all j.

Based on (5.20), the channel's conversion gains can be derived, as well as the gain correction factors. Fig. 5.15 illustrates the V_m to D_{r1} transfer functions for two of the A/D channels with different conversion gains. To equalize the conversion gains, the G_c gain correction factor for the m-th channel is given by

$$G_c = \frac{\Delta V_m}{\Delta D_{r1}} \tag{5.22}$$

Then, the same D_r code range covers the same V_m voltage range. From (5.20) with $D_s = +N_s$ and $D_s = -N_s$, the required G_c can be expressed as

$$G_c = \frac{2}{\sum_{j=1}^{P} \frac{W_j(+N_s)}{G_1 G_2 \cdots G_j} - \sum_{j=1}^{P} \frac{W_j(-N_s)}{G_1 G_2 \cdots G_j}} \times (1 + \varepsilon_g) \tag{5.23}$$

where ε_g is the residual uncorrected gain error which is

$$\varepsilon_g = -\frac{1}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_P} + \sum_{j=1}^{P} \frac{\mu_j}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_j} \tag{5.24}$$

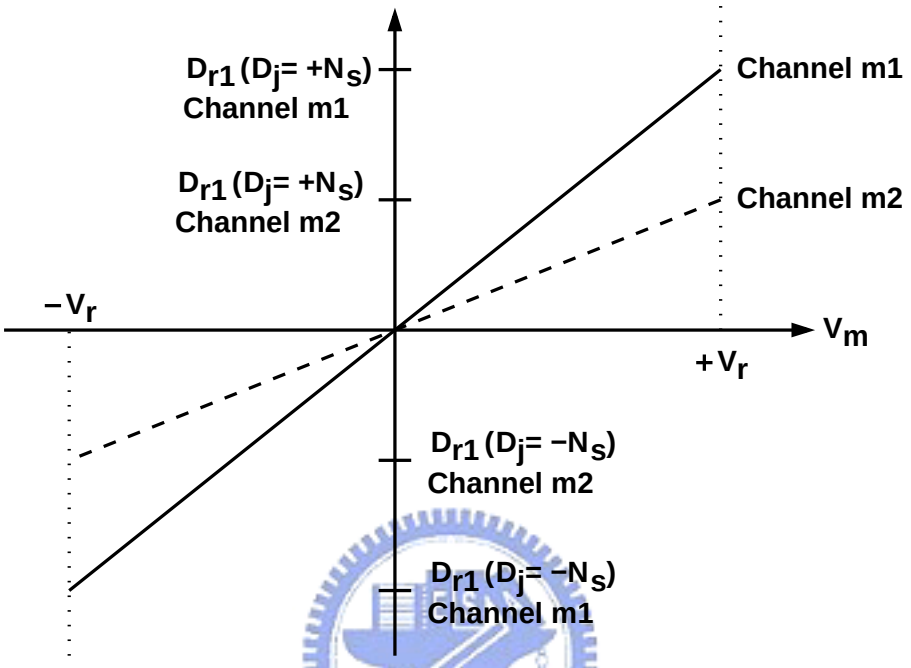


Figure 5.15: V_m to D_{r1} transfer functions.

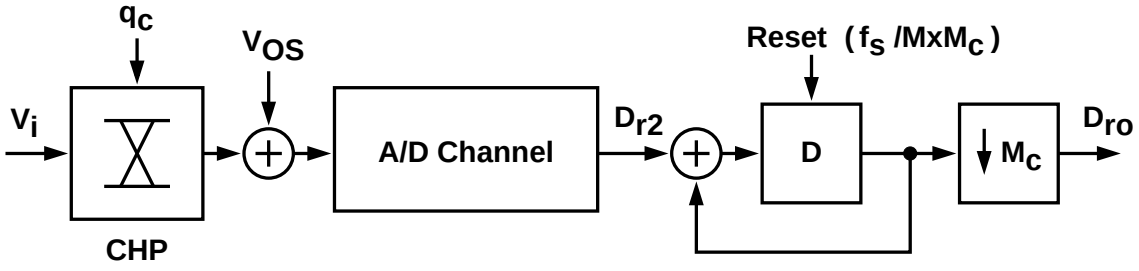


Figure 5.16: Offset extraction signal-flow diagram.

Fig. 5.16 shows the signal-flow diagram for offset extraction, which is similar to the scheme employed in [41] and [7]. Since the V_i input is scrambled by the CHP chopper, the only dc component in the D_{r2} digital stream is the dc offset of the A/D channel, V_{OS}. The integration-and-dump scheme is used to extract the dc offset from the D_{r2} stream. The resulting output D_{ro} is taken only after every M_c samples of integration of D_{r2}, where M_c is the period of the q_c binary pseudo-random sequence which controls the CHP chopper. The value of D_{ro} includes an estimation of the V_{OS} offset and a perturbation caused by the scrambled V_i signal. Assuming that the magnitude of V_i is uniformly distributed between $+0.5V_r$ and $-0.5V_r$, its averaged power can be approximated by $V_r^2/12$. The integration and dump function of the extractor can reduce the effect of this perturbation power by a factor of M_c. Then, the variance of D_{ro} can be expressed as:

$$\sigma^2(D_{ro}) = \frac{1}{M_c} \times \frac{V_r^2}{12} \tag{5.25}$$

To achieve B-bit accuracy for the TI ADC, we want $\sigma(D_{ro}) < V_r/2^B$. Thus, the required value of M_c can be expressed as:

$$M_c > \frac{1}{3} \times 2^{2(B-1)} \tag{5.26}$$

To achieve a resolution of $B = 15$, it is required that $M_c > (1/3)2^{28}$. In this work, $M_c = 2^{28}$ is chosen, so that both the q_c and q sequences have the same period, and can be generated from the same random generator.

5.6 Summary

In this chapter, methods for reducing mismatch errors in a TI-ADC are discussed. The foreground calibration and equalization-based calibration approaches have similar characteristics as those for enhancing linearity in pipelined ADCs. The randomly interleaving method requires extra more than one A/D channels, and create significant analog design complexity and large hardware overhead. In addition, it can only improve the distortions performance by whitening the spurs. Therefore, it is unacceptable for the applications when the noise performance is an issue. The developed method extends the linearity enhancement of a pipelined ADC described in Section 3.5 to correct the gain and offset

errors of a single channel to equalize the mismatches among channels. This method is low-complexity and only requires less hardware cost but achieves significantly improvement in the conversion linearity.

Chapter 6

Sample-and-Hold Amplifiers for Time-Interleaved Analog-to-Digital Converters

6.1 Introduction

To avoid time skew errors, single sample-and-hold amplifier (SHA) is employed in the front-end of a TI-ADC. The SHA is the most critical block of the TI-ADC because it is required to operate at the full sampling rate of the TI-ADC to maintain the linearity requirements. For opamp-based SHAs, their speed is limited by the opamp's settling time. To achieve up to a resolution of 14 bits, and sampling speed of 100-MS/s, the opamp needs relatively high dc gain and wide bandwidth. This makes the opamps are difficult to be designed, especially in using the progressive processing technology.

For a high-resolution SHA, the random errors originated from noise of circuit elements and clock signal are also issues to maintain the performance. In SHAs, the dominating thermal noise are resulted from sampling circuits and opamps. The noise of the sampling circuit is the dominant source in medium- and low-resolution applications. For high-resolution cases, the thermal noise of opamps needs to be taken into account in designs. However, this noise is dependent on the opamp's circuit topology. It is therefore not discussed in this chapter. Only the noise of the sampling circuits-so-called kT/C-noise is

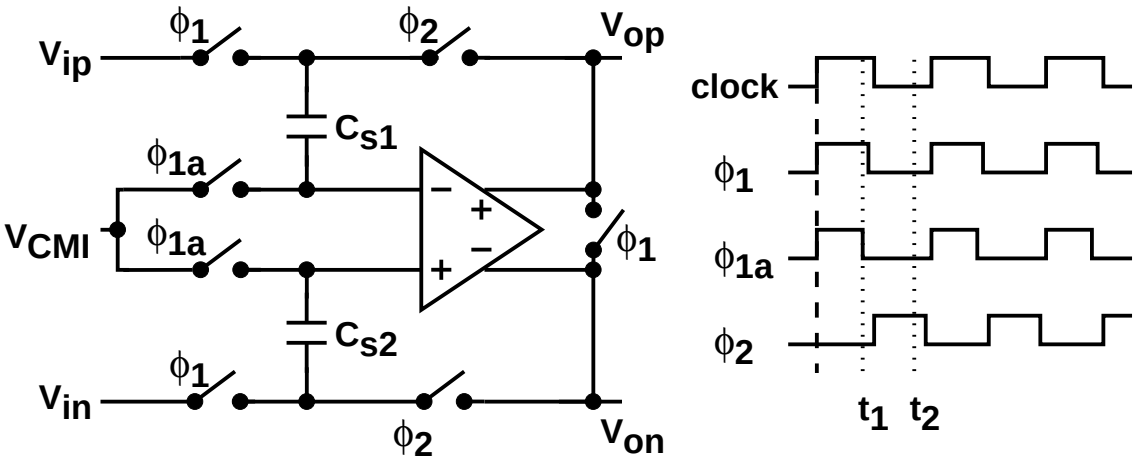


Figure 6.1: A fully-differential FA-SHA and its timing phase.

investigated.

In this chapter, three conventional SHAs and the precharged-SHA (PC-SHA) [42] are examined in their settling speed, and accuracy. Also, the proposed buffered precharged-SHA (BP-SHA) used in a TI-ADC for reducing the loading effect of input networks of A/D channels is introduced.

6.2 Flip-Around SHA

A flip-around (FA) SHA is well-befitted and frequently used in high-speed applications [13] [43] [44] [45]. A FA-SHA's architecture accompanying with its timing diagram is shown in Fig. 6.1. This SHA has two phase operations described in detail in the following. During sampling phase, $\phi_1 = 1$ and $\phi_{1a} = 1$, the opamp's inputs and outputs are reset to its V_{CMI} and V_{CMO} common mode levels respectively. Concurrently, the sampling capacitors, C_{s1} and C_{s2}, track input signals, V_{ip} and V_{in}. At sampling instant, ϕ_{1a} is going to 0, the inputs are sampled on C_{s1} and C_{s2}. During hold phase, $\phi_2 = 1$, C_{s1} and C_{s2} hook up the outputs of opamp as closed-loop to generate output signals, V_{op} and V_{on}, settling to the sampled input levels.

To investigate the accuracy and settling speed of the FA-SHA of Fig. 6.1, its single-ended models corresponding to the two phases for simplicity are presented in Fig. 6.2, where C_{pi} and C_{po} are the parasitic capacitances at the opamp's input and output nodes,

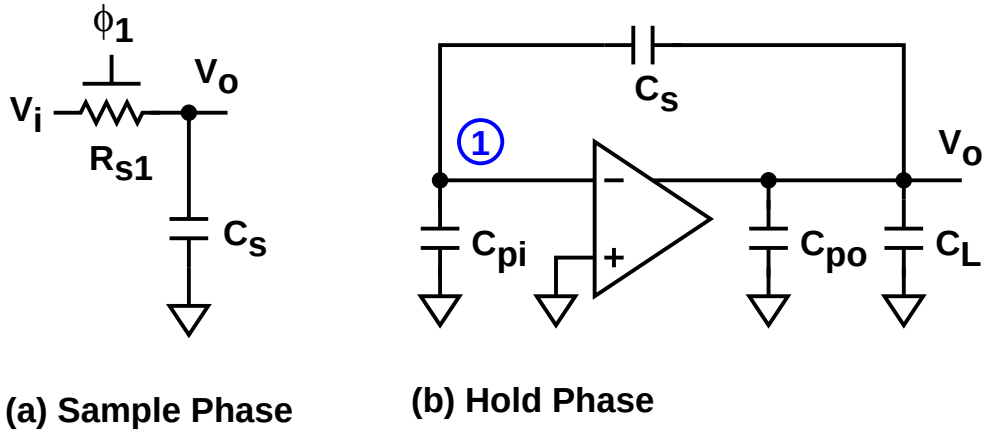


Figure 6.2: Single-ended operating model of an FA-SHA.

C_L is the SHA's output loading capacitance. According to charge conservation, charge on node 1 does not change during both the operating phases. Hence, we have

$$-C_s \times V_i(t_1) = \left[-\frac{V_o(t_2)}{A_0} - V_o(t_2)\right] \times C_s - \frac{V_o(t_2)}{A_0} \times C_{pi} \tag{6.1}$$

where $V_i(t_1)$ is the input level at the t_1 time instant, and $V_o(t_2)$ is the output level at the t_2 time instant. Rearranging (6.1) gives the input/output relationship expressed as

$$V_o(t_2) = \frac{V_i(t_1)}{1 + \frac{1}{A_0}\left(1 + \frac{C_{pi}}{C_s}\right)} \approx V_i(t_1)\left[1 - \frac{1}{A_0}\left(1 + \frac{C_{pi}}{C_s}\right)\right] \tag{6.2}$$

with the feedback factor given by

$$\beta_{fa} = \frac{C_s}{C_s + C_{pi}} \tag{6.3}$$

The opamp's voltage gain A_0 and capacitor ratio C_{pi}/C_s dominate the accuracy of $V_o(t_2)$. To achieve 15-bit resolution, the gain A_0 at dc requires at least 92 dB.

The dynamic performance of a SHA is exactly related to the slew rate (SR) and gain bandwidth (GBW) of the opamps. More severe dynamic errors are caused by the incomplete settling of the opamp's output because of the finite SR and GBW. Here, assume SR is high enough and does not limit the settling behavior; during hold phase, the FA-SHA's settling time constant is given by

$$\tau_{fa} = \frac{1}{\beta_{fa} \times \omega_u} = \frac{C_{po} + C_L + (C_s || C_{pi})}{G_m} \times \frac{(C_s + C_{pi})}{C_s} \tag{6.4}$$

where G_m is the opamp's transconductance. If the opamp's parasitic capacitances are ignored, $\tau_{fa} \approx C_L/G_m$ means larger G_m can achieve higher settling speed for a given C_L.

The kT/C-noise of the FA-SHA since the thermal noise of the sampling switch which can be modeled as a voltage-controlled-resistance (VCR) during the sampling phase is stored to the sampling capacitor has a noise power of

$$n_{th,fa} = \frac{kT}{C_s} \tag{6.5}$$

where k is the Boltzmann's constant, and T is the absolute temperature. Considering the kT/C-noise as the only noise source, the signal-to-noise ratio (SNR) of the FA-SHA for a sinusoidal signal with a full-scale amplitude of $V_{FS}/2$ is given by

$$SNR_{th,fa} = \frac{(V_{FS}/2)^2/2}{kT/C_s} = \frac{V_{FS}^2 \times C_s}{8kT} \tag{6.6}$$

The total kT/C-noise of the SHA determines the minimum size of the sampling capacitors which does not degrade the SNR below the quantization noise level. Hence, for a resolution of 15 bits, the SNR in dB must satisfy the following equation (6.7).

$$SNR_{th,fa} = 10\log\left(\frac{V_{FS}^2 \times C_s}{8kT}\right) > 6.02 \times 15 + 1.76 \tag{6.7}$$

Assume $V_{FS} = 1$ V, it requires $C_s = 53.2$ pF to achieve 15 bits accuracy. However, this value of C_s makes crucial to design the opamps. The C_s value for up to a resolution of 14 bits typically is 4 pF. This value can only give the SNR of 80.8 dB.

6.3 Charge-Transfered SHA

When a closed-loop gain other than unity is desired for a SHA, the charge-transfered SHA (CT-SHA) shown in Fig. 6.3 performs well. It was used as the front-end SHA of a pipelined ADC with a gain approximating to one in the designs of [9] [10] [46] [23]. However, it is suitable for the gain stage of a pipelined ADC, while it can have a gain greater than one [47]. The CT-SHA also has two operation modes. During sampling phase, $\phi_a = 1$ and $\phi_{1a} = 1$, capacitors C_{s1} and C_{s2} track inputs. At sampling instant, i.e. ϕ_{1a} is going to 0, the inputs are sampled on C_{s1} and C_{s2}. During amplification phase,

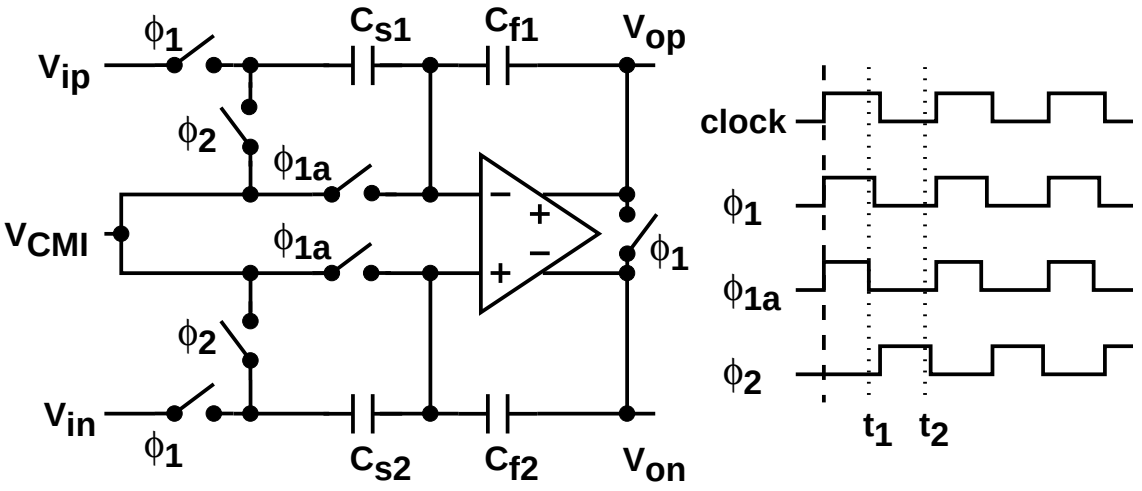


Figure 6.3: A CT-SHA with its timing diagram.

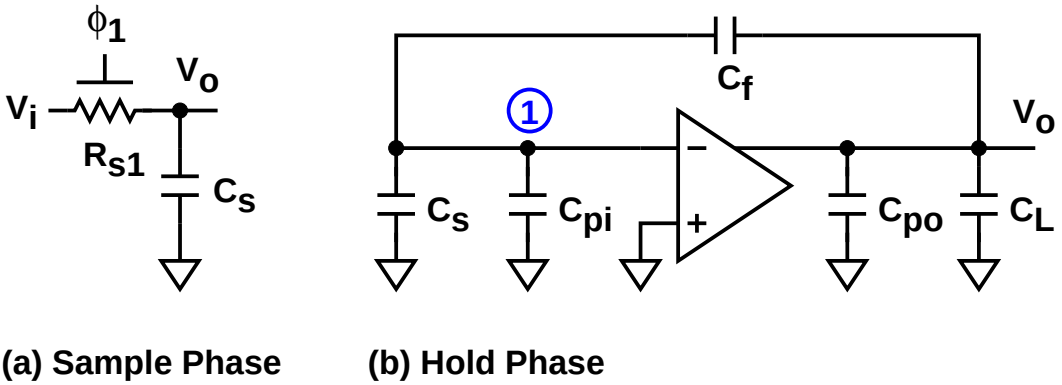


Figure 6.4: Single-ended operating model of a CT-SHA.

$\phi_2 = 1$, C_{f1} and C_{f2} connect opamp's I/O as feedback paths and charges on C_{s1} and C_{s2} transfer onto C_{f1} and C_{f2} respectively to generate output signals.

The CT-SHA's single-ended schematic of the CT-SHA's operation is shown in Fig. 6.4. It is similar to that of Fig. 6.2. The steady-state output is derived according to the charge conservation at node 1; this can be expressed as

$$-V_i(t_1) \times C_s = \left(-\frac{V_o(t_2)}{A} - V_o(t_2)\right) \times C_f - \frac{V_o(t_2)}{A_0} \times (C_s + C_{pi}) \tag{6.8}$$

where $V_i(t_1)$ is the input level at the t_1 time instant, and $V_o(t_2)$ is the output level at the t_2 time instant. Rearranging (6.8), we have

$$\begin{aligned} V_o(t_2) &= \frac{C_s}{C_f} \times V_i(t_1) \times \frac{1}{1 + \frac{1}{A_0} \times \frac{C_s + C_f + C_{pi}}{C_f}} \\ &\approx \frac{C_s}{C_f} \times V_i(t_1) \times \left(1 - \frac{1}{A_0} \times \frac{C_s + C_f + C_{pi}}{C_f}\right) \end{aligned} \tag{6.9}$$

with the feedback factor given by

$$\beta_{ct} = \frac{C_f}{C_s + C_f + C_{pi}} \tag{6.10}$$

The CT-SHA has an amplification gain that is determined by the capacitor ratio, C_s/C_f.

To analyze the dynamic performance, the settling behavior therefore is examined. During the hold phase, the CT-SHA's settling time constant during the hold phase is given by

$$\tau_{ct} = \frac{C_{po} + C_L + [C_f || (C_s + C_{pi})]}{G_m} \times \frac{C_s + C_f + C_{pi}}{C_f} \tag{6.11}$$

Moreover, if C_{pi} and C_{po} are ignored, τ_{ct} becomes as

$$\tau_{ct} = \frac{C_L}{G_m} \times \left(1 + \frac{C_s}{C_f} + \frac{C_s}{C_L}\right) \tag{6.12}$$

which is greater than C_L/G_m. Thus, the CT-SHA has slower settling speed than the FA-SHA with the same G_m and C_L.

The thermal noise due to the sampling circuits, kT/C-noise of the CT-SHA has a noise power of

$$n_{th,ct} = \frac{kT}{C_s} \tag{6.13}$$

which is the same as $n_{th,fa}$ of the FA-SHA. If the kT/C-noise is considered as the only noise source, the CT-SHA has the same SNR performance.

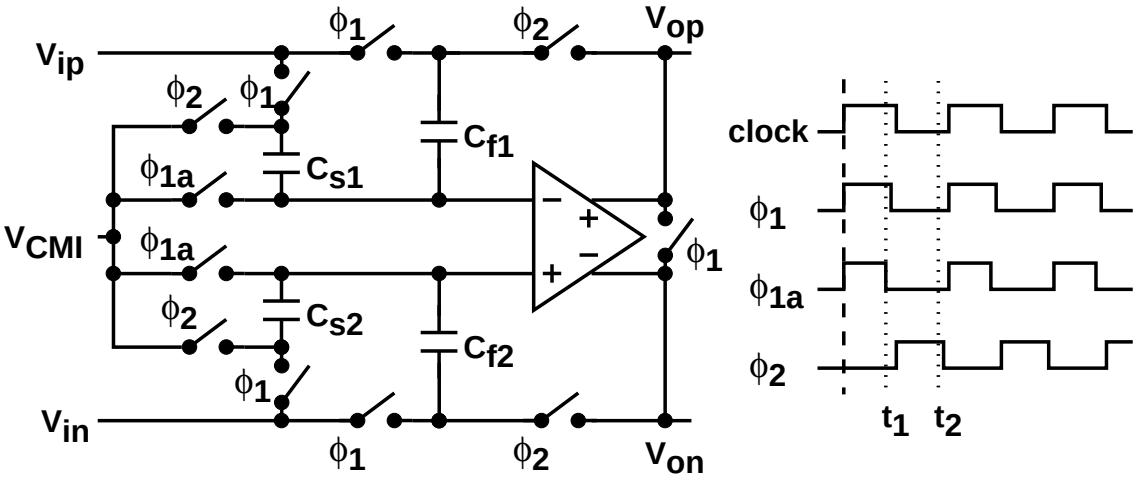


Figure 6.5: A CR-SHA with its timing diagram.

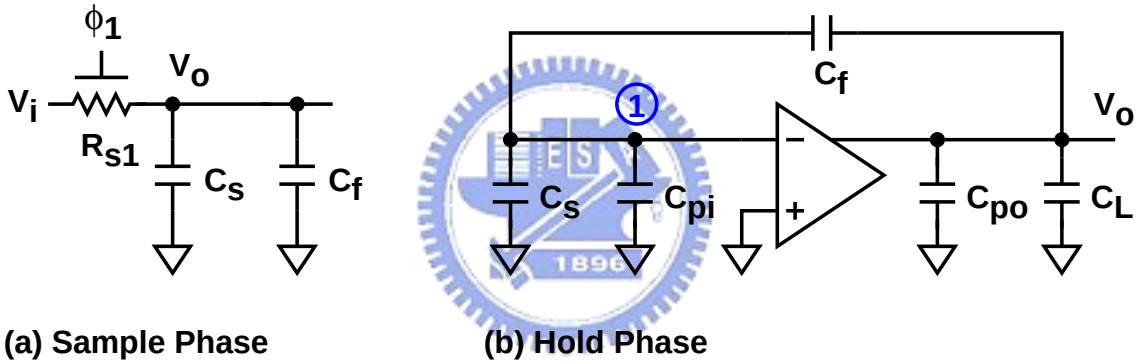


Figure 6.6: Single-ended operating model of a CR-SHA.

6.4 Charge-Redistribution SHA

A charge-redistribution SHA is most frequently used as a gain stage of a pipelined ADC because it can have a gain more than one and has better kT/C-noise performance than a CT-SHA. It is good for implementing a 1.5-bit pipeline gain stage [4]. Fig. 6.5 shows a CR-SHA with sharing the feedback capacitor to sample input and hook up as a feedback path. It also has two operating phases. During sampling phase, $\phi_1 = 1$ and $\phi_{1a} = 1$, both $C_{s\#}$ and $C_{f\#}$ track inputs, where $\# = 1, 2$. At sampling instant, ϕ_{1a} is going to 0, the inputs are sampled on $C_{s\#}$ and $C_{f\#}$. During amplification phase, $\phi_2 = 1$, $C_{f\#}$ hooks up opamp's outputs as closed-loop, and $C_{s\#}$ is connected to input common mode levels, V_{CMI}, to produce the output signals.

The single-ended schematics of a CR-SHA is presented in Fig. 6.6. Similarly, its steady-state output can be obtained according to the charge conservation theorem; the output is expressed as

$$\begin{aligned} V_o(t_2) &= \frac{C_s + C_f}{C_f} \times V_i(t_1) \times \frac{1}{1 + \frac{1}{A_0} \times \frac{C_s + C_f + C_{pi}}{C_f}} \\ &\approx \frac{C_s + C_f}{C_f} \times V_i(t_1) \times \left(1 - \frac{1}{A_0} \times \frac{C_s + C_f + C_{pi}}{C_f}\right) \end{aligned} \tag{6.14}$$

with a feedback factor given by

$$\beta_{cr} = \frac{C_f}{C_s + C_f + C_{pi}} \tag{6.15}$$

which is the same as β_{ct}. The CR-SHA has the gain depending on the value of capacitor ratio $(C_s + C_f)/C_f$. Assume $C_s = C_f$, and C_{pi} is ignored, the opamp's dc gain is required greater than 97 dB to achieve a resolution of 15 bits.

Again, the CR-SHA's settling time constant dominated the dynamic performance is given by

$$\tau_{cr} = \frac{C_{po} + C_L + [C_f || (C_s + C_{pi})]}{G_m} \times \frac{C_s + C_f + C_{pi}}{C_f} \tag{6.16}$$

which has the same value as τ_{ct} of the CT-SHA. The CR-SHA therefore has the same settling speed as the CT-SHA while they have the same circuit components. Neglecting the parasitic capacitances, the settling time constant becomes

$$\tau_{cr} = \frac{C_L}{G_m} \times \left(1 + \frac{C_s}{C_f} + \frac{C_s}{C_L}\right) \tag{6.17}$$

which is limited by the capacitances and the transconductance G_m of opamp. Typically, increasing G_m gives large benefit in improving the settling, while the kT/C-noise is an issue, such that the capacitor size is not reduced any more.

The kT/C-noise power of the CR-SHA is given by

$$n_{th,cr} = \frac{kT}{C_s + C_f} \tag{6.18}$$

Comparing (6.18) to (6.13) dictates that the CR-SHA has only the half of the kT/C-noise power of the CT-SHA, when they have the same values of C_s and C_f. Contrastly, the CR-SHA can have half size of C_s and C_f compared with that of the CT-SHA at the same requirement of noise performance.

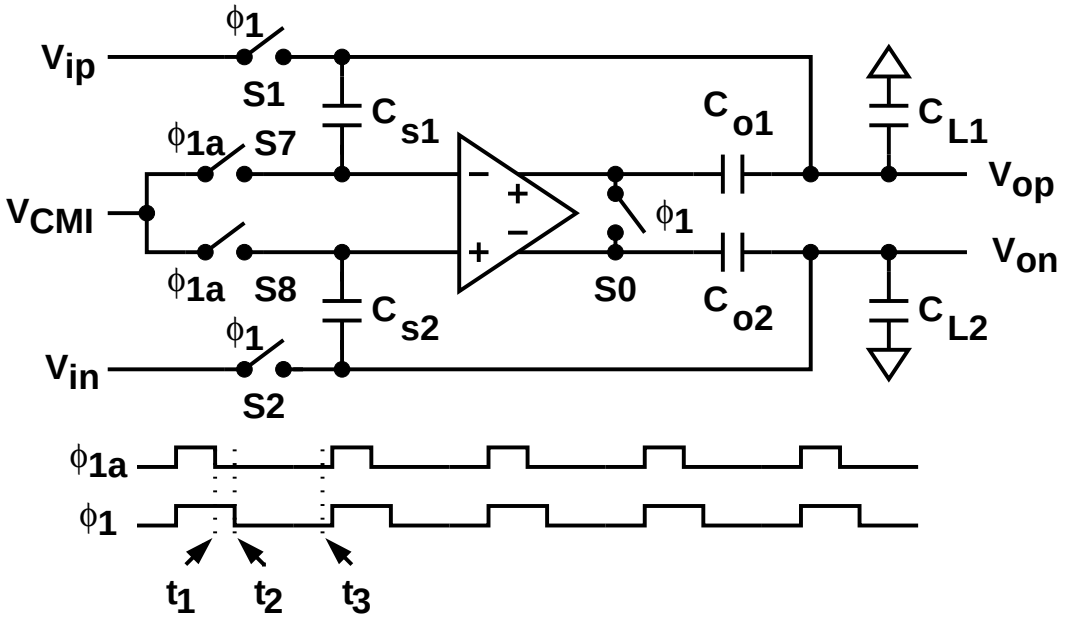


Figure 6.7: A precharged SHA.

6.5 Precharged SHA (PC-SHA)

The SHAs described in the preceded sections need high dc gain and high bandwidth opamps to achieve high-resolution and high speed. These are difficult to implement while employing the advanced technology with low voltage. A precharged SHA (PC-SHA) was therefore developed [42] to release the performance requirements of its opamp. Fig. 6.7 shows the precharged SHA with its timing diagram. It has two operating phase. During sample phase, $\phi_1 = 1$ and $\phi_{1a} = 1$, capacitors C_{s1} and C_{s2} track input signals, and the inputs also precharge output nodes V_{op} and V_{on}. This precharge operation presets the SHA's outputs, V_{op} and V_{on}, close to their respective final values in the succeeding hold-mode period, thus lessening the burden for the opamp. At sampling instant, ϕ_{1a} is going to 0, the input signals are sampled on C_{s1} and C_{s2}. During hold phase, $\phi_1 = 0$, the SHA's outputs settle to their final levels in a much shorter time period without slewing due to the precharging.

To investigate the function of the PC-SHA, simplify the operations of two phases to their corresponding single-ended schematics shown in Fig. 6.8. At t_1 instant, the charges

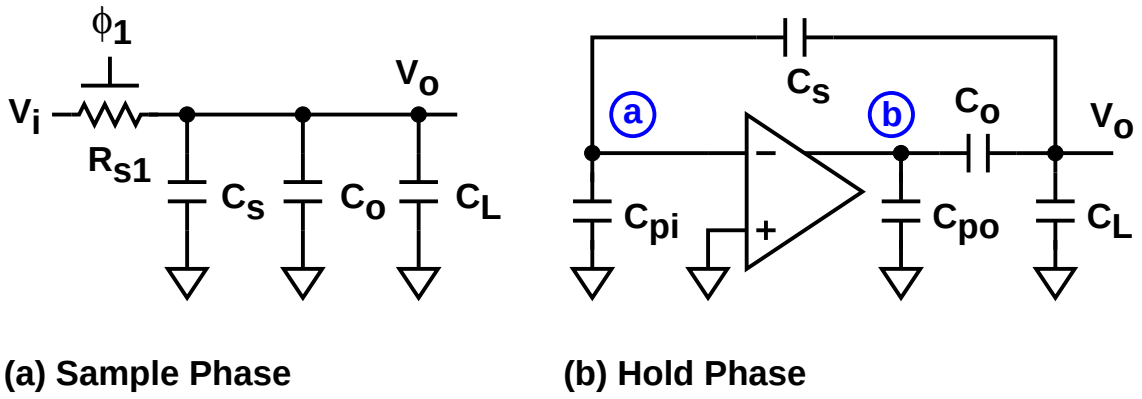


Figure 6.8: Model of the precharged SHA's operation.

stored on capacitor C_s is given by

$$Q_{C_s}(t_1) = C_s \times V_i(t_1) \tag{6.19}$$

where the opamp's input offset is ignored. At t_2 time instant, the SHA enters into the hold phase, and the charges stored on C_s do not change, and the charges stored on capacitors C_o and C_L are expressed respectively as

$$Q_{C_o}(t_2) = C_o \times V_{C_o}(t_2) \tag{6.20}$$

$$Q_{C_L}(t_2) = C_L \times V_{C_L}(t_2) \tag{6.21}$$

where $V_{C_o}(t_2)$ and $V_{C_L}(t_2)$ are the voltages stored on C_o and C_L. During the hold phase, the net charge at node a and output node do not change according to the charge conservation. At the start point of steady-state, we have

$$V_a(t_3) \times C_{pi} + [V_a(t_3) - V_o(t_3)] \times C_s = -V_i(t_1) \times C_s \tag{6.22}$$

and

$$V_b(t_3) \times C_{po} + [V_o(t_3) - V_a(t_3)] \times C_s + [V_o(t_3) - V_b(t_3)] \times C_o + V_o(t_3) \times C_L = Q_{C_s}(t_1) + Q_{C_o}(t_2) + Q_{C_L}(t_2) \tag{6.23}$$

where $V_a(t_3)$ is the voltage at opamp's negative input node a at t_3 time instant, and $V_b(t_3)$ is the voltage at opamp's output node b at t_3 time instant. Hence, $V_b(t_3)$ equals to $-A_0 \times$

$V_a(t_3)$, where A_0 is opamp's dc voltage gain. Rearranging (6.22) and (6.23) and replacing $Q_{C_s}(t_1)$, $Q_{C_o}(t_2)$ and $Q_{C_L}(t_2)$ with (6.19), (6.20), and (6.21) respectively obtain

$$\begin{aligned} V_o(t_3) &= V_i(t_1) + \frac{C_{pi} \times V_i(t_1)}{A_0(C_o - C_{po})} + \left(\frac{V_{C_o}(t_2)}{A_0} \times \frac{C_o}{C_o - C_{po}} \times \frac{C_s + C_{pi}}{C_s} \right) \\ &+ \left(\frac{V_{C_L}(t_2)}{A_0} \times \frac{C_L}{C_o - C_{po}} \times \frac{C_s - C_{pi}}{C_s} \right) - \left(\frac{V_o(t_3)}{A_0} \times \frac{C_o + C_L}{C_o - C_{po}} \right) \\ &- \left(\frac{V_o(t_3)}{A_0} \times \frac{C_{pi}}{C_o - C_{po}} \times \frac{C_s + C_o + C_L}{C_s} \right) \end{aligned} \tag{6.24}$$

Assume $C_{pi} \to 0$ and $C_{po} \to 0$, $V_o(t_3)$ of (6.24) then approximates as

$$V_o(t_3) \approx V_i(t_1) \left[1 + \frac{1}{A_0} \left(\frac{V_{C_o}(t_2)}{V_i(t_1)} - 1 \right) + \frac{1}{A_0} \frac{C_L}{C_o} \left(\frac{V_{C_L}(t_2)}{V_i(t_1)} - 1 \right) \right] \tag{6.25}$$

Clearly, the output error is determined by opamp's dc voltage gain A_0, and the voltage ratios of

$$\begin{cases} V_{C_o}(t_2)/V_i(t_1) \\ V_{C_L}(t_2)/V_i(t_1) \end{cases}$$

For the accuracy of 15-bit, the output error needs to be less than $1/2^{15}$; that is

$$\left| \frac{1}{A_0} \left(\frac{V_{C_o}(t_2)}{V_i(t_1)} - 1 \right) + \frac{1}{A_0} \frac{C_L}{C_o} \left(\frac{V_{C_L}(t_2)}{V_i(t_1)} - 1 \right) \right| < \frac{1}{2^{15}}$$

Assume $[V_{C_o}(t_2)/V_i(t_1)] = [V_{C_L}(t_2)/V_i(t_1)] = 0.95$, and $C_L = C_o$, the voltage gain A requires only 70 dB that is 22 dB smaller than the gain requirement of a FA-SHA's opamp. According to (6.25), the requirement of A_0 can be dramatically reduced as both $V_{C_o}(t_2)/V_i(t_1)$ and $V_{C_L}(t_2)/V_i(t_1)$ are very closed to 1.

Due to the precharging operation, the opamp's output voltage change is given by

$$\Delta V_{o,op} = [V_i(t_1) - V_{C_o}(t_2)] + \frac{C_L}{C_o} \times [V_i(t_1) - V_{C_L}(t_2)] \tag{6.26}$$

which shows that increasing C_o reduces $\Delta V_{o,op}$. However, increasing C_o increases the input capacitive load. Thus, the combination of output capacitor coupling and precharging also reduces the opamp's output voltage swing requirement, which leads to lower distortion.

During the hold phase, the PC-SHA has a feedback factor expressed as

$$\beta_{pc} = \frac{C_o}{C_o + [C_L + (C_s || C_{pi})]} \times \frac{C_s}{C_s + C_{pi}} \tag{6.27}$$

Rearranging (6.27) obtains the relationship between β_{pc} and β_{fa} that is given by

$$\beta_{pc} = \frac{\beta_{fa}}{1 + \frac{C_L}{C_o} + \frac{(C_s||C_{pi})}{C_o}} < \beta_{fa}$$

Furthermore, the PC-SHA's settling time constant can be obtained by

$$\tau_{pc} = \frac{C_{po} + [C_L + (C_s||C_{pi})] \times (1 + \frac{C_{po}}{C_o})}{G_m} \times \frac{C_s + C_{pi}}{C_s} \tag{6.28}$$

Comparing (6.28) to (6.4) obtains

$$\tau_{pc} = \tau_{fa} + \frac{\frac{C_{po}}{C_o} \times [C_L + (C_s||C_{pi})]}{G_m} \times \frac{C_s + C_{pi}}{C_s} > \tau_{fa}$$

which indicates that the speed penalty appears due to the output coupling capacitor C_o, and it can be alleviated by increasing the value of C_o.

The kT/C-noise of the PC-SHA is given by

$$n_{th,pc} = \frac{kT}{C_s + C_o + C_f} \tag{6.29}$$

Hence, the SNR for a sinusoidal signal with a full-scale amplitude of $V_{FS}/2$ is given by

$$SNR_{th,pc} = \frac{(V_{FS}/2)^2/2}{(kT/C_s + C_o + C_L)} = \frac{V_{FS}^2 \times (C_s + C_o + C_L)}{8kT} \tag{6.30}$$

The PC-SHA has better kT/C-noise performance than the FA-SHA, since it has larger effective sampling capacitance if they have the same value of C_s.

6.6 Proposed Buffered-Precharged SHA (BP-SHA)

Although the PC-SHA can significantly release the opamp's requirements, it is inappropriate for a TI-ADC's implementation due to the drawback figured out in the end of the last section. In this work, a buffered-precharged SHA (BP-SHA) is developed to reduce the influence of the input networks mismatches among A/D channels of a TI-ADC.

Fig. 6.9 shows the circuit schematic of the BP-SHA. During the sample mode, $\phi_1 = 1$ and $\phi_{1a} = 1$, the inputs not only drive the C_{s1} and C_{s2} sampling capacitors, but also precharge the SHA's output nodes through the $B1$ and $B2$ buffers. When switching to the

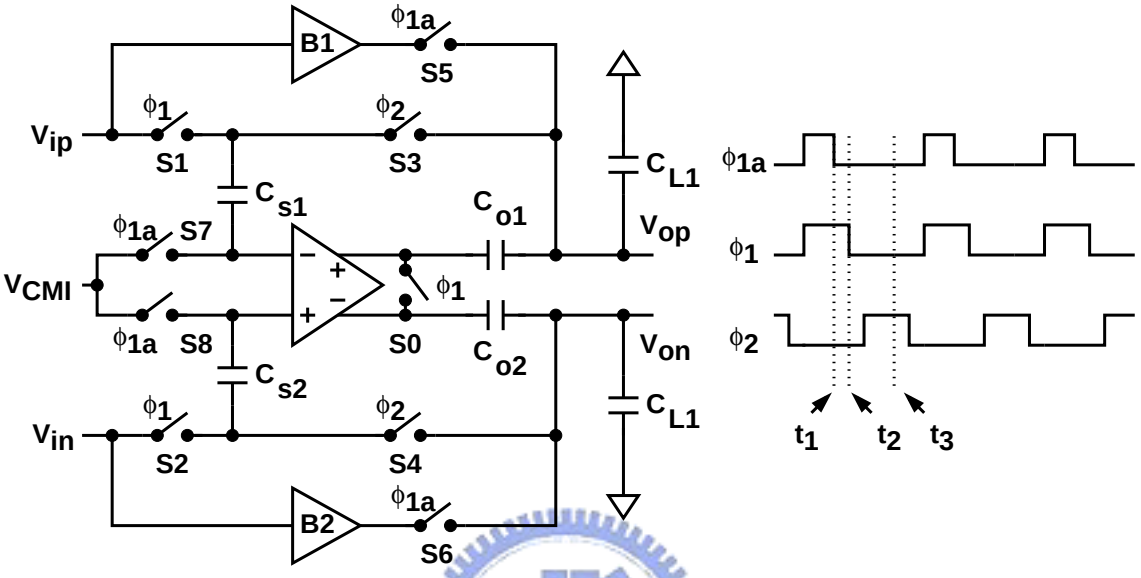


Figure 6.9: A BP-SHA.

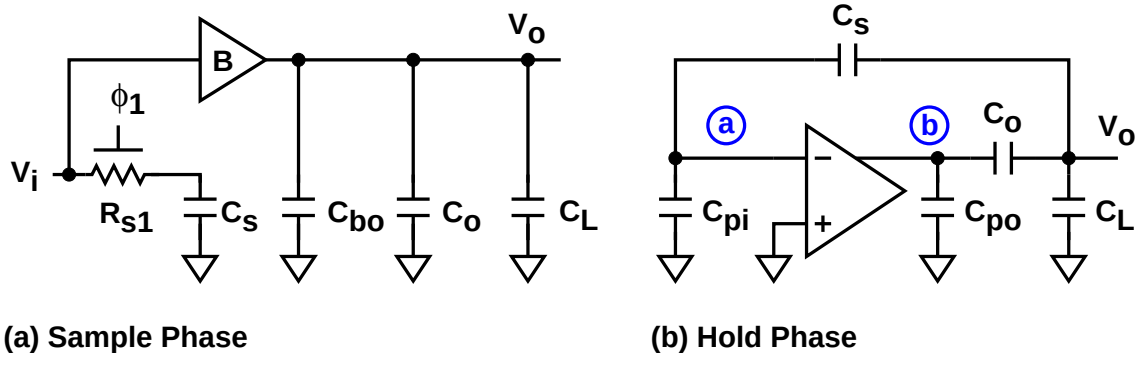


Figure 6.10: Single-ended configuration of the BP-SHA's operations.

hold mode ($\phi_2 = 1$), the opamp's outputs can settle to their final values in a much shorter time period without slewing due to precharging.

To analyze the BP-SHA's operating behavior, the corresponding single-ended configuration of the BP-SHA is presented in Fig. 6.10. During sample phase, input V_i drives capacitor C_s and precharges capacitors C_o and C_L through the buffer (B). During hold phase, the charges on node a and output node do not change due to charge conservation. Therefore, we have

$$V_a(t_3) \times C_{pi} + C_s \times [V_a(t_3) - V_o(t_3)] = -C_s V_i(t_1) \tag{6.31}$$

and

$$\begin{aligned} C_s \times [V_o(t_3) - V_a(t_3)] + C_o \times [V_o(t_3) - V_b(t_3)] + C_L \times V_o(t_3) \\ = C_o \times V_{C_o}(t_2) + C_L \times V_{C_L}(t_2) \end{aligned} \tag{6.32}$$

where V_a and V_b are the opamp's input and output voltages, $V_a = -V_b/A_0$. Solving $V_o(t_3)$ from (6.31) and (6.32) obtains

$$\begin{aligned} V_o(t_3) = V_i(t_1) &+ \frac{C_s + C_{pi}}{A_0 \times C_s} \times [V_{C_o}(t_2) - V_o(t_3)] \\ &+ \frac{(C_s + C_{pi}) \times C_L}{A_0 \times C_o \times C_s} \times [V_{C_L}(t_2) - V_o(t_3)] \\ &+ \frac{C_s \times [V_o(t_3) - V_i(t_1)]}{A_0 \times C_o} \end{aligned} \tag{6.33}$$

If the C_{pi} parasitic capacitance is ignored, and $V_o(t_3) \to V_i(t_1)$ at the steady state. Then, $V_o(t_3)$ can be re-expressed as

$$V_o(t_3) \approx V_i(t_1) \times \left[1 + \frac{1}{A_0} \times \left(\frac{V_{C_o}(t_2)}{V_i(t_1)} - 1\right) + \frac{1}{A_0}\frac{C_L}{C_o} \times \left(\frac{V_{C_L}(t_2)}{V_i(t_1)} - 1\right)\right] \tag{6.34}$$

which is the same as (6.25). Furthermore, the opamp's output voltage change also has the same result as (6.26). Therefore, the BP-SHA has the same advantages as the PC-SHA shown in Fig. 6.7 for its opamp, but its sampled voltage onto capacitor C_s is not affected by the input networks of A/D channels when it is used for a TI-ADC.

During the hold phase, the BP-SHA has a feedback factor expressed as

$$\beta_{bp} = \frac{C_o}{C_o + [C_L + (C_s || C_{pi})]} \times \frac{C_s}{C_s + C_{pi}} \tag{6.35}$$

and the settling time constant given by

$$\tau_{bp} = \frac{1}{\beta_{bp} \times \omega_{u,bp}} = \frac{C_{po} + [C_L + (C_s||C_{pi})] \times \left(1 + \frac{C_{po}}{C_o}\right)}{G_m} \times \frac{C_s + C_{pi}}{C_s} \tag{6.36}$$

Since (6.35) and (6.36) are the same as (6.27) and (6.28), the BP-SHA has similar behavior as the PC-SHA during the hold phase.

The kT/C-noise power of the sampling circuits of the BP-SHA is given by

$$n_{th,bp} = \frac{kT}{C_s} \tag{6.37}$$

If the kT/C noise is considered as the only noise source, the SNR of BP-SHA for a sinusoidal signal with a full-scale amplitude of $V_{FS}/2$ is given by

$$SNR_{th,bp} = \frac{(V_{FS}/2)^2/2}{kT/C_s} = \frac{V_{FS}^2 \times C_s}{8kT} \tag{6.38}$$

which is the same as that of the FA-SHA.

6.7 The PC-SHA and BP-SHA in a TI-ADC

Although the time constant for the PC-SHA to settle during the hold mode is larger than that for a traditional flip-around SHA, the overall settling time of the PC-SHA is shorter, since it takes less number of time constant for the opamp to reach the voltage change of (6.26) if $V_{co}/V_i \approx 1$ and $V_{cl}/V_i \approx 1$ [42]. If a maximum slew rate for the opamp's outputs is imposed, the settling time advantage of the PC-SHA is greater, since its reduced output swing also mitigates the slew-rate effect.

Conclusively, the PC-SHA has loosened requirements in opamp's dc voltage gain and output swing. The alleviated opamp's specifications make the PC-SHA suitable for implementing in the front-end of a high-resolution, high-speed ADC. However, when it is employed in a TI-ADC, its performance is degraded due to the mismatches of input networks of A/D channels.

Fig. 6.11 shows the PC-SHA accompanying with the input networks of a 2-channel TI-ADC. S3$-C_{L1}$ and S4$-C_{L2}$ are the input network of channel 1. S5$-C_{L3}$ and S6$-C_{L4}$ are that of channel 2. To investigate the influences on the precharged SHA's performance,

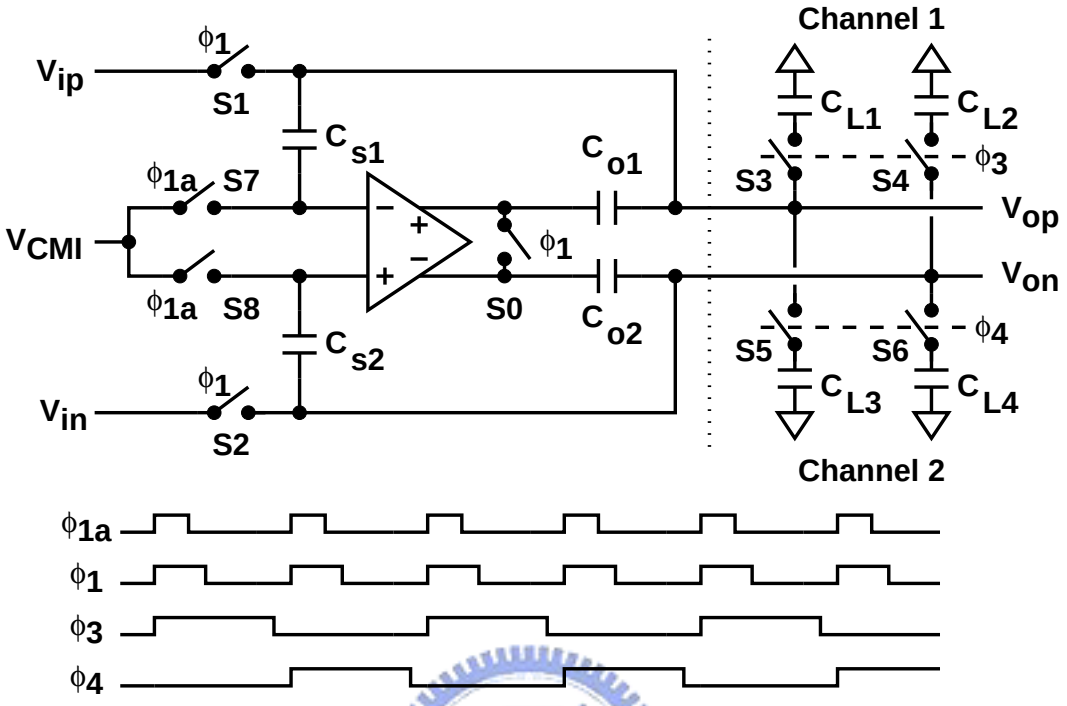


Figure 6.11: The PC-SHA with the input networks of a TI-ADC.

the single-ended schematic with two operating modes is shown in Fig. 6.12. The S3 and S5 switches are modeled as two voltage-controlled resistors, R_{S3} and R_{S5}. During ϕ_3 sample phase, the $R_{S3} - C_{L1}$ network is connected to the V_o node. During ϕ_4 sample phase, the $R_{S5} - C_{L3}$ network is connected to the V_o node. If there are mismatches between the $R_{S3} - C_{L1}$ and $R_{S5} - C_{L3}$ networks, the $V_i - \text{to} - V_o$ frequency response in the sample mode is varied when the SHA alternates between ϕ_3 and ϕ_4 phase. Furthermore, when the SHA is being switched from the sample mode to the hold mode, charges are injected into the V_o node with S1 switch being turned off. If there are mismatches between the $R_{S3} - C_{L1}$ and $R_{S5} - C_{L3}$ networks, the amount of V_o change due to the charge injection in the ϕ_3 phase is different from that in the ϕ_4 phase.

The effect of the output network variation as the SHA being switched between the ϕ_3 and ϕ_4 phases is manifested as a spurious tone at $f_s/2 - f_{in}$ in the SHA's output frequency spectrum, where f_s is the sampling frequency and f_{in} is the frequency of a single-tone input.

When the BP-SHA is used as the front-end of a TI-ADC, its behavior is examined

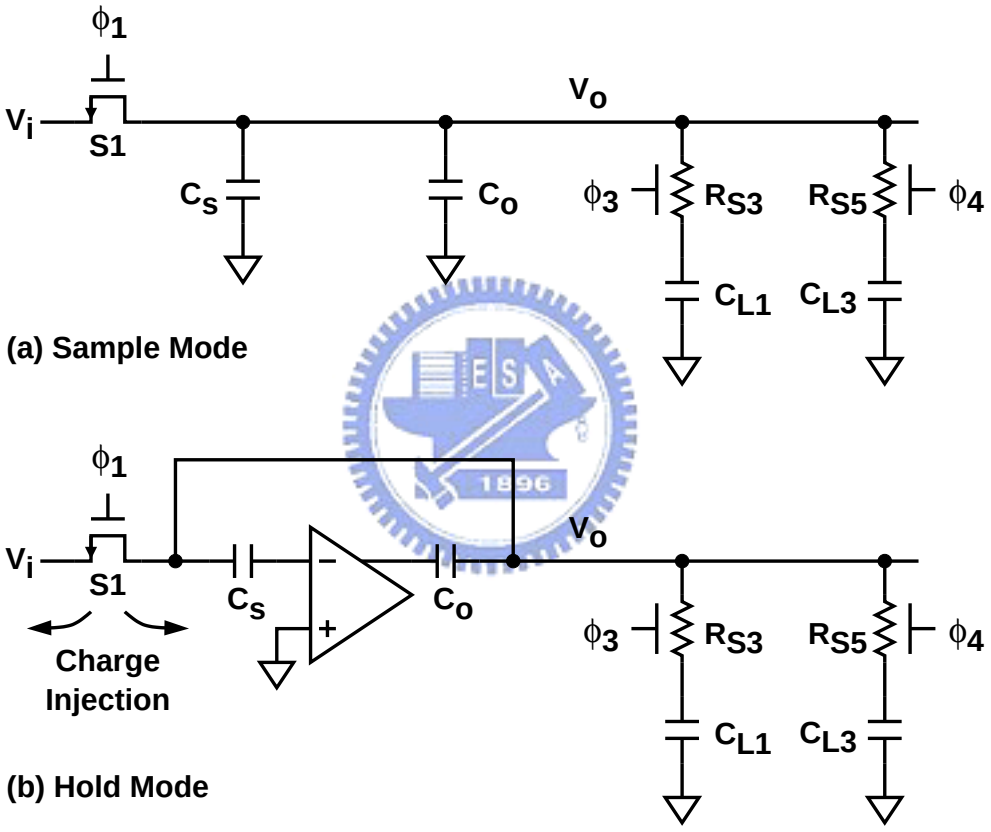


Figure 6.12: PC-SHA's operation in a 2-channel TI-ADC.

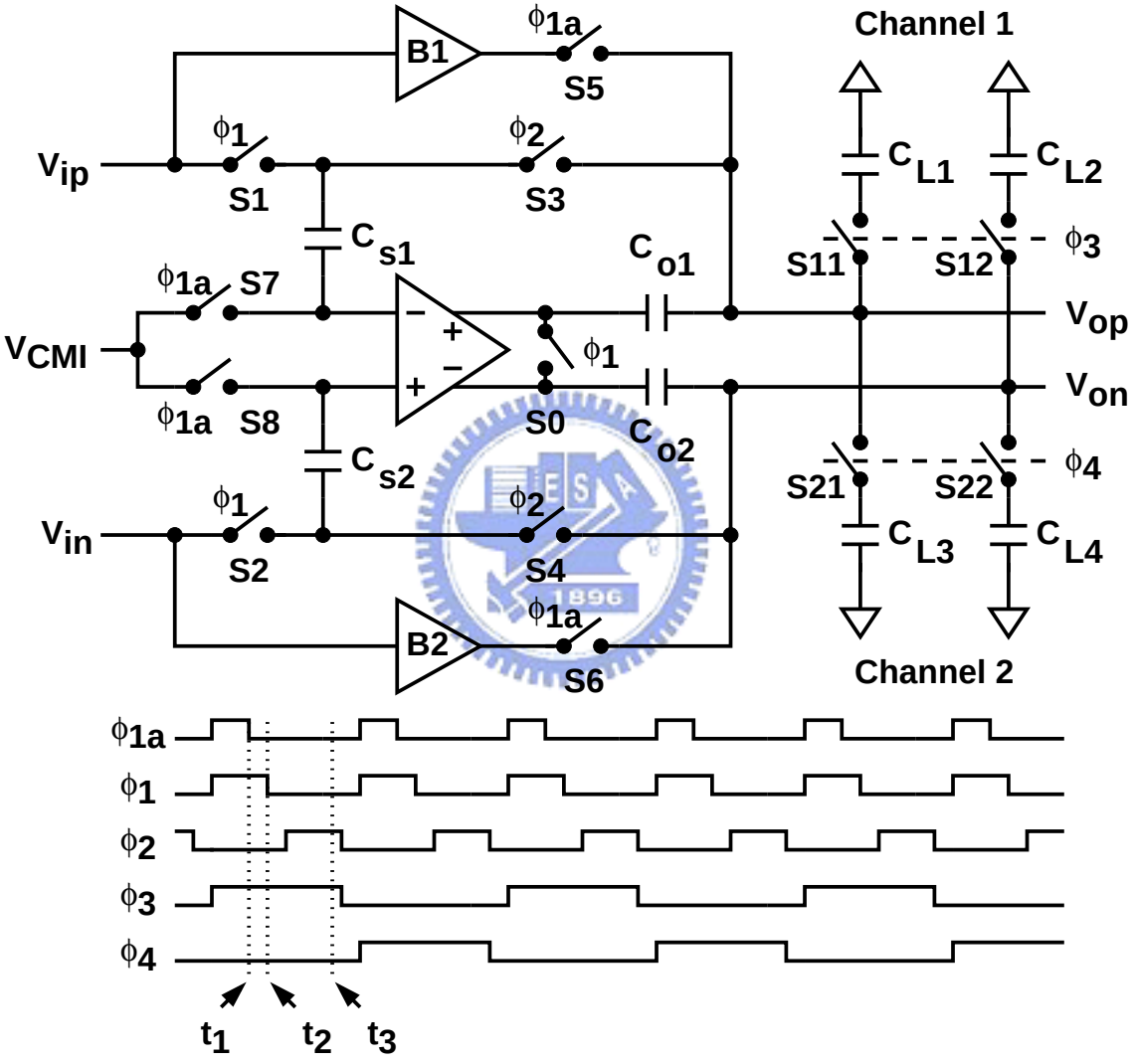


Figure 6.13: The BP-SHA with CHP1 and CHP2 choppers.

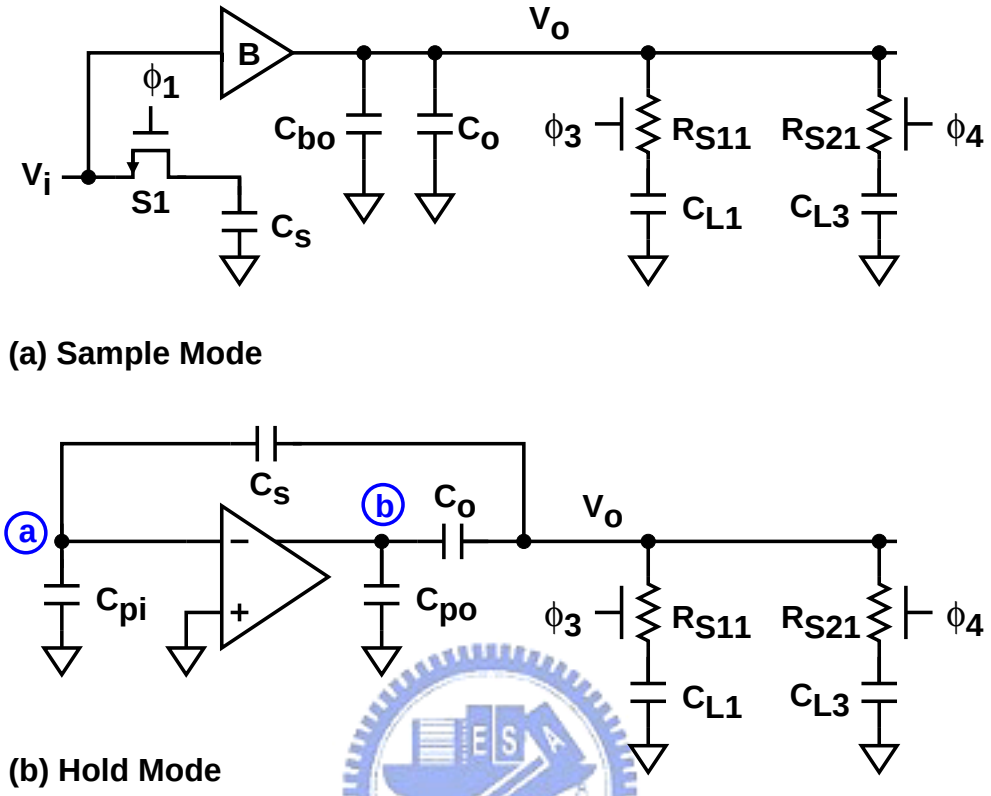


Figure 6.14: BP-SHA's operation in a 2-channel TI-ADC.

using a 2-channel TI-ADC as an example. Fig. 6.13 shows the BP-SHA with the input networks of the two A/D channels. During the channel-1 sample mode, $\phi_1 = 1$, $\phi_{1a} = 1$, and $\phi_3 = 1$, the inputs not only drive the C_{s1} and C_{s2} sampling capacitors, but also precharge the SHA's output nodes including the input capacitive loads of channel 1. When switching to the hold mode ($\phi_2 = 1$), the opamp's outputs can settle to their final values in a much shorter time period without slewing due to precharging. The effect of the mismatches between the two channels during the sample mode is reduced since the input nodes V_{ip} and V_{in} of the SHA are isolated from the sampling networks of the A/D channels by B_1 and B_2. During the channel-2 sample mode, $\phi_1 = 1$, $\phi_{1a} = 1$, $\phi_4 = 1$, the input capacitive loads of channel 2 are precharged alternately.

To examine the effect of the mismatches among A/D channel on the outputs of the PC-SHA and BP-SHA, the HSPICE simulation is done for both the schematics of Fig. 6.12 and Fig. 6.14. Fig. 6.12 and Fig. 6.14 are the models of the single-end configuration of

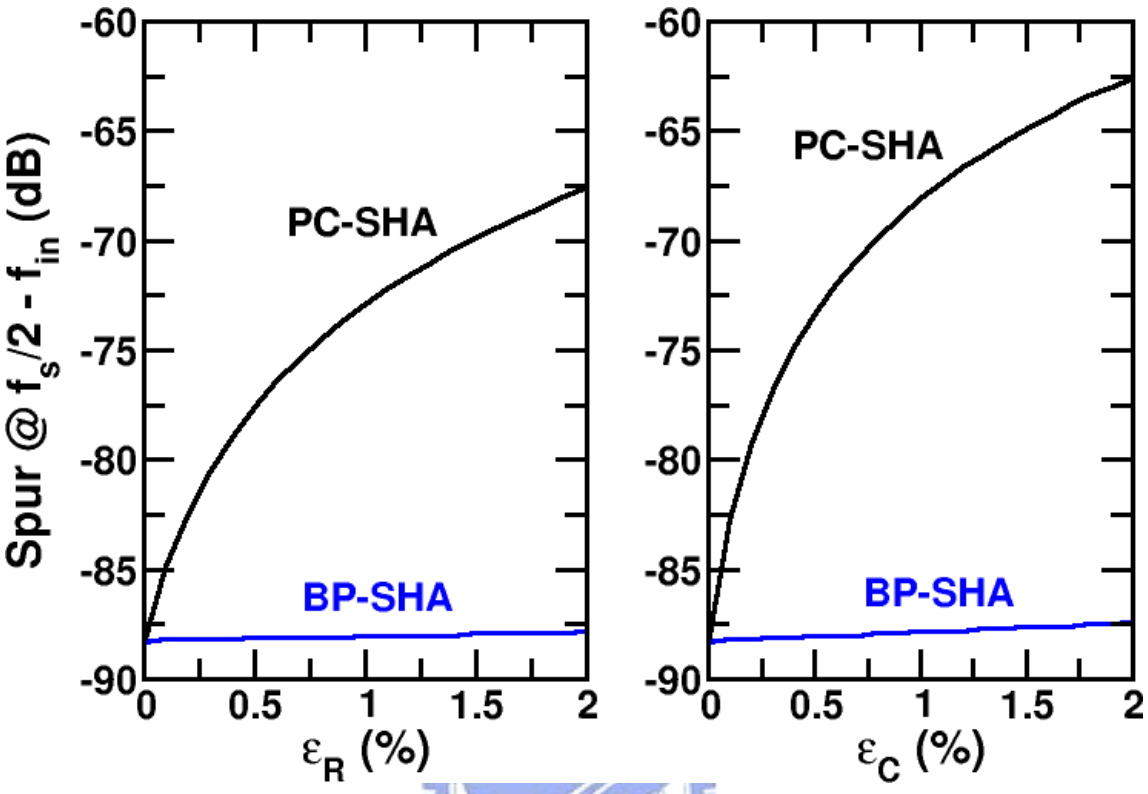


Figure 6.15: Simulation results for the PC-SHA and BP-SHA at various mismatches.

the PC-SHA and BP-SHA respectively.

Fig. 6.15 shows the magnitude of the spurious tone relative to the single-tone signal in the circuit simulations. The square symbols represents the simulation results of Fig. 6.12. It is assumed that $f_s = 125$ MHz, $f_{in} = 60.9$ MHz, $C_s = 4$ pF, $C_o = 6$ pF, $R_{S3} = (1 + \varepsilon_R/2)R$, $R_{S5} = (1-\varepsilon_R/2)R$, $C_{L1} = (1+\varepsilon_C/2)C$ and $C_{L3} = (1-\varepsilon_C/2)C$, where $R = 60\ \Omega$ and $C = 4$ pF. It is also assumed that the opamp is ideal. The S1 switch is realized with a 0.18 μm n-channel MOSFET with $W = 64$ μm and $L = 0.18$ μm. A constant-V_{gs} bootstrapping circuit is used for gate control [2]. The mismatches between the R_{S3}-C_{L1} and R_{S5}-C_{L3} networks of Fig. 6.12 are represented by ε_R and ε_C. It is required that $\varepsilon_R < 0.001$ and $\varepsilon_C < 0.001$ in order to make this spurious tone be less than -85 dB. The similar parameters are applied to the circuit simulation of Fig. 6.14 except that $R_{S11} = (1 + \varepsilon_R/2)R$ and $R_{S21} = (1 - \varepsilon_R/2)R$. The simulation results of are shown as the circle symbols in Fig. 6.15. The simulation results clearly indicate that the mismatches between the SHA's output networks have little influence on the BP-SHA's performance when it

Table 6.1: Summary of SHAs

Type	Closed-loop DC Gain	Feedback Factor (β)	Time Constant (τ)	kT/C Noise
FA-SHA	1	$\frac{C_s}{C_s+C_{ip}}$	$\frac{C_sC_L+C_sC_{ip}+C_{ip}C_L}{G_mC_s}$	$\frac{kT}{C_s}$
CT-SHA	$\frac{C_s}{C_f}$	$\frac{C_f}{C_s+C_f+C_{ip}}$	$\frac{C_fC_L+(C_f+C_L)(C_s+C_{ip})}{G_mC_f}$	$\frac{kT}{C_s}$
CR-SHA	$1+\frac{C_s}{C_f}$	$\frac{C_f}{C_s+C_f+C_{ip}}$	$\frac{C_fC_L+(C_f+C_L)(C_s+C_{ip})}{G_mC_f}$	$\frac{kT}{C_s+C_f}$
PC-SHA	1	$\frac{C_o}{C_o+[C_L+(C_s\|\|C_{pi})]}\times\frac{C_s}{C_s+C_{pi}}$	$\frac{C_{po}+[C_L+(C_s\|\|C_{pi})]\times(1+\frac{C_{po}}{C_o})}{G_m}\times\frac{C_s+C_{pi}}{C_s}$	$\frac{kT}{C_s+C_o+C_L}$
BP-SHA	1	$\frac{C_o}{C_o+[C_L+(C_s\|\|C_{pi})]}\times\frac{C_s}{C_s+C_{pi}}$	$\frac{C_{po}+[C_L+(C_s\|\|C_{pi})]\times(1+\frac{C_{po}}{C_o})}{G_m}\times\frac{C_s+C_{pi}}{C_s}$	$\frac{kT}{C_s}$

being switched between the ϕ_3 and ϕ_4 phases. Therefore, the BP-SHA is well suitable for employing in a TI-ADC.

6.8 Summary

Table 6.1 shows the comparisons of the previously described SHAs, where G_m is the transconductance of opamp, and C_L is SHA's loading capacitance. The CT-SHA and CR-SHA can amplify input signal, but others are not. The FA-SHA has larger feedback factor than others. The flip-around SHA also has smaller time constant, hence it settles faster. Since the outputs of the FA-SHA, CT-SHA and CR-SHA are needed to reset to zero at their sampling phase, they require high slewing rate in their opamps and consume large power. Therefore, they are difficult to implement due to the crucial specifications of opamps when they are employed as the front-end in high-resolution, high-speed TI-ADCs.

The PC-SHA and BP-SHA have the same feedback factor, and settling time constant. The PC-SHA has better kT/C-noise performance because it has the equivalent sampling capacitance equaling to $C_s + C_o + C_L$. On the contrary, it has large input capacitance loading the input driving circuits. The BP-SHA has the similar settling behavior as the PC-SHA during the hold phase, but has small equivalent input capacitance, thus, lessening

the burden for the driving circuits of the SHA. In addition, the proposed SHA also reduces the influence of mismatches of a TI-ADC's input networks. Therefore, it is favorable for TI-ADCs.

Chapter 7

A 15-bit 125 MS/s Time-Interleaved Pipelined Analog-to-Digital Converter

7.1 Introduction

The 15-bit 125 MS/s TI-ADC's prototype presented here utilizes a front-end BP-SHA and digital background calibration to overcome the timing skew, gain, and offset mismatches between A/D channels, as well as the nonlinearity resulted from capacitor mismatch. This prototyping ADC was implemented using 0.18 μm CMOS logic process with metal-insulator-metal (MIM) capacitors. It can achieve a spurious free dynamic range (SFDR) greater than 85 dBc over a band up to the Nyquist frequency at a 1.8 V supply.

This chapter addresses in describing the functional blocks of this prototype. The design parameters corresponding to key circuits are also presented. Then, the experimental results are shown to demonstrate the ADC's performance. Finally, the comparisons with other related works are discussed.

7.2 ADC's Architecture

The block diagram of the 15-bit 125-MS/s TI-ADC is depicted in Fig. 7.1. It consists of a single front-end SHA and two identical pipeline A/D channels, both of which operate at 62.5 MS/s. The use of a single SHA avoids the sampling skew errors between the two

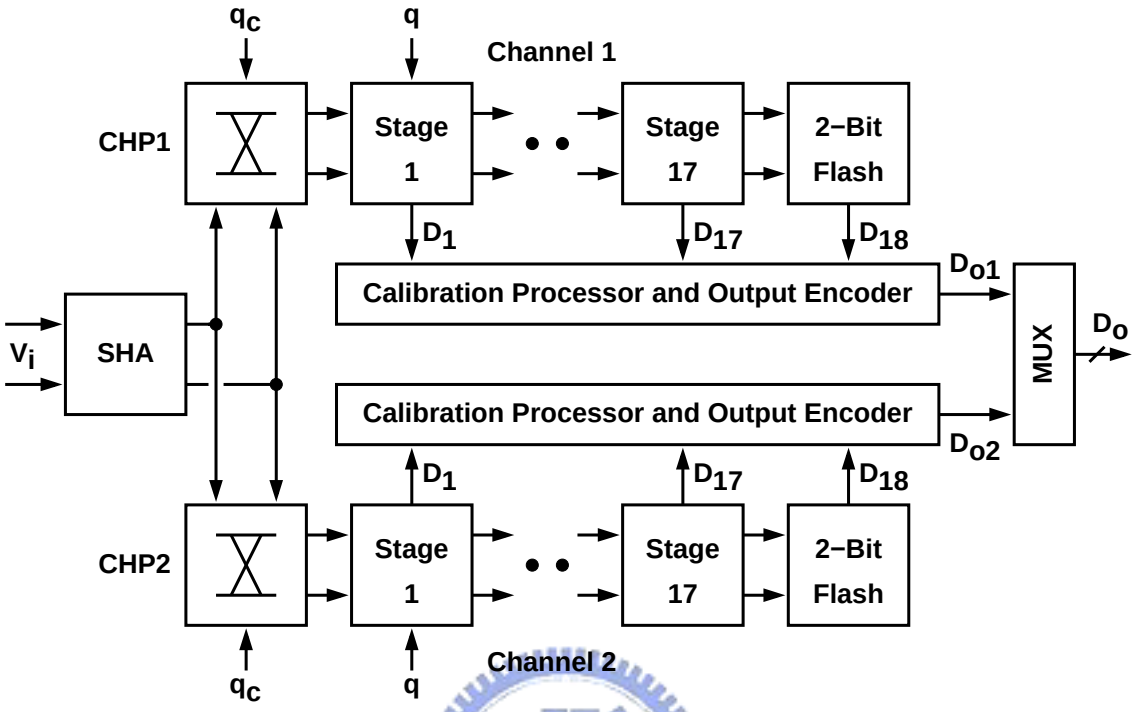


Figure 7.1: Time-interleaved pipeline ADC with single SHA.

channels. Each channel consists of 6 split-capacitor 1.5-bit stages followed by eleven 1.5-bit stages and a 2-bit flash giving 19 bits raw digital output. The raw output is then processed by using the digital calibration technique to compensate the nonlinearity within the channel, caused by capacitor mismatches and finite opamp's dc gain, as well as to remove the gain and offset mismatches between the channels. The final digital output is then obtained by multiplexing the channel outputs after the calibration processing.

The two random choppers, CHP1 and CHP2, are placed in front of the A/D channels to time interleave the SHA's outputs and also calibrate the overall offsets of the A/D channels [7]. The choppers are controlled by a binary-valued random sequence, q_c, which has the maximum length of 2^{28} for a calibration iteration.

7.3 Front-end SHA

At high input frequencies, the ADC's performance is predominantly set by the front-end SHA. Fig. 7.2 shows the front-end SHA accompanying with the CHP1 and CHP2 chop-

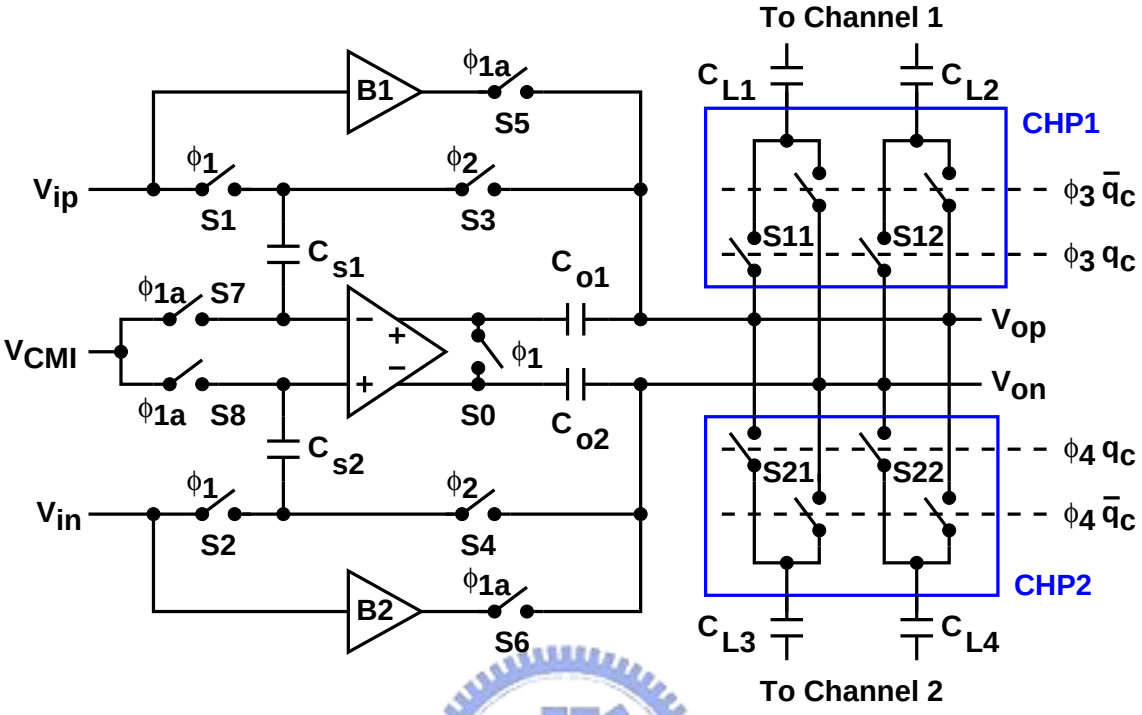


Figure 7.2: BP-SHA with CHP1 and CHP2 choppers.

pers in the TI-ADC implementation. This SHA samples the input using the ϕ_1 clock with sampling rate at f_s. The choppers consist of analog switches controlled by either ϕ_3 or ϕ_4 clocks with frequency at $f_s/2$. Their outputs are inverted when $q_c = 0$. To maintain high sampling linearity, the $S1$ and $S2$ switches are designed using the bootstrapped switches [2], while other switches using the CMOS switch. According to (6.38), to achieve a resolution up to 15 bits, the sampling capacitance C_{s1} and C_{s2} requires 52.5 pF for $V_{FS} = 1$ V, if only the kT/C-noise is considered. This value is rarely realized since it is a heavy load to the SHA's input driving circuits. The C_{s1} and C_{s2} capacitance are hence chosen as 4 pF, and theoretically only 81 dB SNR can be achieved at $V_{FS} = 1$ V. Furthermore, increase V_{FS} to improve the SNR. The sub-circuits, the bootstrapped switch and buffer, are described in the following. The opamp's design is presented later in Section 7.4, while it has the same configuration as that used in the pipeline stages.

The primary factor determining the sampling linearity is the signal dependent on-resistance of the input switches. This problem can be overcome by making the switch's on-resistance constant by applying bootstrapping to the input switch [2] [48]. Fig. 7.3

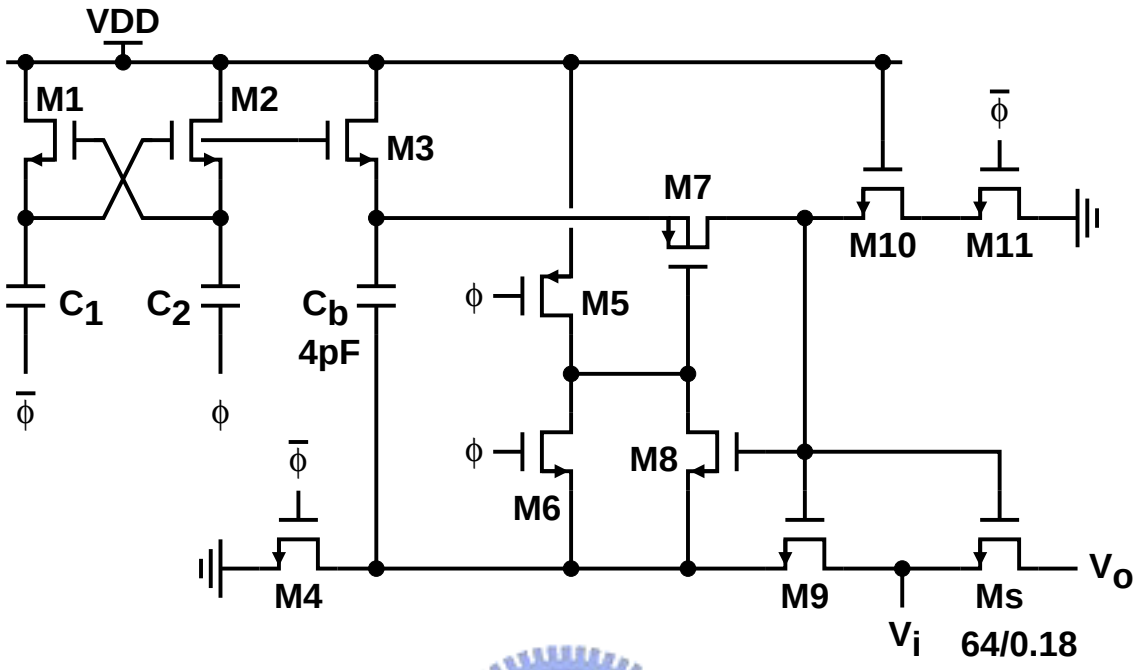


Figure 7.3: Bootstrapped switch [2].

shows the constant-V_{GS} bootstrapped switch [2] employed as the input sampling MOS switches in this design to maintain the reliability of the these MOS devices. The gate controlled voltage of the Ms switch is boosting along with the input V_i to keep its gate-to-source voltage as a constant, and hence the distortion caused from on-resistance is reduced. The C_b boosting capacitor is chosen to have a value of 4 pF to decrease the effect of the thermal noise for the high resolution requirement.

To perform the precharging, the B1 and B2 unity-gain buffers are introduced in the proposed SHA of Fig. 6.9. The schematic of the buffers is shown in Fig. 7.4. It is a simple

Table 7.1: Device Sizes of Buffer

Device	Size (μm/μm)
M1-M2	600/0.18
M3-M4	400/0.18
I_B	7 mA

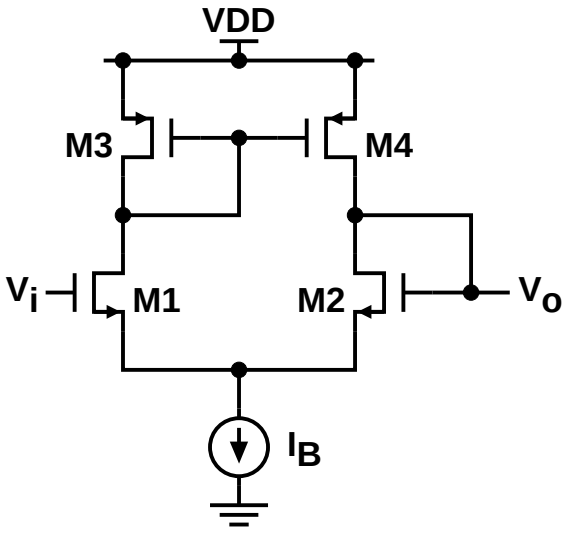


Figure 7.4: Unity-gain buffer for BP-SHA.

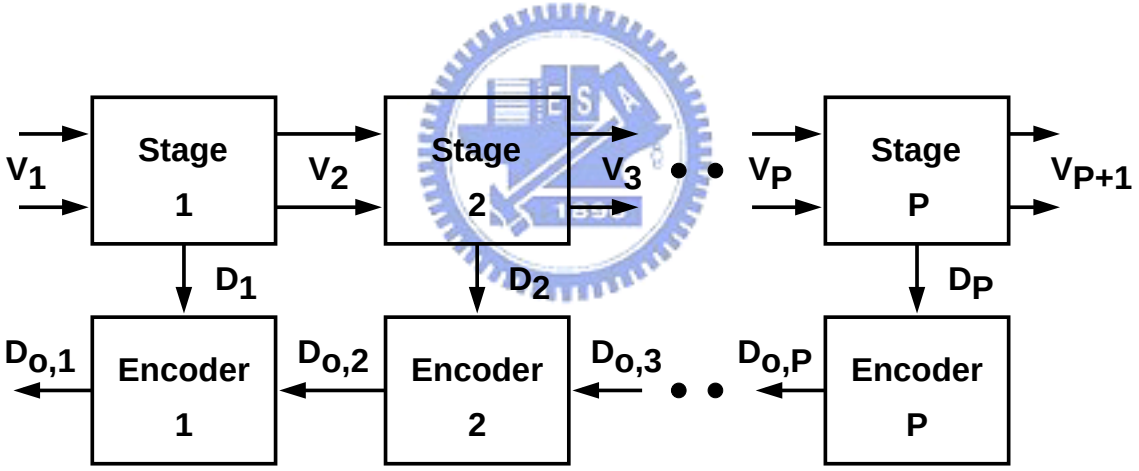


Figure 7.5: Block diagram of the single A/D channel.

single-stage amplifier with an open-loop dc voltage gain of 32 dB. Each buffer dissipates 12.96 mW of power while driving a total output capacitive load of 7 pF, and has a unity-gain frequency of 2.3 GHz and a slew rate of 1 V/nsec. The behavior of the buffers can deviate from an ideal one due to the offset and low open-loop voltage gain of the amplifier. This non-ideal buffer behavior is not crucial, but the deviation results in a less accurate precharge operation. The device sizes of the buffer design are shown in Table 7.1.

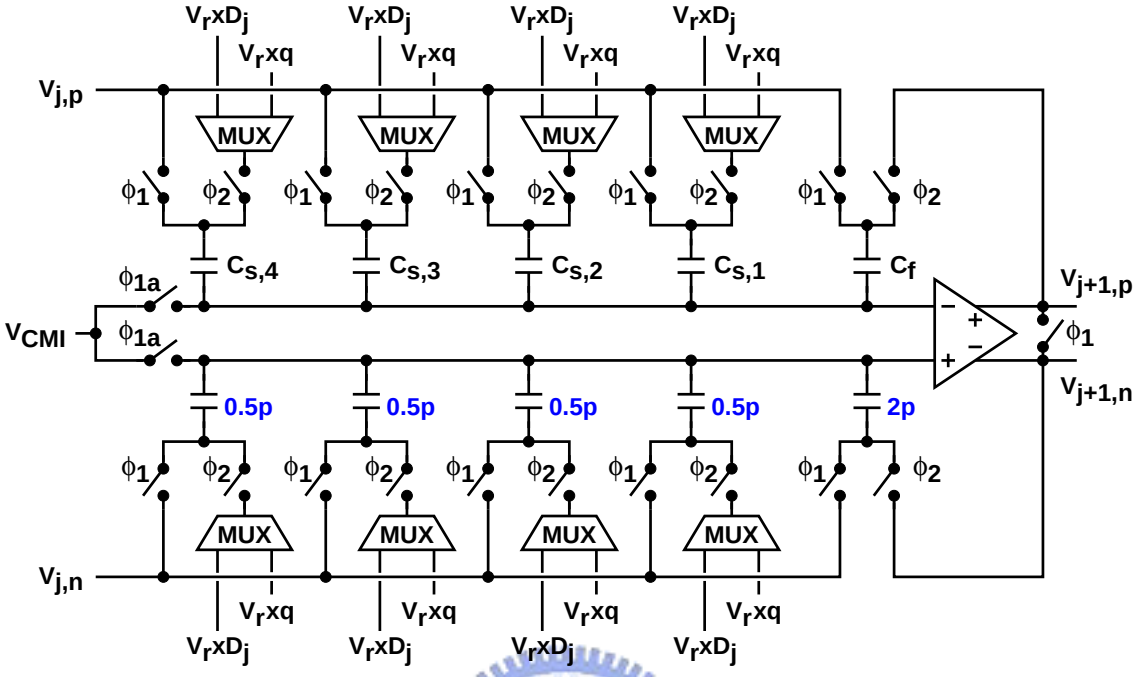


Figure 7.6: 1.5-bit fully differential MDAC for calibration.

7.4 Pipelined A/D Channel

Fig. 7.5 shows the block diagram of the single channel of the prototyping ADC. All signals are realized in differential mode. The first six stages are calibrated using the split-capacitor radix-2 1.5-bit SC pipeline stage. The first six stages use the identical opamps and capacitors. The opamps and capacitors are reduced by half in the next five stages. Another scaling by half is applied to the remaining stages.

Fig. 7.6 shows the fully differential schematic of the 1.5-bit SC MDAC of the first six stages under calibration. The C_s and C_f capacitors have a value of 2 pF, and C_s is equally divided into 4 small capacitor segments. Each small capacitor, $C_{s,i}$, $i \in \{1, 2, 3, 4\}$, therefore has a value of 0.5 pF. During the sampling phase, all capacitors track the inputs, and the opamp's outputs are reset to its common mode. At the sampling instant, the inputs are sampled on these capacitors with bottom-plate sampling. During hold phase, one of which $C_{s,i}$ is connected to $V_r \times q$ depends on the controlling signal of the multiplexer (MUX) from the calibration processor, and other $C_{s,i}$'s are connected to $V_r \times D_j$. Fig. 7.7 shows the fully differential configuration of the conventional 1.5-bit SC MDAC employed

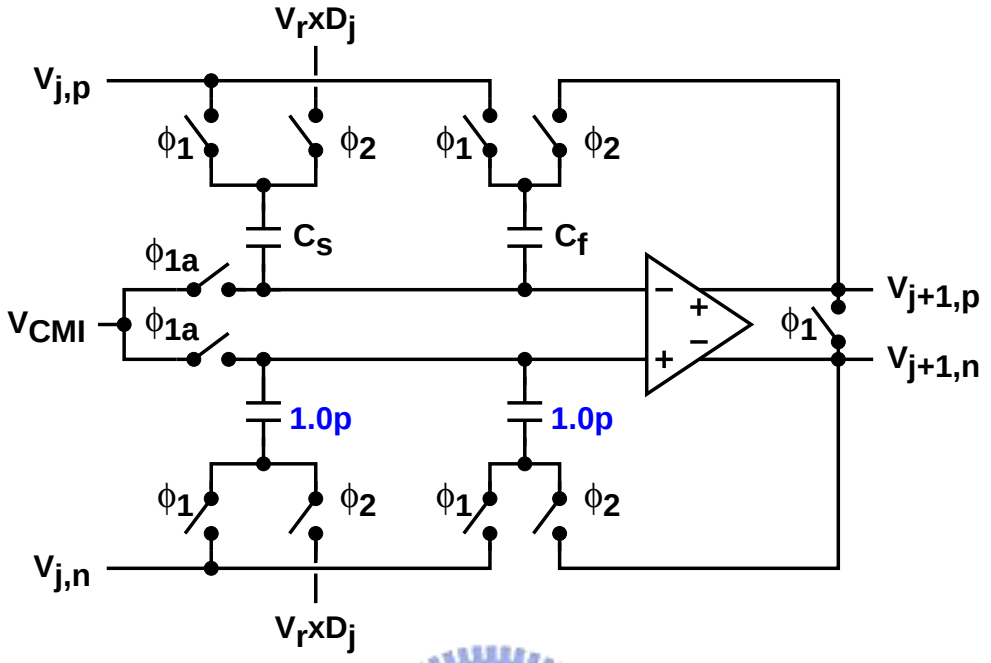


Figure 7.7: Conventional 1.5-bit fully differential MDAC.

in the 7-th stage to the 17-th stage. The C_s and C_f capacitors from the 7-th stage to the 11-th stage equal to 1.0 pF, and they have the value of 0.5 pF from the 12-th stage to the 17-stage.

The opamp is the primary building block of the SC MDAC and the SHA. A pipeline ADC's resolution and speed are usually determined by the opamps of the pipeline stages. The schematic of the opamp used in the SHA and the pipeline stages is shown in Fig. 7.8. The fully differential two-stage configuration consists of a telescopic first stage followed by a common-source second stage [49] [50]. The C_{c1} and C_{c2} capacitors provide conventional current-buffering Miller compensation [51] [52]. The C_{c3} and C_{c4} capacitors are added to improved gain margin [53]. Two separate switched-capacitor common-mode feedback circuits are used to generate the control voltage, V_{cf1} and V_{cf2}, for the first and the second stages of the opamp respectively. The overall dc voltage gain of the opamp is more than 90 dB. The opamp of the SHA dissipates 100 mW of power and achieves a unity-gain frequency of 1.66 GHz with $C_i = 4$ pF, $C_o = 6$ pF, and $C_L = 4$ pF.

In the first pipeline stage, the opamp dissipates 47 mW of power and achieves a unity-gain frequency of 1.5 GHz with $C_s = C_f = 2$ pF and external load of 4 pF. The device

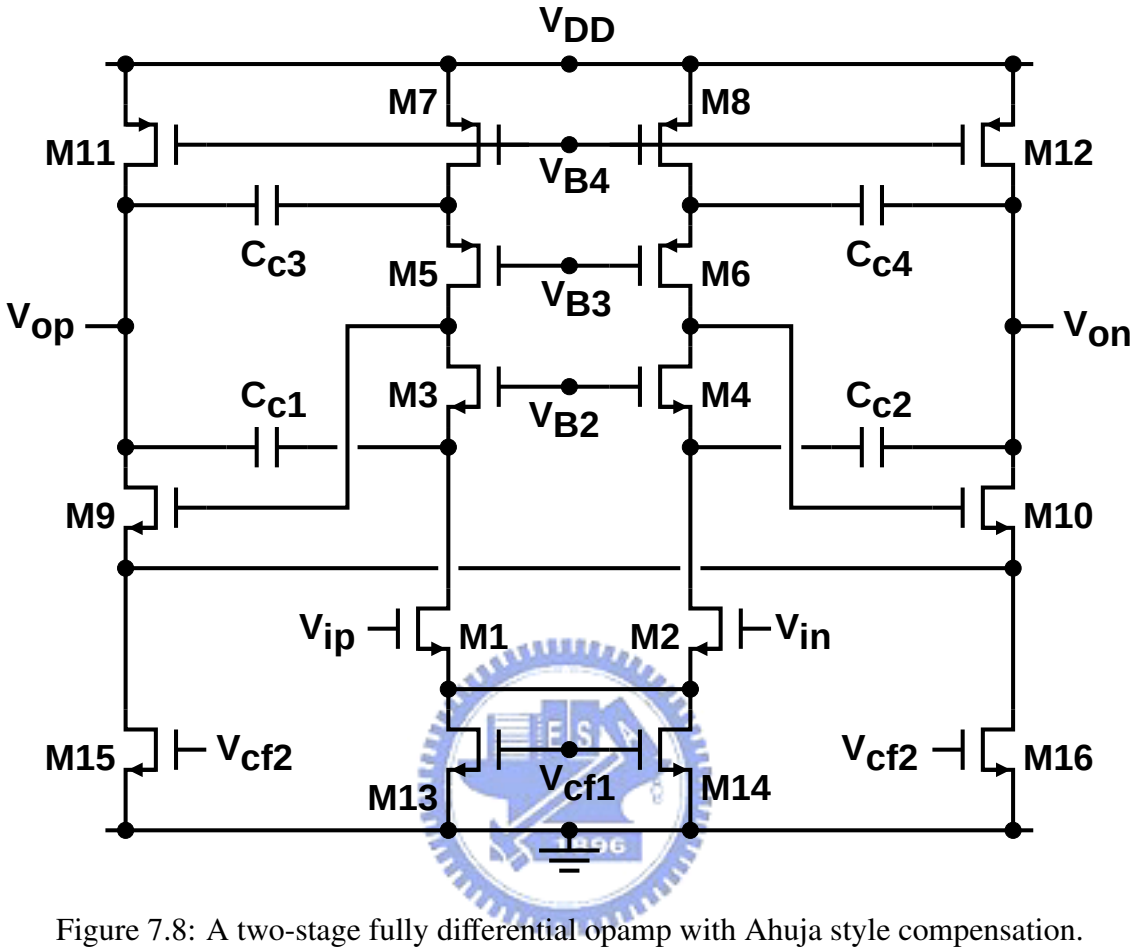


Figure 7.8: A two-stage fully differential opamp with Ahuja style compensation.

Table 7.2: Device Sizes of Opamp

Device	Size (μm/μm)
M1-M2	320/0.35
M3-M4	400/0.35
M5-M6	320/0.5
M7-M8, M13-M14	480/1.2
M9-M10	800/0.22
M11-M12, M15-M16	3600/1.2
C_{c1}-C_{c4}	1.5 pF

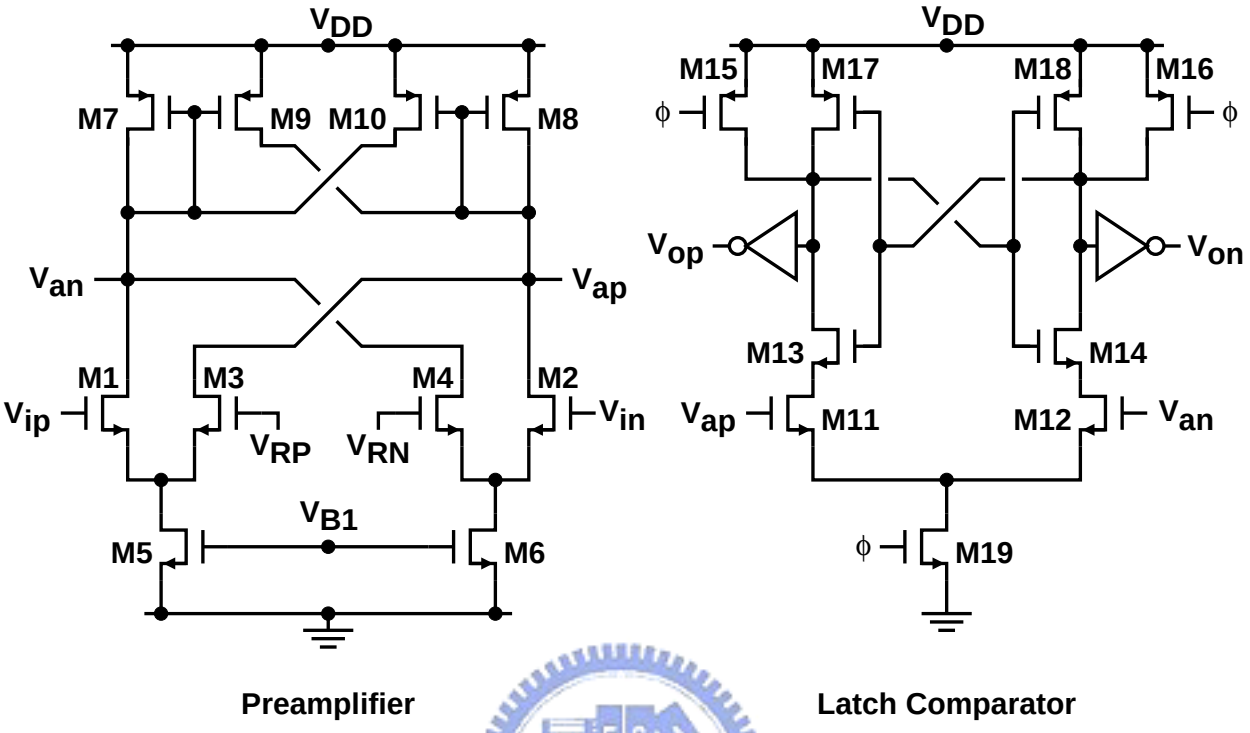


Figure 7.9: Comparator schematic.

sizes of the opamp used in the first stage are described in Table 7.2.

The entire comparator schematic is shown in Fig. 7.9. It consists of a differential-difference preamplifier with a voltage gain of 8.6 dB to reduce the kick-back noise from the following dynamic latch comparator. The transistors M11-M12 of this dynamic comparator behave as a voltage-to-current translator and generate the current difference according to their inputs, V_{ap} and V_{an}. At the reset mode, $\phi = 0$, the outputs, V_{op} and V_{on} are reset to the ground. When ϕ goes high, the cross-coupled latch, M13-M14 and M17-M18, has positive regeneration and V_{op} and V_{on} quickly reach to their final state determined by the current difference generated by M11 and M12. The device dimensions of the comparator for all pipeline stages are described in Table 7.3.

7.5 Digital Circuits

In this section, the detail implementation of the digital calibration blocks of the prototyping ADC is described. The implemented calibration schemes are based on those de-

Table 7.3: Device Sizes of Comparator

Device	Size (μm/μm)
M1-M4	16/0.18
M5-M6	20/1.2
M7-M8	3/0.18
M9-M10	2.5/0.18
M11-M14, M19	8/0.18
M15-M16	4/0.18
M17-M18	16/0.18
PMOS of Inverter	4/0.18
NMOS of Inverter	2/0.18

scribed in Section 3.5 and Section 5.5. These digital blocks consist of the functional units including adders, multipliers, multiplexers, dividers, registers for storing the measured calibration parameters, and a state machine that provides the control signals for the logic and the pipeline ADC. All the logic functions are described at the RTL level in Verilog hardware description language (Verilog HDL), and implemented using cell-based design.

The calibration processing for a single channel shown in Fig. 5.14 is re-depicted accompanying with the detail signal wordlengths as shown in Fig. 7.10. These wordlengths are determined depending on the bit number of the raw output of the pipeline A/D channel. The output after each arithmetic operation is truncated rather than rounded off to reduce the requirement of registers storing the data. The multiplier, MUL1, is required to operate in real time to compensate the gain of each D_{r1} every clock cycle. This means that the MUL1 needs to achieve high speed, and hence consumes large power. The MUL2 multiplier is used to unscramble D_{r3} with q_c. Since q_c is binary sequence varied between -1 and $+1$, the MUL2 is hence implemented using a 2-input multiplexer (MUX). If $q_c = 0$, the output of the MUX is $\overline{D}_{r3}$. Conversely, if $q_c = 1$, the output of the MUX is D_{r3}.

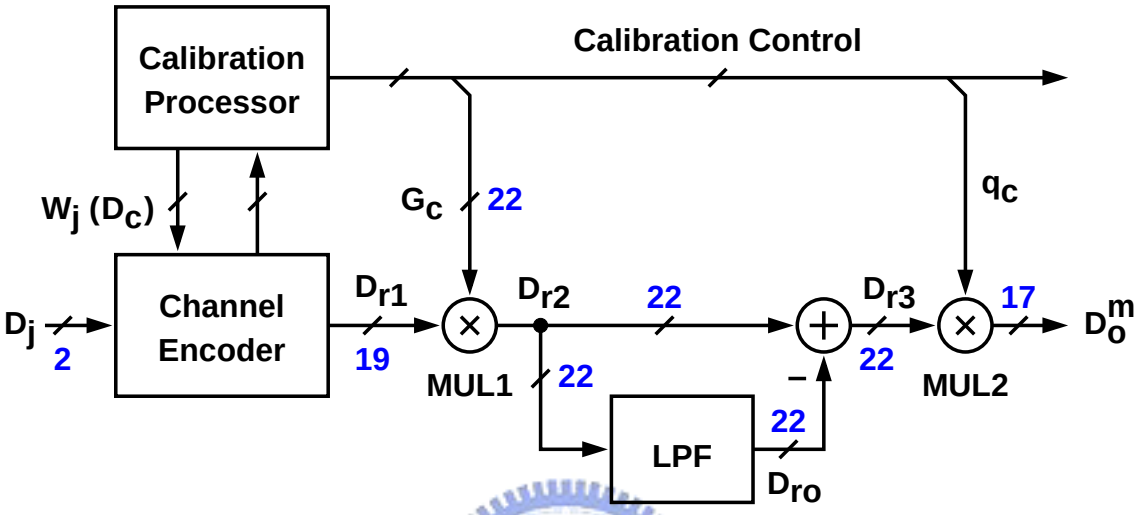


Figure 7.10: Digital output encoding and correction.

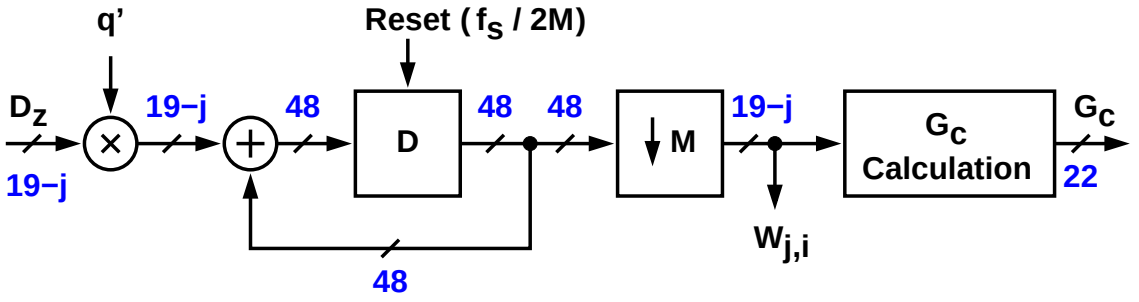


Figure 7.11: Calibration processor.

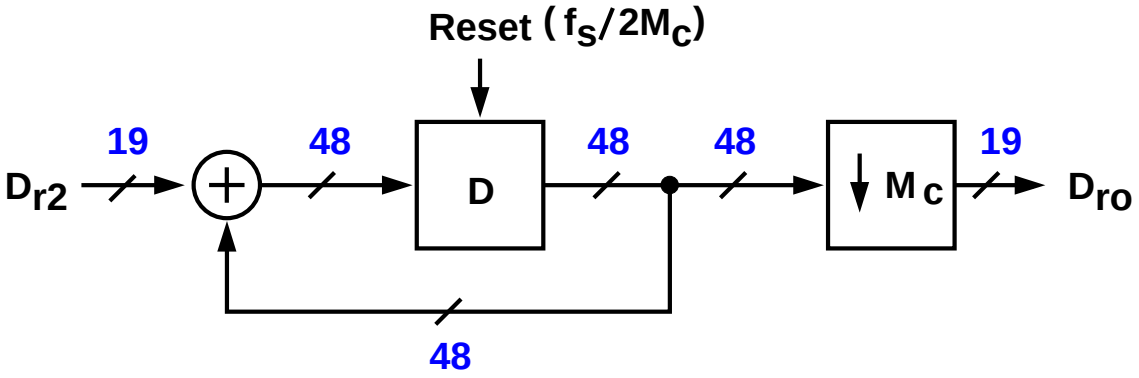


Figure 7.12: Offset extraction.

The block diagram of the calibration processor (CP) is shown in Fig. 7.11. It consists of the integration-and-dump for the $W_{j,i}$ extraction, and the G_c gain correction factor calculation according to (5.23). The D_z data are correlated with q', and then integrated M samples by a digital accumulator which is reset by a control signal with the frequency of $f_s/2M$, where f_s is the sampling frequency of the prototyping ADC. M is the length of the q' random sequence, as well as the length of the q random sequence injected into the pipeline. Here, M is chosen as 2^{28} to achieve a resolution more than 14 bits, and for simplicity, the value of M is the same for all calibrated pipeline stages. The integrated data are then dumped by M. Since M is power of 2, the dumping operation is designed just using a right shift by 28 bits. After dumping, the $W_{j,i}$ calibration parameter is obtained, and is used for the G_c calculation.

The primary functional blocks of the G_c calculation are the adder for summing all $W_{j,i}$'s and the divider for calculating the G_c factor. Because the calculation is not required in real time, it can take several clock cycles to complete the calculating process. It is hence implemented by employing the sequential divider to save the required hardware.

Fig. 7.12 shows the digital block diagram of the offset extraction incorporating with the signal wordlength. The extraction mechanism is also the integration-and-dump similar to the $W_{j,i}$ extraction. The number of the accumulated samples M_c is determined the same as M which has the value of 2^{28}. Thus, the random sequences q and q_c shown in Fig. 7.1 can share the same random generator implemented using a 28-tap linear feedback shift register (LFSR).

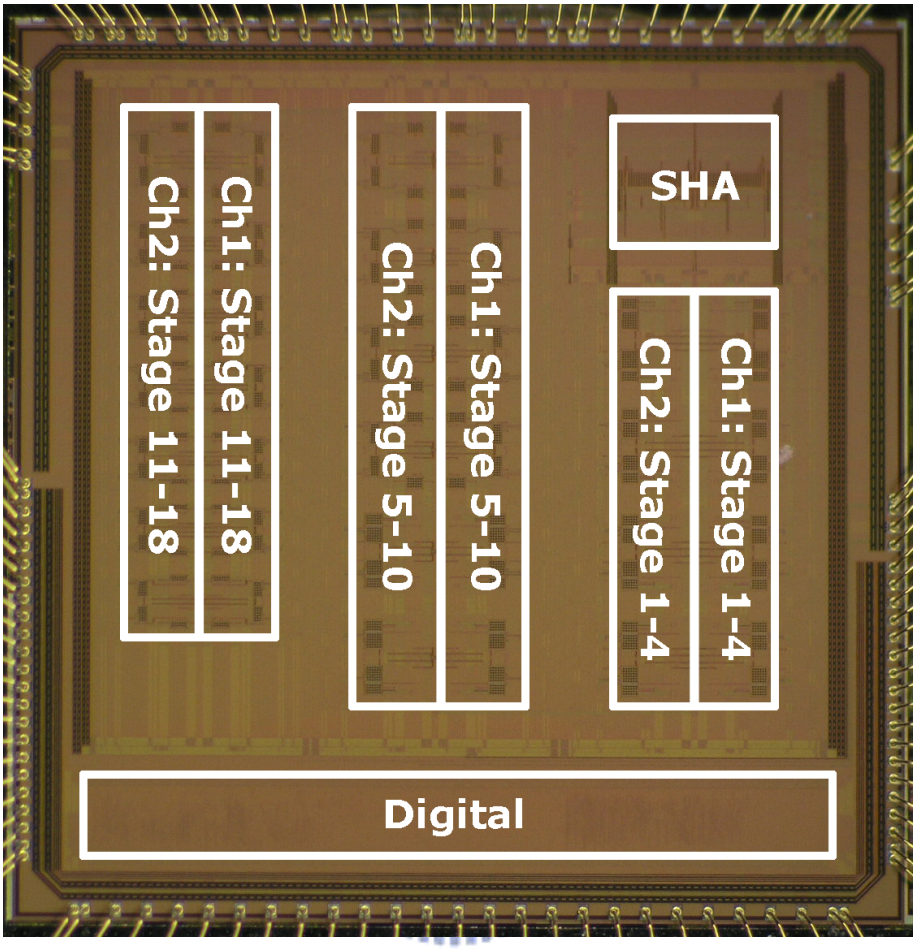


Figure 7.13: ADC's microphotograph.

7.6 Experimental Results

The ADC prototype was fabricated in a 0.18μm 1P6M 1.8-V CMOS logic technology with MIM capacitors. All voltage references are externally applied. Fig. 7.13 shows the ADC's die micrograph, where the stage 18 is the 2-bit flash ADC. The core area is 4.3 × 4.3 mm^2. Digital circuits occupy about 11% of the total area. Digital block and analog block use separate power lines. Operating at 125 MS/s sampling rate under a single 1.8 V supply, the analog part consumes 891 mW of power, while the digital part consumes only 18 mW. This ADC prototype was not optimized for minimium power dissipation.

Fig. 7.14 shows the simplified block diagram of the instrumentations setup. The input signal is generated by Agilent E4438C signal generator, and the CKI clock signal is

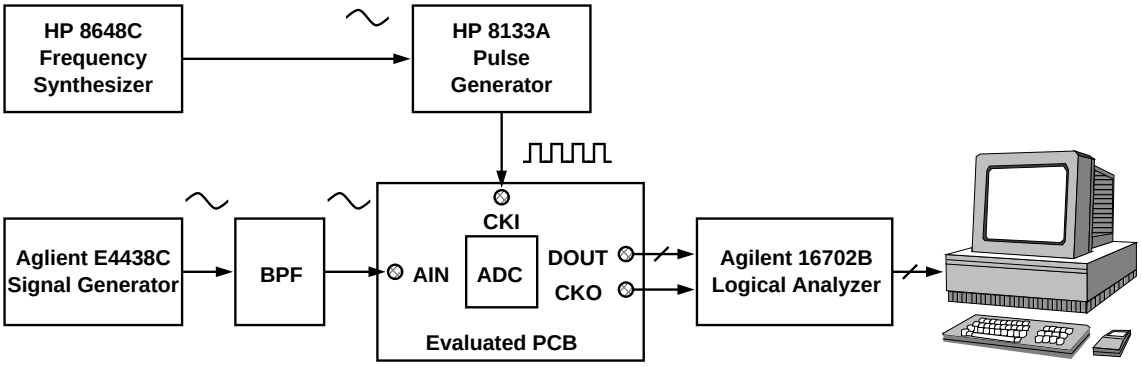


Figure 7.14: Block diagram of instrumentation setup.

generated by HP 8133A pulse generator which is external triggered by HP 8648C frequency synthesizer. The frequency of the CKI signal is twice of the TI-ADC's sampling frequency, f_s. It is then divided by 2 inside the ADC by a frequency divider to generate the sampling clock and make sure the 50% duty cycle. The final digital data are captured using Agilent 16702B logical analyzer (LA), and then analyzed using Matlab program. These digital data are synchronized with the CKO signal which is the clock signal of the TI-ADC.

Fig. 7.15 shows the photo of the evaluated printed-circuit-board (PCB), 4-layer FR4 PCB. The input signal and CKI clock signal of the PCB are connected using SMA connectors, and the reference signals and supply voltages are connected using BNC connectors. The digital output data are connected to the LA by the flying probes.

The static linearity curves are obtained using the code density test [54]. Fig. 7.16 and Fig. 7.17 show the measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC operating at 125 MS/s sample rate with 1.99 MHz sinusoidal input. Fig. 7.16 shows the results before the calibration, and Fig. 7.17 presents the results after the calibration. Digital output codes from a single channel are collected to calculate the DNL and INL. Note that the LSB in both Fig. 7.16 and Fig. 7.17 is normalized to 16-bit resolution. The number of registered output codes is approximately $(3/4) \times 2^{16}$. Before activating the calibration processor, the native DNL is $+1.16/-0.61$ LSB and the INL is $+29.8/-29.7$ LSB. After the background calibration is activated. The DNL is reduced to $+0.25/-0.27$ LSB and the INL is reduced to $+5.5/-5.7$ LSB.

Fig. 7.18 shows the ADC's output FFT spectrum at 125MS/s sampling rate. The input

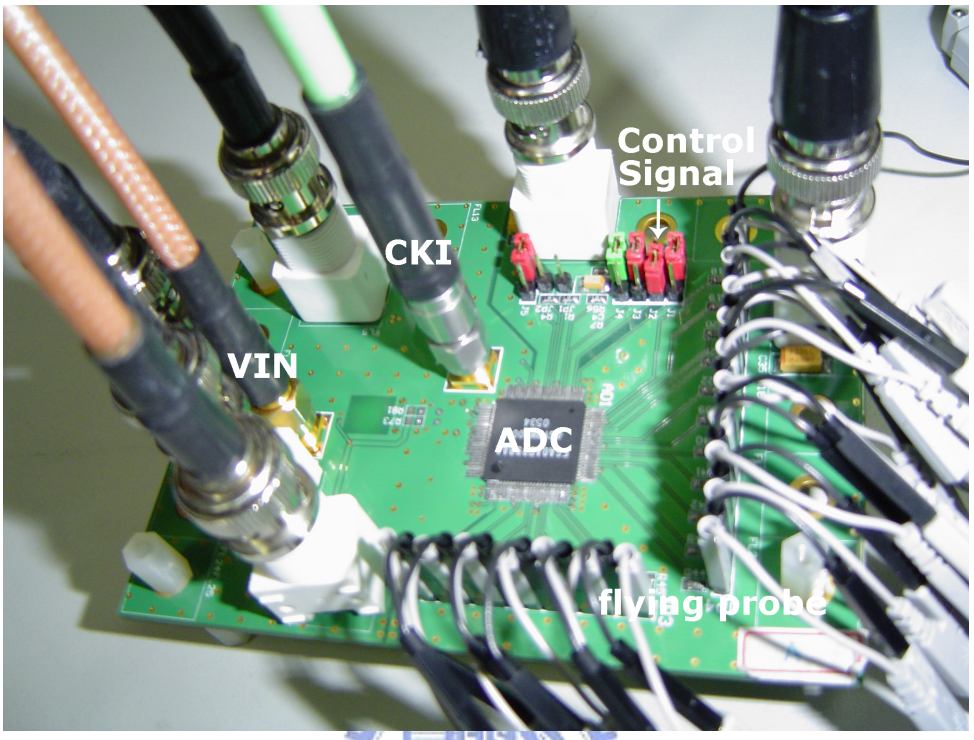


Figure 7.15: Evaluated PCB photo.

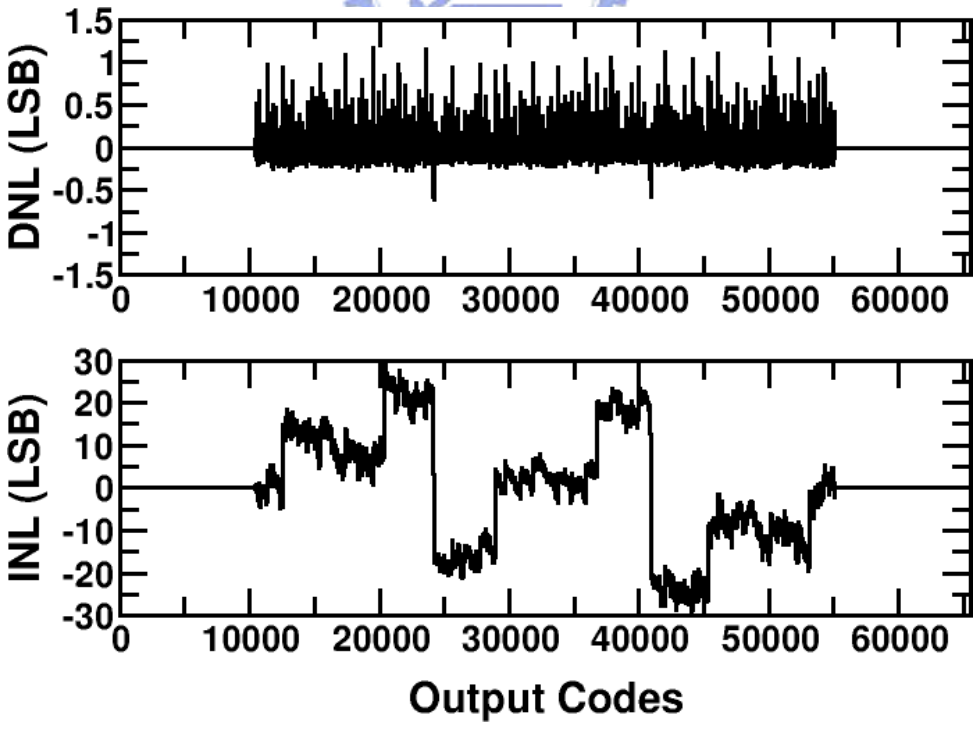


Figure 7.16: Measured DNL and INL of the TI-ADC before calibration.

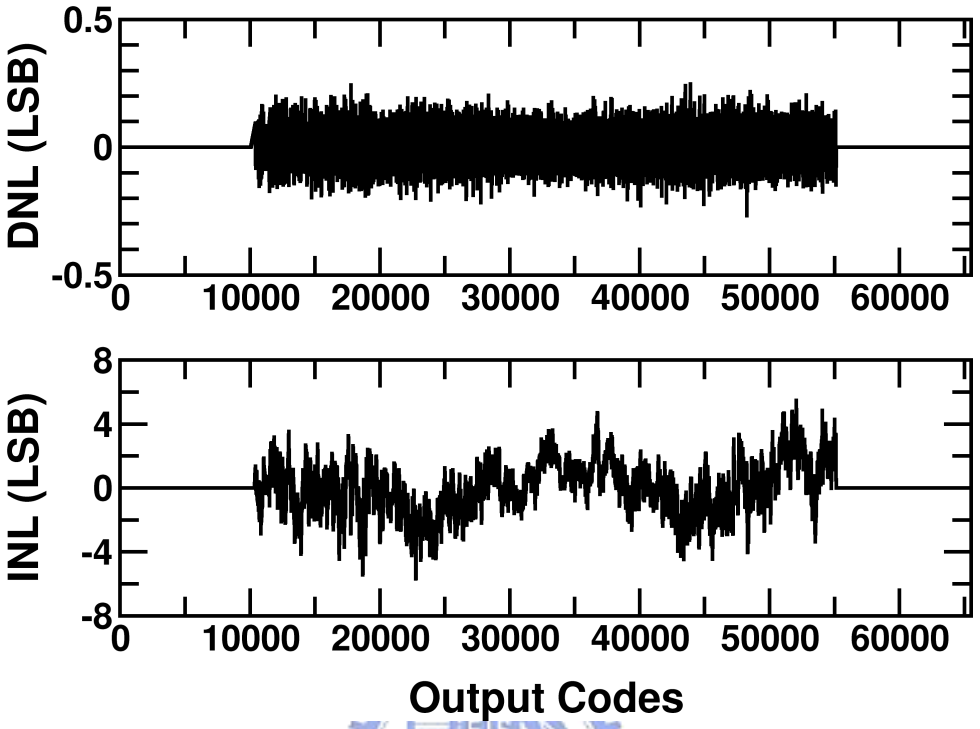


Figure 7.17: Measured DNL and INL of the TI-ADC after calibration.

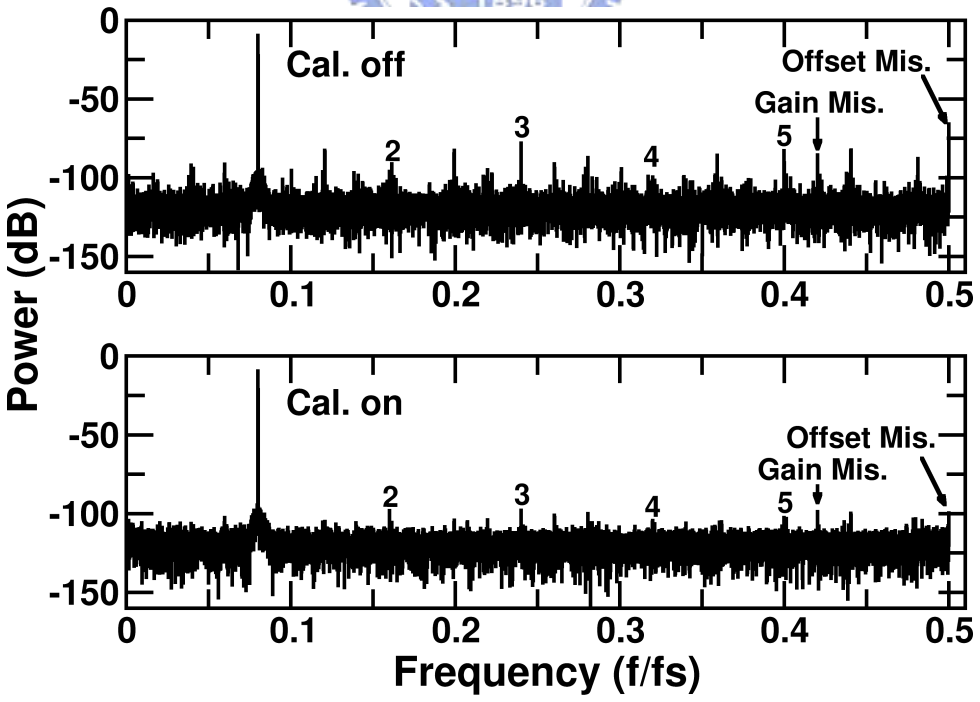


Figure 7.18: Measured FFT spectrum (f_s@125MS/s).

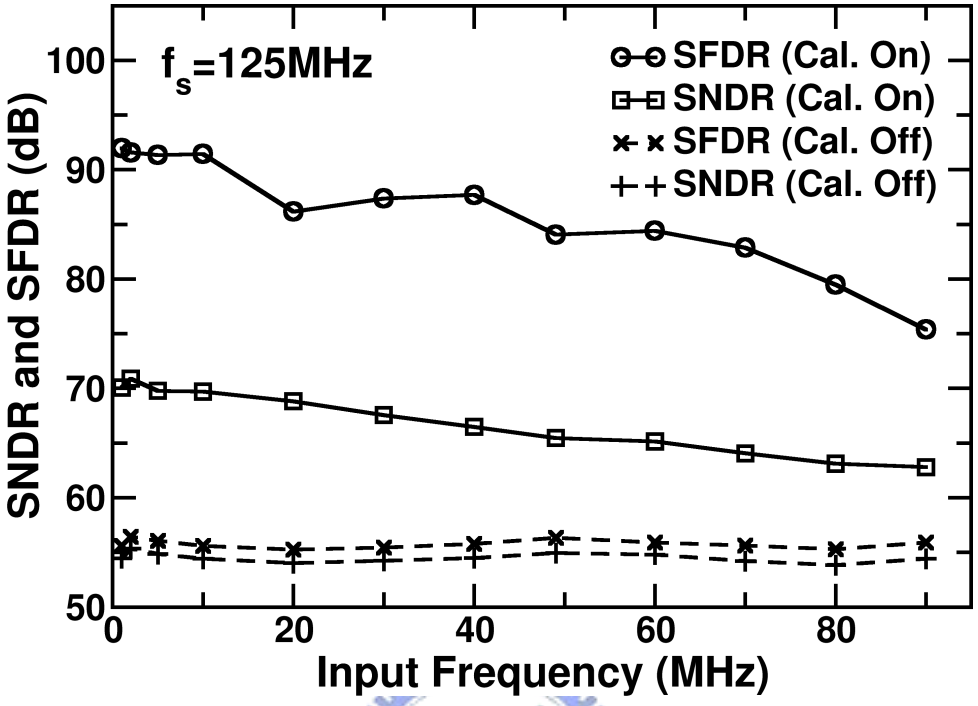


Figure 7.19: Measured SNDR and SFDR versus f_{in} at normal calibration.

is a differential $1.4V_{pp}$ 9.99MHz sinusoidal signal. Without calibration, the offset error is the dominant distortion term. The signal-to-distortion-plus-noise (SNDR) is 54.4 dB and the spurious-free dynamic range (SFDR) is 55.6 dB. After the calibration is activated, the SNDR is improved by 15.5 dB to 69.9 dB and the SFDR is improved by 36.3 dB to 91.9 dB. Fig. 7.19 shows the ADC's measured SNDR and SFDR versus input frequencies at 125 MS/s sampling rate. The calibration can improve the SNDR by more than 10 dB and the SFDR about 30 dB when the input frequencies up to the Nyquist frequency.

Fig. 7.20 shows the ADC's measured SNR and SFDR versus input signal levels with the calibration on and off respectively by applying a sinusoid at the frequency of 1.99MHz. This results reveal that the noise power excluding the distortion is not affected by the input levels, and the injected random term, $q \times V_r$. The measured dynamic range is approximately 73 dB at the supply voltage of 1.8 V.

Fig. 7.21 shows the ADC's measured signal-to-noise ratio (SNR) versus input frequencies at 125 MS/s sampling rate. The input is a differential 1.4 V_{pp} 9.99MHz sinusoidal signal. The SNR is calculated from the ADC's output FFT spectrum while ignoring the

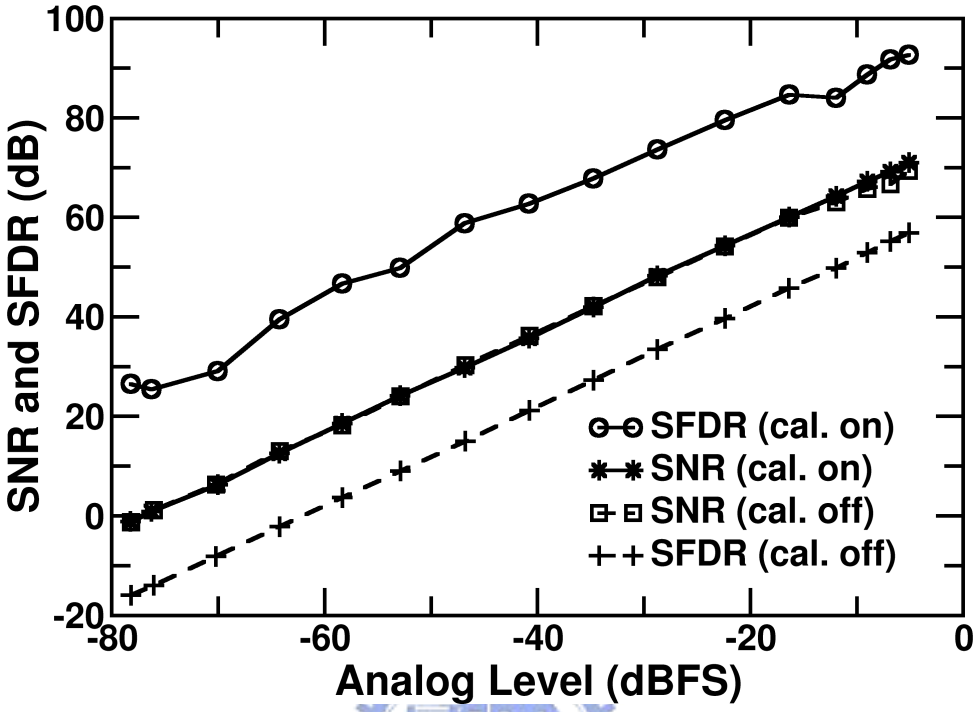


Figure 7.20: Measured SNR and SFDR versus input levels.

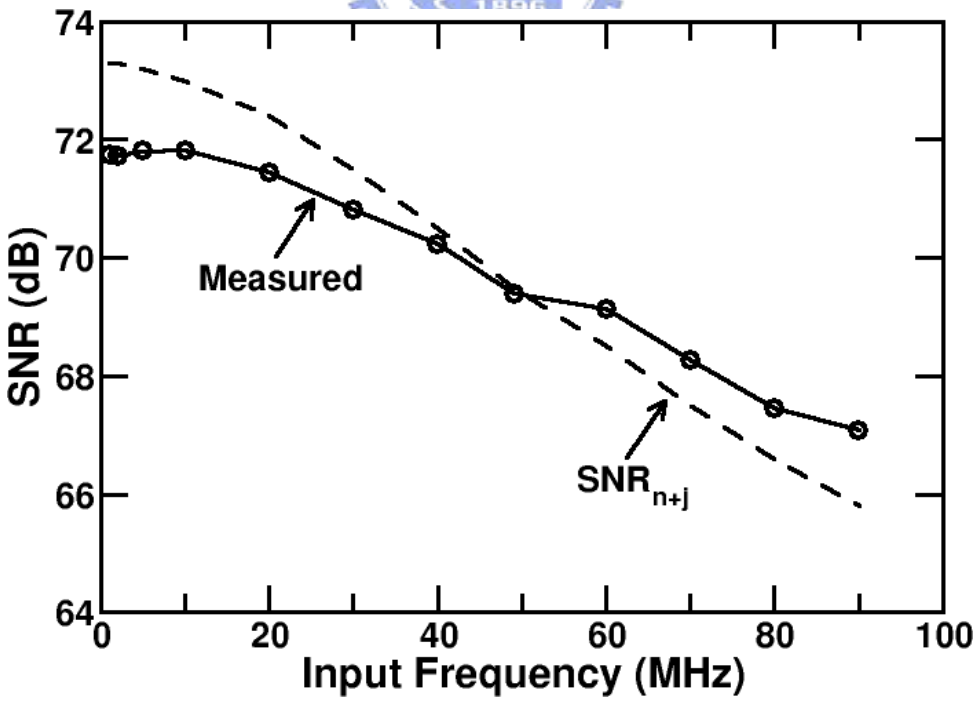


Figure 7.21: Measured SNR versus input frequencies.

harmonic tones caused by A/D nonlinearity and the spurious tones caused by inter-channel offset and gain mismatches. Also shown in Fig. 7.21 is the calculated SNR of an ADC model which includes the effect of sampling clock jitter Δt. Its input is $A\sin(2\pi f_{in}t)+n_{ex}$ where n_{ex} is an external noise source. Its SNR can be expressed as [55]:

$$\mathrm{SNR}_{n+j} = \frac{A^2/2}{2\pi^2 f_{in}^2 A^2 \overline{\Delta t^2} + \overline{n_{ex}^2}} \tag{7.1}$$

By curve-fitting (7.1) against measured data, the root-mean-square (rms) value of n_{ex} is estimated to be $n_{ex,rms} = 137\ \mu$V, and the rms value of Δt is estimated to be $\Delta t_{rms} =$ 0.82 psec.

7.7 Summary

The comparisons of this prototyping ADC with other works are described in the following. Table 7.4 shows the measured specifications of this ADC chip and compare it with published works that claim to have a maximum sample rate of more than 100 MS/s and a resolution of more than 14 bits.

Fig. 7.22 shows the performance of pipelined and time-interleaved pipelined ADCs of more than 12-bit resolution reported in the Custom Integrated Circuits Conference (CICC), International Solid-State Circuits Conference (ISSCC), Journal of Solid-State Circuits (JSSC), and commercial product's data sheets of Analog Device and Texas Instruments Incorporated. The corresponding references are listed in Table 7.5. The 12-bit, 13-bit, 14-bit, 16-bit designs implemented using different technologies are labeled, as well as this work. The ADCs with outstanding performance are highlighted using the corresponding item in Table 7.5. The results indicate that BiCMOS implementations can have better effective number of bits (ENOB) and faster sampling rate than CMOS implementations. This is true because BiCMOS is the best technology for the design of an opamp in all aspects except for money cost when it combines the benefits of Bipolar and those of CMOS [58]. The qualitative comparison for an opamp implemented using CMOS, Bipolar and BiCMOS technology is shown in Table 7.6 [59].

For a high resolution ADCs, two dominant noise sources are the thermal noise and the aperture noise. If the thermal noise is considered as the only noise source, the reachable

Table 7.4: Performance Comparison

	This Work	[3]	[56]	[57]
Technology	0.18 μm CMOS	0.13 μm CMOS	0.35 μm BiCMOS	0.35 μm BiCMOS
Architecture	TI Pipelined	Pipelined	Pipelined	TI Pipelined
Calibration	Digital Background	Digital Background	None	Digital Foreground
Supplies	1.8 V	1.5 V	3.3 V/5 V	3.0 V
Input Range (V_{pp})	1.4 V	1.5 V	2 V	4 V
Power Consumption	0.909 W	0.224 W	1.95 W	1.4 W
Resolution	15 Bits	14 Bits	14 Bits	14 Bits
Max. Sampling Rate	125 MS/s	100MS/s	125 MS/s	100 MS/s
DNL (LSB)	−0.27/+0.25	−1.1/+1.1	−0.2/+0.2	0.97
INL (LSB)	−5.7/+5.5	−2.0/+2.0	−0.5/+0.5	6.9
SNR (@ f_{in} = 5 MHz)	70.4 dB	70 dB	75 dB	
SNR (@ f_{in} = 49 MHz)	67.3 dB	65 dB	75 dB	
THD (@ f_{in} = 5 MHz)	−81.7 dB	−71.1 dB		
THD (@ f_{in} = 49 MHz)	−76.9 dB	−68 dB		
THD (@ f_{in} = 210 MHz)				−76.3 dB
SFDR (@ f_{in} = 5 MHz)	91.6 dB		100 dB	
SFDR (@ f_{in} = 70 MHz)	82.9 dB		95 dB	
SFDR (@ f_{in} = 210 MHz)				79.9 dB
Active Area	18.5 mm^2	1.02 mm^2	70 mm^2	10.2 mm^2

Table 7.5: Nyquist-rate ADC Survey

Item	Publication/ Year	Sampling Rate (MS/s)	ENOB (bits)	Author	Title
CMOS					
1	ISSCC / 2006	100	10.5	P. Bogner, etc.	A 14b 100MS/s Digitally Self-Calibrated Pipelined ADC in 0.13μm CMOS
2	ADI / 2006	125	11.8	Analog Device	AD9246 Data Sheet
3	ADI / 2006	150	11.9	Analog Device	AD9254 Data Sheet
4	JSSC / 2005	110	10.7	T. N. Andersen, etc.	A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS
5	CICC / 2005	180	10.6	k. Gulati, etc.	A Highly-Integrated CMOS Analog Baseband Transceiver with 180MSPS 13b Pipelined CMOS ADC and Dual 12b DACs
6	Texas In. / 2005	125	11.3	Texas Instrument	ADS5500 Data Sheet
7	JSSC / 2005	80	11.8	C. R. Grace, etc.	A 12b 80MS/s Pipelined ADC with Bootstrapped Digital Calibration
8	ISSCC / 2004	50	12.5	K. Nair, etc.	A 96 dB SFDR 50MS/s Digitally Enhanced CMOS Pipeline A/D Converter
9	JSSC / 2003	75	11	B. Murmann, etc.	A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification
10	JSSC / 2001	54	10.5	H. v. d. Ploeg, etc.	A 2.5-V 12-b 54-MSample/s 0.25-μm CMOS ADC in 1-mm^2 with Mixed-Signal Chopping and Calibration
11	JSSC / 2001	75	12	W. Yang, etc.	A 3-V 340-mW 14-b 75-MSample/s CMOS ADC with 85-dB SFDR at Nyquist Input
12	ISSCC / 2000	65	11.6	L. Singer, etc.	A 12b 65MSample/s CMOS ADC with 82dB SFDR at 120MHz
13	JSSC / 2000	50	10.5	H. Pan, etc.	A 3.3-V 12-b 50-MS/s A/D Converter in 0.6-μm CMOS with over 80-dB SFDR
14	ISSCC / 1997	128	10.1	R. Jewett, etc.	A 12b 128MSample/s ADC with 0.5LSB DNL
BiCMOS					
15	JSSC / 2006	125	12.5	A. M. Ali, etc.	A 14-bit 125-MS/s IF/RF Sampling Pipelined ADC with 100dB SFDR and 50fs Jitter
16	Texas In. / 2006	170	11.4	Texas Instrument	ADS5545 Data Sheet
17	Texas In. / 2006	210	12.1	Texas Instrument	ADS5547 Data Sheet
18	JSSC / 2005	65	12.9	A. Zanchi, etc.	A 16-bit 65-MS/s 3.3-V Pipeline ADC Core in SiGe BiCMOS with 78-dB SNR and 180-fs Jitter
19	ADI / 2005	100	13.1	Analog Device	AD9446 Data Sheet
20	Norchip / 2004	100	12.1	V. Hakkarainen, etc.	A 14b 200MHz IF-Sampling A/D Converter with 79.9dB SFDR
Bipolar					
21	JSSC / 2000	100	12.5		A 14-bit 100-MSample/s Subranging ADC

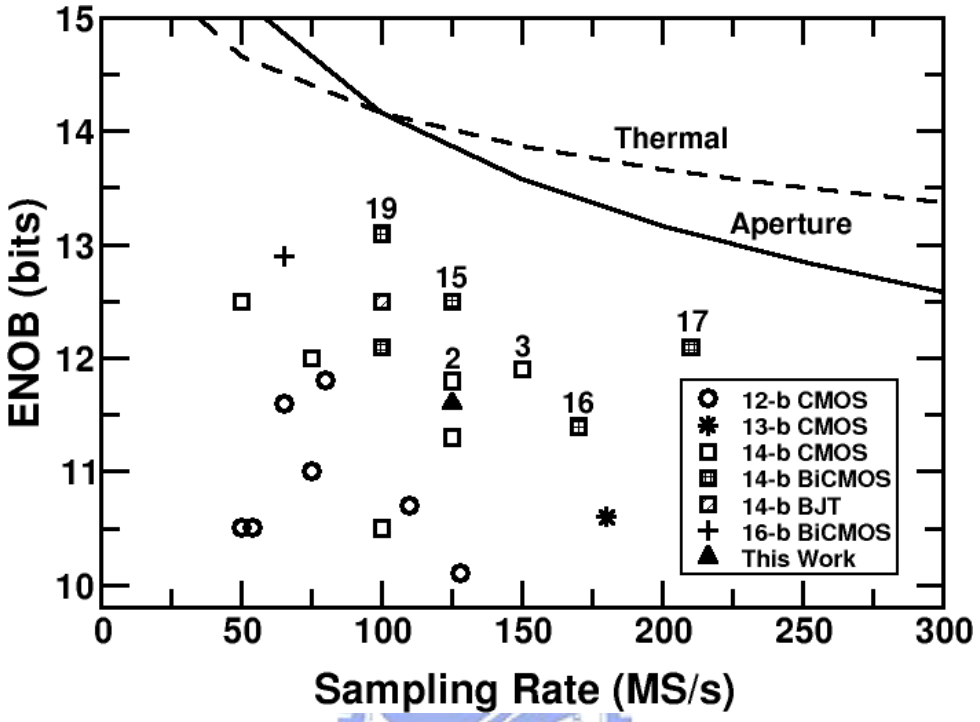


Figure 7.22: High-resolution (≥ 12 bits) high-speed (≥ 50 MS/s) pipeline and time-interleaved ADCs.

Table 7.6: Qualitative Comparison for An Opamp Implemented Using Bipolar, CMOS and BiCMOS Technologies

Qualitative Comparison	CMOS	Bipolar	BiCMOS
High Gain		√	√
High Gain-Bandwidth Product		√	√
Ease of Compensation		√	√
Low Voltage Noise		√	√
Low Current Noise	√		√
Low Power Supply Limit		√	√
Common Rejection	√	√	√
Low Voltage Offset		√	√
High Input Impedance	√		√

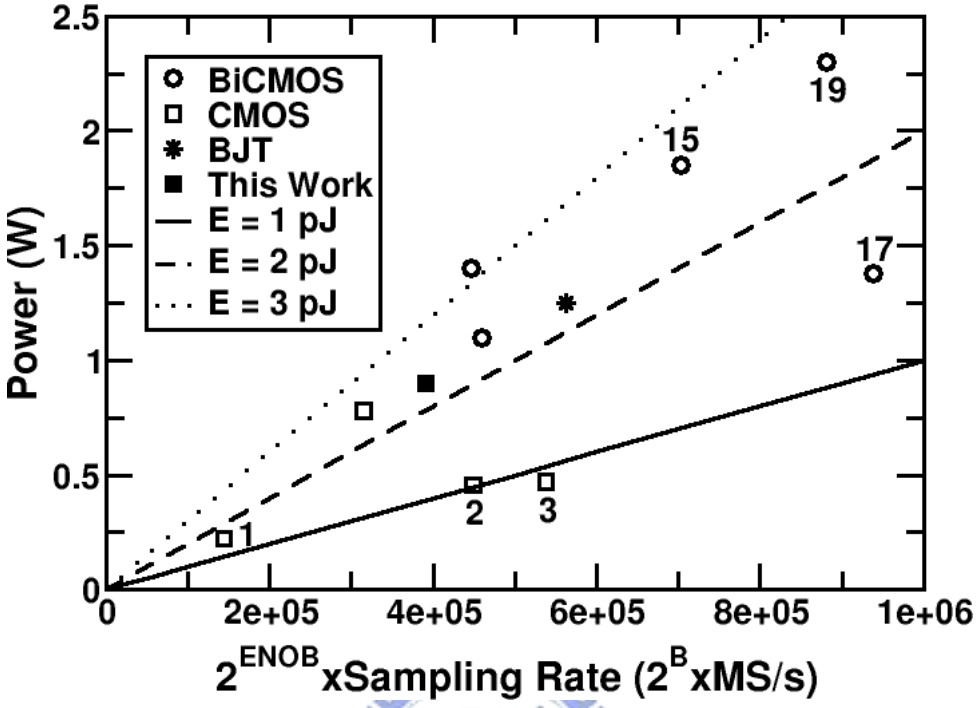


Figure 7.23: Figure of merit.

resolution is given by

$$N_{thm} = \frac{1}{2}\log_2\left(\frac{V_{FS}^2}{6kTR_{eff}f_s}\right) - 1 \tag{7.2}$$

where k is the Boltzmann's constant, T is the absolute temperature, f_s is the sampling rate, and R_{eff} is an effective thermal resistance, which includes the effects of all noise sources [60]. If the aperture noise is only considered, the attainable resolution is limited as

$$N_{apt} = \log_2\left(\frac{2}{\sqrt{3}\pi f_s \sigma_a}\right) - 1 \tag{7.3}$$

where σ_a is the rms aperture jitter [60]. Both N_{thm} and N_{apt} boundaries are plotted in Fig. 7.22 with $R_{eff} = 300\ \Omega$ and $\sigma_a = 0.1$ psec. The thermal noise truly limits the resolution above 14 bits. The aperture jitter degrades the available resolution more as the sampling rate increases. However, the designs labeled in Fig. 7.22 do not close to the limitation due to physical uncertainty, so does this work.

The figure of merit, the energy per conversion step, defined as

$$E_{conv} = \frac{P_d}{2^{\mathrm{ENOB}} \times f_s} \tag{7.4}$$

is widely used to evaluate the efficiency of ADCs, where P_d is ADC's power dissipation, and f_s is ADC's sampling rate. Fig. 7.23 shows the efficiency comparison of the ADCs surveyed in Table 7.5 which have the resolution more than 14 bits and the sampling rate more than 100 MS/s. The three boundaries of $E_{conv} = 1$ pJ, $E_{conv} = 2$ pJ and $E_{conv} = 3$ pJ are also plotted in Fig. 7.23 to clearly exhibit this comparison. Most designs locate between $E_{conv} = 1$ pJ and $E_{conv} = 2$ pJ. The CMOS design of reference 3 has the best conversion efficiency among these references. BiCMOS designs reveal better $2^{\mathrm{ENOB}} \times f_s$, but larger power consumption. The design of reference 17 has outstanding efficiency among the BiCMOS designs. Although it has little worse conversion efficiency than that of CMOS designs of reference2 and 3, it has much better $2^{\mathrm{ENOB}} \times f_s$.

Chapter 8

Conclusions and Future Works

8.1 Conclusions

High-resolution pipelined ADC's linearity can be degraded by the imperfections of circuit components. Digitally corrected analog circuit design is becoming increasingly necessary and popular. In this work, these techniques for linearity enhancement of pipelined ADCs are investigated. The proposed digital background calibration technique can track environmental conditions without taking the ADC out of normal operation.

The TI-ADC's architecture can overcome the speed limitation imposed by the opamps and increase the ADC's overall sampling rate. However, the time-interleaved architecture also introduces A/D errors caused by the gain, offset and sampling phase mismatches. To correct those errors requires extra hardware resources and consumes extra power. This work tried to minimize these overheads without sacrificing the ADC's performance. In this thesis, methods for mismatch error correction are investigated. In particular, we proposed a low-complexity gain mismatch error correction technique.

A CMOS 15-bit 125 MS/s TI-ADC has been demonstrated. The TI-ADC uses a single front-end SHA to avoid sampling phase mismatch. However, this SHA has to operate at full sampling rate. The precharging operation can mitigate the dc gain and unity-gain frequency requirements for the opamp. The percharging operation is to estimate the final SHA's output in advance, thus relaxing the opamp's duty in forcing the SHA to reach its final output value. This precharging precedure can be easily deployed in a TI-ADC,

requiring no extra time period.

This ADC uses simple digital signal processing to correct errors caused by gain and offset mismatches. For offset calibration, two additional analog random choppers are inserted at the input of the two A/D channels. No additional calibration procedure is required for gain correction. The information of gain mismatch is calculated directly from the calibration data obtained during the calibration of the two pipelined A/D channels. All calibration techniques incorporated in this ADC do not rely on input signal condition as long as the input is uncorrelated with the injected q and q_c random sequences.

8.2 Future Works

The large power consumption in the ADC's prototype which was not optimized is the major drawback which needs to be improved. The capacitors and the biasing currents of the pipeline stages should be scaled further from the first stage to the last stage according to the resolution requirements of the dedicated pipeline stage under the scaling. The minimum capacitor size can be determined according to the thermal noise requirement. The minumum power dissipation will be set by the minimum size of capacitor of each pipeline stage [61].

The performance of high-resolution time-interleaved ADCs is often significantly degraded by timing mismatch errors. Low-complexity techniques for estimating unknown time skew parameters and for correcting the output signal from these estimates should be developed.

Methodologies for improving the SNR should be investigated when the SNR performance is an issue, especially implemented in the low-voltage progressive technology.

Bibliography

[1] Y. Chiu, "Inherently linear capacitor error-averaging techniques for pipelined A/D conversion," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 3, pp. 229–232, March 2000.

[2] A. M. Abo and P. R. Gray, "A 1.5-v, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999.

[3] P. Bogner, F. Kuttner, C. Kropf, T. Hartig, M. Burian, and H. Eul, "A 14b 100MS/s digitally self-calibrated pipelined ADC in 0.13μm CMOS," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 224–225, 650, February 2006.

[4] H.-C. Liu, Z.-M. Lee, and J.-T. Wu, "A 15-b 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1047–1056, May 2005.

[5] E. Siragusa and I. Galton, "A digitally enhanced 1.8-v 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, December 2004.

[6] J. William C. Black and D. A. Hodges, "Time interleaved converter arrays," *IEEE Journal of Solid-State Circuits*, vol. SC-15, no. 6, pp. 1022–1028, December 1980.

[7] S. M. Jamal, D. Fu, N. C.-J. Chang, P. J. Hurst, and S. H. Lewis, "A 10-bit 120 MSample/s time-interleaved analog-to-digital converter with digital background cal-

ibration," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1618–1627, December 2002.

[8] J. Elbornsson, F. Gustafsson, and J.-E. Eklund, "Blind adaptive equalization of mismatch errors in a time-interleaved a/d converter system," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 1, pp. 151–158, January 2004.

[9] S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 6, pp. 954–961, December 1987.

[10] Y.-M. Lin, B. Kim, and P. R. Gray, "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 4, pp. 628–636, April 1991.

[11] J.-H. Koo, Y.-J. Kim, S.-H. Kim, W.-J. Yun, S.-I. Lim, and S. Kim, "An 8-bit 250MSPS CMOS pipelined ADC using open-loop architecture," *IEEE Asia-Pacific Conference on Advanced System Integrated Circuit*, pp. 94–97, August 2004.

[12] T. Ito, D. Kurose, T. Ueno, T. Yamaji, and T. Itakura, "Low-power design of 10-bit 80-MSPS pipeline ADCs," *IEICE Transactions on Electronics*, vol. E89-A, no. 7, pp. 2003–2008, July 2006.

[13] B.-S. Song and M. F. Tompsett, "A 12b 1MHz capacitor error averaging pipelined A/D converter," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 226–227,380, February 1988.

[14] Y. Chiu, P. R. Gray, and B. Nikolic, "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2139–2151, December 2004.

[15] P. C. Yu, S. Shehata, A. Joharapurkar, P. Chugh, A. R. Bugeja, X. Du, S.-U. Kwak, Y. Papantonopoulous, and T. Kuyel, "A 14b 40MSample/s pipelined ADC with DFCA," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 136–137,439, February 2001.

[16] S. Bardsley, C. Dillon, R. Kummarguntla, C. Lane, A. M. Ali, B. Rigsbee, and D. Combs, "A 100-dB SFDR 80-MSPS 14-bit 0.35-μm BiCMOS pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 2144–2145, September 2006.

[17] H.-S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrationg 15 Bit CMOS A/D converter," *IEEE Journal of Solid-State Circuits*, vol. sc-19, no. 6, pp. 813–819, December 1984.

[18] S.-H. Lee and B.-S. Song, "Digital-domain calibration of multistep analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1679–1688, December 1992.

[19] A. N. Karanicolas, H.-S. Lee, and K. L. Bacrania, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, December 1993.

[20] D. W. Cline and P. R. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 294–303, March 1996.

[21] M. K. Mayes and S. W. Chin, "A 200mW, 1 Msample/s, 16-b pipelined A/D converter with on-chip 32-b micocontroller," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 12, pp. 1862–1872, December 1996.

[22] L. Singer, S. Ho, M. Timko, and D. Kelly, "A 12b 65MSample/s CMOS ADC with 82dB SFDR at 120MHz," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, February 2000.

[23] S.-Y. Chuang and T. L. Sculley, "A digitally self-calibrating 14-bit 10-MHz CMOS pipelined A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 6, pp. 674–683, June 2002.

[24] H.-S. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 4, pp. 509–515, April 1994.

[25] M. Underweissacher, J. Goes, N. Paulino, G. Evans, and M. D. Ortigueira, "Efficient digital self-calibration of video-rate pipeline ADCs using white gaussian noise," *IEEE International Symposium on Circuits and Systems Digest of Technical Papers*, pp. I–877–I–880, May 2003.

[26] B. Provost and E. S*á*nchez-Sinencio, "A practical self-calibration scheme implementation for pipeline ADC," *IEEE Transactions on Instrumentation and Measurement*, vol. 53, no. 2, pp. 448–456, April 2004.

[27] S. R. Sonkusale, J. V. der Spiegel, and K. Nagaraj, "Background digital error correction technique for pipelined analog-digital converters," *IEEE International Symposium on Circuits and Systems Digest of Technical Papers*, pp. I–408–I–411, May 2001.

[28] A. J. Gines, E. J. Peralias, and A. Rueda, "Digital background calibration technique for pipeline adcs with multi-bit stages," *Proceedings of Symposium on Integrated Circuits and Systems Design*, September 2003.

[29] A. Larsson and S. Sonkusale, "A background calibration scheme for pipelined ADCs including non-linear operational amplifier gain and reference error correction," *IEEE SoC Conference*, pp. 37–40, September 2004.

[30] J. Li and U.-K. Moon, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 9, pp. 531–538, September 2003.

[31] K. Nair and R. Harjani, "A 96dB SFDR 50MS/s digitally enhanced CMOS pipeline A/D converter," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 456–457, February 2004.

[32] J. McNeill, C. E. Coln, and B. J. Larivee, ""split ADC" architecture for deterministic digital background calibration of a 16-bit 1-MS/s ADC," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2437–2445, December 2005.

[33] C. S. G. Conroy, D. W. Cline, and P. R. Gray, "An 8-b 85-MS/s parallel pipeline a/d converter in 1-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 447–454, April 1993.

[34] J. Elbornsson, F. Gustafsson, and J.-E. Eklund, "Blind equalization of time errors in a time-interleaved adc system," *IEEE Transactions on Signal Processing*, vol. 53, no. 4, pp. 1413–1424, April 2005.

[35] S. Huang and B. C. Levy, "Adaptive blind equalization of timing offset and gain mismatch for two-channel time-interleaved adcs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 6, pp. 1278–1288, June 2006.

[36] D. Morin, F. Normandin, M.-E. Grandmaison, H. Dang, Y. Savaria, and M. Sawan, "An intellectual property module for auto-calibration of time-interleaved pipelined analog-to-digital converters," *IEEE International Workshop on System-on-Chip for Real-Time Applications*, 2004.

[37] J.-E. Eklund and F. Gustafsson, "Digital offset compensation of time-interleaved adc using random chopper sampling," *IEEE International Symposium on Circuits and Systems Digest of Technical Papers*, pp. III–447–III–450, May 2000.

[38] M. Tamba, A. Shimizu, H. Munakata, and T. Komuro, "A method to improve sfdr with random interleaved sampling method," *IEEE International Test Conference*, pp. 512–517, 2001.

[39] K. El-Sankary, A. Assi, and M. Sawan, "New sampling method to improve the sfdr of time-interleaved adcs," *IEEE International Symposium on Circuits and Systems Digest of Technical Papers*, pp. I–833–I–836, May 2003.

[40] J. Elbornsson, F. Gustafsson, and J.-E. Eklund, "Analysis of mismatch effects in a randomly interleaved a/d converter system," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 3, pp. 465–476, March 2005.

[41] K. Gulati and H.-S. Lee, "A low-power reconfigurable analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1900–1911, December 2001.

[42] C.-C. Hsu and J.-T. Wu, "A CMOS 33-mW 100-MHz 80-dB SFDR sample-and-hold amplifier," *IEICE Transactions on Electronics*, vol. E86-C, no. 10, pp. 2122–2128, October 2003.

[43] D. kelly, W. Yang, I. Mehr, M. Sayuk, and L. Singer, "A 3v 340mW 14b 75MSPS CMOS ADC with 85dB SFDR at nyquist," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, February 2001.

[44] Y.-J. Cho, H.-H. Bae, and S.-H. Lee, "An 8b 220MS/s 0.25μm CMOS pipeline ADC with on-chip RC-filter based voltage references," *IEICE Transactions on Electronics*, vol. E88-C, no. 4, pp. 768–772, April 2005.

[45] B.-H. Min, Y.-J. Cho, H.-S. Chae, H.-W. Park, and S.-H. Lee, "A 10b 100MS/s 1.4mm^2 56mW 0.18μm CMOS A/D converter with 3-D fully symmetrical capacitors," *IEICE Transactions on Electronics*, vol. E89-C, no. 5, pp. 630–635, May 2006.

[46] J. Ming and S. H. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1489–1497, October 2001.

[47] C. R. Grace, P. J. Hurst, and S. H. Lewis, "A 12-bit 80-MSample/s pipelined ADC with bootstrapped digital calibration," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1038–1046, December 2005.

[48] M. Dessouky and A. Kaiser, "Input switch configuration for rail-to-rail operation of switched opamp circuits," *IEE Electronics Letters*, vol. 35, no. 1, pp. 8–10, January 1999.

[49] I. Mehr and L. Singer, "A 55-mW, 10-bit, 40Msample/s nyquist-rate CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 318–325, March 2000.

[50] S.-U. Kwak, B.-S. Song, and K. Bacrania, "A 15-b, 5-Msample/s low-spurious CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1866–1875, December 1997.

[51] B. K. Ahuja, "An improved frequency compensation technique for cmos operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. SC-18, no. 6, pp. 629–633, December 1983.

[52] P. J. Hurst, S. H. Lewis, J. P. Keane, F. Aram, and K. C. Dyer, "Miller compensation using current buffers in fully differential CMOS two-stage operational amplifiers," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 51, no. 2, pp. 275–285, February 2004.

[53] G. S. Ostrem, O. Moldsvor, and O. Aaserud, "A compact 3v, 70mw, 12-bit video-speed cmos adc," *Analog Integrated Circuits and Signal Processing*, vol. 15, no. 1, pp. 27–36, January 1998.

[54] M. Burns and G. W. Roberts, "An introduction to mixed-signal ic test and measurement," *Oxford University Press*, 2001.

[55] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 220–224, February 1990.

[56] A. M. Ali, C. Dillon, R. Sneed, A. Morgan, J. Kornblum, L. Wu, and S. Bardsley, "A 14-bit 125MS/s IF/RF sampling pipelined A/D converter," *IEEE Custom Integrated Circuits Conference*, pp. 391–394, September 2005.

[57] V. Hakkarainen, M. Aho, L. Sumanen, M. Waltari, and K. Halonen, "A 14b 200MHz IF-sampling A/D converter with 79.9dB SFDR," *IEEE Norchip Conference Proceeding*, pp. 171–174, November 2004.

[58] T. H. Ning, "Why bicmos and soi bicmos?" *IBM Jorunal of Research and Developement*, vol. 46, no. 2/3, pp. 181–186, March/May 2002.

[59] G. A. Rincon-Mora, "Low voltage design techniques and considerations for integrated operational amplifier circuits," *Technical Report, Georgia Institute of Technology*, May 1995.

[60] L. Sumanen, “Pipeline analog-to-digital converters for wide-band wireless communications,” *PHD Dissertation, Helsinki University of Technology*, December 2002.

[61] G. Chien, “High-speed, low-power, low voltage pipelined analog-to-digital converter,” *Master Thesis, University of California, Berkeley*, Spring 1996.

Vita

Zwei-Mei Lee was born in Tau-Yuan, Taiwan, in 1976. She received the B.S.E.E. degree from National Central University, Chung-Li, Taiwan, in 1998, and the M.S.E.E. degree from National Chiao-Tung University, Hsin-Chu, in 2000. She worked toward the Ph.D. degree in electronic engineering at National Chiao-Tung University. From 1999 to 2000, she was a full-time teaching assistant in electronic engineering at National Central University.
Her research interests are high-performance data converters and VLSI designs.

住址: 桃園縣龍潭鄉三水村一鄰 50 號

本論文使用 LaTeX[1] 系統排版.

[1]LaTeX 是 TeX 之下的 macros 集. TeX 是 American Mathematical Society 的註册商標. 本論文 macros 的原始作者是 Dinesh Das, Department of Computer Sciences, The University of Texas at Austin. 交大中文版的作者是吳介琮, 交通大學電子工程學系, 新竹, 台灣.