

On the Origin of Hole Valence Band Injection on GIFBE in PD SOI n-MOSFETs

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Abstract—This letter systematically investigates the mechanism of gate-induced floating-body effect (GIFBE) in advanced partially depleted silicon-on-insulator metal-oxide-semiconductor field-effect transistors. Based on different operation conditions, we found that the hole current collected by the body terminal is strongly dependent on electrons in the inversion layer under a source/drain ground. This implies that GIFBE can be attributed to anode hole injection (AHI) rather than the widely accepted mechanism of electron valence band tunneling. Moreover, GIFBE was also analyzed as a function of temperature. The results provide further evidence that the accumulation of holes in the body results from the AHI-induced direct tunneling current from the gate.

Index Terms—Electron-valence band (EVB) tunneling, gate-induced floating-body effect (GIFBE), linear kink effect, silicon-on-insulator (SOI).

I. INTRODUCTION

WITH the scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs), the aggressive shrinking of gate oxide thickness results in an increase of direct gate tunneling current, which is responsible for the increase of power consumption in CMOS circuits [1]. The increasing tunneling current in advanced silicon-on-insulator (SOI) devices has been reported to cause a new floating-body (floating) effect in the linear operation region [2], a phenomenon referred to as “linear kink effect” (LKE). Some previous research has also found that LKE gives rise to a second peak of transconductance (gm), particularly in partially depleted (PD) SOI MOSFETs with an FB condition, as well as in fully depleted ones with back gate bias [2], [3]. In addition, numerous studies have re-

ported that LKE increases the low-frequency noise and strongly impacts the history effects in digital circuits [4]–[7].

LKE differs from the well-known kink effect that occurs at a high drain voltage due to impact ionization. It is closely related to the vertical electrical field. Therefore, LKE is also referred to as gate-induced FB effect (GIFBE) [3]. The mechanism of electron-valence band (EVB) tunneling through an ultrathin oxide is widely accepted as an explanation for GIFBE [2]–[7]. However, there are few studies that confirm the validity of this mechanism in an SOI device by using systematic operation conditions. The aim of this letter is to clarify the mechanism of GIFBE for PD SOI nMOSFETs. The experimental results demonstrate that anode hole injection (AHI) from the poly gate is the main dominant mechanism responsible for GIFBE rather than EVB tunneling.

II. EXPERIMENT

Using 65-nm SOI CMOS technology, PD SOI n-type MOSFETs are employed with a T-gate structure to investigate the GIFBE mechanism. The distance from the body contact to the active region is $0.35\ \mu\text{m}$. The silicon film and buried oxide thicknesses for the devices are 75 and 145 nm, respectively. The gate oxide with a thickness of 12 Å was grown by *in situ* steam generation, with the channel doping concentration being about $3 \times 10^{18}\ \text{cm}^{-3}$. The channel currents follow in the $\langle 110 \rangle$ direction on (100) substrates. In this letter, devices with a channel width (W) of $1\ \mu\text{m}$ and a length (L) ranging from 1 to $0.2\ \mu\text{m}$ were selected. The devices with an FB or a grounded body (GB) were measured to study the phenomenon of LKE. To further investigate the GIFBE mechanism, temperature-dependent electrical characteristics were performed at temperatures ranging from 303 to 453 K. All experimental curves were measured using a Keithley 4200 semiconductor parameter analyzer.

III. RESULTS AND DISCUSSION

Fig. 1 shows the gm in the linear region ($V_D = 50\ \text{mV}$) for the PD SOI n-type MOSFETs under FB and GB operations. It can be clearly observed that a second gm peak appears in the FB device. In addition, the body current (I_B) under GB operation increases rapidly beyond the gate voltage of $0.9\ \text{V}$, corresponding to the second gm peak. This phenomenon indicates that, under FB operation, additional carriers (holes) accumulate in the body beyond this voltage. Therefore, the body potential increases exponentially, which causes a reduction in the threshold voltage (V_T), resulting in a higher drain current and the second gm peak in the linear region.

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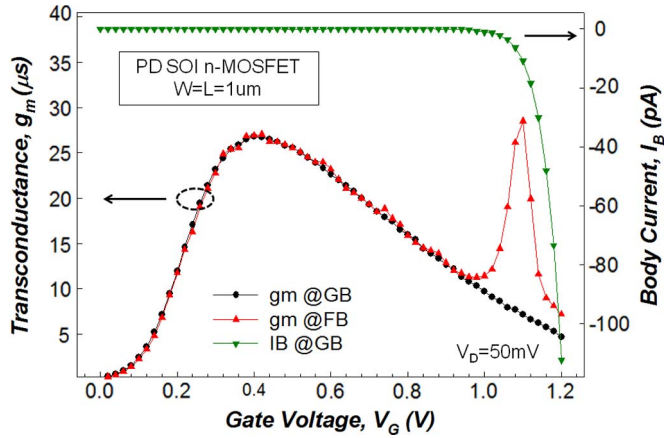


Fig. 1. g_m as a function of gate voltage for PD SOI n-MOSFETs under GB and FB operations in the linear region ($V_D = 50$ mV). I_B is measured under GB operation.

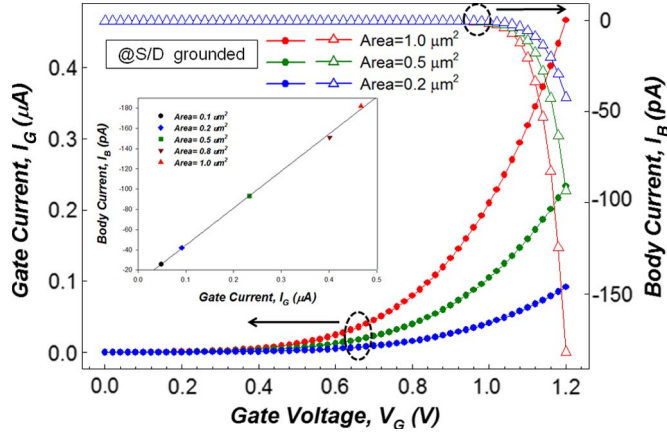


Fig. 2. I_G - V_G and I_B - V_G curves for different N^+ poly-gate areas. The inset displays the linear relationship between I_B and I_G for different N^+ poly-gate areas.

To examine the origin of additional carriers (holes) caused by the gate leakage current (I_G), Fig. 2 shows I_G and I_B versus gate voltage (V_G) for different N^+ poly-gate areas (1 – $0.2 \mu\text{m}^2$), while the source/drain (S/D) are grounded. Clearly, I_B has significant enhancement as I_G increases, meaning that the source of I_B is strongly dependent on I_G . Furthermore, the linear relationship between I_B and I_G is also obtained and shown in the inset of Fig. 2. The I_B - V_G curve in Fig. 2 shows that V_G corresponding to the rapid increase of I_B for different N^+ poly-gate areas is always located around 0.9 V. This indicates that additional carriers can only be generated at a certain vertical electrical field (~ 4.5 MV/cm) regardless of the poly-gate area.

It was proposed that I_G consisted of three components: electron tunneling from the conduction band, electron tunneling from the valence band (EVB), and hole tunneling from the valence band (HVB) [8]. In fact, the hole accumulation in the p^- substrate has been explained due to EVB and HVB tunneling currents under an FB condition. However, the EVB tunneling model was widely accepted to explain the LKE phenomenon because the HVB component is typically very small for NMOS. In the inset of Fig. 3, the EVB tunneling schematic band diagram shows that the electrons tunnel from the valence band of the Si substrate to the poly-gate conduction band under

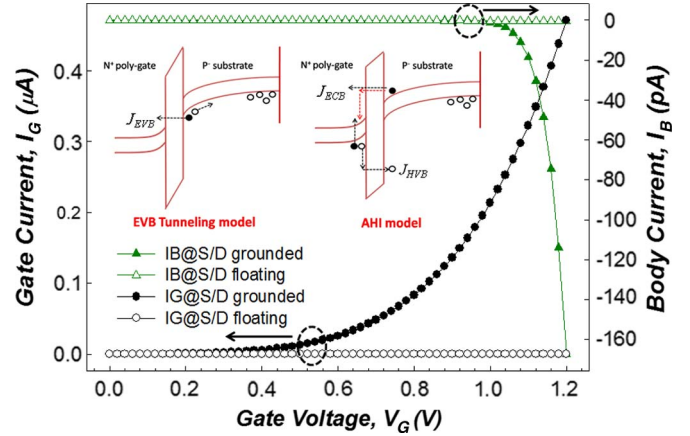


Fig. 3. I_G - V_G and I_B - V_G characteristics for a PD SOI n-MOSFET under floating and grounded S/D operations. The inset shows the schematic diagrams of EVB tunneling and AHI model for an ultrathin gate oxide of a PD SOI n-MOSFET.

a sufficiently large vertical electric field. As a result, holes accumulate in the body due to FB, which leads to a rise in body potential. However, the other mechanism, i.e., that of AHI [9], also shown in the inset of Fig. 3, is also a possible model to explain LKE. In AHI, when the gate oxide is thin enough, electrons can tunnel from the inversion layer to the poly gate (anode) and generate hot holes by impact ionization in the poly-depletion region. Then, these hot holes can inject over or through the anode/oxide interface energy barrier and traverse the oxide layer to the body (cathode). Consequently, the HVB tunneling current becomes significant due to the increase of AHI tunneling current from the poly gate to the p^- substrate. Both mechanisms generate holes that accumulate in the body, but there are two key differences between the EVB tunneling and the AHI model. One is the source of electrons: The electrons in the EVB tunneling model come from the valence band, but the source of electrons in the AHI model is from the conduction band. The other difference is that the intensity of the vertical electric field in the EVB tunneling model is larger than that in the AHI model. This is because the V_G in the EVB tunneling model needs to be larger than the silicon band gap (1.1 V) to make the valence band energy level in the silicon substrate align with the gate conduction band [8]. Our experimental results that identify the rapid increase of I_B for different N^+ poly-gate areas located at around 0.9 V imply that the AHI model is more likely to be responsible for GIFBE.

To further verify that the AHI model is the dominant mechanism of GIFBE, two operation conditions are performed to distinguish the different sources of I_G that result in hole accumulation. We measured the I_G and I_B versus V_G of the device under floating and grounded S/D operations. The result under S/D floating operation is shown in Fig. 3, where it can be clearly observed that the gate leakage current becomes insignificant because the S/D cannot supply sufficient minority carriers (electrons) to the inversion layer. The I_B is not evident (~ 0.1 pA) in this operation. On the contrary, both currents show very pronounced increases under grounded S/D operation. The results prove that the origin of GIFBE can be attributed to the electrons in the inversion layer rather than the electron-hole pair

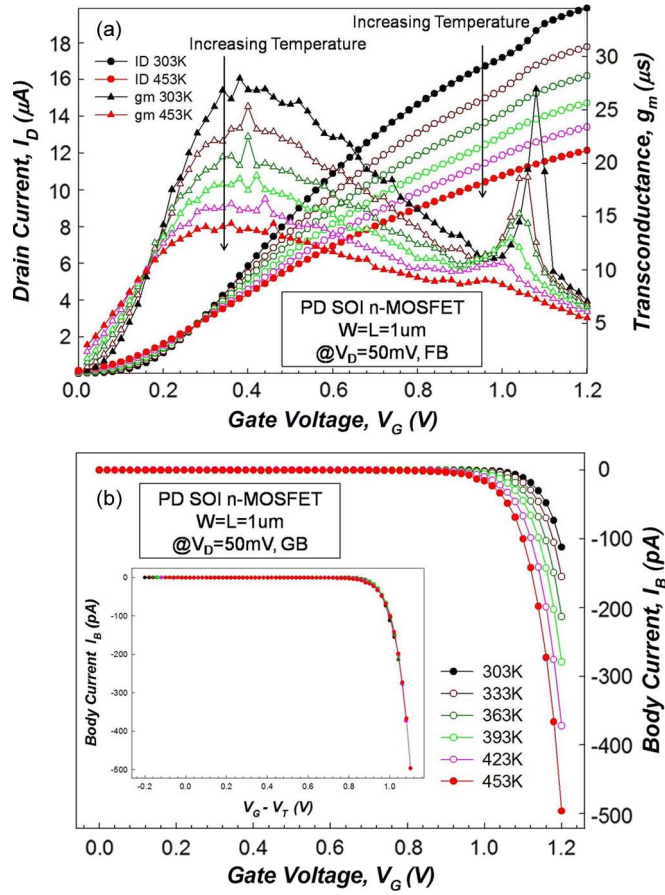


Fig. 4. (a) Transfer characteristics as a function of temperature varying from 303 K to 453 K under FB operation. (b) I_B - V_G characteristics of the PD SOI n-MOSFET with body contact for different temperatures. The inset shows the I_B - V_G after V_T correction, where V_T is obtained from linear extrapolation from $g_{m\max}$.

separated in the valence band of the p^- substrate. Therefore, the AHI model is the dominant mechanism responsible for GIFBE.

The second g_m peak shown in Fig. 1 was also analyzed as a function of temperature in the range of 303 K to 453 K. Fig. 4(a) shows that the second peak amplitude becomes smaller and shifts left as temperature increases. This reduction is ascribed to an increase in recombination rate in the source and drain junctions as temperature increases [10]. To investigate the second g_m peak shift, the I_B - V_G curve as a function of temperature was also measured and is shown in Fig. 4(b) for comparison. It shows that the left-shift trend of I_B against temperature is similar to that of the second g_m peak. However, I_B has no significant change after a V_T correction for different temperatures, as shown in the inset of Fig. 4(b). The results provide further evidence that hole injection from the anode is direct tunneling because it is independent of temperature.

IV. CONCLUSION

In this letter, we have demonstrated that the EVB tunneling model is not the dominant mechanism for GIFBE. Even if oxide thickness is reduced to only 12 Å, EVB still cannot occur in S/D floating operation. Therefore, GIFBE can be attributed to the electrons of the inversion layer supplied from the S/D. This result indicates that the increase of HVB tunneling current induced by AHI is the dominant mechanism responsible for GIFBE. By analyzing I_B as a function of temperature, we also prove that the hole current (I_B) is direct tunneling from the poly gate. This is because I_B is independent of temperature after a V_T correction.

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REFERENCES

- [1] C.-H. Choi, K.-Y. Nam, Z. Yu, and R. W. Dutton, "Impact of gate direct tunneling current on circuit performance: A simulation study," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2823–2829, Dec. 2001.
- [2] A. Mercha, J. M. Rafi, E. Simoen, E. Augendre, and C. Claeys, "Linear kink effect' induced by electron valence band tunneling in ultrathin gate oxide bulk and SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1675–1682, Jul. 2003.
- [3] M. Cassk, J. Pretet, S. Cristoloveanu, T. Poiroux, C. Fenouillet-Beranger, F. Fmleux, C. Raynaud, and G. Reimbold, "Gate-induced floating-body effect in fully depleted SOI MOSFETs with tunneling gate oxide and back-gate biasing," *Solid State Electron.*, vol. 48, no. 7, pp. 1243–1247, Jul. 2004.
- [4] S. K. H. Fung, N. Zamdmer, I. Yang, M. Sherony, S.-H. Lo, L. Wagner, T.-C. Chen, G. Shahidi, and F. Assaderaghi, "Impact of the gate-to-body tunneling current on SOI history effect," in *Proc. IEEE Int. SOI Conf.*, Oct. 2000, pp. 122–123.
- [5] F. Dieudonné, J. Jomaah, and F. Balestra, "Gate-induced floating body effect excess noise in partially depleted SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 737–739, Dec. 2002.
- [6] A. Mercha, E. Simoen, H. van Meer, and C. Claeys, "Low-frequency noise overshoot in ultrathin gate oxide silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 82, no. 11, pp. 1790–1792, Mar. 2003.
- [7] N. B. Lukyanchikova, M. V. Petrichuk, N. Garbar, A. Mercha, E. Simoen, and C. Claeys, "Electron valence band tunneling-induced Lorentzian noise in deep submicron silicon-on-insulator metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 94, no. 7, pp. 4461–4469, Oct. 2003.
- [8] W.-C. Lee and C. Hu, "Modeling CMOS tunneling currents through ultrathin gate oxide due to conduction- and valence band electron and hole tunneling," *IEEE Trans. Electron Devices*, vol. 48, no. 7, pp. 1366–1373, Jul. 2001.
- [9] K. F. Schuegraf and C. Hu, "Hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 761–764, May 1994.
- [10] L. Vancaillie, V. Kilchyska, P. Delatte, L. Demeus, H. Matsuhashi, F. Ichikawa, and D. Flandre, "Peculiarities of the temperature behavior of SOI MOSFETs in the deep submicron area," in *Proc. IEEE Int. SOI Conf.*, 2003, pp. 78–79.