Chapter 4

NiSi contacted n^+p shallow junction

4.1 Introduction

With the progress of submicron technology, the reduction in source/drain junction depth is necessary to minimize short channel effects. In addition, advanced devices require not only scale-down of p^+n junctions but also sacle-down of n^+p junctions. Conventionally, the n^+p shallow junction can be easily realized because implanted n-type dopants, such as phosphorus and arsenic, are much heavier than p-type dopant boron. However, it is hard to form ultra shallow sub-0.1 μm n^+p junctions because of the transient dopant diffusion, although the effect of transient dopant diffusion is less severe for arsenic than for boron and phosphorus [1]. Phosphorus is often used in n-well and n-region in light of its high diffusivity and light mass. On the other hand, arsenic is often used in source/drain junction formation. However, arsenic needs higher annealing temperature for dopant activation, which in turn may change the channel doping profile. To further reduce the junction depth, novel techniques have been proposed to fabricate ultra shallow n^+p junction as follows.

(1) Antimony implantation [2-3]

Antimony was proposed to be an alternative n-type dopant to fabricate ultra shallow n^+p junction using Sb^+ implantation; however, the junction characteristic of the n^+p junction formed was unacceptable.

(2) Plasma immeration ion implantation (PIII) [4-5]

PIII technique has many unique advantages over the conventional implantation, such as low cost, low energy, high dose rate and large implant areas; therefore it has a good prospect in fabricating ultra-shallow junction in future ULSI technology.

(3) ITS/ITM technique [6-12]

The implant through silicide (ITS) and implant through metal (ITM) techniques have been used for shallow junction formation. Arsenic or phosphorus ions are implanted into/through the silicide or metal film to reduce ion implantation damage to Si substrate. Arsenic is preferred because of its heavier mass, smaller diffusivity, and less transient diffusion. However, arsenic may seriously damage the silicide film, leading to increase the film resistivity and worsen its high temperature thermal stability.

In this chapter, we investigate the formation and characterization of

NiSi-silicided n^+p shallow junctions fabricated using ITS scheme with phosphorus ion (P^+) implantation. Phosphorus ion (P^+) was used instead of arsenic ion (As^+) to promote the drive-in efficiency during the post-implant annealing process because of its higher diffusivity. In addition, the knock-on effect of Ni atoms can also be reduced because P is a much lighter element than As. Feasibility of low-temperature processing and high-temperature stability of the NiSi/n^+p shallow junction are evaluated by analyzing the electrical characteristics and material properties of the silicided junction.

4.2 Experimental procedures

The NiSi/n^+p junction diodes were fabricated on p-type, (100)-oriented silicon wafers with 0.4~0.6 Ω-cm nominal resistivity. After standard RCA cleaning, a 200 Å screen oxide was thermally grown in dry oxygen atmosphere followed by BF_2^+ implantation at 30 keV to a dose of 2×10^{13} cm^{-2} to raise the surface doping level for preventing the surface from depletion. Then, the screen oxide was removed and a 5500 Å thick SiO_2 was thermally grown by pyrogenic oxidation at 1050°C. Active regions with areas of 580×580, 270×270, and 120×120 μm^2 were defined by photolithography and chemical wet etching. A nickel (Ni) film of 300 Å thickness was sputter deposited in a dc sputtering system with a base pressure of less than 2.5×10^{-8}

torr, using a Ni target in Ar ambient at a pressure of 2×10^{-3} torr with a deposition rate of about 10 Å/sec. After the Ni film deposition, the samples were rapid thermal annealed (RTA) at 500°C for 30 sec in a N_2 ambient to form NiSi. The unreacted Ni film was selectively etched using a solution of H_2SO_4:H_2O_2=3:1 at 75~85°C. The NiSi film formed was determined to be 615 Å in thickness by cross-sectional TEM observation. The n^+p junction diodes were formed by P^+ implantation or P^+/F^+ dual implantation into/through the NiSi silicide followed by thermal annealing at temperatures ranging from 600 to 750°C in a N_2 ambient for 90min. The P^+ implantation was performed at an energy of 35 (sample P1) or 50 keV (sample P2) to a dose of 5×10^{15} cm^{-2}, while the P^+/F^+ dual implant was performed first with 35 keV/5 $\times10^{15}$ cm^{-2} P^+ implantation followed by F^+ implantation at 30 keV to a dose of 5×10^{15} cm^{-2} (sample P1F5) or with 50 keV/5×10^{15} cm^{-2} P^+ implantation followed by F^+ implantation at 30 keV to a dose of 2×10^{15} (sample P2F2), 4×10^{15} (sample P2F4) or 5 $\times10^{15}$ cm^{-2} (sample P2F5). The sample identification and the implantation conditions are summarized in Table 2.1 (chapter 2). Since the presence of fluorine in silicide can promote the thermal stability of the silicide film, as reported in chapter 2 of this dissertation as well as elsewhere in the literature [13-14], the F^+ implant is designed to improve the high temperature thermal stability of the P^+ implanted NiSi film. Finally, a 5000-Å-thick Al layer was deposited on the backside of Si substrate for all samples

for a better contact in electrical measurements.

The thickness of the as-deposited Ni film and the NiSi film formed was determined by cross-sectional TEM observation. Sheet resistance was measured by four-point probe on the unpatterned area. X-ray diffraction (XRD) analysis was used for material phase identification. Secondary ion mass spectrometry (SIMS) was used to determine the elemental concentration profiles. Surface morphology was observed by scanning electron microscopy (SEM). The n^+p junction depth was determined by spreading resistance profiling (SRP) measurement. The current-voltage (I-V) characteristics of the NiSi/n^+p junction diodes were measured by a semiconductor parameter analyzer HP-4145B. The open circuit leakage current of the measuring system was kept below 0.5 pA. The forward bias from 0 to -1 V at a step of 0.01 V and the reverse bias from 0 to 5 V at a step of 0.05 V were used for the I-V characteristics measurement. Temperature dependence of the reverse junction current was measured from room temperature to 200^{o}C on a thermal vacuum chunk.

4.3 TRIM simulation

Before making the P^+ or P^+/F^+ implantation, the as-implanted dopant distributions in NiSi film and Si substrate were predicted by TRIM (transport of ions in matter) simulation. Figure 4-1 shows the as-implanted phosphorus and fluorine

profiles obtained by TRIM simulation for P^+ implantations at energies of 35 and 50 keV to a dose of 5×10^{15} cm^{-2} and F^+ implantations at 30 keV to a dose of 2, 4, and 5×10^{15} cm^{-2}. For the P^+ implantation at 35 keV, nearly all implanted phosphorus ions are located inside the silicide layer. In this case, the silicide film serves as a diffusion source of phosphorus for the n^+p junction formation during the subsequent thermal annealing process. Phosphorus in the silicide layer has to diffuse into the silicon substrate and become electrically active to form a good junction. For the P^+ implantation at 50 keV, the interface phosphorus concentration is about 3×10^{20} cm^{-3}, which is high enough to form a good junction provided that sufficient dopant can be electrically activated. In this study, the implantation of P^+ ions was used in stead of As^+ ions to promote the drive-in efficiency in the subsequent annealing process because of the higher diffusivity of phosphorus atom and the lesser degree of Ni knock-on effect by P^+ implant. Since the NiSi film tends to agglomerate at higher temperatures, the P^+/F^+ dual implant is designed to improve the thermal stability of the silicide film by the incorporation of fluorine atoms [13-14].

4.4 Results and discussion

[A] Material characterization

The sheet resistance, XRD spectra, SIMS depth profile of fluorine and surface

morphology for the BF_2^+ implanted NiSi/Si samples with a post-implant furnace annealing at various temperatures are already presented and discussed in section 2.3.3.1 and 2.3.3.2 in chapter 2 (Fig. 2-10 to Fig. 2-15). It was confirmed once again that the incorporation of fluorine atoms in the NiSi film promotes the thermal stability of NiSi film and retard the formation of $NiSi_2$ silicide phase.

[B] Junction depth

The n^+p junction depth was determined by SRP measurement using an SSM-150 SRP system. All samples prepared for the SRP measurement were first capped with a 3000-Å-thick plasma-enhanced chemical vapor deposited (PECVD) oxide layer and then were polished to a small beveling angle of 17' for better resolution [15]. Table 4.1 lists the junction depths measured from the silicide/Si interface for the NiSi/n^+p junction diodes studied in this work. Only the samples fabricated with thermal annealing at 700 and 750^{o}C were measured, since thermal annealing at 600 and 650^{o}C did not result in a good junction. Thermal annealing at the higher temperature of 750^{o}C resulted in an increase of junction depth. Moreover, the F^+ ion implanted samples have a shallower junction than the corresponding samples without the F^+ implantation because the fluorine incorporation has the effect of reducing diffusivity of phosphorus atoms [16].

[C] Electrical characteristics

(a) Forward ideality factor

The forward ideality factor η of the NiSi/n^+p junctions was extracted from the basic I-V relation $I=Is[\exp(qV/\eta kT)-1]$, similar to that shown in section 3.4.1 [C] (a) in chapter 3. Figure 4-2 shows the ideality factor versus annealing temperature for the NiSi/n^+p junction diodes. For the samples annealed at low temperatures (600 and 650^{o}C), the large ideality factor is presumably due to insufficient number of activated dopant in Si substrate; thus the junction position is too close to the NiSi/Si interface. Much better results were obtained when the annealing temperature was raised to 700^{o}C, in particular for the P^+/F^+ dual implanted samples. With thermal annealing at 750^{o}C, further improvement in ideality factor was obtained for the samples implanted with F^+ ions to a higher dose ($\geqq 4\times10^{15}$ cm^{-2}). Specifically, the η value is about 1.08 for the sample P1F5. The variation of the ideality factor with respect to the annealing temperature is consistent with that of the sheet resistance and surface morphology (chapter 2, Fig. 2-10 and Fig. 2-13 to Fig. 2-15). However, it is notable that there is a totally different annealing temperature dependence of ideality factors for the samples P1 and P2, which were prepared under the same conditions except their implantation energies. For the P1 sample, nearly all implanted phosphorus ions are located inside the silicide layer, and the phosphorus in the silicide layer has to diffuse into the silicon

substrate and become electrically active to form a good junction. Upon annealing at temperatures above 700°C, the NiSi film became agglomerate and the non-uniform NiSi/Si interface may induce silicide spiking into the junction region, leading to the increase of ideality factor. On the other hand, the P2 sample has a deeper junction than the P1 sample, and thus has a higher tolerance to the roughness of the NiSi/Si interface. Nonetheless, the ideality factor is still too large for the 750°C-annealed non-fluorinated P2 sample because of serious silicide film agglomeration.

(b) Reverse current density

Figure 4-3 shows the reverse bias current density (J_R) versus annealing temperature for the NiSi/n^+p junction diodes with an area of 580×580 μm^2 measured at a reverse bias of 5 V. A remarkable increase in reverse current was observed for the samples without or with insufficient F^+ implantation (samples P1, P2, and P2F2) annealed at 750°C. In these samples, the NiSi silicide film is seriously agglomerated and, in fact, has turned into isolated islands. The silicide film agglomeration always leads to rugged silicide/Si interface, and the roughness of the silicide/Si interface in a shallow junction may lead to localized silicide spiking and/or the formation of localized Schottky contacts, resulting in the increase of reverse bias current. For the samples annealed at and below 650°C, the large reverse current is presumably due to

low level dopant activation and insufficient phosphorus concentration in the Si substrate. Annealing at higher temperatures (700 and 750°C) significantly reduces the reverse current for the samples implanted with high dose F^+ ions ($\geqq 4\times10^{15}$ cm^{-2}) because of the improved dopant activation and the sufficient phosphorus concentration and implantation-induced damage recovery in the Si substrate, as well as the NiSi film integrity due to its improved thermal stability. A very low reverse current density of 0.7 nA/cm^2 was obtained for the samples annealed at 750°C.

(c) Area and peripheral current

The reverse bias leakage current (I_R) of a n^+p junction consists of the reverse area leakage current (I_{RA}) and the reverse peripheral leakage current (I_{RP}):

$$I_R=I_{RA}+I_{RP}=A\times J_{RA}+P\times J_{RP}$$

where A is the junction area, P is the length of junction perimeter, J_{RA} is the junction area leakage current density, and J_{RP} is the junction peripheral leakage current density. A simple arrangement gives

$$J'_R=J_{RA}+J_{RP}(P/A)$$

where $J'_R=I_R/A$. Thus, by measuring the I_R of junctions with different P/A ratio, the slope of J_R' versus P/A plot gives the J_{RP} and the Y-axis intersection gives the J_{RA}. The I_R at 5 V reverse bias was measured on the junction diodes with three different sizes

of 580×580, 270×270, and 120×120 μm^2. Figure 4-4 shows the extracted J_{RA} and J_{RP} for the NiSi/n^+p junctions of sample P1F5 thermally annealed at 600 to 750°C. It was found that the J_{RA} is 1.47×10^{-10} A/cm^2 and the J_{RP} is 1.02×10^{-15} A/um for the 750°C-annealed sample P1F5. For the junction diode with a size of 580×580 μm^2 formed by annealing at 750°C, the area and peripheral current are 0.49 and 2.4 pA, respectively. This indicates that 83% of the total reverse current leaks through the junction's perimeter. For a smaller junction with an area of 120×120 μm^2, the perimeter component accounts for 96% of the total reverse current, indicating the major role of the perimeter leakage component. In section 2.3.3.2 of chapter 2, we have shown that the sample P1F5 was able to retain the integrity of its NiSi film and NiSi/Si interface up to thermal annealing at 750°C, which is capable of annealing out most of the implantation-induced damage. Thus, the J_{RA} and J_{RP} reach their lowest values after annealing at 750°C. The peripheral leakage is sensitive to the interfacial behavior of Si/SiO_2 along the junction perimeter because the junctions formed in this study are all surrounded by field oxide. It is notable that the distance from the silicide/Si interface to the junction at the diodes perimeter is much shorter than that at the diodes bottom area after the post implant thermal annealing. Moreover, the mechanical stress induced defects along the diodes perimeter is presumed to cause a higher peripheral leakage [17]. Thus, the junction characteristics are very sensitive to

the silicide/Si interface property. Figure 4-5 illustrates a typical I-V characteristic for the NiSi(615 Å)/n^+p junction (sample P1F5) which was fabricated by P^+/F^+ dual implantation at 35/30 keV to a dose of $5\times10^{15}/5\times10^{15}$ cm^{-2} followed by a 750°C thermal annealing for 90 min. It is clear that NiSi can serve as an efficient diffusion source for phosphorus diffusion during the low-temperature thermal annealing process, resulting in the formation of NiSi/n^+p shallow junction with superb electrical characteristics.

(d) Activation energy measurement

The temperature dependence of reverse bias junction current can provide insight into the junction leakage mechanism. The temperature dependence of reverse current I_R is given by

$$I_R \propto T^3 \exp(-E_a/kT)$$

where Ea is the activation energy of the junction, k is the Boltzmann constant, and T is the temperature at measurement. The Ea can be extracted from the slope of the semilogarithmic plot of log (I_R/T^3) vs 1/T. The value of Ea is close to the bandgap of silicon Eg when the reverse current is dominated by the diffusion current and is close to Eg/2 when the reverse current is dominated by the generation current. Figure 4-6 shows the Arrhenius plots of reverse currents for the NiSi/n^+p junction of the

750°C-annealed sample P1F5 measured at 1 V reverse bias. Four data sets are illustrated including the Arrhenius plots of J_{RA}, J_{RP}, and two I_R of different diode area. In the entire temperature range from 40 to 200°C, the value of Ea for the J_{RA} indicates that the reverse area current was dominated by the minority carrier diffusion current. This also implies that the 90 min thermal annealing at 750°C efficiently diffused and activated the implanted phosphorus dopant and eliminated the implantation-induced damage in the diode's flat bottom area. However, the value of Ea for the J_{RP} shows a different behavior; it is 0.97 eV at temperatures above 100°C, while it is 0.63 eV at temperatures below 100°C. This indicates that the reverse peripheral current was dominated by the minority carrier generation current at low temperatures (including room temperature). The implication is the presence of generation centers in and/or close to the junction region along the perimeter. If these generation centers are located within the depletion region of the n^+p junction, the minority carrier generated will contribute to the reverse leakage current. Thus, the peripheral current I_{RP} and the I_R of junctions with smaller areas are easily dominated by the generation current, particularly at low temperatures.

4.5 Conclusion

This chapter investigates the formation of NiSi-contacted n^+p shallow junction

diodes using P^+/F^+ dual implantation into/through thin NiSi silicide layer followed by low temperature furnace annealing. For the NiSi-contacted n^+p shallow junctions studied in this work, the junction depth ranges from 61 to 149 nm measured from the NiSi/Si interface, and the reverse bias current density of less than 1 nA/cm^2 can be easily achieved. Specifically, the NiSi(615 Å)/n^+p junction fabricated with P^+/F^+ dual implantation at 35/30 keV to a dose of $5\times10^{15}/5\times10^{15}$ cm^{-2} followed by a 90 min thermal annealing at 750^{o}C, has a forward ideality factor of 1.08, a reverse bias current density (at 5 V) of 0.7 nA/cm^2, and a junction depth of 71 nm. The activation energy measurement shows that the reverse bias area current (I_{RA}) is dominated by the diffusion current while the reverse bias peripheral current (I_{RP}) is dominated by the generation current at low temperatures (including room temperature). This implies the presence of generation centers in and/or close to the junction region along the perimeter. For the diode's size smaller than 120×120 μm^2, the total reverse current would be dominated by the minority carrier generation current induced by the generation centers in and/or close to the junction region along the perimeter.

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Table 4.1 Junction depths (in unit of nanometer) of NiSi(615Å)/n^+p junction diodes studied in this work.

Annealing temperature	Sample ID					
	P1	P2	P1F5	P2F2	P2F4	P2F5
700°C	61	110	54	93	85	65
750°C	73	149	71	127	110	93

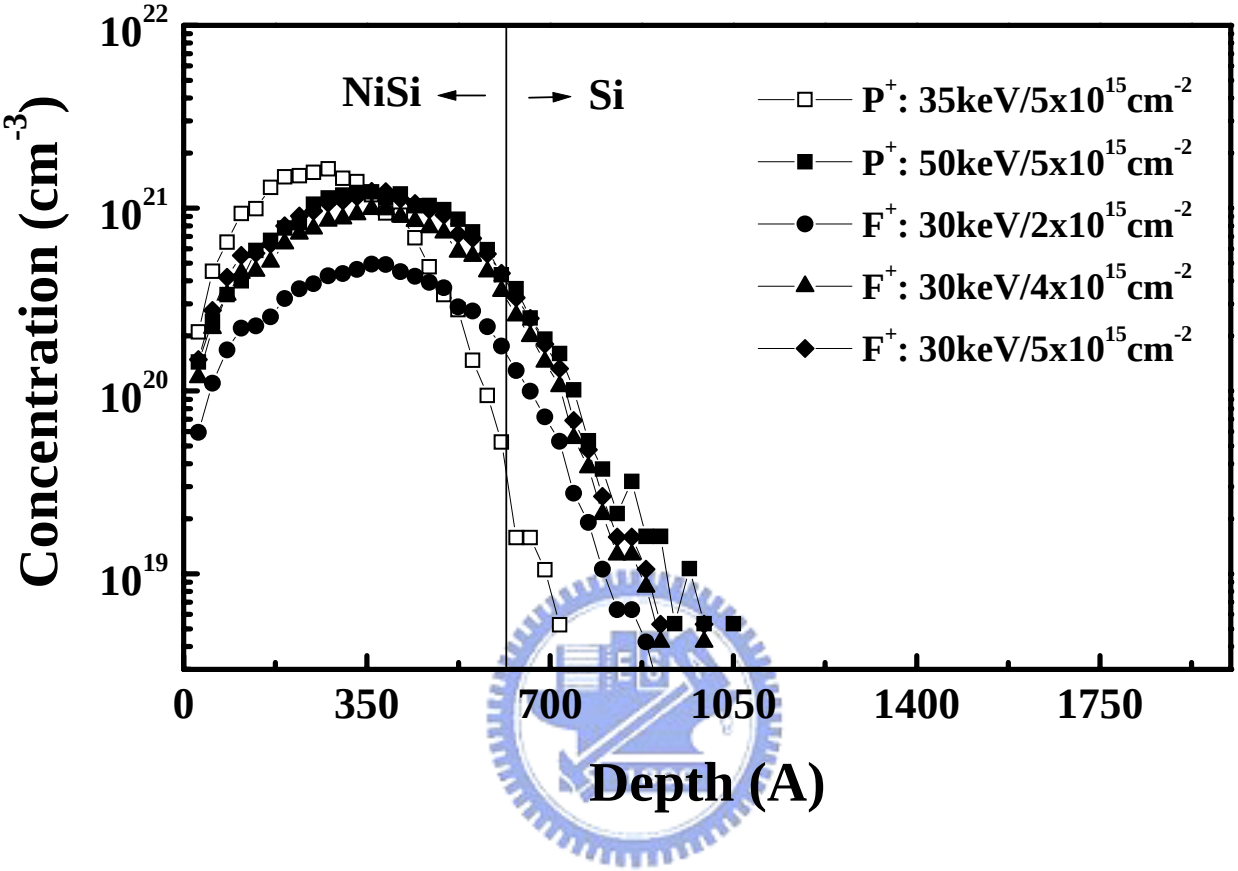

Fig. 4-1 The as-implanted phosphorus and fluorine profiles obtained by TRIM simulation for various P^+ and F^+ implantations.

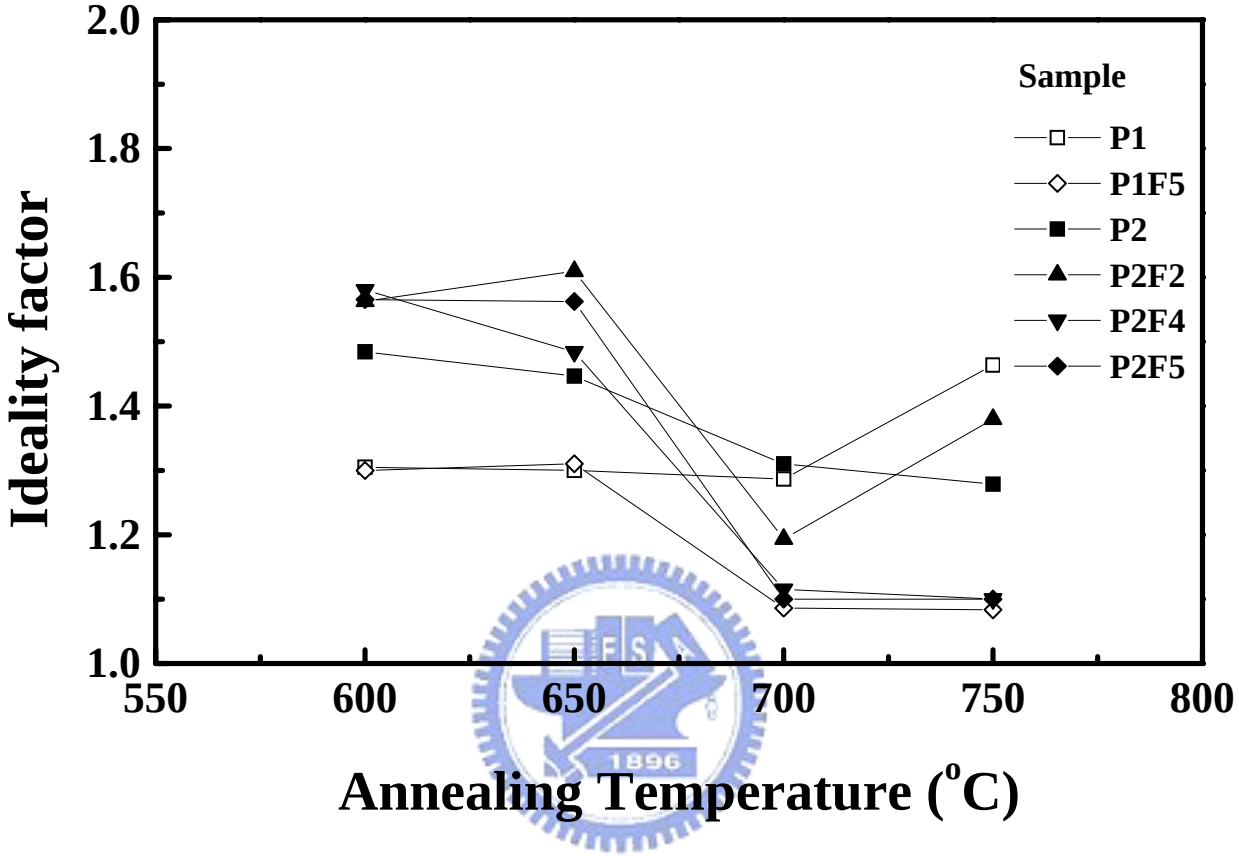

Fig. 4-2 Forward ideality factor vs. annealing temperature for the NiSi(615Å)/n^+p junction diodes.

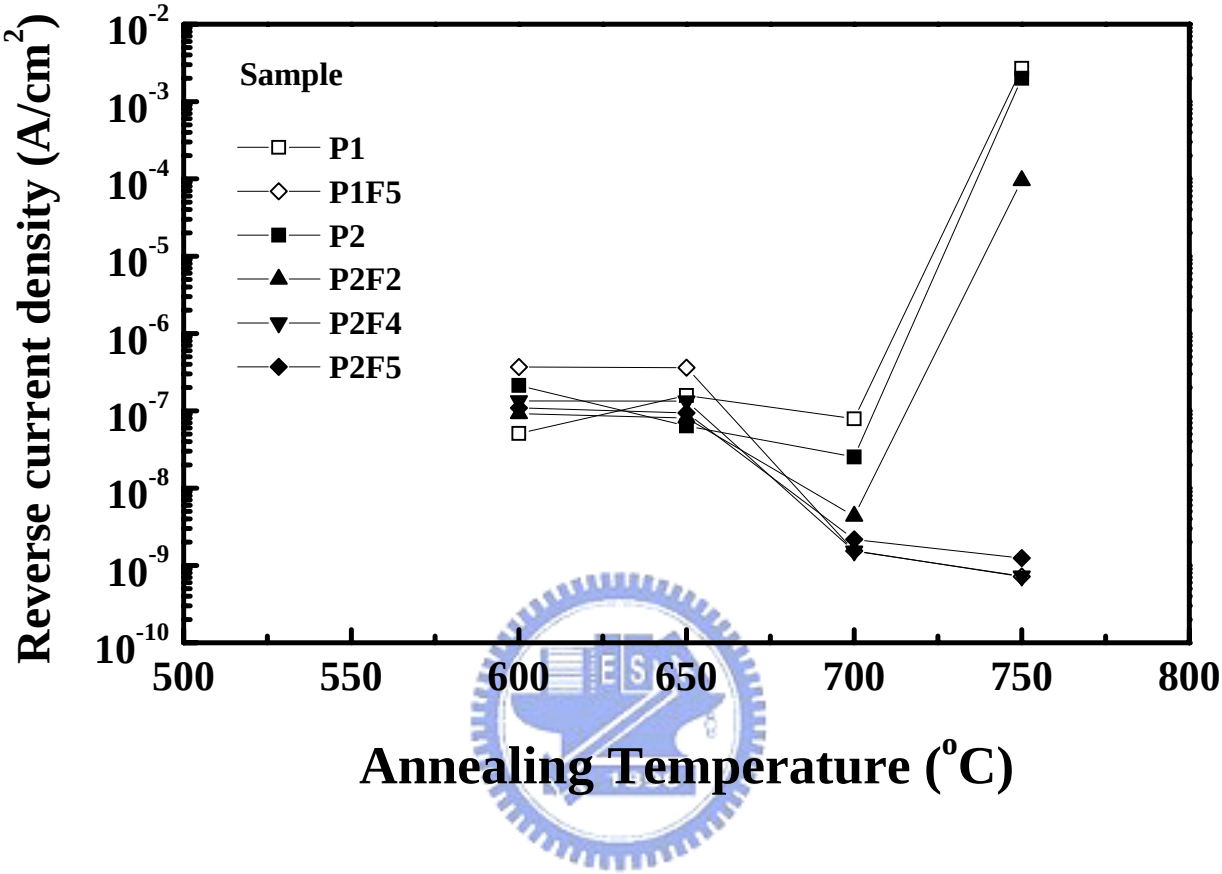

Fig. 4-3 Reverse bias (5V) current density vs. annealing temperature for the NiSi (615Å)/n^+p junction diodes with a junction area of 580×580μm^2.

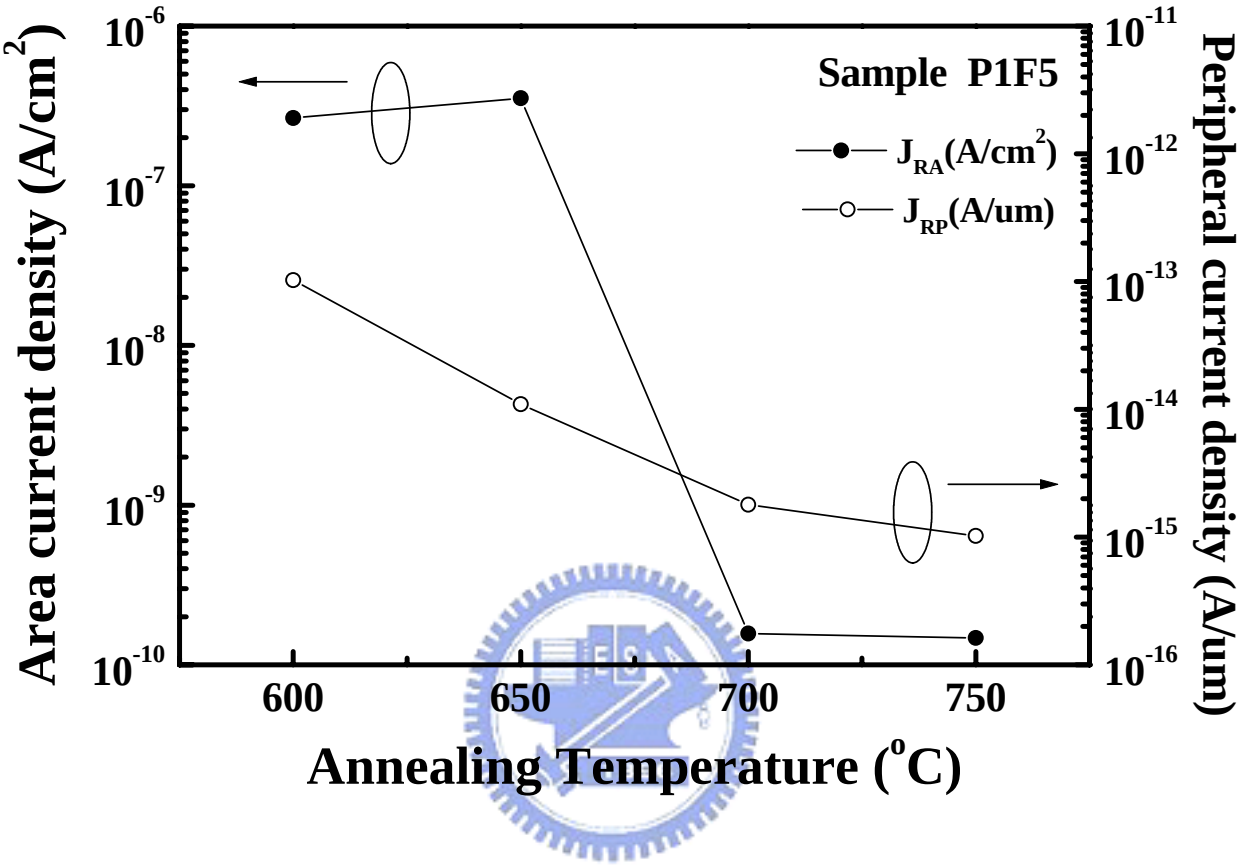

Fig. 4-4 Area and peripheral leakage current densities for the NiSi(615Å)/n^+p junction of sample P1F5 thermally annealed at 600 to 750^{o}C.

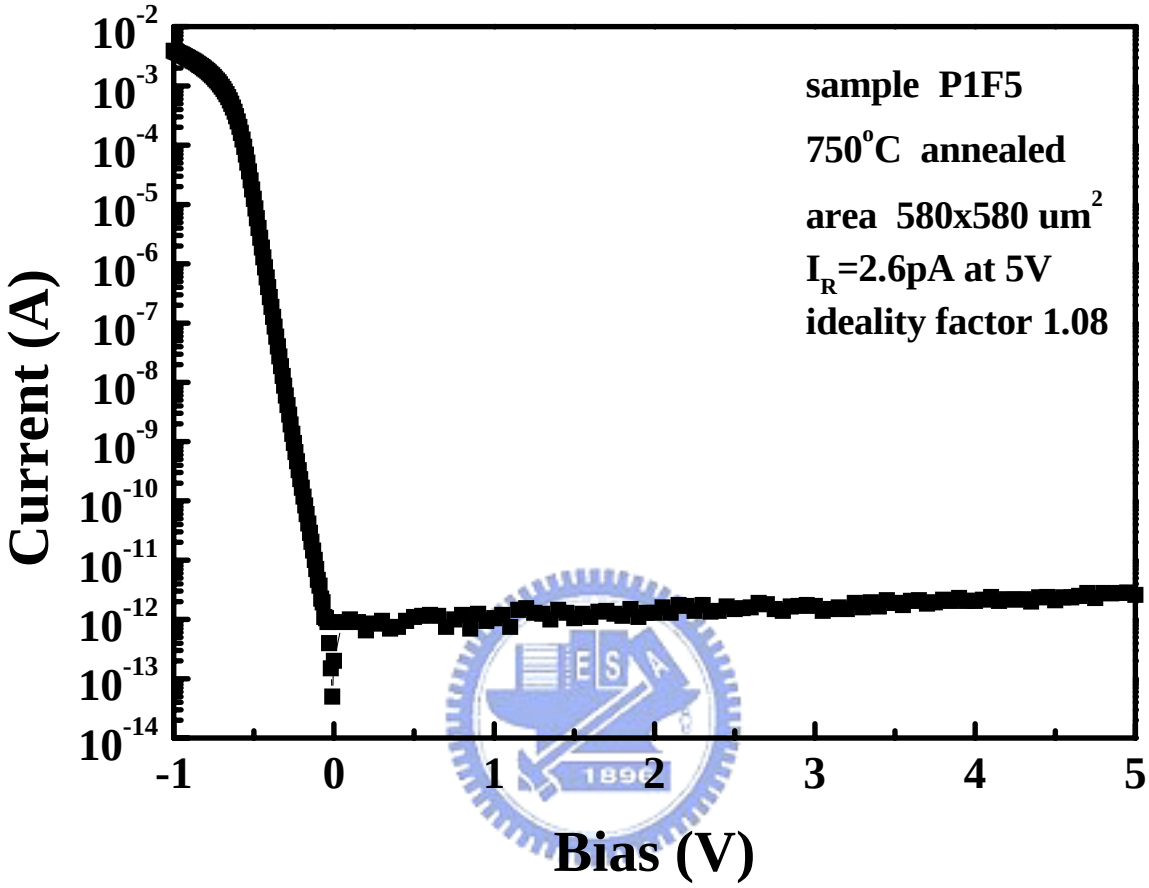

Fig. 4-5 Typical I-V characteristic for the NiSi(615Å)/n^+p junction of sample P1F5 fabricated with P^+/F^+ dual implantation at 35/30keV to a dose of $5\times10^{15}/5\times10^{15}cm^{-2}$ followed by a 90 min thermal annealing at 750°C.

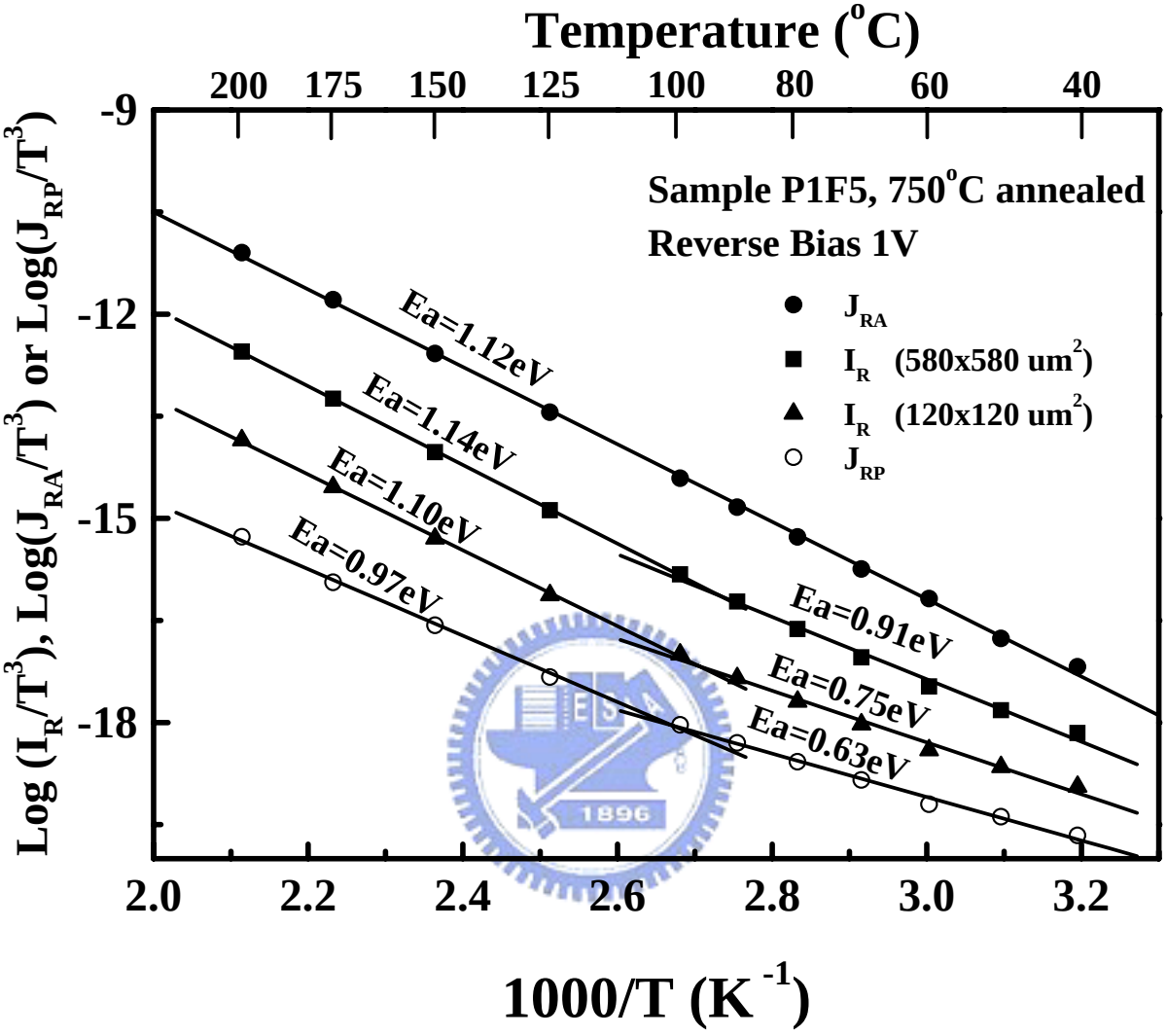

Fig. 4-6 Arrhenius plots of reverse current for the NiSi(615Å)/n^+p junction of 750°C-annealed sample P1F5, measured at 1V reverse bias.