Chapter 1

Introduction

1.1 Overview

In order to improve the performance and packaging density of MOS integrated circuits, device dimension has been scaled down to deep sub-micron regime. Therefore, the line width of interconnects also becomes narrower and the interconnect resistance is increasing. Moreover, the reduced contact areas of poly gate and source/drain regions result in the increase of contact resistance, leading to the increase of RC time delay and power dissipation within the circuit. Thus, the drawback of resistance increase must be reduced effectively to achieve high performance integrated circuits with faster speed and less power consumption.

In the past twenty years, many efforts have been made to develop a new technology for reducing parasitic resistance to improve the devices and circuit performance. Since 1966, metal silicides have been proven valuable to both ohmic and Schottky contacts [1]. In order to increase the devices operation speed, polycide structure, in which a high conductivity metal silicide combines with an underlayer of doped polysilicon in a form of silicide/polysilicon, was proposed to reduce polysilicon gate resistance [2]. The resistivity of metal silicide is normally one order of magnitude lower than that of the heavily doped polysilicon. In 1981, the concept was extended to

diffusion area simultaneously for improving both contact and interconnect [3].

Many noble and refractory metals interact with silicon to form stable silicide phase. These silicides have fairly low resistivity and good high-temperature-stability. The self-aligned-silicide (salicide) process is widely used in integrated circuits to reduce polysilicon gate resistance and source/drain contact resistance. The self-aligned-silicide technology possesses a number of advantages. First, the silicide is selectively formed on the polysilicon gate and source/drain diffused regions, while oxide or nitride can serve as a reaction mask. Thus, the process is simple because no additional mask is needed. Second, silicidation of source/drain regions can ease aluminum-induced junction spiking; as a result, the junction characteristics can be considerably improved. Third, the silicidation of source/drain regions not only reduces the sheet resistance, but also converts the diffusion surface into silicon-metal contact area [4-5]; thus, lower contact resistance between silicide and silicon can be achieved. It is obvious that metal silicides have become an indispensable part of IC technology. However, each meal silicide has its own technical difficulties and no single metal can satisfy all electrical and material characteristics in the salicide process. Thus, it is necessary to study the silicide properties and process technology so as to master the application of metal silicides in integrated circuits.

1.2 Selection of a silicide

Many metals, including most refractory and near-noble metals, have been studied for the salicide process. Before introducing silicides into integrated circuits, many properties of silicides related to the remaining process must be considered carefully for the best choice of a suitable silicide. The desired properties of silicides for IC process are low resistivity, ease of formation, ease of pattern definition, minimum silicon consumption, high thermal stability, less stress, good adhesion, no metal-compound formation, low contact resistance, smooth surface and silicide/silicon interface, no lateral growth, easy selective etching, no contamination to device, wafer, or equipment, and high barrier height for Schottky applications [6]. No single silicide can meet these requirements all together. For example, PtSi reveals low resistivity but it suffers from poor high-temperature-stability, whereas WSi_2 shows excellent thermal stability but its resistivity is too high [7].

Among the metal silicides, titanium disilicide ($TiSi_2$) and cobalt disilicide ($CoSi_2$) are widely used in salicide process across the industry because of their good thermal stability and low electrical resistivity. However, some critical drawbacks limit their applications to the future ULSI technology. It has been reported that Ti may react with implanted dopant to form compounds such as Ti-B and Ti-As, making $TiSi_2$ a very ineffective diffusion source for boron or arsenic [8-9]. Moreover, the processing

temperature window of $TiSi_2$ is relatively narrow due to the high temperature requirement for the high resistivity C49 to low resistivity C54 phase transition (≧ 800°C) and the silicide agglomeration temperature limit (~950°C) [10]. More importantly, when the linewidth is scaled down below 2μm, there is an increase in sheet resistance in the narrow $TiSi_2$ lines because the lack of nucleation center in the narrow lines causes incomplete transformation from C49 to C54 $TiSi_2$ phase [11-13]. This is becoming a serious problem for device scaling. The C49 structure is characterized by smaller grain (0.2 μm) and larger resistivity (60-80 μΩ-cm) while the C54 structure features a large grain as compared with the line width and lower resistivity (10-16 μΩ-cm). The increase of sheet resistance for the $TiSi_2$ line with decreasing line width limits the feature of $TiSi_2$ salicide in 0.1μm CMOS applications [14-15]. In addition, the creep-up phenomenon during the formation of $TiSi_2$ silicide may form a bridge between the gate and source/drain regions, causing device failure [16].

Unlike $TiSi_2$, cobalt disilicide ($CoSi_2$) has neither adverse linewidth dependence nor creep up phenomenon. Thus, Co-silicide has been extensively used in the quarter and sub-quarter micron technology. In addition, $CoSi_2$ has other advantages over $TiSi_2$, such as better stability in the presence of dopants [17], better plasma etching resistance, and less film stress because of its excellent lattice match

with Si (-1.2% at room temperature). However, high Si consumption (Co : Si : $CoSi_2$ = 1 Å : 3.63 Å : 3.49 Å) during the formation of $CoSi_2$ silicide is a major drawback, which restricts the vertical scaling for $CoSi_2$ to achieve shallow junction [18]. Moreover, junction spiking of $CoSi_2$-contacted shallow junction due to its sensitivity to native oxide and oxygen-contained environment needs a more complex silicidation process, such as capping a passivation film during silicidation [19-20].

Recently, nickel monosilicide (NiSi) has been recognized as a promising candidate for a contact metal in the future ULSI salicide applications [21-27]. For a Ni film on a Si substrate (assuming infinite supply of Si material), there are three Ni-silicide phases, Ni_2Si, NiSi and $NiSi_2$, formed in sequence at temperatures of 250, 350 and 750°C, respectively [22]. Among the three Ni-silicide phases, NiSi is a low resistive phase with an electrical resistivity of 14-20 $\mu\Omega$-cm, which is comparable to those of $TiSi_2$ and $CoSi_2$. NiSi shows neither adverse resistivity dependence on linewidth nor creep-up phenomenon [23-24]. Moreover, NiSi has a lower formation temperature than $TiSi_2$ and $CoSi_2$, making it suitable for the low-temperature process required in future device fabrication. The further advantage of NiSi relies on its smaller consumption of Si (0.82 Å Si for 1 Å NiSi) compared to the formation of $CoSi_2$ (1.04 Å Si for 1 Å $CoSi_2$) and $TiSi_2$ (0.9 Å Si for 1 Å $TiSi_2$) [18], which facilitates the formation of shallow junction at the silicide/Si contact. Besides, NiSi

has the properties of low NiSi/Si contact resistance [25], wide process window (350~750°C), and low film stress [26-27]. These peculiarities make NiSi suitable for use in the low-temperature process for sub-100nm CMOS technology.

The use of metal silicides in CMOS technology is mostly found at the source/drain contacts, polycide gate electrode, and local interconnects. Silicidation of souce/drain junctions is a more skilled work than that of gate electrodes. Improper silicidation scheme may result in unacceptable high leakage current and make the devices consuming enormous power. Silicidation of source/drain junctions consumes most of the heavily doped regions; consequently, the resultant I-V characteristics and contact resistance may be degraded. Furthermore, it is very hard to fabricate sub-0.1um junctions by means of conventional high temperature process. The implant–through-silicide (ITS) scheme is a promising solution to the formation of sub-0.1um shallow junctions at a low temperature [28-30]. The ITS scheme uses a silicide film to function as an implantation damage basin and thus the process temperature can be greatly reduced. The silicide film also acts as an energy barrier for the implanted ions and thus shallow junctions can be obtained. This merit is especially important and useful for $p^{+}n$ junctions because boron is a very light element and is a fast diffuser in silicon. Using ITS scheme has another merit of alleviating channeling effect due to different structure between silicide and silicon. The feasibility of the ITS

scheme is carefully evaluated in this study because it offers many bountiful advantages.

1.3 Thesis Organization

In the first chapter of this dissertation, we briefly review the necessity of applying silicides in CMOS technology, and the reasons of selecting NiSi as the object in this study. In Chapter 2, we investigate the thermal stability of the NiSi/Si system. The improvement of therml stability by the incorporation of fluorine atoms in the NiSi/Si system via fluorine ion implantation is systematically investigated.

Chapter 3 and chapter 4 report, respectively, the formation and characterization of the NiSi-contacted p^+n and n^+p shallow junctions using implantation into/through silicide (ITS) scheme. By using various techniques of electrical and material analyses, we determine the most favorable process conditions for the formation of NiSi-contacted p^+n and n^+p shallow junctions.

Chapter 5 investigates the thermal stability of Cu/NiSi-contacted p^+n shallow junction diodes. The barrier capability of NiSi layer as well as the degradation mechanism of the Cu/NiSi-contacted p^+n junction diodes is studied by electrical and various techniques of material analysis.

Finally, Chapter 6 gives the conclusion of this dissertation and the suggestion

for future work.

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