低溫多晶矽薄膜電晶體的雷射退火技術暨晶粒邊界對元件電性與熱載子可靠度探討

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摘要

利用雷射再結晶技術製作低溫多晶矽薄膜電晶體（LTPS TFTs）於大面積玻璃基板上已成為發展主動陣列液晶顯示器(AMLCDs)和主動陣列有機發光顯示器(AMOLEDs)的關鍵技術，然而傳統雷射再結晶技術無法有效控制通道內晶粒邊界的方向、相對位置及其數量多寡，如此會造成元件電特性的變動進而無法整合類比電路於面板上，這將是決定低溫多晶矽薄膜電晶體可否取代非晶矽薄膜電晶體的關鍵因素。本論文提出三種新穎的雷射再結晶技術，除了利用溫度調變方式拉大通道內矽晶粒而有效地提升薄膜電晶體的場效載子移動率之外，我們也提出利用單晶矽作為雷射再結晶之晶種來製作單晶矽薄膜電晶體的方法，另外我們也製作了晶粒邊界不對稱地分佈於通道內的薄膜電晶體，藉由單一顆元件順向與反向的量測來研究晶粒邊界數量多寡在汲極端的高電場下對元件電特性及其熱載子可靠度的影響。

傳統雷射製作低溫多晶矽薄膜電晶體的方法是先對非晶矽薄膜進行雷射再結晶後才定義出元件主動層區域，如此元件與元件間的電特性會因為不可控制的晶粒邊界方向、相對位置及其數量多寡而變動，若先定義元件主動層區域後再進行雷射再結晶，雖然單一顆元件電特性會因主動層區域邊緣的晶粒較大而變好，但如此作法會使主動區域因熔融矽的表面張力而微縮變形，無法用在實際生產線上，因此我們提出了一個先將主動層區域的邊緣增厚後再進行雷射再結晶的作法，我們利用非等向性的電漿蝕刻技術將主動層區域的邊緣增厚，經由雷射照射後，矽島的邊緣永遠只會部分熔融且熔融矽有一高度差存在，加上主動層上方的低溫氧化層，如此便徹

底地解決了矽島會微縮的問題，且一溫度梯度存在於矽島邊緣附近，若使用準分子雷射照射可使矽晶粒從邊緣處拉大進而提高薄膜電晶體的場效載子移動率，之後再利用非等向性的電漿蝕刻以矽島上的低溫氧化膜作為保護層可將邊緣增厚區域完全去除，如此的製作可抑制薄膜電晶體的漏電流及汲極端導致能障下降(DIBL)效應。

另外，雖然讓通道座落在單一顆矽晶粒上可使薄膜電晶體電特性達到最佳化，但矽晶粒之間存在著不同的結晶方向，仍然無可避免元件跟元件間電特性的差異，因此我們提出一個以單晶矽作為雷射再結晶之晶種來製作單晶矽薄膜電晶體於玻璃基板上的方法，我們一開始用矽晶片來模擬此實驗，在完成傳統 LOCOS 製程後讓（111）（110）（100）三種結晶方向的矽晶面與非晶矽薄膜接觸，利用準分子雷射對矽薄膜進行再結晶，期待熔融矽以單晶矽基板作為晶種而進行單晶矽的再結晶，以便在緩衝氧化層上製作出不同晶格方向的單晶矽薄膜電晶體，然而在玻璃基板的實現上，利用有圖案的單晶矽基板與玻璃基板上的非晶矽薄膜接觸後，利用雷射光從玻璃基板背面照射，讓非晶矽薄膜與單晶矽之晶種熔融後，熔融矽薄膜會以單晶矽作為晶種而觸發單一晶格方向的矽薄膜成長。

其次，我們用氮化矽作為硬式光罩對50nm厚的複晶矽薄膜進行選擇性氧化，在去除氮化矽後再疊上一層 100nm 厚的非晶矽薄膜，此時以準分子雷射進行再結晶，由於存在一溫度梯度可使矽晶粒橫向拉大，利用此法所製作的薄膜電晶體於較短通道長度會有場效載子移動率明顯上升的現象，此乃歸因於晶粒邊界數量於通道內減少的原因，但利用此法所製作的短通道硼摻雜 P 型薄膜電晶體在量測幾次後會有次臨限區域平行飄移的現像，我們認為這是因為閘極處的硼原子在 600℃長時間活化下會在閘極氧化層內形成電洞缺陷，這些缺陷在量測時會捕捉電洞而帶正電於閘極氧化層內，因此造成下一次量測時次臨限區域平行向較負偏壓方向移動，由於關電

流與開電流幾乎沒有改變，因此我們斷定這是閘極氧化層內電洞缺陷所造成的現象。

最後，本論文針對晶粒邊界數量多寡在汲極端的高電場下對元件電特性及其熱載子可靠度（Hot-carrier reliability）的影響做了深入的分析，我們製作了晶粒邊界不對稱地分佈於通道內的薄膜電晶體，藉由單一顆電晶體順向與反向的量測以保證不會有因元件與元件間的不同而造成特性差異的因素，在元件電特性的表現上，晶粒邊界在汲極端的高電場作用下會產生較大的漏電流使得開關電流比值下降，這是因為晶粒邊界會捕捉載子，而被捕捉的載子在高電場下會藉由場效熱離子放射（thermionic-field emission）方式被釋放出來而使漏電流大幅上升，此外晶粒邊界在汲極端的高電場作用下會使臨限電壓值隨著汲極電壓的上升而下降，因晶粒邊界所捕捉的載子會使汲極端的空乏區額外的往源極端延伸，這暗示了晶粒邊界在汲極端附近會有短通道效應的發生。在熱載子可靠度分析上，外加偏壓(V_{GS}=10V、V_{DS}=20V）於未氫化單一顆元件上，先順向持續偏壓 10^4 秒後再反向持續偏壓 10^4 秒，我們發現在順向 10^4 秒後的元件電特性幾乎不變，但在緊接著反向 10^4 秒後的元件電特性會被徹底破壞，這是因為元件在反向模式下，其晶粒邊界在汲極端會產生多處的局部高電場，在高電場的作用下容易使晶粒邊界的弱 Si-Si 鍵結產生斷鍵，同一時間斷鍵所造成的熱電洞會被注入到靠近汲極端的閘極氧化層內而產生正電荷的累積，如此會抑制元件因通道內產生更多缺陷而變差的現象，但當元件緊接著進行順向持續偏壓 10^2 秒過程中，靠近源極端閘極氧化層內先前所注入的熱電洞會被通道電子中和掉，因此中和後的元件特性由通道破壞區域所主導，出現了大幅度衰退現象，這是注入於閘極氧化層的熱電洞遮蔽了通道內缺陷產生的屏蔽效應（Screen Effect），另外若將元件做 4 小時的 NH_3 電漿處理則看不到上述順向反向模式下的差

異，這乃歸因於NH_3電漿處理可以有效鈍化晶粒邊界所造成的缺陷，雖然鈍化所產生的矽氫（Si-H）、矽氮（Si-N）等弱鍵結會使元件的熱載子可靠度變差，但氫化前晶粒邊界所造成在汲極端的局部高電場效應可被有效排除。

Laser Annealing Techniques for LTPS TFTs and Influence of Grain Boundaries on Electrical Characteristics and Hot-carrier Reliability of Poly-Si TFTs

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ABSTRACT

Low-temperature polycrystalline silicon thin film transistors (LTPS-TFTs) fabricated using laser crystallization have been considered as the most promising candidates for integrating peripheral driver circuits with active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) on large area glass substrates. However, the inability to control grain boundaries and their location in the channel region reduces the uniformity of devices. This is a key point of whether LTPS TFTs can replace a-Si:H TFTs. In this thesis, there are three novel laser annealing techniques proposed to promote performance of poly-Si TFTs. In addition to modulating thickness of a-Si films to establish a temperature gradient, a-Si films are crystallized using single-crystal silicon as re-crystallization seed. The influence of laser-induced grain boundaries on performance and hot-carrier reliability of poly-Si TFTs with and without NH_3 plasma treatment is investigated.

First, a novel 4-mask-processed polycrystalline silicon thin film transistor (Poly-Si TFT) is fabricated using 50-pulse KrF excimer laser to crystallize an edge-thickened amorphous silicon (α-Si) active island without any shrinkage. This method introduces a temperature gradient across the width of the island to enlarge grains from the edge, especially when the channel width is narrow. The grain boundaries across the width of the channel suppress the leakage current and the drain-induced barrier lowing (DIBL). Moreover, the proposed poly-Si TFT with a channel length of L=2μm and a channel width

of W=1.2μm possesses a high field-effect mobility of 260 cm^2/Vs and an ON/OFF current ratio of 2.31×10^8. The proposed TFTs with divided channel units can meet the application of various gate widths. However, their performances still depend on the grain-boundary control of each channel unit.

It is believed that the performance of laser-crystallized poly-Si TFTs depends on the orientation of grains when the device is located on a whole grain. However, no study about how to control grain orientations on glass substrates is reported. In this thesis, a novel seeding technique is proposed to produce single-crystal silicon films on glass substrates. The a-Si films on glass substrate contact with single-crystal tip, and then excimer laser irradiates through the transparent substrate to crystallize the contacted a-Si films. This technique has been developing for LTPS TFTs.

The third laser annealing technique is about modulated thickness of laser-crystallized poly-Si films. A LOCOS process is employed to produce two various thicknesses of silicon film, establishing a temperature gradient for ELC. When channel length is shortened, the device located with few grain boundaries has excellent performance. High ON/OFF current ratio of over 8 orders magnitude and high field-effect mobility of exceeding 300 cm^2/Vs for the n-channel TFTs and 100 cm^2/Vs for the p-channel TFTs are ascribed to large grains in the channel region. However, there is an issue about boron penetration from the doped poly-Si gate during activation at 600℃ around 12 h. The diffused boron creates hole traps in the gate oxide. After a boron-doped TFT measures for several times, its threshold voltage shifts to more negative values because the gate oxide near drain junction is positively charged. Our SIMS depth profile supports this explanation.

Additionally, this technique is applied to examine the effects of grain boundaries on the performance and hot-carrier reliability of excimer-laser-annealed polycrystalline silicon

thin film transistors (poly-Si TFTs) before and after NH_3 plasma treatment. Self-aligned poly-Si TFTs, whose channel regions include a 150 nm thick laser-crystallized poly-Si layer with small grains and a 100 nm thick layer with large grains, are fabricated. Other TFTs, with large grains throughout their channel regions, are fabricated nearby for comparison. The trapping of electrons at grain boundaries in the drain junction creates strong local electric fields that boost the leakage current; cause the threshold voltage to decline as the drain bias increases; enhance the kink effect in the output characteristics, and degrade the hot-carrier reliability of devices. When static hot-carrier stress has been applied to non-hydrogenated poly-Si TFTs for under 10^4s at V_{GS}=10V and V_{DS}=20V, hot holes are injected into the gate oxide at the same time as trap states are created in the drain junction. The screening effect is observed when the same stress is applied to devices that have many grain boundaries in their drain junctions. Moreover, NH_3 plasma treatment prevents the trapping of electrons at grain boundaries. The performance of hydrogenated poly-Si TFTs becomes better, but the hot-carrier reliability of those TFTs with large grains in their drain junctions is degraded. The hydrogenation causes a tradeoff between the electrical characteristics and the hot-carrier reliability, and introduces irregular humps in the sub-threshold region.

誌謝

本論文的完成首先要感謝我的指導教授**葉清發**老師，葉老師在研究上的指導嚴謹詳盡，在生活上的關心無微不至，讓我這五年的博士生活中受益良多，其次也要感謝**羅正忠**老師在平時開會上所給予的指導。

在這多年的學術研究與日常生活上，我很慶興能有多位貴人的相助使我順利獲得學位，在此特別要感謝**林敬偉**學長、**曾章和**學長及**常鼎國**學弟在準分子雷射技術上所給予的協助，雷射設備多虧有他們的維護，我才得以順利完成我的研究;感謝**Yeh's Group** 的成員**蕭智文**、**王碩晟**、**楊家驊**、**劉俊彥**、**林榮祥**、**蔣陳偉**等多位學弟及多位已畢業的學長學弟們在實驗上及日常生活上的幫忙，尤其受到蕭智文與王碩晟兩位學弟的幫助甚多，如實驗室電腦與實驗機台的維護、研究計畫上的支援等等;感謝國家奈米元件實驗室（**NDL**）**宋金龍**先生、**許慶龍**先生、**徐台鳳**小姐、**陳繡芝**小姐、**李春杏**小姐、**巫振榮**先生、**趙子綾**小姐、**顏似妙**小姐在實驗上的幫忙;感謝交通大學奈米中心（NCTU-NFC）**彭兆光**先生、**陳聯珠**小姐、**張昭檳**先生、**林素珠**小姐、**何惟梅**小姐在實驗上的幫忙;感謝曾經幫助過我的人：**莊景桑**同學、**林家彬**學弟、**張芳龍**學弟、**鄧至剛**學弟等等。

最後謹以此論文獻給我的父母親**陳水秤**先生、**簡雪雲**女士，感謝他們二十多年來的支持與照顧，同時也感謝哥哥、姊姊們多年來的支持與關心。

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS

CHAPTER2

CHAPTER3