Chapter 1

Introduction

1.1. BACKGROUND

Recently, there has been expanding the broad band networks, and mobile information and communication tools have been widely used. The flat panel display (FPD) which acts as a critical interface to connect with people is assembled into those mobile tools, such as cellular phones, personal digital assistants (PDA), digital cameras, notebook PCs, and so on [1]. Therefore, the FPD plays an important role in human life. To date, the FPD has been replacing the cathode ray tube (CRT) based traditional display. Meanwhile, the current FPD market has been dominated by amorphous silicon thin film transistors (α-Si TFTs) based active matrix liquid crystal display (AMLCD) [2]. However, α-Si TFTs have a low carrier mobility to limit the signal response time, and are with a large and dark area on a panel to limit the resolution. They inherently limit the performance of active matrix displays. In order to overcome these disadvantages, many techniques on low-temperature polycrystalline silicon thin film transistors (LTPS-TFTs) have been proposed to replace α-Si TFTs. LTPS TFTs integrated peripheral driver circuits with AMLCDs have been widely used [3~4], and an average of their carrier mobility is more than one hundred times the mobility of α-Si TFTs. This technology is being considered as the candidate to achieve a system on panel (SOP) and ultimately sheet computer in the future [5~6].

Many techniques for fabricating the high-performance LTPS-TFTs have been extensively investigated, such as methods of α-Si crystallization, defect reduction, and novel structure fabrication.

α-Si crystallization means that an amorphous silicon layer is crystallized into a polycrystalline silicon layer by annealing. The α-Si crystallization is the most important step in the fabrication of LTPS-TFTs. This step is the key process of limiting the thermal budget on large area glass substrates. The performance of LTPS-TFTs is strong dependent on the quality of an active layer. The solid phase crystallization (SPC) [7~9], metal induced crystallization (MIC) [10~12], and laser crystallization (LC) [13~15] are the main methods in the fabrication of LTPS-TFTs, respectively. Polycrystalline silicon is typically produced by annealing α-Si films in furnace at 550℃~600℃. This method is conventionally called SPC. Large grains can be formed by SPC, but the films of polycrystalline silicon contain a high density of intragrain defects [16~17]. Additionally, this crystallization needs higher temperature and takes a long time. Therefore, the metal-induced crystallization (MIC), such as using nickel (Ni) as a mediator, was found to reduce the temperature of solid phase crystallization and to improve the quality of active islands. The rate at which the metal-induced crystallization takes place can be markedly enhanced in the presence of an electric field [18~20]. The LTPS-TFTs fabricated by MIC have some inevitable disadvantages, resulting in degrading the performance, such as many $NiSi_2$ precipitates remaining in the crystallized Si matrix and some uncrystallized α-Si regions remaining between needlelike crystalline phases [21]. Consequently, metal-induced crystallization followed by laser annealing (L-MIC) was further proposed to improve the performance of the LTPS-TFTs [22~23].

Among all methods of α-Si crystallization, laser crystallization of α-Si films has been considered as the most promising technology in the fabrication of LTPS-TFTs based active matrix displays. Since laser-crystallized poly-Si films have a low concentration of in-grain defects, such as stacking faults and twins, by complete melting of α-Si, the field-effect mobility of laser-crystallized poly-Si TFTs can be significantly promoted. However, the number of grain boundaries and their corresponding locations, which are not controlled in the channel region following the laser irradiation, strongly affect the electrical characteristics and the hot-carrier reliability [24]. Many methods of artificially controlled super lateral growth (ACSLG) using excimer laser annealing (ELA) are reported to enlarge grains in the channel region [25~28]. Additionally, continuous-wave laser crystallization using a frequency-doubled (2ω) diode-pumped solid-state (DSPP) $Nd:YVO_4$ (λ =532nm) is successful for forming high-performance LTPS-TFTs [29~32]. So far, only laser-crystallized poly-Si TFTs has the potential to achieve a system on a panel.

Although the performance of LTPS-TFTs fabricated by laser annealing can approximate to that of single crystalline Silicon-on-Insulator Metal-Oxide-Semiconductor Field-Effect Transistor (SOI-MOSFET) [33], the mobility enhancement limit and the poor device uniformity are pronounced in laser-crystallized poly-Si TFTs. This is because of the inability to control grain boundaries and their location in the channel region, leading to carrier scattering via grain boundaries and lattice vibration (phonon) [32, 34]. Therefore, defect reduction technologies, such as treating the laser-crystallized poly-Si films and the gate oxide/channel interface by the high-pressure H_2O vapor and plasma, and laser-induced passivation [35~42], are developed to fabricate the high-performance LTPS-TFTs. Among them, the poly-Si TFTs fabricated by defect reduction methods with a high carrier mobility of 830 cm^2/Vs were proposed by Watakabe [36]. Therefore, the passivation of grain boundaries is an important step in the fabrication of LTPS-TFTs.

Whether a-Si films are crystallized by solid phase crystallization (SPC) or by laser crystallization (LC), it is impossible to avoid existences of grain boundaries in the channel regions for big dimension devices. However, grain boundaries under the high drain electric field cause an increase in the leakage current, a variation in the threshold voltage with the drain bias, a kink effect in the output characteristics, and a poor hot-carrier stress endurance [24]. These effects can be eliminated by reducing the electric field in the drain junction. Therefore, many novel structures are created to reduce the electric field. For example, the field-induced drain [43-46], sub-gate coupling structure [47-50], dual-gate structure [51], double-gate structure [52-54], lightly-doped drain [55-61], and T-shaped gate structure [62-65] have been under investigation. Among them, structures of field-induced drain and double gates usually need complicated processes, causing a barrier for being fabricated on a large area glass substrate. And T-shaped gate structure which usually needs no additional mask in the fabrication of MOSFETs doesn't be applied to poly-Si TFTs so far. How to simplify the fabrication of high-performance poly-Si TFTs is the most important thing in LTPS TFT-based active matrix displays [66].

1.2. MOTIVATION

As far as the manufacturing cost of the TFTs-based displays is concerned, the mask counts in TFT array processes must be reduced and the high performance of TFTs must be remained. Four masks used to fabricate top-gated poly-Si TFTs are essential. How to promoted TFT performance and to remain the mask counts are the most important thing. However, no four-mask process associated with a temperature gradient for laser crystallization is proposed to produce lateral-grained poly-Si TFTs. In this thesis, we develop an a-Si spacer capping method not only to meet the requirements of laser-crystallized large-grained poly-Si TFTs, but also to keep the essential mask counts for fabricating poly-Si TFTs. The artificial grain-growth technique widens the laser process window so that the yield of large area displays may be promoted by this technique.

Amorphous silicon films are crystallized into polycrystalline films through random nucleation so that the orientation of laser-crystallized poly-Si grains is varied. There has been no method proposed to uniform the orientation of laser-crystallized silicon films, so the difference of device performance between TFTs cannot be eliminated even if the channel of a TFT is produced on a single grain. In this thesis, we create a new crystallization method, a seeding technique using single-orientation silicon patterns as a seed to contact a-Si films deposited on a transparent glass substrate and then to produce the orientation silicon thin film after laser irradiation. Among patents and papers we have searched, this idea initially appears in this thesis. The seeding technique only needs an additional process to make the seed of single-orientation silicon patterns. The silicon substrates can be used repeatedly so that the manufacturing cost can be remained. This technique is expected to produce large area silicon films with a fixed orientation.

The performance of a laser-crystallized poly-Si TFT whose channel is within one grain is similar to that of SOI MOSFETs. The grain size is usually limited so that the channel length and width must be simultaneously scaled down. It is important to know how a short channel laser-crystallized poly-Si TFTS behaves. In order to obtain a high-resolution LTPS-TFTs based active matrix displays, high-performance and good-reliability laser-crystallized poly-Si TFTs are fabricated and characterized in this thesis. We create a novel thickness modulation method to build a thermal gradient across the channel length. When a channel length of the TFT is below 2μm, the device performance is enhanced due to less grain boundaries within its channel region.

On the other hand, the effects of grain-boundary location on the performance of poly-Si TFTs are investigated using two-dimensional (2-D) device simulations by M. Kimura et al [67]. However, it is difficult to involve real conditions of grain-boundary location in the channel region by device simulations. For example, local electric field caused by carrier trapped in the grain boundaries is difficult to be estimated and then to characterize the behavior of laser-annealed poly-Si TFTs. How randomly distributed grain boundaries affect the performance and reliability of laser-crystallized poly-Si TFTs must be recognized. However, many studies have no enough evidences to support the results of device variations after the laser-crystallized poly-Si TFTs are measured and stressed. Hence, we characterize the effects of grain boundaries on laser-crystallized poly-Si TFTs in this thesis.

1.3. THESIS ORGANIZATION

In this thesis, we fabricate and characterize excimer-laser crystallized poly-Si TFTs whose grain boundaries are controlled using novel excimer-laser crystallization techniques. These TFTs have grain boundaries parallel and perpendicular to the direction of current flow. The organization of chapters in this thesis is presented as follows.

In chapter 2, a novel laser crystallization method is introduced to fabricate high performance poly-Si TFTs without any additional mask. Anisotropic plasma etching makes edges of a-Si active islands thicken. The edge-thickened island provides a thermal gradient across the channel width to enlarge silicon grains when the molten silicon commences solidifying. The formation and removal of a-Si spacer play a critical role for the fabrication of excimer-laser crystallized poly-Si TFTs. We think that the edge-thickened technique can provide a wide process range of laser irradiation so that the uniformity and yield of TFTs are enhanced.

In chapter 3, we propose a seeding technique to fabricate single-crystal silicon TFTs on glass substrates. In order to reduce the variations of poly-Si TFT performance, the orientation of silicon grains must be uniformed by seeding techniques. Although the seeding technique was used to fabricate SOI-MOSFETs on silicon substrate, it is not employed to fabricate poly-Si TFTs on glass substrate. How to use the seeding technique to fabricate TFTs on glass substrate is the main point in this chapter.

In chapter 4, a LOCOS-like process is performed to fabricate large-grained poly-Si TFTs. Grains are laterally enlarged because of a temperature gradient built by silicon thin film thickness modulation, so the short-channel TFTs have high field-effect mobility due to less grain boundaries in the channel region. Some destructive phenomena, such as avalanche multiplication, and self-heating effect, are observed in those short channel devices. Especially, the electrical characteristics of boron doped TFTs are unstable under measurements of several times. It can be concluded that boron activation during 600℃ will introduce many hole traps into the gate oxide.

In chapter 5, we further investigate the effects of grain boundaries in the drain junction on the performance and hot-carrier reliability of excimer laser-crystallized poly-Si TFTs. A self-aligned TFT with asymmetric grain boundaries distributed in the source-drain direction is fabricated. How grain boundaries in the drain junction affects the performance and hot-carrier reliability of a single TFT is understood because interdevice variations are eliminated by comparing the forward and reverse modes of the single device. The investigation of NH_3 plasma treatment on these TFTs with grain boundaries randomly distributed is also included in this chapter.

In chapter 6, we finally make conclusions and list some intriguing topics for future works.

Chapter 2

High-performance Poly-Si Thin Film Transistors Fabricated Using Excimer Laser Crystallization of Edge-thickened a-Si Islands

2.1 INTRODUCTION

Laser-annealed polycrystalline silicon thin film transistors (poly-Si TFTs) have become the most promising candidates for use in active matrix displays because they potentially enable peripheral drive circuits to be integrated into a panel [1]. The fabrication of high-mobility poly-Si TFTs by a lateral temperature modulation usually involves complex processes, such as the use of additional masks to enlarge channel grains [2], [3], and the application of homogenizing and shaping laser beam profiles to make device performance uniform [4], [5]. Simplifying the processes involving in fabricating high-performance poly-Si TFTs is very important in replacing amorphous silicon (α-Si) TFT-based active matrix displays [6]. Notably, the performance of conventional 4-mask-processed poly-Si TFTs can be improved by excimer laser crystallization (ELC) of pre-patterned α-Si films [7], but surface tension shrinks the active islands [8], reducing the uniformity of device performances. Hence, conventional poly-Si TFTs are fabricated by patterning pre-crystallized poly-Si films as active islands. However, un-patterned α-Si films cannot be directly irradiated using a continuous wave (CW) laser because the CW laser irradiation strips the films and thermally damages the glass substrates. An additional mask is used to pattern the α-Si films before the CW laser crystallization is performed [9].

In this chapter, the KrF excimer laser is used to crystallize α-Si islands whose edges are thickened by α-Si spacers formed by anisotropic plasma etching. There are downward and upward edge-thickened α-Si islands whose crystallization mechanisms are investigated. The downward edge-thickened α-Si islands without capping the top low-temperature oxide are shrunk by excimer laser crystallization due to the surface tension of the molten silicon. However, the shrinkage effect can be suppressed in the upward edge-thickened α-Si islands with capping the top low-temperature oxide. Subsequently, the thickened edges are completely removed by anisotropic plasma etching with the top oxide as a protective layer, needing no additional mask. This method improves the device performance due to the enlargement of channel grains by an establishment of a temperature gradient across the channel width. The authors believe that this method can be applied to fabricate a high-performance poly-Si TFT with a neck to grow a single crystal of Si by appropriately modulating CW laser scanning in the source-drain direction[10], [11], since the upward edge-thickened α-Si active islands are very robust against laser-induced distortion.

2.2 DEVICE FABRICATION

A. ELC of downward edge-thickened α-Si islands without capping the top oxide.

First, a 100 nm thick α-Si layer was deposited on thermally oxidized (1.5μm thick) Si wafers by decomposing SiH_4 in a low pressure chemical vapor deposition (LPCVD) system at 550℃. Next, a 100 nm thick low-temperature tetraethylorthosilicate (TEOS) oxide layer was deposited by plasma-enhanced CVD (PECVD) at 350℃. A mask of active regions was used to define the active islands. Meanwhile, exchanged dry etching recipes were employed to completely etch the stacked TEOS oxide/α-Si layers and slightly etch the buffer oxide layer. The TEOS and buffer oxide were then laterally etched using Buffered Oxide Etch (BOE) solution as plotted in Fig. 2-1 (a). After removing the top photoresist (PR), the 100 nm thick TEOS layer was thinned with a diluted HF solution. Subsequently, a 50 nm thick α-Si layer was deposited by decomposing SiH_4 in a LPCVD system at 550℃. Notably, the silicon films always keep the amorphous phase during the 550℃ deposition. Anisotropic plasma etching was then used to form the edge-thickened α-Si spacers with the residual TEOS oxide (about 15 nm thick) as a stop layer, as shown in Fig. 2-1 (b). Afterward, the α-Si active islands were crystallized using KrF excimer laser irradiation following the removal of the residual TEOS oxide by a dilute HF solution, as shown in Fig. 2-1 (c). The remaining steps were performed to finish the top self-aligned poly-gated poly-Si TFTs, including a 100 nm thick TEOS oxide layer as the gate insulator deposited by PECVD at 350℃, a 250 nm thick α-Si layer as the gate electrode deposited by LPCVD at 550℃, a self-aligned ion implantation of phosphorous with a dosage of 5×10^{15} cm^{-2} at 35 keV, activation at 600℃ for 16 h in a furnace with a nitrogen ambient, a 300 nm thick TEOS passivation oxide layer deposited by PECVD at 350℃, and sintering at 400℃ for 30 min. No further hydrogenation step was carried out.

B. ELC of upward edge-thickened α-Si islands with capping the top oxide.

First, a 93 nm thick α-Si layer was deposited on thermally oxidized (1.5 μm thick) Si wafers by decomposing SiH_4 in a LPCVD system at 550℃. Next, a 160 nm thick low-temperature TEOS oxide layer was deposited by PECVD at 350℃. A mask of active channel was used to pattern the TEOS oxide layer. The under α-Si layer was directly etched by plasma following a slight lateral wet etching of the TEOS oxide, as shown in Fig. 2-2 (a). After removing the top photo-resists (P.R), a 93 nm thick α-Si layer was deposited by LPCVD at 550℃. Subsequently, edge-thickened α-Si islands were formed by anisotropic plasma etching with oxide as a stop layer, and then were crystallized by the 50-pulse KrF excimer laser with energy density of around 335mJ/cm^2 at a substrate temperature of 400℃. Plasma etching was then used, first to reduce the thickness of the TEOS oxide using a low silicon-to-oxide selectivity, and last to remove completely the thickened edges of α-Si islands using a high silicon-to-oxide selectivity, as illustrated in Fig. 2-2 (b). The proposed active islands were uniquely formed after the residual TEOS oxide was removed using a dilute HF solution. In addition, the blanket excimer laser-crystallized poly-Si films were patterned as the active islands of conventional poly-Si TFTs. Notably, the only difference of the proposed and conventional poly-Si TFTs is the formation of crystallized islands. Finally, the same steps were simultaneously implemented to finish the proposed and conventional poly-Si TFTs, such as a 110 nm thick TEOS oxide layer as the gate insulator deposited by PECVD at 350℃, a 170 nm thick α-Si layer as the gate electrode deposited by LPCVD at 550℃, a self-aligned ion implantation of phosphorous with a dosage of 5×10^{15} cm^{-2} at 35 keV, activation at 600℃ for 16 h in a furnace with a nitrogen ambient, a 300 nm thick TEOS passivation oxide layer deposited by PECVD at 350℃, and sintering at 400℃ for 30 min. No further hydrogenation step was carried out.

C. Optimized edge-thickened process

The procedures of ELC of upward edge-thickened α-Si islands with capping the top oxide have to be further optimized as illustrated in Fig. 2-3. Fig. 2-3 (a) shows that the top oxide must be completely etched and then the under a-Si layer must be partially etched using anisotropic plasma etching. The wet lateral etching is no longer introduced into this process because of the inability to the width of the channel. Anisotropic plasma etching is then performed to form a-Si spacer without changing the initial layout of the active islands as shown in Fig. 2-3 (b). After CW or excimer laser crystallization of the a-Si island is carried out, the top oxide and the thickened edge are completely removed by anisotropic plasma etching. The process flows without introducing any additional mask to enlarge channel grains are the most promising procedures for manufacturing flatted-panel displays. Although we cannot provide an optimized condition about the thickness of low-temperature oxide and a-Si spacer, a wide process range between film thickness and laser energy is guaranteed.

2.3 RESULTS AND DISCUSSION

A. Effects on ELC of the downward edge-thickened α-Si islands without capping the top oxide

The channel and edge regions have the same level height of silicon molten during multi-pulse excimer laser irradiation on the downward edge-thickened α-Si islands without capping the top oxide so that the surface tension shrinks these islands. Fig. 2-4 (a) shows the SEM image of one side of a large area ELC poly-Si island. A temperature gradient established by different heat conduction rates near the edge of the island facilitates the grain growth. It can be seen that the island is shrunk from the edge and the grains beside the edge are longitudinally enlarged. Prior to the solidification of the molten silicon, the shrunk edge firstly solidifies, acting as seeds to trigger the longitudinal grain growth. These lateral grains stop growing until they meet the fronts of other homogeneously nucleated grains from the opposite direction. Therefore, there are smaller grains located away from the edge.

As the channel width decreases, the longitudinal grains will occupy the whole channel, resulting in effectively enhancing the device performance. Fig. 2-4 (b) shows the SEM image of the grain distribution of an ELC poly-Si island of about 5 μm wide. One can see that the longitudinal grains growing from both sides of the width meet at the center. Grain boundaries of excimer-laser crystallized poly-Si films always coexist with the protrusions, roughening the surface of laser-annealed poly-Si films. The grain boundaries are located in the positions where the protrusions appear. The protrusions are formed due to significant mass transport toward the grain boundaries, and the mass transport is caused by surface tension of the molten silicon. This statement can be evidenced by our AFM image.

However, if the width of the edge-thickened island is further narrow (about <

1μm), the shrinkage of this island from the edges and the clear grain boundary at the center will not be found, as shown in Fig. 2-5. The island is narrow enough so that the surface-tension-induced mass transport in the perpendicular to source-drain direction is confined. The shrinkage of the island from the edges disappears, but the mass transport in the parallel to source-drain direction still occurs. Hence, the shrinkage of this island happens near the necked region, as shown in Fig. 2-5 (a). It can be also seen from Fig. 2-5 (b) that two grains growing from both sides of the width either meet at the center or are merged into one grain. The merged grain results from effectively eliminating mass transport of the molten silicon. The mass transport of the molten silicon causes the formation of protrusions. Silicon lattice mismatch happened in the protrusions leads to the formation of grain boundaries. If the protrusions are not formed at the center and the cooling rate of molten silicon is kept low, perhaps two grains will meet at the center and then will be merged into one grain. Fig. 2-6 (a) shows that most of the grains meet at the center but there are two grains merged into one grain after meeting at the center. The tension force is larger than the adhesion force, resulting in the shrinkage of islands as shown in Fig. 2-6 (b). The merged grain comes from a cancellation of tension induced mass transport in the Y-direction. Therefore, adopting this process to fabricate unshrunk large-grained poly-Si islands must be realized under crystallizing narrow a-Si islands and the island layout must be not the dog-bone shape.

Fig. 2-7 shows the transfer characteristics of the edge-thickened poly-Si TFT whose 150 nm laser-crystallized poly-Si spacer is unable to be removed. The curves of ON currents at V_{DS}=0.1V and V_{DS}=5V are normally separated, but the curves of OFF currents at the same drain bias abnormally approach to overlapping together. This result suggests that the kept poly-Si spacer with poor crystalline silicon dominates the OFF currents. The leakage primarily results from carrier generation via thermionic-field emission at the grain-boundary defects, and the both edges with 150 nm thick silicon spacer provide the leakage current path.

B. Effects on ELC of the upward edge-thickened α-Si islands with capping the top oxide

Fig. 2-8 shows the SEM micrographs of excimer laser-crystallized poly-Si grains obtained after Secco etching of the proposed poly-Si island. The channel region was completely melted and the edge-thickened region was partially melted during 50-pulse excimer laser irradiation. The both regions have two different heights of the molten silicon, building a temperature gradient perpendicular to the source-drain direction and then facilitating the grain growth by the un-melted α-Si of the edge-thickened region as seeds. The top TEOS oxide not only releases the surface tension of the molten silicon [12], effectively suppressing the shrinkage of the island, but also acts as a heat source to reduce the quenching rate of the molten silicon [13]. Therefore, in addition to meeting each other at the center, some of the grains laterally elongated from the un-melted edge are merged while the channel width is narrow, clearly shown in Fig. 2-8 (b). On the other hand, residual a-Si uncrystallized by excimer laser maybe remains on the channel edges, introducing a barrier to turn on the current path of the channel edges when the device is being biased. The uncrystallized edges are narrow enough so that they benefit the device because of reducing edge-field effect. The inset in Fig. 2-8 (a) shows a general layout between channel and gate for TFT fabrication. Fig. 2-9 shows the laser-crystallized poly-Si film with randomly distributed grain boundaries. Differences among sizes of grains in the conventional laser-crystallized poly-Si film cannot be prevented because of the applied laser with a Gaussian beam profile and a deviation of energy density of pulse-to-pulse. Therefore, the channels in the proposed poly-Si TFTs exhibit a more regular arrangement of grains as compared with the channels in the conventional poly-Si TFTs. After defining pre-crystallized poly-Si films as active islands, the conventional poly-Si TFTs have grain boundaries randomly distributed within the channel regions, resulting in a poor uniformity of device performance.

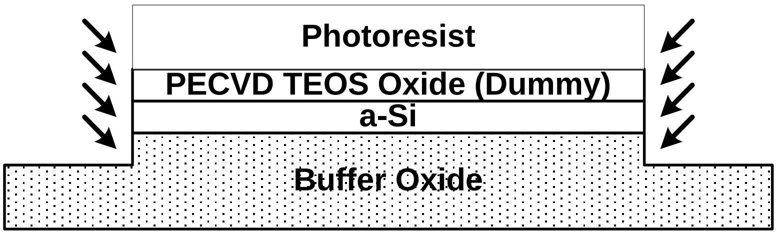
Fig. 2-10 (a) shows the transfer characteristics of the proposed and conventional poly-Si TFTs with a channel length of 2μm and a channel width of about 1μm. Notably, the ON/OFF current ratios at V_{DS}=5V are 2.31×10^8 for the proposed poly-Si TFT and 2.15×10^7 for the conventional TFT. This difference of one order of magnitude is mainly ascribed to the difference in leakage current. Besides, the shift of threshold voltage ΔV_{th} is defined as $V_{th,1} - V_{th,2}$ where $V_{th,1}$ denotes the V_{GS} of drain current of (W/L)×10^{-8}A at V_{DS}=0.1V and $V_{th,2}$ represents the V_{GS} of drain current of (W/L)×10^{-7}A at V_{DS}=5V. The ΔV_{th} of 0.23V in the proposed poly-Si TFT is smaller than that of 0.80V in the conventional poly-Si TFT. Those results imply that the grain boundaries perpendicular to the direction of current flow suppress the leakage current [14] and the drain-induced barrier lowing (DIBL) in the proposed poly-Si TFTs. However, preventing grain boundaries from lying across from the source to drain is difficult in the conventional poly-Si TFTs, and such grain boundaries provide extra paths for current and cause punchthrough effects as the channel length is shortened. Therefore, the proposed poly-Si TFTs simultaneously benefit more from device scaling than the conventional poly-Si TFTs. On the other hand, an ON/OFF current ratio of eight orders of magnitude at V_{DS}=5V is also obtained from the proposed poly-Si TFT with L=2μm and W=1.2μm×100 as shown in Fig. 2-10 (b). The self-heating reliability of a TFT with divided channel units can be further improved due to the rapid heat diffusion when the TFT is operated in a high drain current [15], [16].

Fig. 2-11 shows the dependence of field-effect mobility on the channel length for the proposed and conventional poly-Si TFTs. Twenty TFTs with channel widths from 1μm to 4μm for each channel length are included. The maximum mobility of the proposed poly-Si TFTs decreases as the channel length increases, indicating that grain boundaries perpendicular to the direction of current flow act as strong scattering centers that limit the transport of carriers. However, some conventional TFTs with mobility more than the proposed TFTs are obtained due to the instability of the applied laser, resulting in a large variation of field-effect mobility in the conventional poly-Si TFTs. This result suggests that the proposed method can partially compensate for the non-uniform beam profile and the unstable pulse-to-pulse energy density of the applied laser.

2.4 CONCLUSION

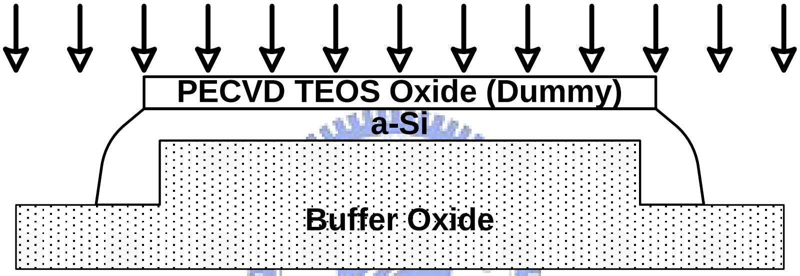
The surface tension-induced shrinkage effect of multi-pulse excimer laser irradiation on pre-patterned α-Si islands was successfully eliminated through the edge-thickened method. The proposed method can make uniform the performance of poly-Si TFTs due to the regular arrangement of the channel grains by the lateral modulation of temperature. The proposed TFTs with divided channel units can meet the application of various gate widths, and their performances depend on the grain-boundary control of each channel unit. Hence, how to further control the quality of a channel unit is still the major concern of the proposed TFTs.

Slightly Etching Side Wall Oxide



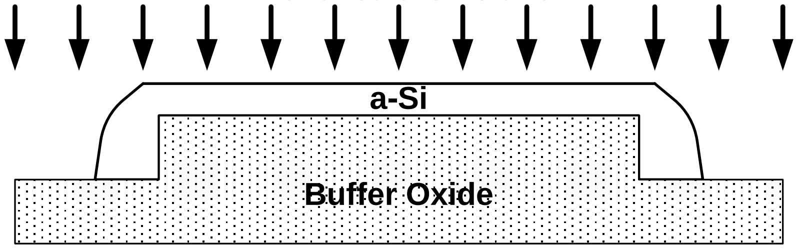
(a)

After Dry Etching of the Top a-Si Layer with Dummy Oxide as a Stop Layer



(b)

Excimer Laser Crystallization of the Edge-thickened a-Si Island



(c)

Fig. 2-1 Key process flow for crystallization of downward edge-thickened a-Si island without capping the top TEOS oxide by excimer laser irradiation.

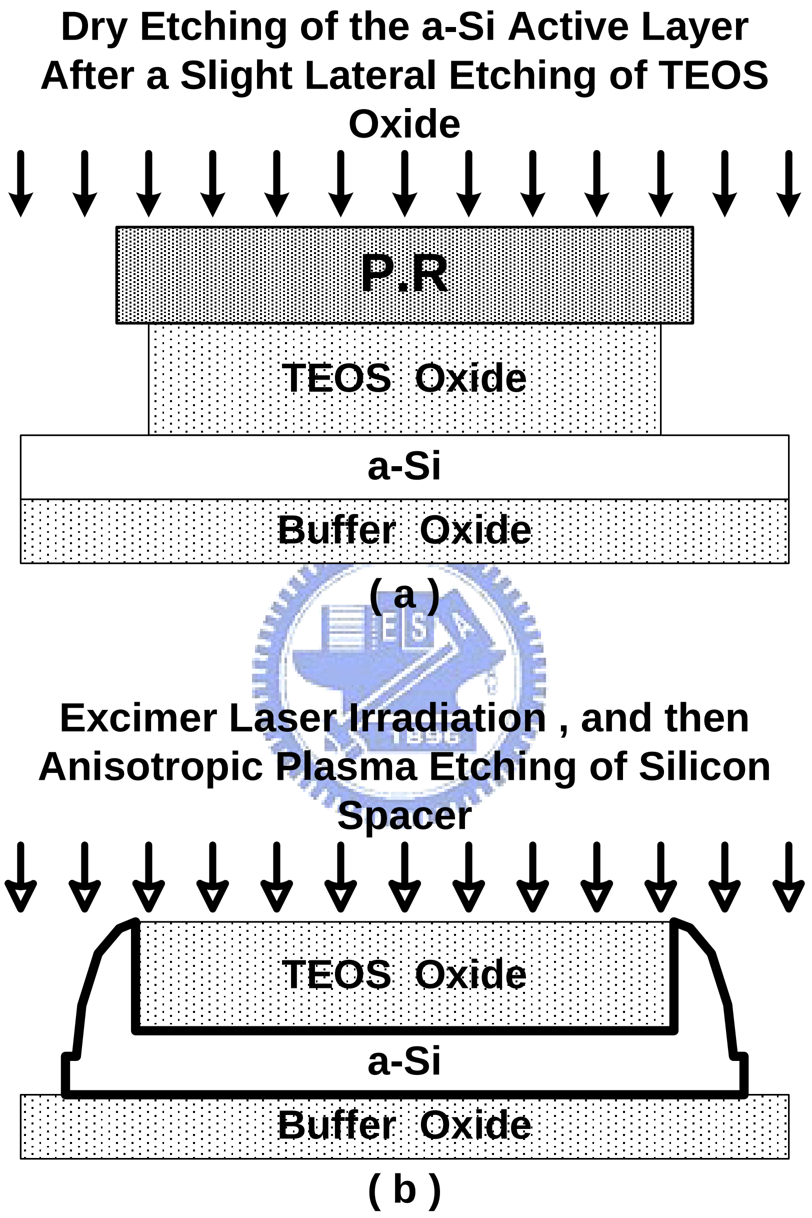


Fig. 2-2 Key process flow for crystallization of upward edge-thickened a-Si island with capping the top TEOS oxide by excimer laser irradiation.

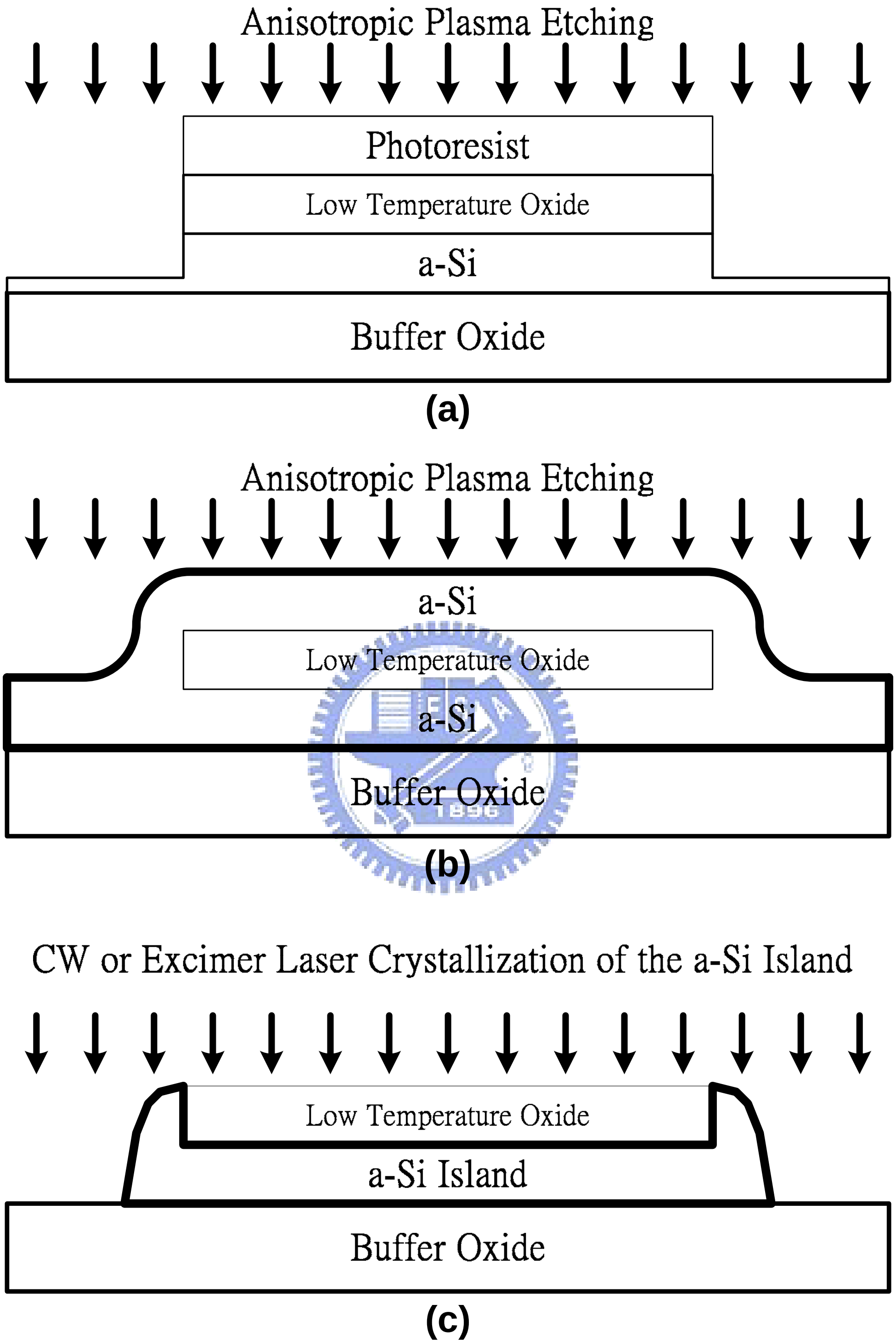
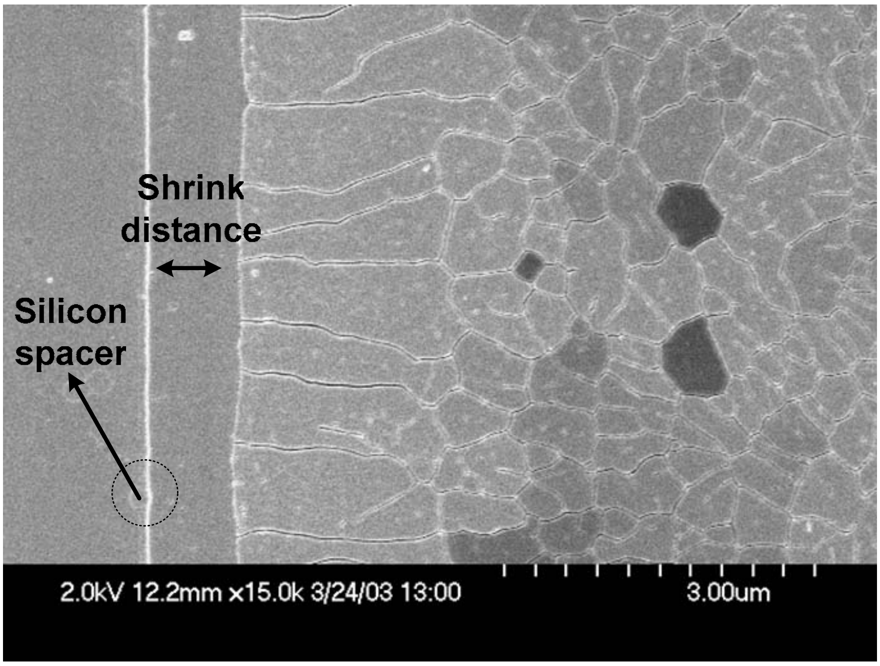
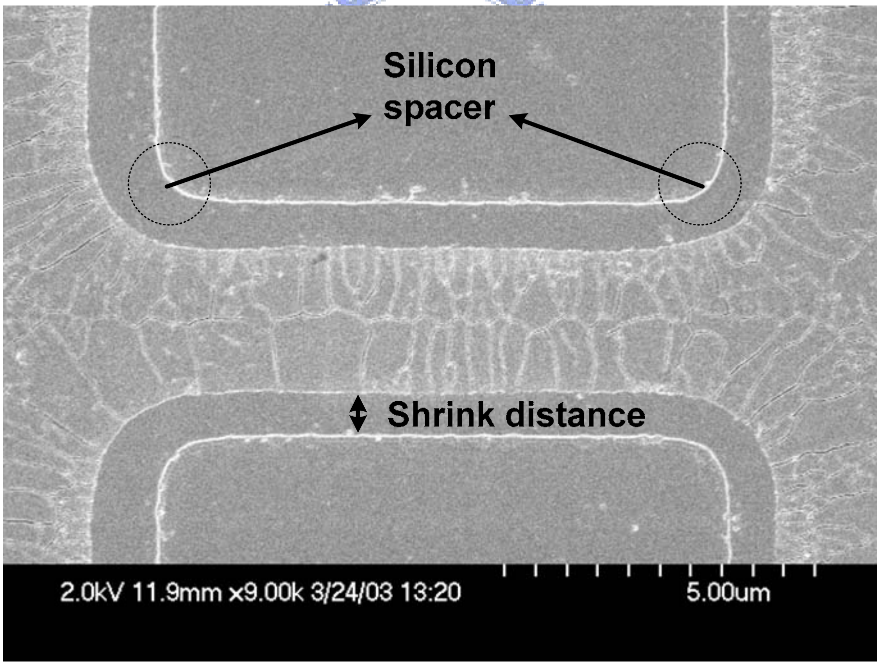


Fig. 2-3 Optimized process flow for crystallization of upward edge-thickened a-Si island with capping the top oxide by excimer laser irradiation.



(a)



(b)

Fig. 2-4 SEM images of downward edge-thickened poly-Si islands without capping the top oxide crystallized by excimer laser irradiation.

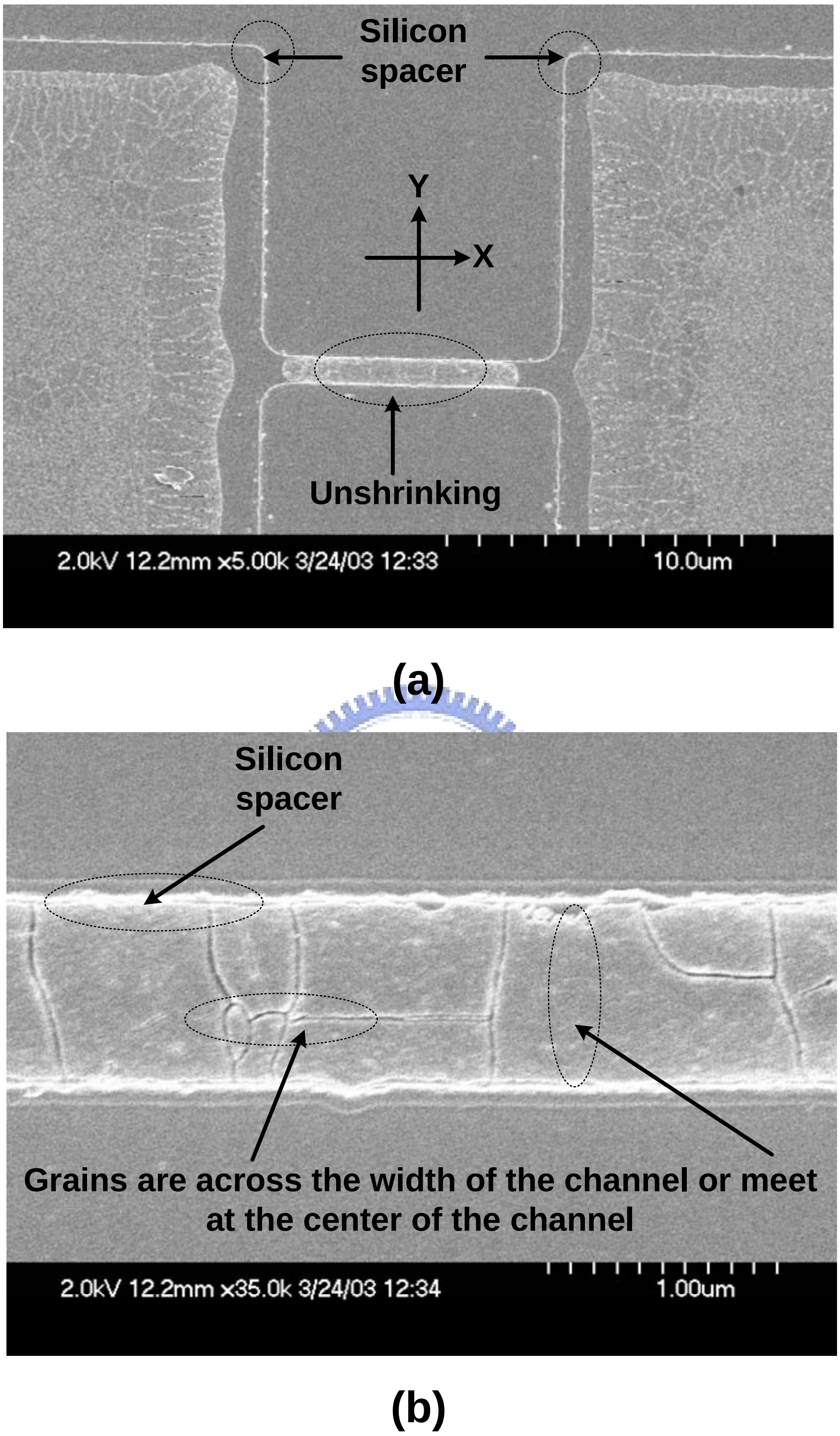


Fig. 2-5 SEM images of downward edge-thickened poly-Si island with narrow width. The channel is shrunk in the X-direction but in the Y-direction.

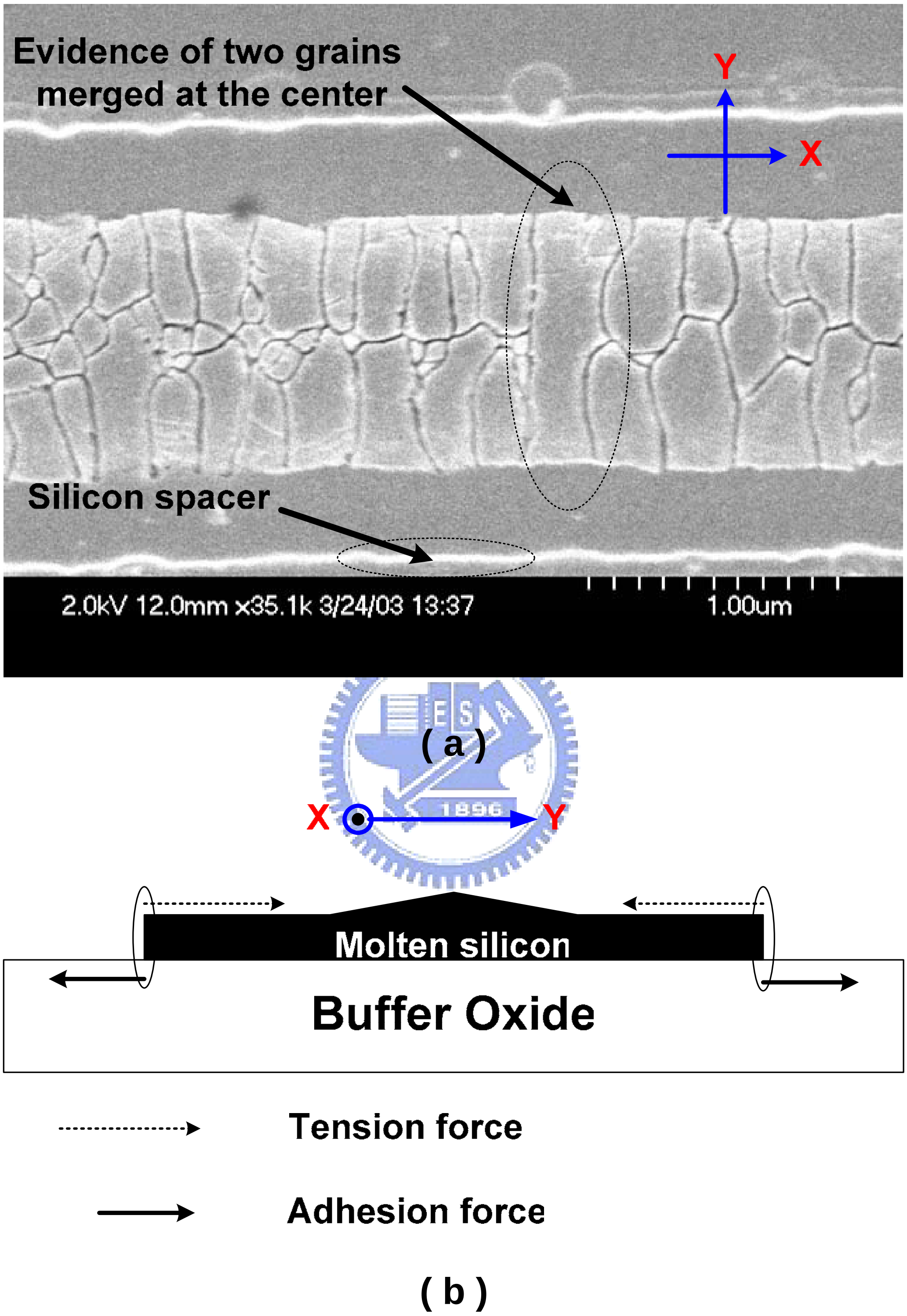


Fig. 2-6 (a) SEM image showing an evidence of two grains merged at the center of the channel, (b) explanation for shrinkage of a molten silicon island.

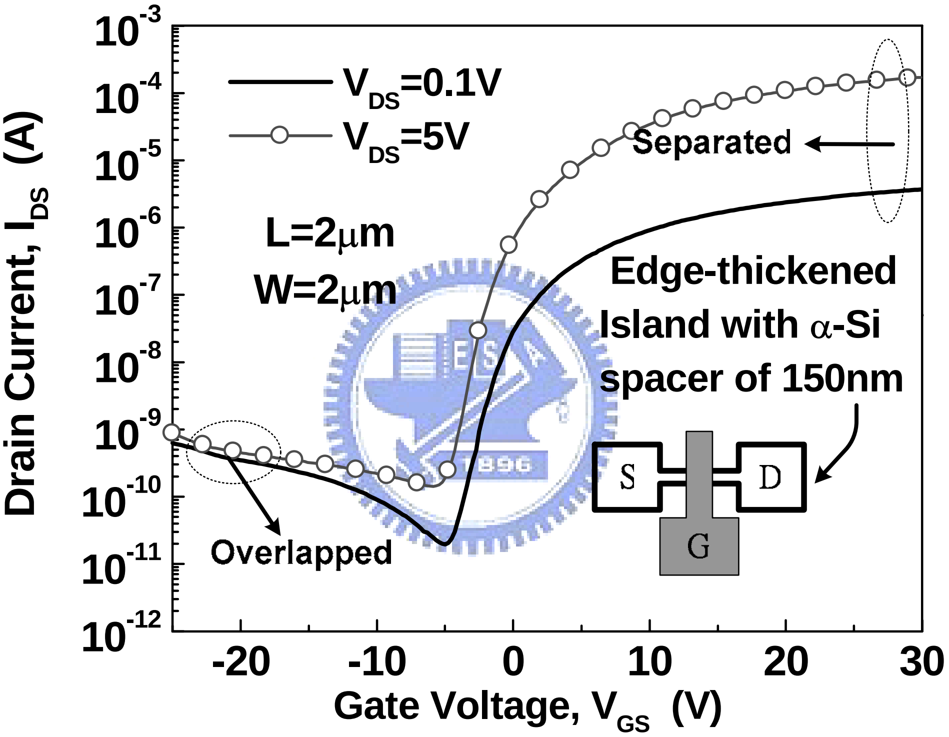
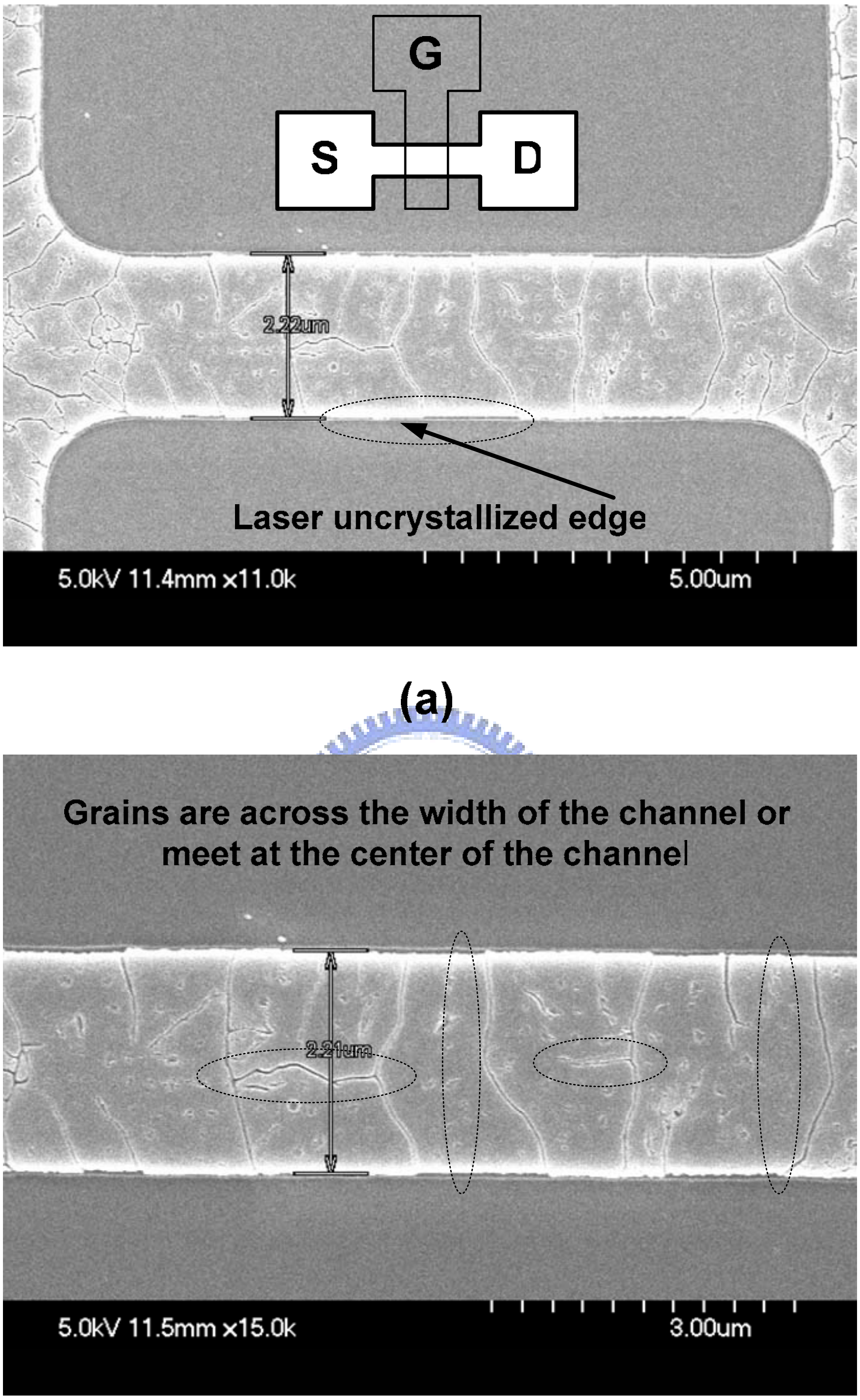


Fig. 2-7 Transfer characteristics of a downward edge-thickened poly-Si TFT without an optimized edge process in relation to excimer-laser crystallization.



(a)

(b)

Fig. 2-8 SEM images of (a) crystallization of upward edge-thickened poly-Si island with capping the top oxide by excimer laser irradiation and of (b) the grain boundaries within the channel.

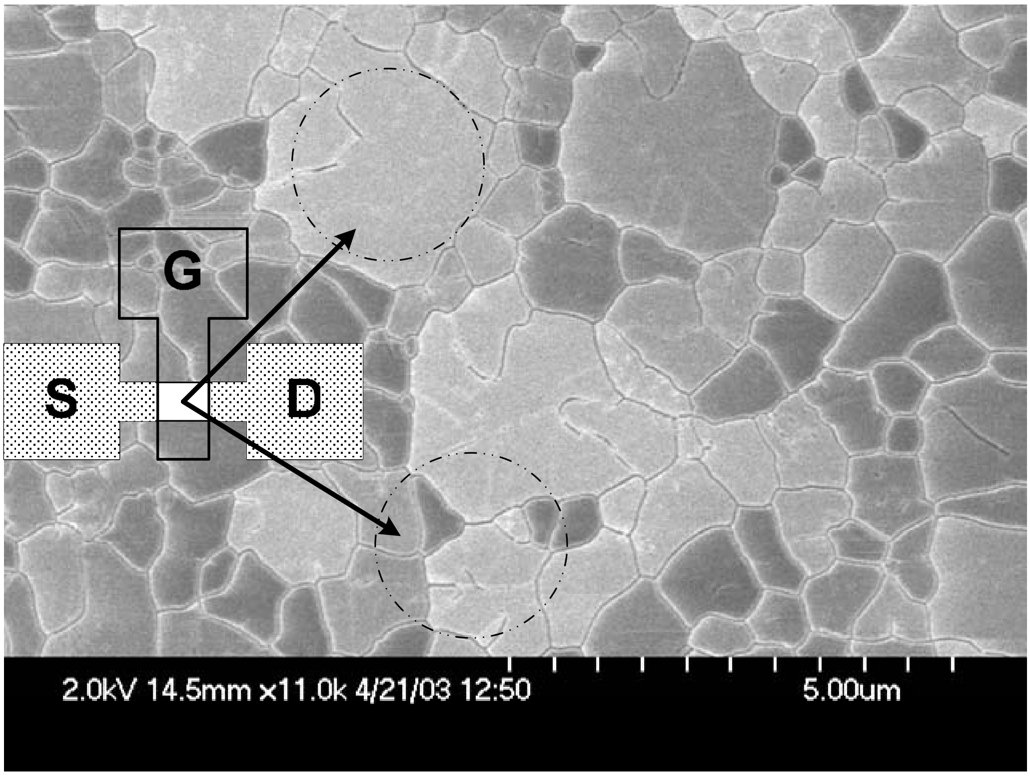


Fig. 2-9 SEM image of laser-crystallized poly-Si film showing randomly distributed grain boundaries. The channel of a conventional TFT maybe locates in the regions of the above circle or the below circle.

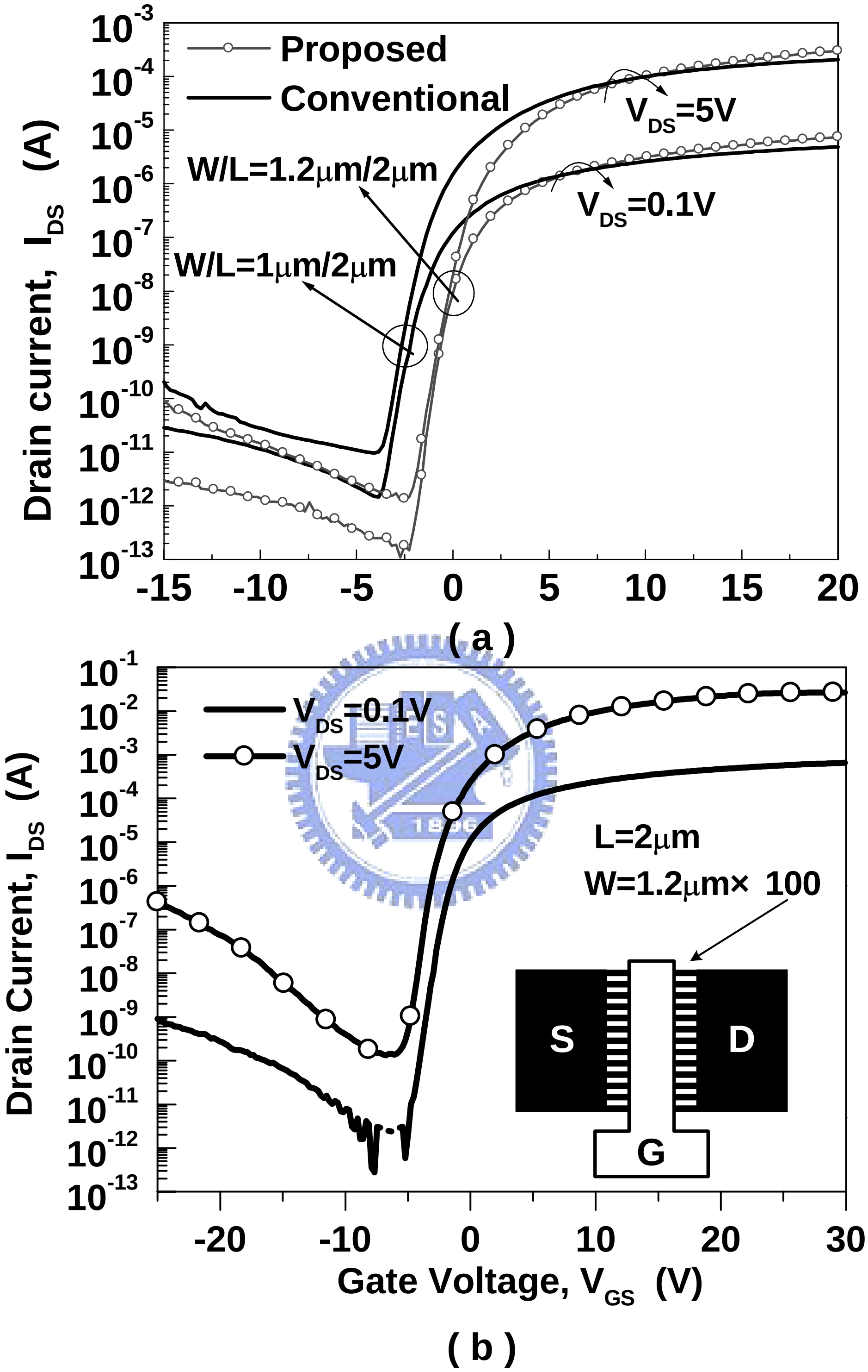


Fig. 2-10 Transfer characteristics of (a) the proposed and conventional poly-Si TFTs with channel widths of about 1μm, and (b) the proposed poly-Si TFT with 100 channel units.

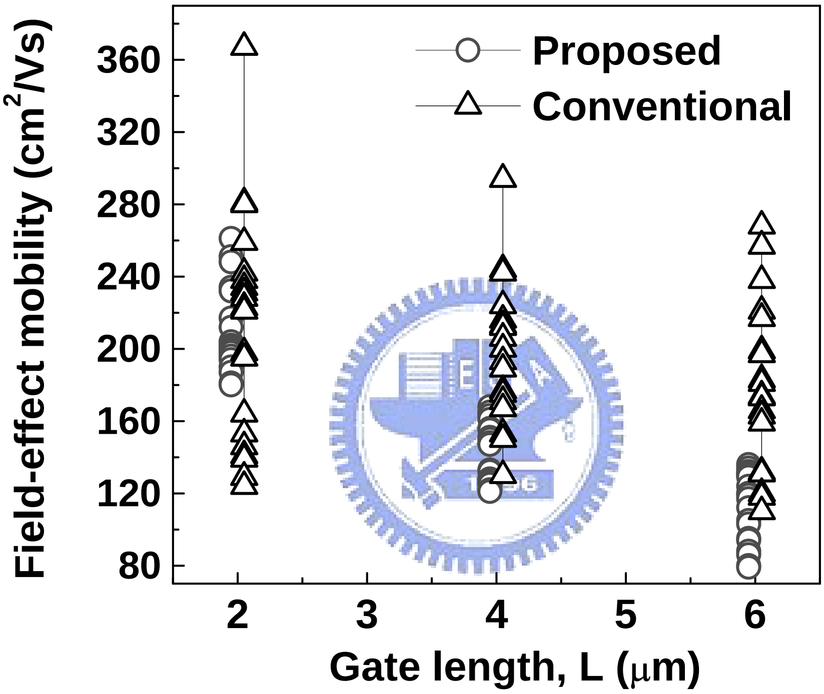


Fig. 2-11 Dependence of field-effect mobility on the channel length given channel widths from 1μm to 4μm for the proposed and conventional poly-Si TFTs. The field-effect mobility was evaluated at V_{DS}=0.1V.

Chapter 3

A Novel Laser-Induced Lateral Seeding (LILS) Technique for Fabrication of Single-Crystal Silicon Thin Film Transistors

3.1 INTRODUCTION

Laser-crystallized polycrystalline silicon thin film transistors (Poly-Si TFTs) have been considered as the most promising candidates to integrate peripheral driver circuits into the TFT-based active matrix displays [1]-[3]. Many techniques have been proposed to promote the performance of laser-crystallized poly-Si TFTs; however, it is difficult to control the uniformity of device performance due to uncontrollable grain boundaries and orientations of grains [4]-[7]. The modulated thickness of α-Si films or phase of laser beams can enlarge channel grains to promote carrier mobility of the device, but it cannot control the surface orientation of grains [8], [9]. The α-Si films are crystallized into poly-Si films with a random crystallographic orientation. Additionally, single-crystal silicon films can be made by the wafer bonding technique [10], [11], but it is difficult to be realized onto large area glass substrates due to the requirement of high temperature processes [12]. Another method for fabricating large-area single-crystal silicon films is by seeding technique. According to previous reports, seeding techniques by an applied laser can produce single-orientation silicon films on a buffer oxide layer of silicon substrate to fabricate single crystal silicon thin film transistors [13]-[17], but the growth of single crystal of Si uniformly on large area glass substrate doesn't be realized so far.

In this chapter, we introduce a novel crystallization method for fabricating single orientation silicon films on glass substrates using a laser-induced lateral seeding (LILS) technique. Silicon wafer patterned into stripes with a high aspect ratio is used to contact the amorphous silicon film of the glass substrate, and then laser irradiates from the back side of the transparent glass substrate to crystallize the a-Si film by the patterned silicon as a crystallization seed. The large area single-crystal silicon film will be produced on the glass substrate, because the a-Si silicon film and the surface of silicon substrate will be melted simultaneously and then solidification will take place using the patterned silicon as a crystallization seed. The TFTs can be then fabricated within the controlled single-crystal region after the contact between the glass substrate and the patterned silicon wafer is separated. This method is similar to the metal imprint technology [18], [19] and the higher quality of silicon films produced by this method is expectable. We first use the conventional LOCOS process to contact a-Si films with the single-crystal silicon surface to investigate the seeding technique of excimer laser crystallization of a-Si films. And then a-Si films on glass substrates contacted with single-crystal tips are crystallized by excimer laser.

3.2 EXPERIMENTS

A. LILS technique using silicon substrate

A LOCOS process was performed to open seeding areas isolated by thermal oxide. First, a 150 nm thick silicon nitride (Si_3N_4) layer was deposited on thermally oxidized (10 nm thick) Si wafers by a chemical reaction of SiH_4 and NH_3 in a LPCVD system at 781℃. Next, the Si_3N_4 layer was patterned and then selective wet oxidation (producing 150 nm thick SiO_2) was carried out using Si_3N_4 patterns as hard masks. The Si_3N_4 patterns were selectively etched in a hot phosphoric acid bath at 165℃. After completely removing the 10 nm thick pad oxide, a 50 nm thick polycrystalline silicon film was deposited. Multi-pulse KrF excimer laser directly irradiates the poly-Si film, and the film was re-crystallized with single crystal silicon as seeds as shown in Fig. 3-1 (a). Afterward, active islands were defined on the buffer oxide region. The conventional 4-mask processes were sequentially implemented to finish the fabrication of poly-Si TFTs. Meanwhile, a 110 nm thick TEOS oxide layer as the gate insulator was deposited at 350℃ by PECVD, and a 170 nm thick α-Si layer as the gate electrode was deposited by LPCVD at 550℃. A self-aligned ion implantation of phosphorous with a dosage of 5×10^{15} cm^{-2} at 35 keV, and then activation at 600℃ for 16 h in a furnace with a nitrogen ambient were performed. Finally, a 300 nm thick TEOS passivation oxide layer was deposited by

PECVD at 350℃. Aluminum as the electrodes of source, drain, and gate was sintered at 400℃ for 30 min. No further hydrogenation step was carried out. The relative position of TFTs denoted Type-A and Type-B to the seeding areas was shown in Fig. 3-1 (b).

B. LILS technique using quartz substrate

Quartz substrates were used as starting substrates. First, a-Si films were deposited onto the quartz substrates by decomposing SiH_4 in LPCVD system at 550 ℃. Photoresist was coated onto one side of a quartz substrate, and the a-Si film on the other side of a quartz substrate was completely removed by wet poly-Si etchant. After the photoresist was removed, laser could irradiate through the transparent substrate to crystallize the a-Si film on the other side. Fig. 3-2 shows the cross-sectional diagrams of contact seeding technique by single-crystal silicon as crystallization seed and amorphizing single-crystal silicon as crystallization seed, respectively. The amorphization of single-crystal silicon substrates is achieved by ion implantation, and is to absorb laser energy easily.

The single-crystal seed was made by the spacer formation technology. First, a 150 nm thick Si_3N_4 film was deposited onto {100}-, {110}-, and {111}-oriented silicon substrates by a chemical reaction of SiH_4 and NH_3 in a LPCVD system at 781℃. The Si_3N_4 film was patterned and then the under silicon was directly etched down to a depth of around 1.5 μm. Thermal oxidation was performed to grow a SiO_2 layer protecting silicon against anisotropic plasma etching using Si_3N_4 patterns as hard masks as shown in Fig. 3-3 (a). After removing the Si_3N_4 patterns, anisotropic plasma etching was used to form a silicon spacer as shown in Fig. 3-3 (b). Silicon tips were formed following the removal of the protected SiO_2 layer as shown in Fig. 3-3 (c). We used silicon tips to act as crystallization seeds, including the amorphization of silicon tips as crystallization seeds. Fig. 3-4 shows the optical micrographs of silicon tips formed by spacer technology.

3.3 RESULTS AND DISCUSSION

Fig. 3-5 shows the SEM photographs of laterally seeded silicon films on (a) (100)-, (b) (110)-, and (c) (111)-orientated silicon substrates. The single-crystal silicon is not melted during excimer laser irradiation so that large area seeded silicon film is not found. One can see that there are very small grains and many clear pinholes and voids on the silicon substrates, which is different from the grains on the buffer oxide layer. This result is ascribed to that the adhesion of molten silicon on oxide layer and single-crystal silicon substrate are quite different. The molten silicon well adheres to oxide layer but to un-melted single-crystal silicon substrate. The fully molten silicon film on the un-melted single-crystal silicon substrate condenses into pillar-shaped grains due to poor interface adhesion, resulting in void-rich poly-Si films. Once the under surface of silicon substrate is melted, the seeded crystallization will be triggered and the single crystal film will be obtained.

Fig. 3-6 shows the transfer and output characteristics of a laterally seeded TFT on (110)-orientated silicon substrate. The TFT has threshold voltage of -1.58 V, subthreshold swing of 3.97 V/dec, on-off current ratio of 1.48×10^4, and field-effect mobility of around 10 cm^2/Vs. Owing to small grains in the channel region, the poor subthreshold swing is ascribed to many deep states located at grain boundaries. The deep states associated with the dangling bonds have energies near the middle of the forbidden energy gap. Besides states near mid-gap resulting from broken bonds, strained bonds cause a high density of shallow tail states near the band edges. The small grains introduce more grain boundaries in the channel region, and the more trap states will affect the performance of the device. Additionally, the on-currents seem to be limited because the thickness of source/drain region is 50 nm and the ion implantation is hard to be accurately performed. Therefore, a large source to drain resistance R_{SD} dominates the on-currents. On the other hand, the off-currents are ascribed to a large trap density N_t placed in the drain junction. It can be seen from Fig. 3-6 (b) that the kink effect dominates the output characteristics of the device. The thinner the drain junction is, the higher the electrical field is. And the grain boundaries also contribute high local electrical field near the drain junction [20]. Therefore, the thickened drain junction and lightly doped drain are proposed to release the electrical field.

3.4 CONCLUSION

The laser-induced lateral seeding (LILS) technique for fabrication of single-crystal silicon thin film transistors on glass substrates has been investigating. According to pervious studies on SOI devices of bulk silicon substrates, single-crystal silicon films are undoubted to be formed near the seed region. Hence, the proposed technique in this chapter is the most promising method for fabricating single-crystal silicon thin film transistors on glass substrates.

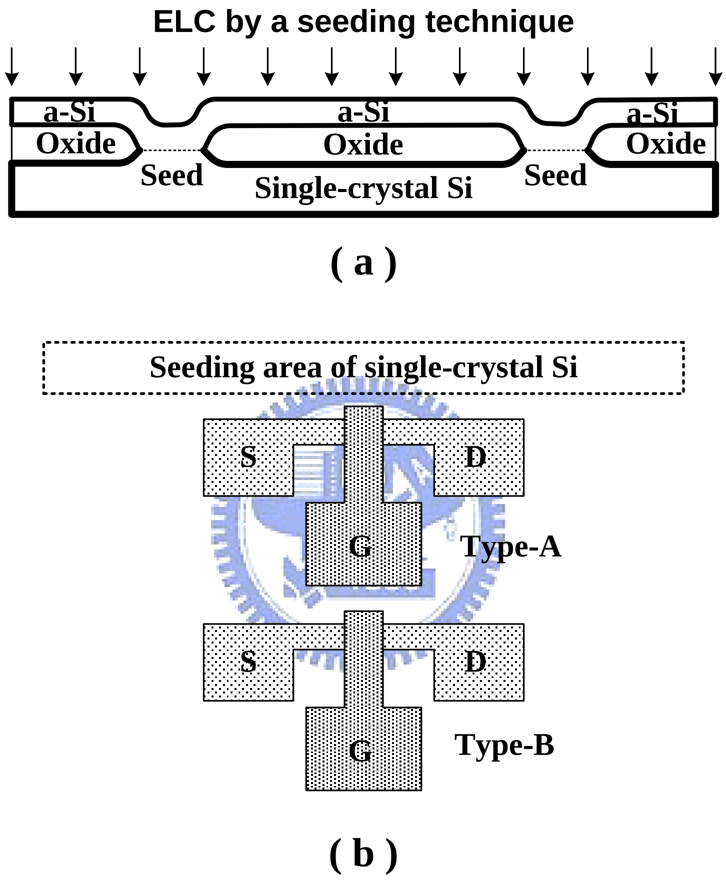


Fig. 3-1 Schematic diagrams of (a) cross-sectional view and (b) top view associated with a laser-induced lateral seeding process.

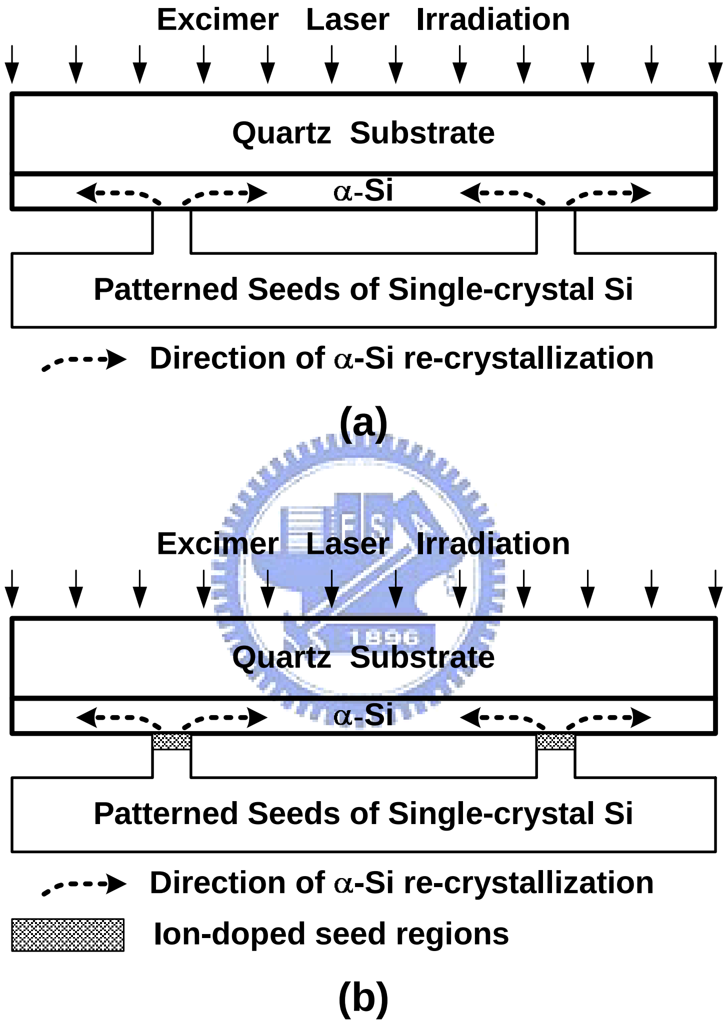


Fig. 3-2 Cross-sectional diagrams showing contact seeding technique by (a) single-crystal silicon as crystallization seed and (b) amorphizing single-crystal silicon as crystallization seed. The amorphization of single-crystal silicon substrates is achieved by ion implantation in order to absorb more laser energy.

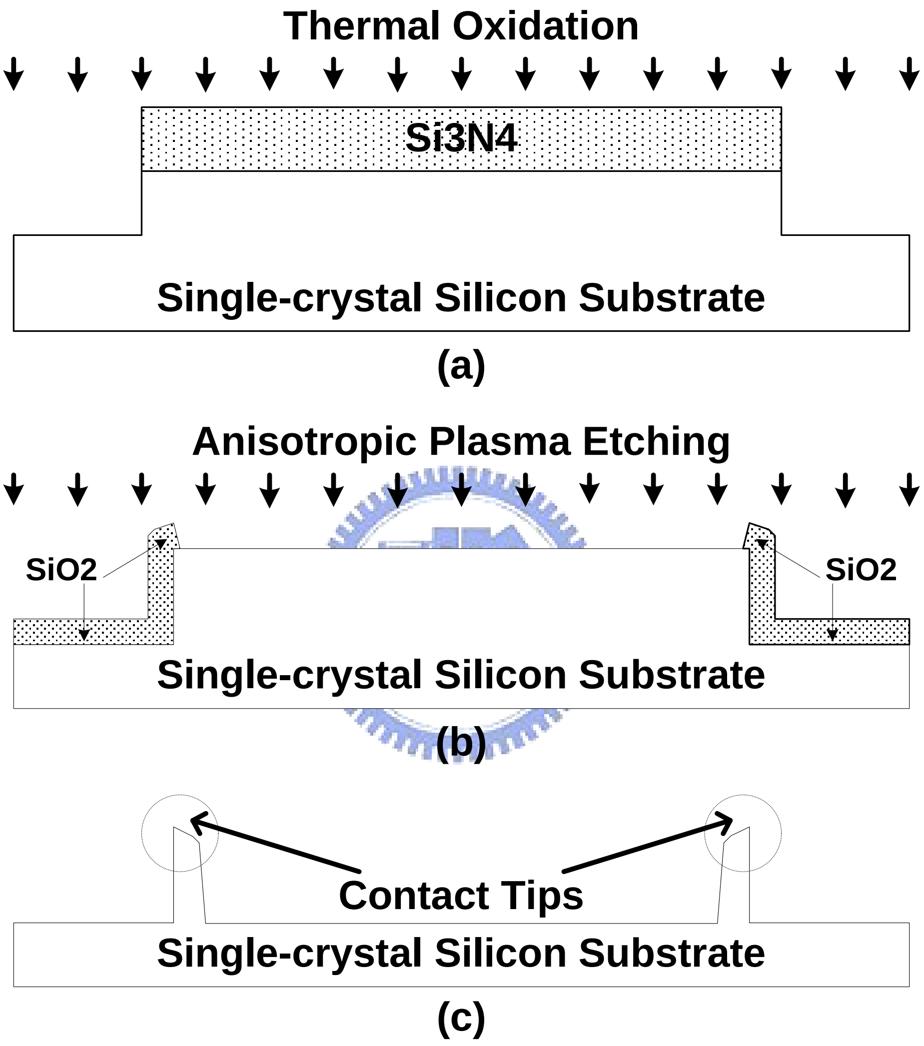


Fig. 3-3 Key process flows for forming silicon tips as crystallization seeds. Some of the silicon tips are amorphized by ion implantation in order to absorb more laser energy.

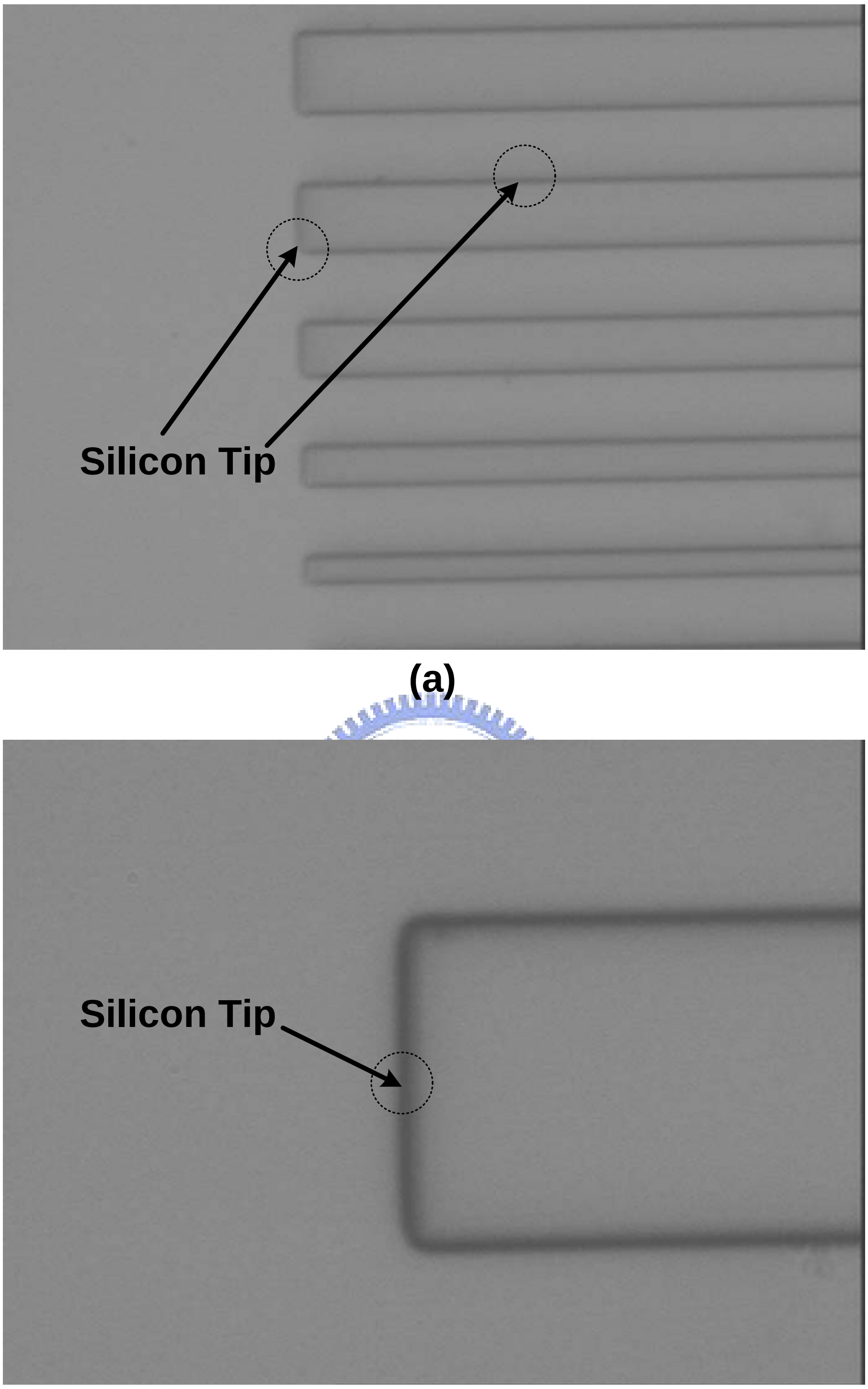


Fig. 3-4 Optical micrographs of silicon tips formed by spacer technology. The silicon tips provide single-crystal seeds for excimer laser crystallization of amorphous silicon films on glass substrates.

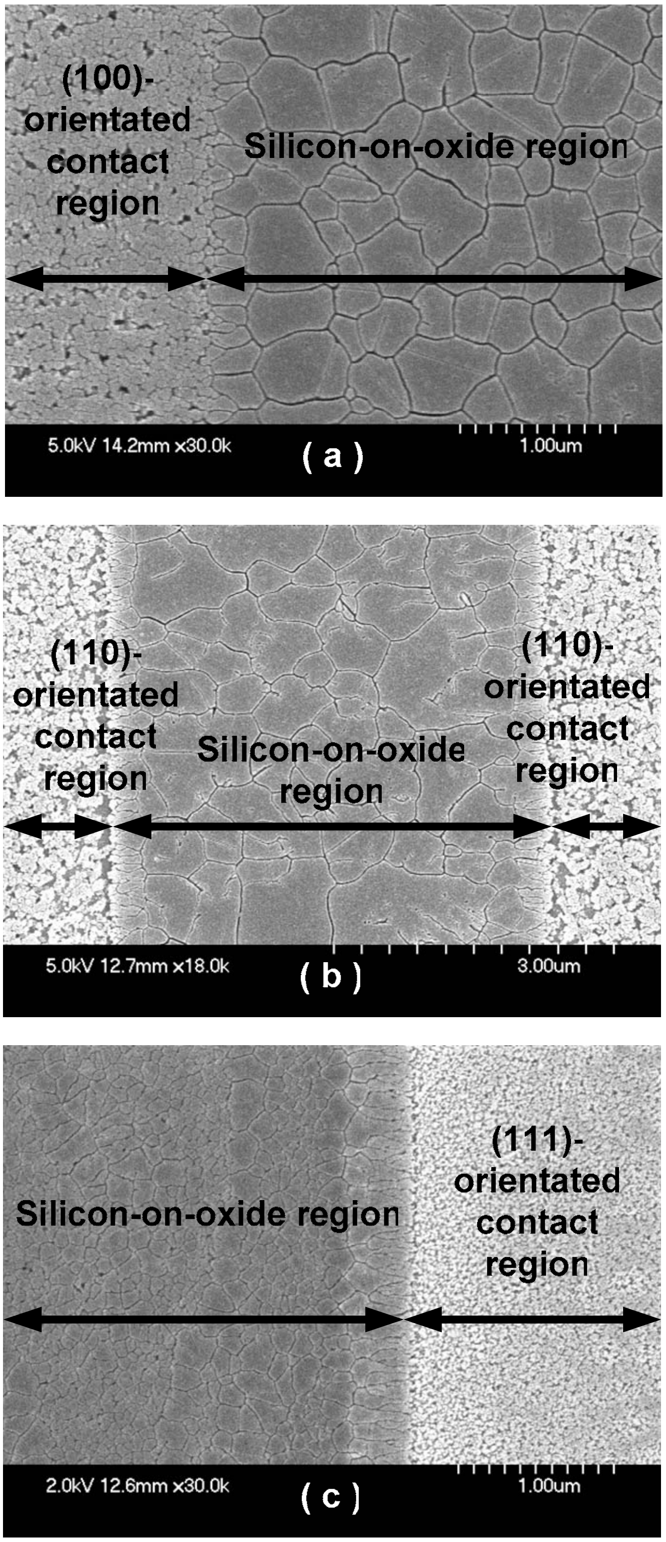


Fig. 3-5 SEM photographs of laterally seeded silicon films on (a) (100)-, (b) (110)-, and (c) (111)-orientated silicon substrates.

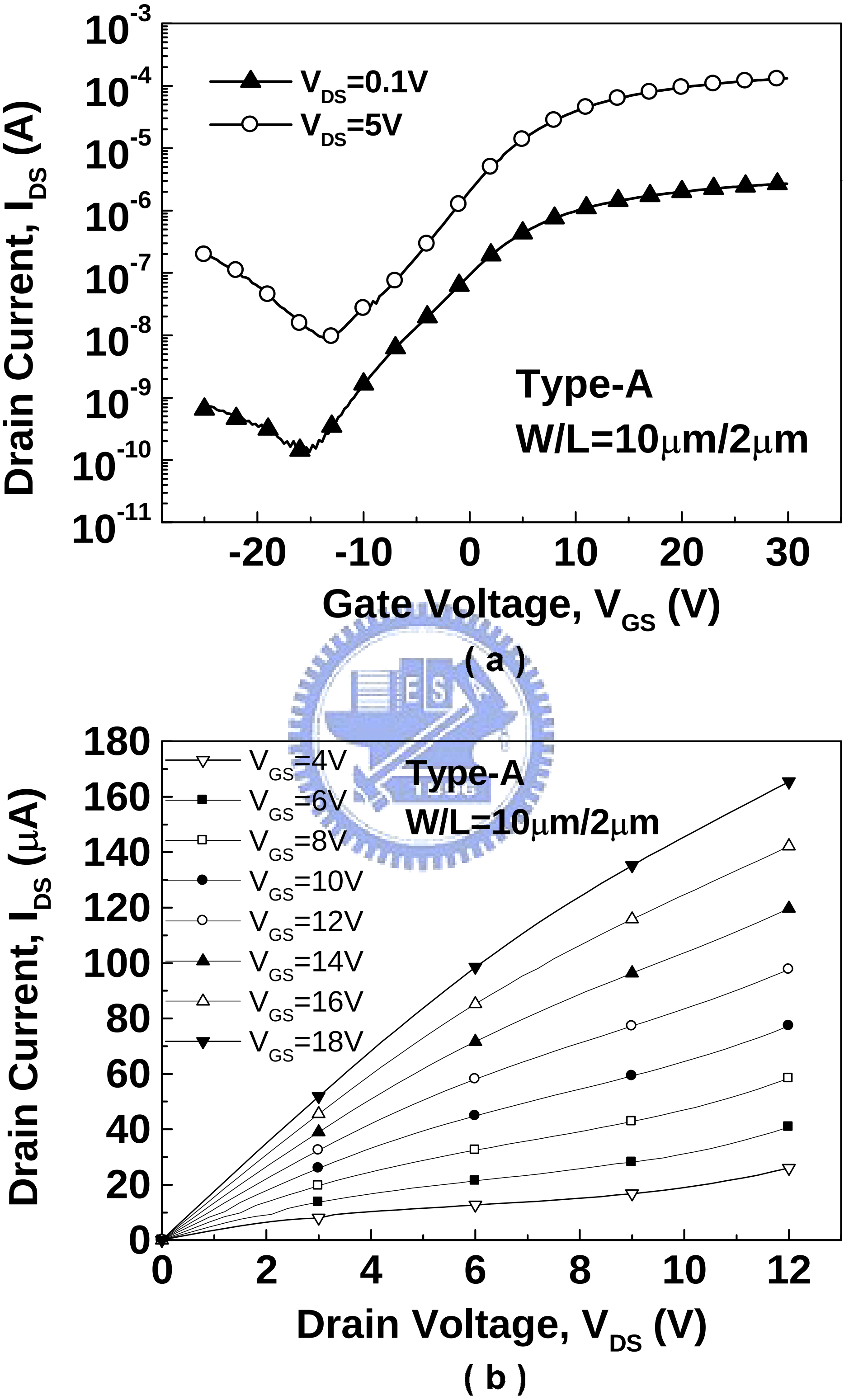


Fig. 3-6 (a) transfer and (b) output characteristics of a laterally seeded TFT on (110)-orientated silicon substrate.

Chapter 4

Short Channel Effects of Large-grained Poly-Si Thin Film Transistors Fabricated by a Sequential Lateral Solidification Technique

4.1 INTRODUCTION

Fabrication of high-performance polycrystalline silicon thin film transistors (Poly-Si TFTs) which are integrated into high-resolution active matrix displays are strongly dependent on the techniques of excimer laser annealing (ELA), because amorphous silicon films can be crystallized into high-quality polycrystalline silicon films on large area glass substrates [1]. However, the grain size is about ten times the thickness of a-Si films by a conventional ELA technique [2], which limit the device performance [3]. Many modified methods have been proposed to form large grains by modulating the thickness of a-Si films [4], [5], the phase of an excimer laser [6], [7], and the scanning speed of a CW laser [8]-[10]. The purpose of all methods is to build a temperature gradient in the a-Si films. In this chapter, we propose a thickness-modulated method to make a sequential lateral solidification (SLS) for grain growth, and further investigate the short channel effects of large-grained excimer-laser crystallized poly-Si TFTs. We used high-temperature wet oxidation to pre-oxidize the channel region selectively, but oxidation of silicon films can be performed at or below 600℃ for glass substrate. Many techniques of low-temperature oxidation have been proposed such as plasma oxidation [11]-[14], wet oxygen oxidation [15], steam ambient oxidation [16], and wet ozone-enriched oxidation [17], [18]. Those methods were used to form high-quality gate insulators at low temperature. Therefore, the processes in this work can be actually carried out at low temperature.

Moreover, dopants must be activated at low temperature, which is a critical issue on TFT array process of flatted panel display (FPD). Several dopant activation techniques are being proposed [19]-[21], whereas activation efficiency affects the uniformity of poly-Si TFTs. Using PMOS technology to integrate peripheral driver circuits into a panel has been attracting many attentions because of its simple fabrication process and good device reliability [22], [23]. Therefore, fabricating stable p-type poly-Si TFTs is important. In this chapter, 600℃ activation of boron-doped poly-gated TFTs for several hours generates many hole traps in the gate oxide, resulting in a parallel shift of threshold voltage among measurements of several times. This is ascribed to boron diffusion at 600℃ for several hours. However, this phenomenon does not be clearly observed in BF_2-doped TFTs.

4.2 DEVICE FABRICATION

Fig. 4-1 shows the key CMOS process flows for fabricating short-channel large-grained poly-Si TFTs. First, silicon wafers with a 2μm thermal oxide layer were used as starting substrates. A 50 nm thick amorphous silicon (α-Si) layer was deposited by decomposing SiH_4 in a LPCVD system at 550 ℃. Next, a 150 nm thick silicon nitride (Si_3N_4) layer was deposited and then patterned. The exposed silicon film was fully oxidized at 925 ℃ using Si_3N_4 patterns as hard masks, shown in Fig. 4-1 (a). Afterward, the Si_3N_4 patterns were selectively etched in a hot phosphoric acid bath at 165 ℃. After the native oxide was removed from the silicon film region, a 100 nm α-Si layer was deposited by the decomposition of SiH_4 in a LPCVD system at 550 ℃. The α-Si films were then crystallized by KrF excimer laser irradiation, as shown in Fig. 4-1 (b). After the active channel region was defined, a T_{ox} thick TEOS layer was deposited as the gate insulator by PECVD at 350 ℃. Thereafter, a 250 nm α-Si layer was deposited and then patterned as the gate electrode. The source and drain regions were formed after self-aligned ion implantation of phosphorous with a dosage of $5\times10^{15}cm^{-2}$ at 50KeV and boron with a dosage of $5\times10^{15}cm^{-2}$ at 15keV. Meanwhile, photoresist (P.R) patterns were used to selectively define the positions of dopants, as shown in Figs 4-1 (c) and (d). A 300 nm TEOS oxide layer was deposited, and then the dopants were activated at 600 ℃ for 12 h. Finally, contact opening and metallization were performed to complete the self-aligned structure, as shown in Fig. 4-1 (e). Additionally, BF_2-doped TFTs were fabricated as a comparison of boron diffusion into the gate oxide.

4.3 RESULTS AND DISCUSSION

A. Characteristics of large-grained poly-Si films

The silicon film thickness was modulated in order to establish a thermal gradient facilitating the grain growth. The laser energy densities between completely melting 100 nm thick silicon film and partially melting 150 nm one were employed to form large grains in the channel region. Super lateral growth (SLG) in the 100 nm thick silicon film took place, while homogeneous nucleation in the 150 nm thick silicon film occurred. Meanwhile, a lateral thermal gradient facilitated the formation of large longitudinal grains and small grains were grown up in the partially melting 150 nm region through the unmelted layer as nucleation sites, as the SEM photographs shown in Fig. 4-2 near where the 100 nm and 150 nm thick channel regions are connected. Owing to grains elongated from the 150 nm side to the 100 nm side, a short channel region is occupied by the longitudinal grains, enhancing the performance of the short channel poly-Si TFTs.

Notably, a clear grain boundary is formed at the center of channel if a distance between both 150 nm thick regions is short enough, as shown in Fig. 4-3. The grains grow from the thicker part and meet each other at the center of the thinner part. The center boundary comes from significant mass transport induced by surface tension of the molten silicon. As channel length is being scaled, the center grain boundary affects the performance of the device significantly. Device behaviors of scaled poly-Si TFTs with a single grain boundary in the channel have been numerically simulated by Philip et al [24]. Philip makes a conclusion that the presence of a grain boundary at the center of the TFT channel aids in both suppression of the off current and improving the pseudo-subthreshold slope. Complete removal of grain boundaries may not be desirable for optimal TFT design.

Fig. 4-4 shows three-dimensional AFM images of a 100 nm thick amorphous silicon film before and after excimer-laser crystallization. The a-Si film possesses surface roughness of about 0.65 nm root mean square (RMS), while the excimer laser-annealed poly-Si film has surface roughness of about 5.50 nm RMS. Excimer-laser annealed poly-Si film becomes rougher due to mass transport induced by surface tension of molten silicon. Surface roughness of laser-crystallized poly-Si films has been ascribed to the differences in latent heat and thermal conductivity between polycrystalline and amorphous silicon [25], positive feedback of optical interference effects in multiple shot crystallization [26], capillary waves excited by the volume change at the solid-melt transition [27], and the adhesion force between the melted silicon and microcrystalline silicon [28].

B. I-V characteristics of large-grained poly-Si TFTs

Fig. 4-5 shows the output characteristics of short n- and p-channel poly-Si TFTs whose channels are crystallized by the proposed SLS technique. As drain voltage

V_{DS} increases when gate voltage V_{GS} keeps low, the absence of drain current I_{DS}, which is generally called kink effect causing excess drain currents, comes from avalanche multiplication effect and drain induced grain-boundary barrier lowing (DIGBL) effect. The excess currents from the former effect are ascribed to impact ionization generating electron-hole pairs. The excess currents from the latter effect are ascribed to the trapped charges modulating the potential profile of the drain junction. The saturated I_{DS} are then observed under the same applied V_{DS} when V_{GS} becomes higher. However, the saturation-like I_{DS} are not normal but from the compensation of self-heating effect. The self-heating effect causes negative resistances to compensate for the avalanche multiplication effect. Therefore, it can be seen from Fig. 4-5 (a) that I_{DS} decrease with V_{DS} increase when the TFT is operated in high current mode.

Fig. 4-6 shows the transfer characteristics of short n- and p-channel poly-Si TFTs whose channels are crystallized by the proposed SLS technique. High field-effect mobility and ON/OFF current ratios are obtained because of large-grained poly-Si channel of the TFTs. Fewer grain boundaries not only promote ON currents of the device but also reduce the device's leakage current. Grain boundaries have the characteristics of trapping charges so that device's ON currents are not improved and its OFF currents are not reduced. As a result, trying to fabricate a TFT on a single grain is the most important. Additionally, Fig. 4-7 shows the transfer characteristics of a CMOS-TFT inverter made up of a p-channel TFT with W=200μm L=2μm and a n-channel TFT with W=120μm L=2μm. There has a good switching characteristic. The threshold voltage of the CMOS inverter is not adjusted using moderate channel doping.

C. Issues of B- and BF2-doped ploy-Si TFTs activated at 600℃ for 12 h

Fig. 4-8 shows the transfer characteristics of non-hydrogenated B-doped poly-Si TFT extracted from measurements of the 1st and 4th times. One can be seen that there has a parallel shift in the sub-threshold region between the both measurements but the ON and OFF currents of the single TFT are remained the same. The parallel shift in the sub-threshold is not found in long channel devices. This is because the major holes are injected into the gate oxide under high drain electric field after the 1st measurement. It can be inferred that there are hole traps in the gate oxide created during 600℃ activation of boron-doped poly-gated TFTs. However, these hole traps can be passivated using NH_3 plasma treatment. Fig. 4-9 shows the transfer characteristics of NH_3 plasma hydrogenated B-doped poly-Si TFT extracted from measurements of the 1st and 4th times. The shift range of threshold voltage is reduced because the activation-induced hole traps are passivated by NH_3 plasma treatment. After the 4th time measurement, the I_{DS}-V_{GS} characteristics keep stable because these hole traps have been positively charged from the previous measurements.

Fig. 4-10 shows the transfer characteristics of non-hydrogenated BF_2-doped poly-Si TFT extracted from measurements of the 1st and 5th times. The perturbation in OFF currents and a shift in sub-threshold regions are observed under this device are measured several times. The unstable OFF currents become stable after several times measurements. This phenomenon is associated with the efficiency of BF_2-doped poly-Si films at 600℃ for 12 h. Fig. 4-11 shows SIMS plots for boron concentration before and after 600 ℃activation of B and BF_2 ion implantation, respectively. It can be seen that boron atoms penetrate into the gate oxide after 12 h activation at 600 ℃. Boron atoms in the gate oxide create hole traps which trap hot-holes injected into the gate oxide near the drain junction. Therefore, the subthreshold region shifts toward smaller V_{GS}. These hole traps in the gate oxide can be passivated by post plasma treatment.

4.4 CONCLUSION

This chapter introduces a novel crystallization method for fabricating high performance poly-Si TFTs. The modulated thickness of silicon film builds a temperature gradient for enlargement of channel grains. When channel length of the TFTs is shortened, the performance of devices is improved. However, the p-channel TFT has an issue of boron penetration into the gate oxide. Its threshold voltage shifts after measurements of several times due to hole traps created in the gate oxide. NH_3 plasma treatment can passivated those traps, leading to an improvement in the shift of the threshold voltage.

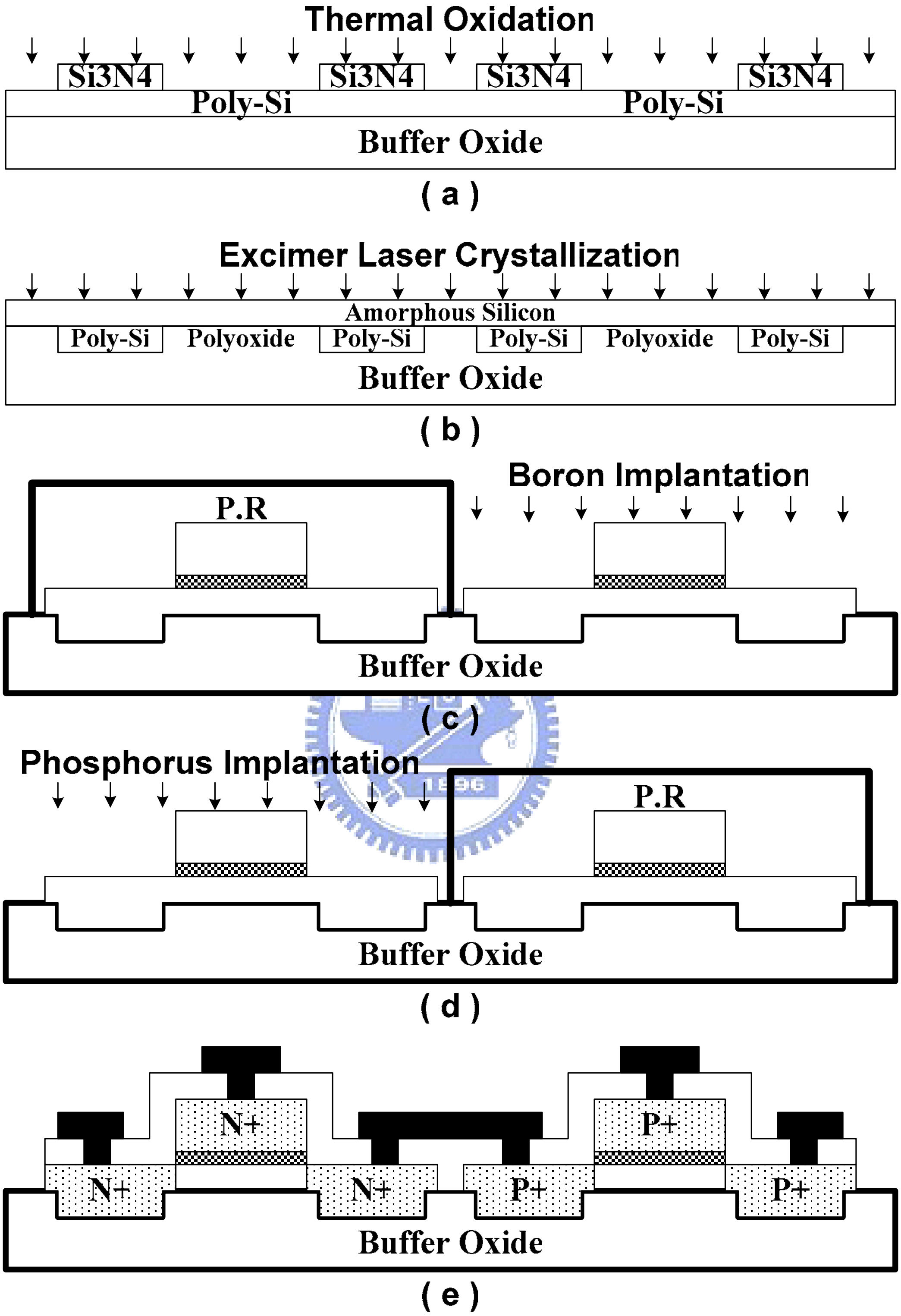


Fig. 4-1 Key CMOS process flow for fabricating short-channel large-grained poly-Si TFTs.

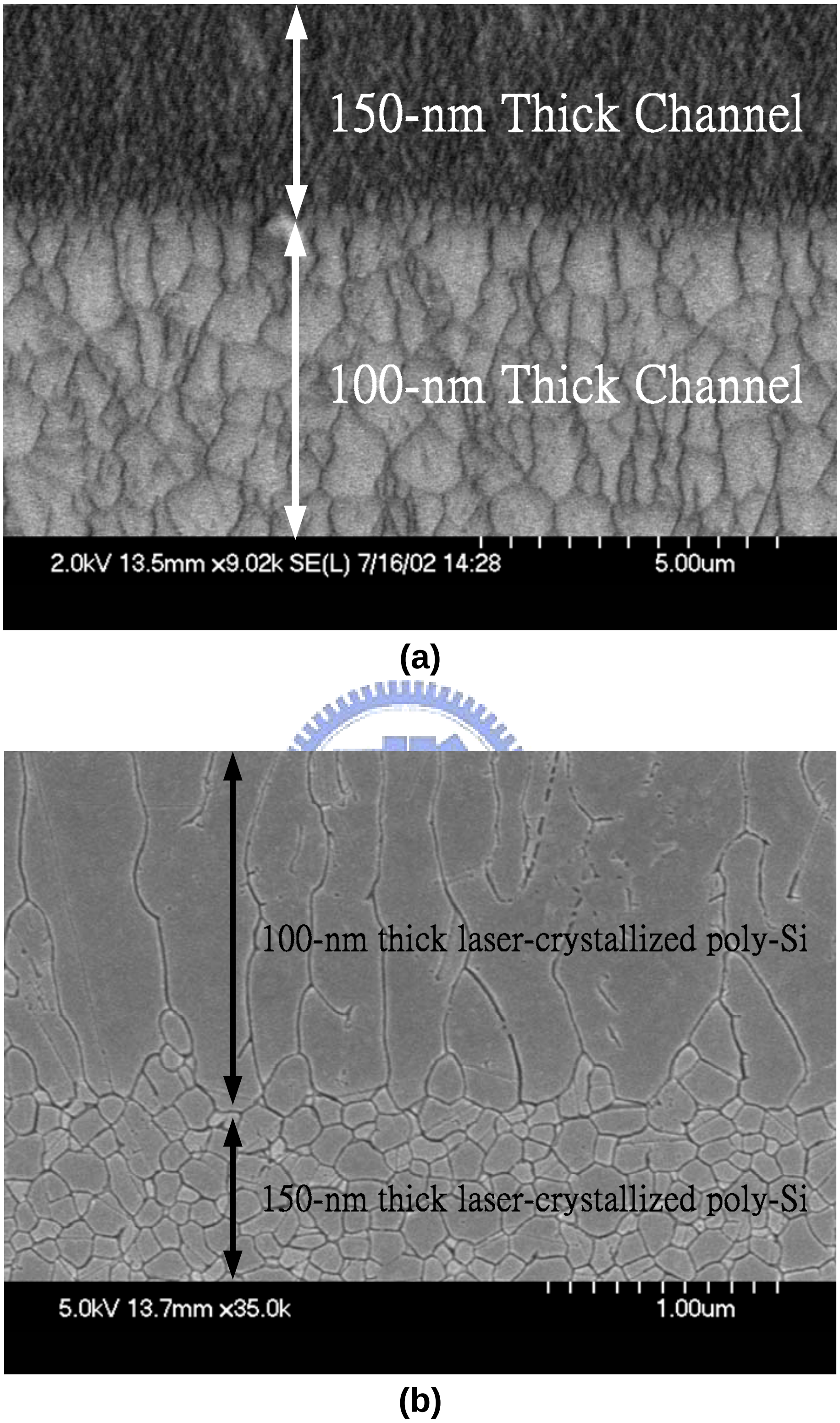


Fig. 4-2 SEM photographs of excimer-laser-crystallized poly-Si showing the grain sizes near where the 100 nm and 150 nm thick channel regions are connected. Larger scale (a) and smaller scale (b) are used to exhibit the delineation of grains.

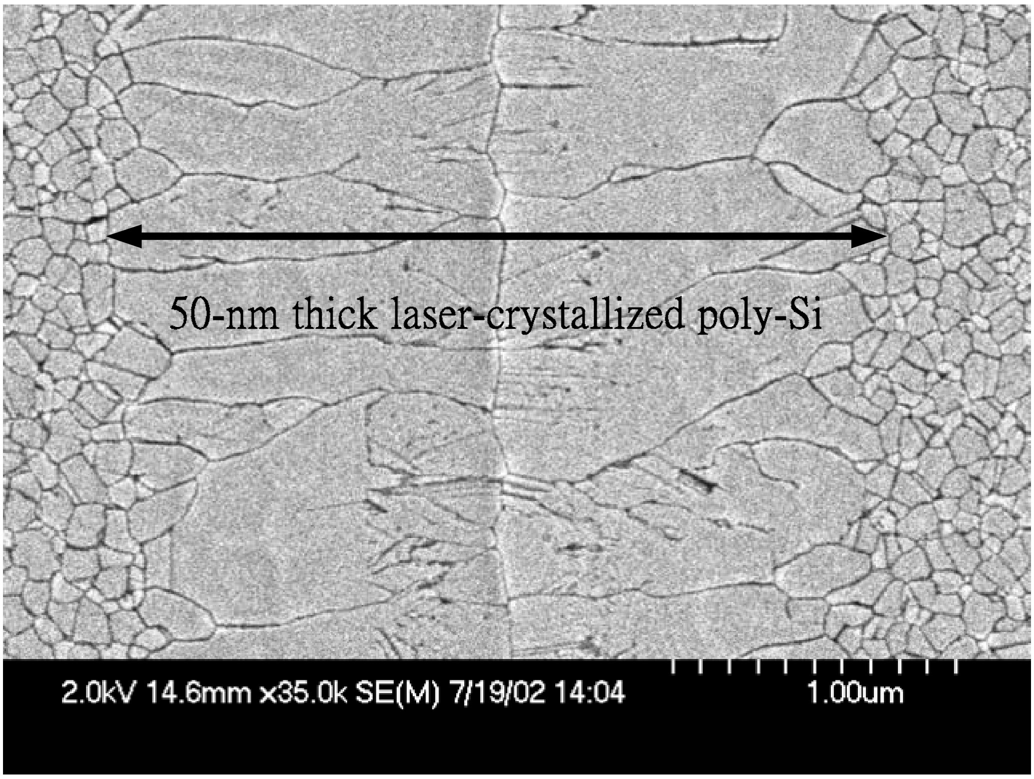
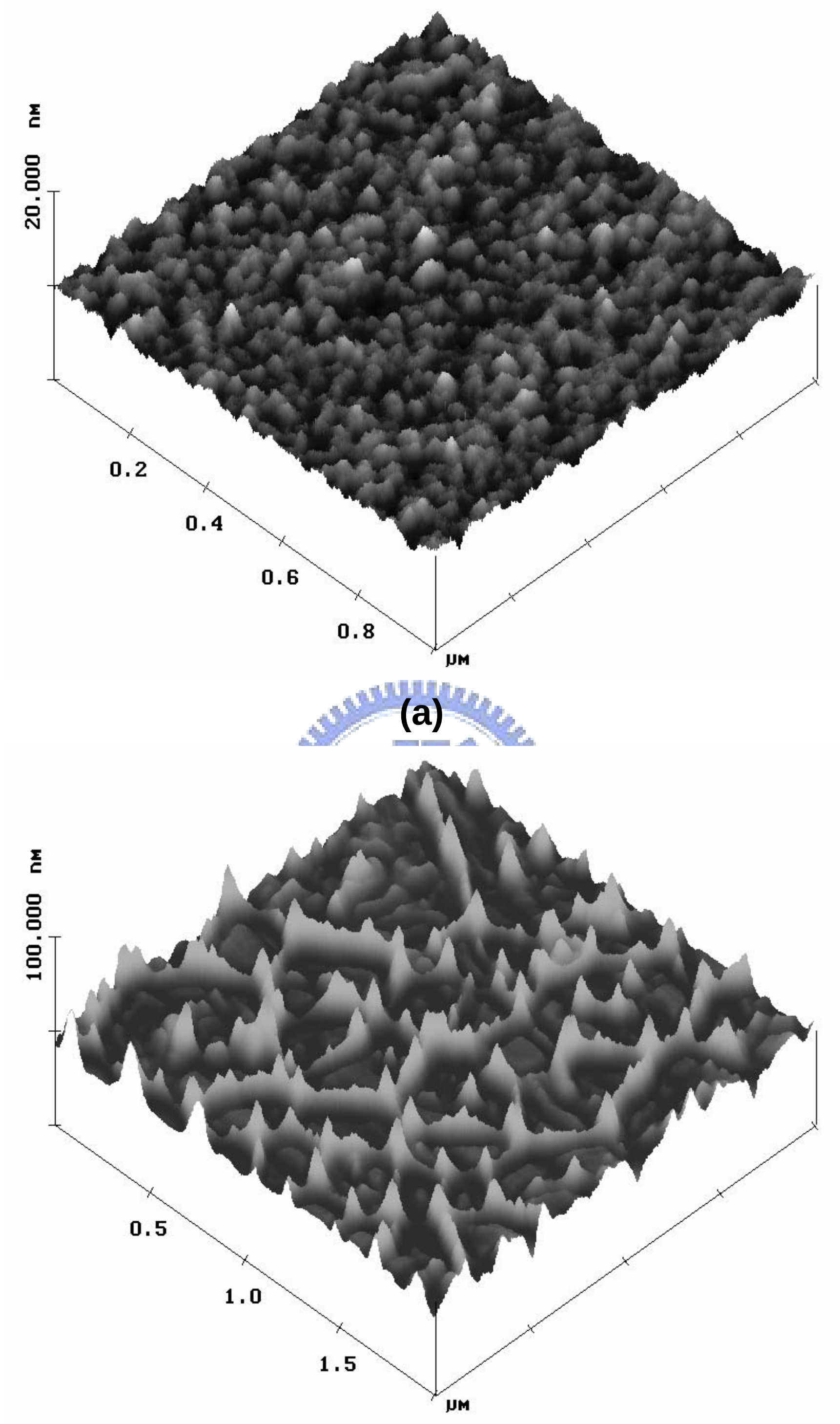


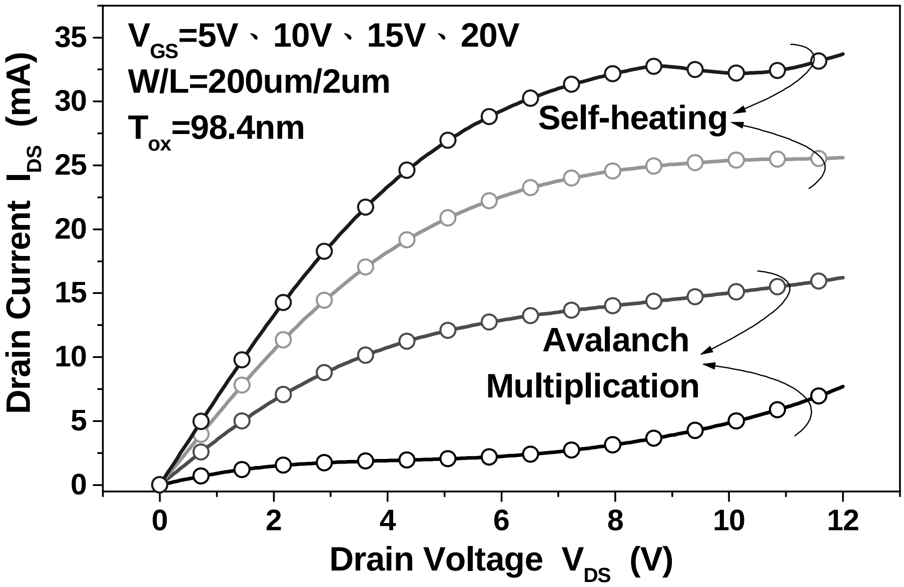
Fig. 4-3 SEM photograph of excimer-laser-crystallized poly-Si showing a clear grain boundary located within channel center. The clear grain boundary results from mass transport of molten silicon induced by surface tension.



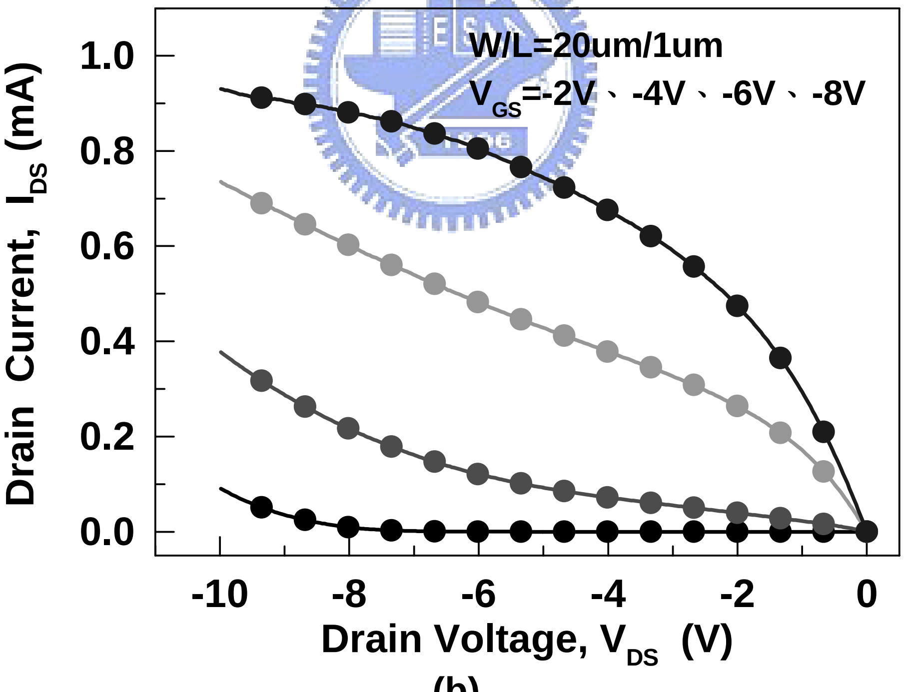
(a)

(b)

Fig. 4-4 Three-dimensional AFM images of a 100 nm thick amorphous silicon film (a) before and (b) after excimer-laser crystallization. Excimer-laser annealed poly-Si film becomes rougher due to mass transport induced by surface tension of molten silicon.



(a)



(b)

Fig. 4-5 Output characteristics of short (a) n-channel and (b) p-channel poly-Si TFTs. The avalanche multiplication effect can be compensated by the self-heating effect as the drain current increases.

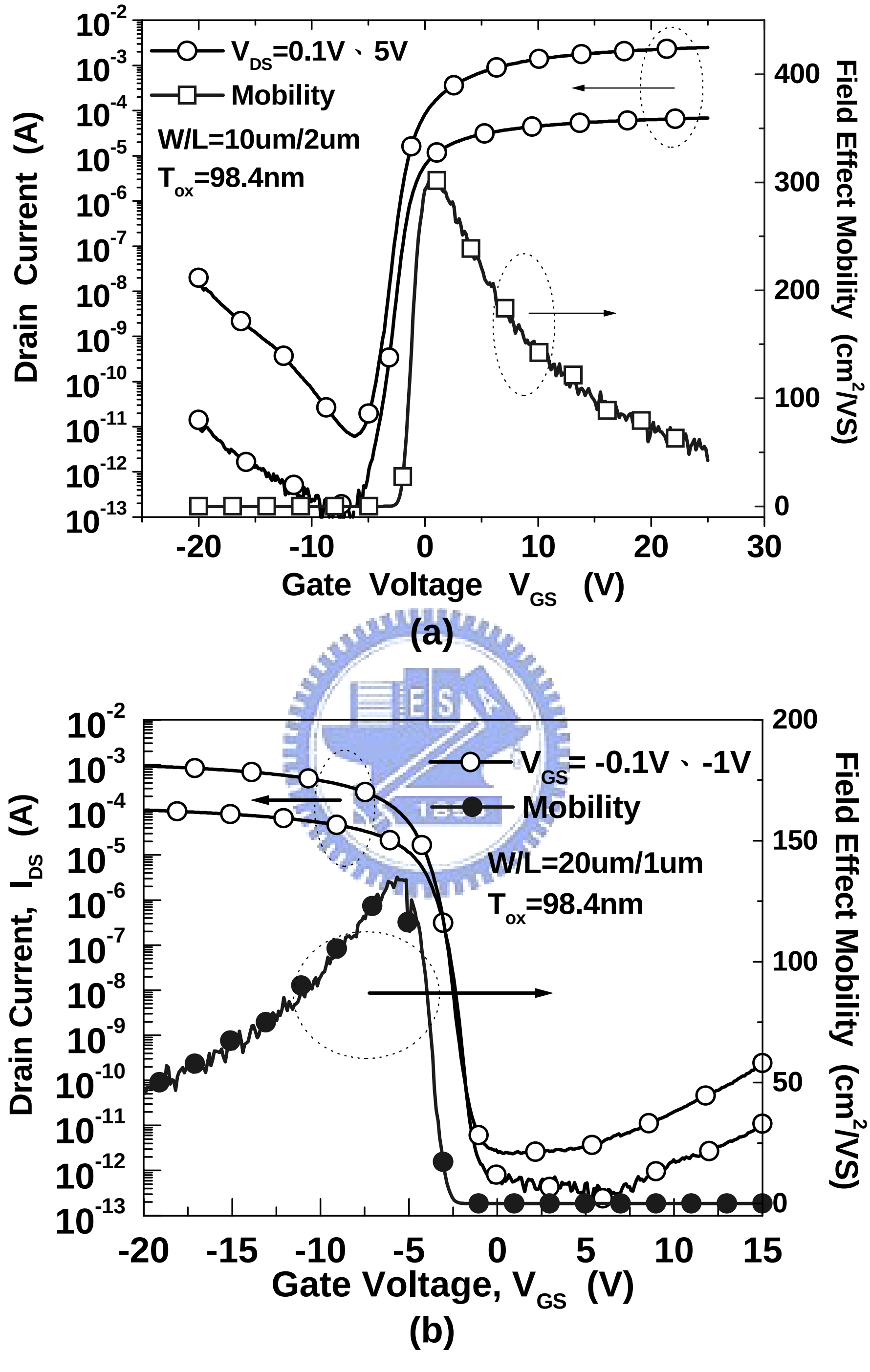


Fig. 4-6 Transfer characteristics of short (a) n-channel and (b) p-channel poly-Si TFTs with high mobility and high ON/OFF current ratio.

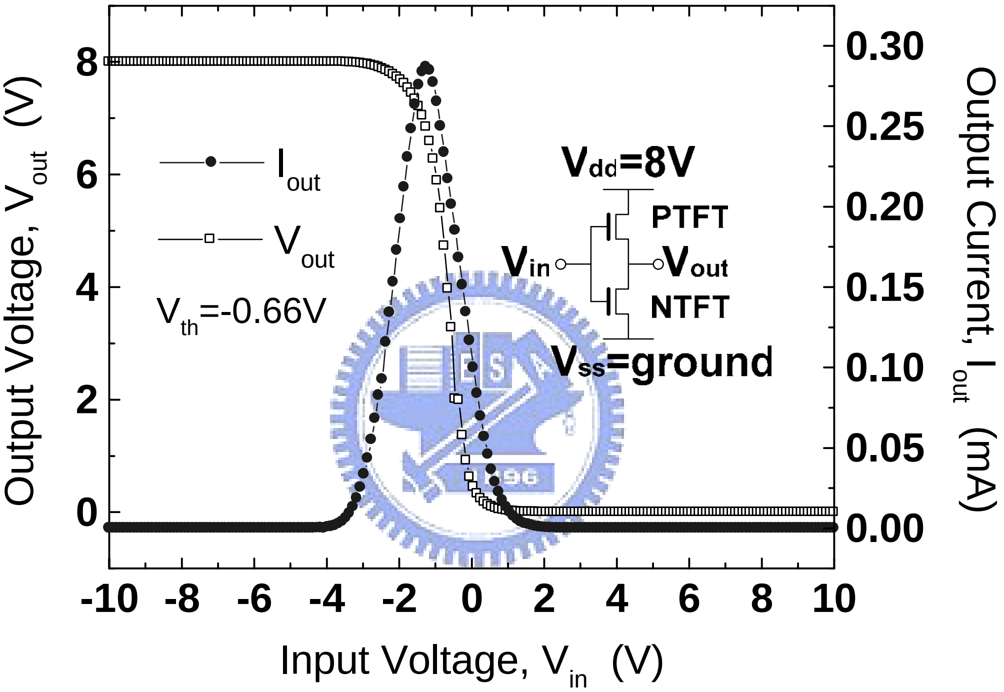


Fig. 4-7 Transfer characteristics of CMOS-TFT inverter made up of a p-channel TFT with W=200μm L=2μm and a n-channel TFT with W=120μm L=2μm.

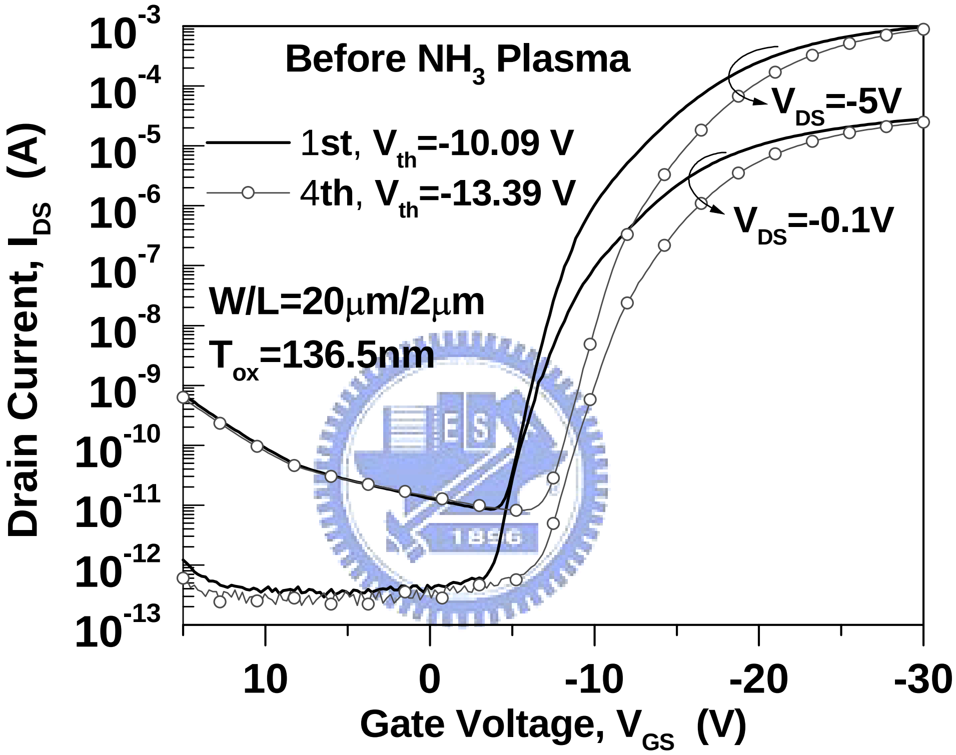


Fig. 4-8 Transfer characteristics of non-hydrogenated B-doped poly-Si TFT extracted from measurements of the first and fourth times. A parallel shift in the sub-threshold region is due to the creation of hole traps in the gate oxide during 600℃ activation of boron dopants.

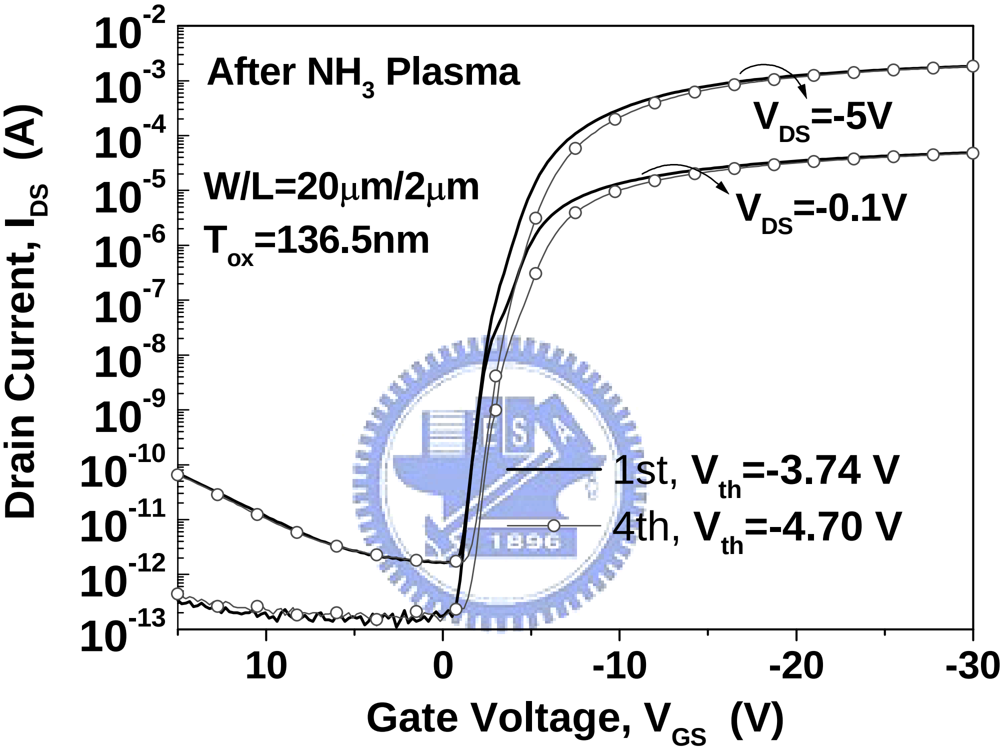


Fig. 4-9 Transfer characteristics of NH_3 plasma hydrogenated B-doped poly-Si TFT extracted from measurements of the first and fourth times. The shift range of threshold voltage is reduced because the activation-induced hole traps are passivated by NH_3 plasma treatment.

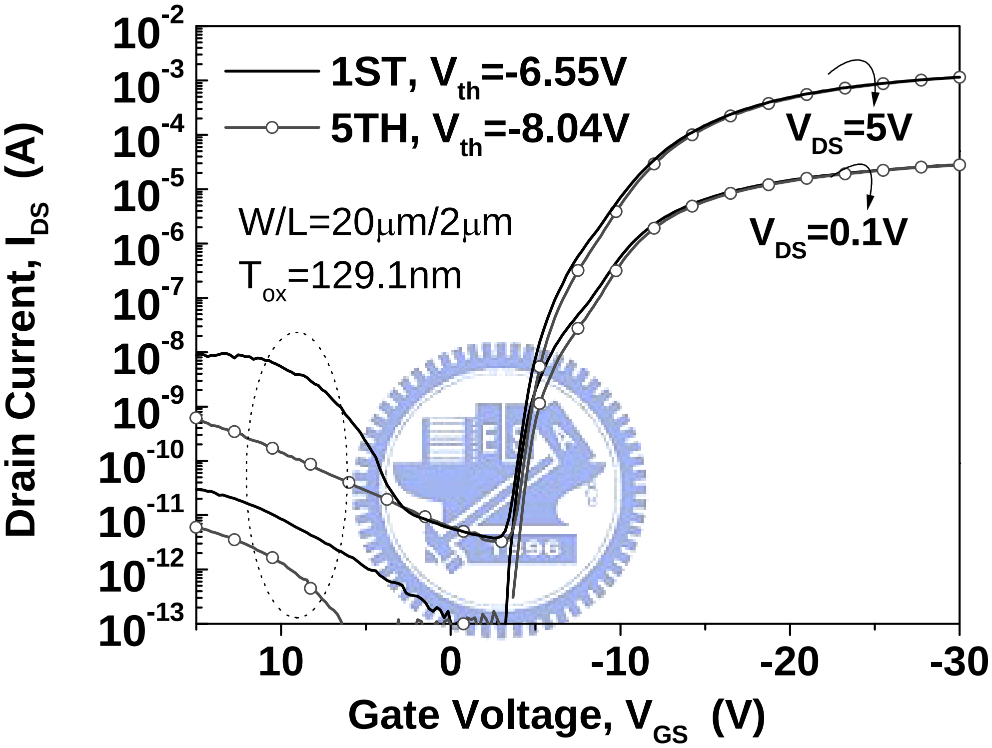


Fig. 4-10 Transfer characteristics of non-hydrogenated BF_2-doped poly-Si TFT extracted from measurements of the first and fifth times. The perturbation in OFF currents and a shift in sub-threshold regions are observed under this device are measured several times.

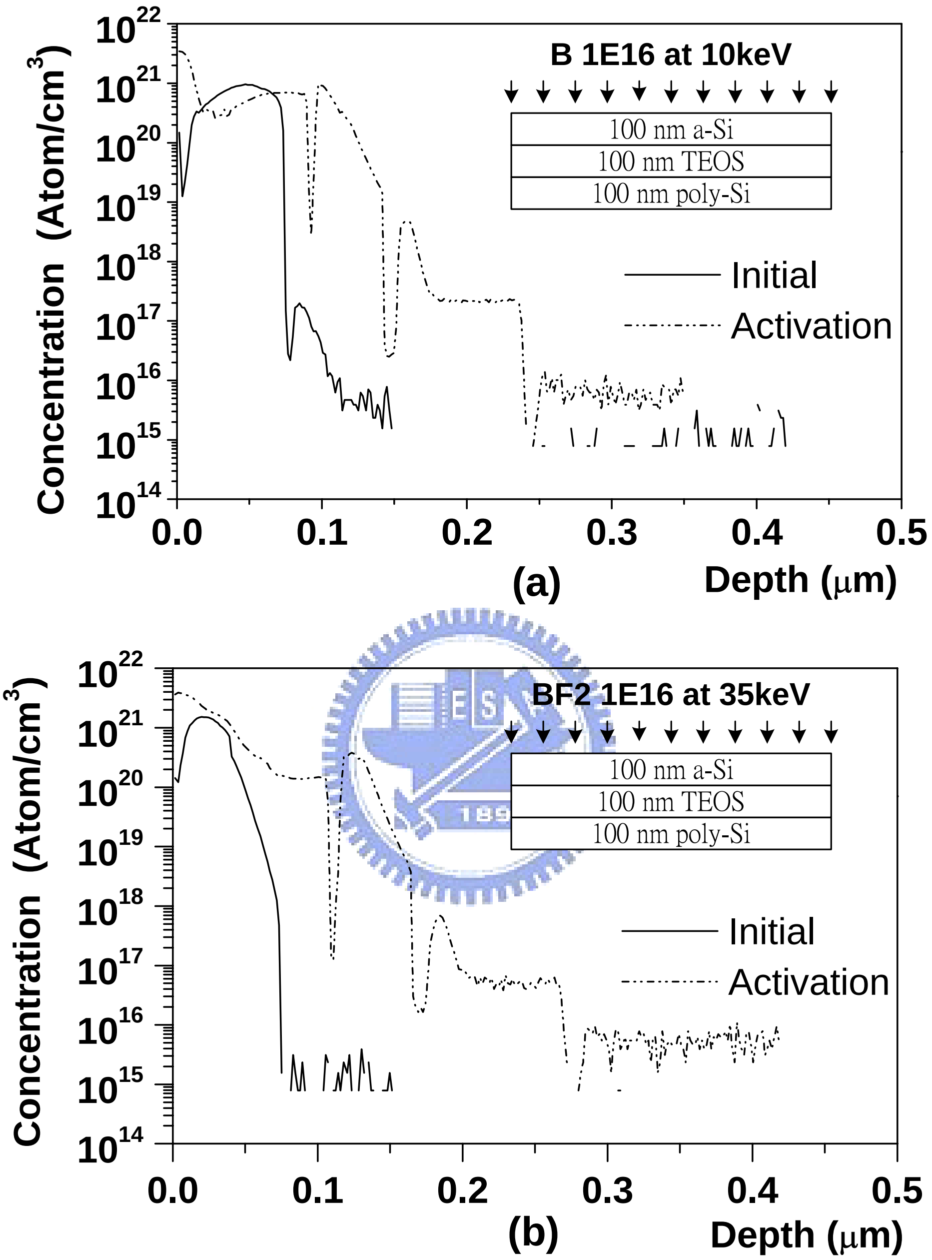


Fig. 4-11 SIMS plots showing boron concentration before and after 600 ℃ activation for (a) B and (b) BF_2 ion implantations, respectively.

Chapter 5

Effects of Grain Boundaries in the Drain Junction on Performance and Hot-carrier Reliability of Excimer-laser Annealed Poly-Si TFTs

5.1 INTRODUCTION

Excimer-laser-annealed (ELA) polycrystalline silicon thin film transistors (poly-Si TFTs) have been extensively investigated due to their potential for being integrated into peripheral driver circuits with active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) on large area glass substrates [1]. A laser-crystallized poly-Si TFT with a high driving current, good reliability and uniform device performance is necessary to develop a system on a panel (SOP). Many techniques have been proposed to improve the electrical characteristics of poly-Si TFTs, such as enlarging the channel grains by laser-induced lateral crystallization [2] and reducing the number of grain-boundary trap states by plasma treatment [3]. However, the uncontrollability of grain boundaries and their locations in the channel region reduce the uniformity of devices. In particular, the instability of an applied laser can simultaneously introduce grains of various sizes into the channel regions [4], because the formation of channel regions follows the definition of active islands. Meanwhile, the charges trapped at the grain boundaries, which are always associated with the surface roughness, enhance the local electric fields [5]. A self-aligned poly-Si TFT may exhibit different behaviors in its forward and reverse modes because of the asymmetry of the grain boundaries, particularly in the drain junction [6]. Although many studies of the influence of grain-boundary locations and trap states on device performance have involved simulation [7], none has yet applied experimental methods to laser-crystallized poly-Si TFTs [8].

In this work, self-aligned poly-Si TFTs are fabricated with various numbers of grain boundaries in their drain junctions. Other TFTs with fewer grain boundaries throughout their channel regions are fabricated nearby as a reference. Various numbers of grain boundaries in the drain junctions and throughout the channel regions are used to determine the effects of grain boundaries on the performance and hot-carrier reliability of excimer-laser-crystallized poly-Si TFTs with and without NH_3 plasma treatment. The inter-device variations, such as the difference between the numbers of grain boundaries in the channels [9] and the channel shortening effect by the diffusion of dopants from the source and drain [10], can be eliminated by comparing the forward and reverse modes of a single device. The strong local electric fields created by the trapping of electrons at the grain boundaries critically affect the performance and hot-carrier reliability of excimer-laser-crystallized poly-Si TFTs [11]. The local electric fields can be then reduced by passivating grain boundaries using NH_3 plasma treatment [12].

5.2 EXPERIMENT

Fig. 5-1 shows the key process flows for fabricating self-aligned poly-Si TFTs. Silicon wafers with 2μm thermal oxide layers were used as starting substrates. A 50nm thick amorphous silicon (α-Si) layer was deposited by decomposing SiH_4 in an LPCVD system at 550℃. Next, a 150nm thick silicon nitride (Si_3N_4) layer was deposited and then patterned. The exposed silicon films were fully oxidized at 925℃ using the Si_3N_4 patterns as hard masks, as indicated in Fig. 5-1 (a). Subsequently, the Si_3N_4 patterns were selectively etched in a hot phosphoric acid bath at 165℃. After the native oxide was removed from the region of silicon films, a 100nm α-Si layer was deposited by decomposing SiH_4 in an LPCVD system at 550 ℃. The α-Si films were then crystallized under irradiation from a KrF excimer laser, as shown in Fig. 5-1 (b). After the active channel regions were defined, a 135nm thick TEOS gate oxide was deposited by PECVD at 350℃. Thereafter, a 250nm α-Si layer was deposited and then patterned as the gate electrodes. The source and drain regions were formed after the self-aligned ion implantation of phosphorous with a dosage of $5\times10^{15}cm^{-2}$ at 50keV. A 300nm TEOS oxide layer was deposited, and then the dopants were activated at 600℃ for 12h. Finally, contact opening and metallization were performed to complete the self-aligned structure. The TFT shown in Fig. 5-1 (c) is called TFT-A; it has large grains throughout its channel region. The other TFT, shown in Fig. 5-1 (d), is called TFT-B, and has large and small grains on both sides of its channel region.

The electrical characteristics of those devices were evaluated before and after NH_3 plasma hydrogenation in a parallel plate reactor at 300℃ at a power density of 0.7 W/cm^2. The Secco etchant, which consists of 7.30g of $K_2Cr_2O_7$ dissolved in 165ml of H_2O and 335ml of HF was used to delineate grain-boundary defects. The side of the 100nm-thick channel of the TFT-B is defined as a drain of the forward mode, and the other side of the 150nm-thick channel of the TFT-B is defined as a drain of the reverse mode. The channel length L of the TFT-B includes the channel length L_A of the 150nm-thick region and the channel length L_B of the 100nm-thick region. In the evaluation of the transfer characteristics of the devices, the threshold voltage V_{th} is defined as the gate voltage V_{GS} at constant drain currents; for example, $I_{DS} = (W/L)\times 10nA$ at a drain voltage of $V_{DS} < 5V$ and $I_{DS} = (W/L)\times 100nA$ at a drain voltage of $V_{DS} \geq 5V$. The field-effect mobility and the transconductance are evaluated at V_{DS}=0.1V. All hot-carrier stresses on the devices with and without NH_3 plasma treatments are applied at a drain voltage of V_{DS}=20V and a gate voltage of V_{GS}=10V. The dimensions of the stressed devices are L=6μm and W=10μm.

Meanwhile, the channel length of the TFT-B is the sum of L_A=2μm and L_B=4μm. ΔV_{th} is defined as $V_{th,s} - V_{th,i}$ where $V_{th,i}$ represents the initial V_{th} and $V_{th,s}$ represents the V_{th} at each stress time. Moreover, the degradation of $G_{m\ max}$ is defined as $\Delta G_{m\ max}/G_{m\ max,i}$, where $\Delta G_{m\ max}=G_{m\ max,s} - G_{m\ max,i}$; $G_{m\ max,i}$ denotes the initial $G_{m\ max}$, and $G_{m\ max,s}$ represents the $G_{m\ max}$ at each stress time.

5.3 RESULTS AND DISCUSSION

A. Features of ELA poly-Si films

Fig. 5-2 (a) shows the SEM photograph of grains of different sizes of the laser-crystallized poly-Si film between the 150nm-thick and 100nm-thick regions. Laser energy densities between that which completely melted the 100nm-thick silicon films and that which partially melted the 150nm-thick films were employed to form variously sized grains of the laser-crystallized poly-Si films. Large grains in the 100nm-thick regions are formed in the super lateral growth (SLG) regime [13]. Meanwhile, a lateral thermal gradient from the modulated thickness of silicon films facilitates the formation of longitudinal grains [14]. Small grains of the 150nm-thick regions are grown from the un-melted residuals that act as nucleation sites. In the fabrication of TFT-B devices, large and small grains are formed simultaneously in the channel regions, leading to the different numbers of grain boundaries in the drain junctions when measurements of a TFT-B were made in the forward and reverse modes. However, grain boundaries of excimer-laser-crystallized poly-Si films always coexist with the protrusions, roughening the surface of the poly-Si films [15]. Fig. 5-2 (b) shows the AFM image of the surface of excimer-laser-crystallized poly-Si films near the connection between the 150nm-thick region and the 100nm-thick region. The 150nm-thick channel with a surface roughness of 5.36 nm RMS (Root Mean Square) and the 100nm-thick channel with a surface roughness of 2.88 nm RMS are evaluated from Fig. 5-2 (b). Significant mass transport toward the grain boundaries roughens the surface and then causes carriers trapped at the grain boundaries to enhance the local electric fields.

Additionally, Secco etching was also used to delineate grain boundaries with and without passivation. As shown in Fig. 5-3, a 100nm-thick laser-crystallized poly-Si film was selectively treated with NH_3 plasma, using aluminum patterns as hard masks, the insertion of which was schematically depicted above Fig. 5-3. The aluminum patterns were then selectively removed using wet etchant. The grain boundaries in the aluminum capping region were clearly seen after Secco etching. However, the grain boundaries near the aluminum-capped edge were ambiguous because they were passivated by hydrogen lateral diffusion [16], reducing the etching rate around the grain boundaries. This result implies that the lateral diffusion of hydrogen may lead to a lack of uniformity of passivation of grain boundaries throughout the channel region. Therefore, irregular I-V characteristics, such as hump effects, are evident in the sub-threshold region.

B. I-V characteristics of ELA poly-Si TFTs

Fig. 5-4 (a) and (b) show the transfer characteristics of a single TFT-A and the forward and reverse modes of a single TFT-B before and after NH_3 plasma treatment. A comparison between TFT-A and TFT-B, reveals that the decrease in the number of grain boundaries of the channel regions accompanies a reduction in the threshold voltage and an increase in the field-effect mobility. This is because the grain boundaries trap electrons when the gate voltage V_{GS} is applied, generating surrounding depletion regions and leading to the formation of potential barriers. Meanwhile, strained bonds and dangling bonds at the grain boundaries generate band tail states and deep level states in the band gap, respectively. These states can trap electrons, reducing the ON current and increasing the OFF current. However, the states can be passivated during NH_3 plasma treatment [17], yielding a steeper sub-threshold slope for the hydrogenated TFT than that for the non-hydrogenated TFT. The ON/OFF current ratios and the field-effect mobility improve simultaneously after the grain boundaries are passivated. Notably, the leakage current of the non-hydrogenated TFT-B at V_{DS}=12V in the reverse mode is significantly higher than that in the forward mode, as shown in Fig. 5-4 (b). The increase in the leakage current results from the marked increase in the number of grain-boundary trap states in the drain junction. Many carriers released by thermionic-field emission from the trap sites cause the leakage current in the reverse mode to exceed that in the forward mode [18]-[19]. The leakage current is a function of the trap density in the drain junction, which was formulated by Olasupo et al. [18] and Fossum et al. [20]. Besides, the ON currents in both modes are almost identical because the TFT-B is operated in the linear region. Fig. 5-4 (b) also indicates that the measured threshold voltage V_{th} at V_{DS}=12V is 7.91V in the forward mode and 6.60V in the reverse mode. The fall in the V_{th} in the reverse mode results from the avalanche-induced short channel effect [21]. Electrons trapped at the grain boundaries enhance the drain depletion length, effectively shortening the channel length at high drain bias. Furthermore, the transfer characteristics of the TFT-B in both modes become symmetric following NH_3 plasma treatment for 4h because the grain boundaries are effectively passivated, reducing the difference between the numbers of trap states in the drain junctions in both modes. Table 5-1 summarizes several important parameters obtained from the both devices in Fig. 5-4.

The effects of grain boundaries in the drain junction on the performance of devices can be further elucidated from the output characteristics of a single TFT-B in both modes and by comparing variation of V_{th} of devices of TFT-A and TFT-B with the drain voltage. As shown in Fig. 5-5 (a), the kink effect of the non-hydrogenated TFT-B at V_{GS}=20V in the reverse mode appears to be stronger than that in the forward mode. This phenomenon can be ascribed to the drain-induced grain-boundary barrier lowering effect [22]-[23], and the grain-boundary traps induced avalanche generation effect [11]. The former effect is caused by the drain bias V_{DS} modulating the grain-boundary potential barrier heights in the drain junction to form asymmetric barriers. Extra carriers, which are injected from the lowered side of the barriers into the side of the drain junction, increase the drain current as the drain bias increases. The latter effect results from the high local electric fields created by the charged states at grain boundaries of the drain junction. Impact ionization process generates electron-hole pairs, resulting in the absence of saturation in the output characteristics [24]. Rates of carrier ionization, often expressed as an exponential function of the electric field, depend strongly on the electric field of the drain junction [25]. The following section on hot-carrier reliability further elucidates this phenomenon.

Furthermore, the guaranteed linear regions of the forward and reverse modes overlap because of being from the same device. One can see from Fig. 5-5 (b) that the reverse currents enter the saturation mode earlier than the forward currents as the drain voltage increases. This is because the trapped charges at grain boundaries can help the drain voltage to deplete the drain junction. Afterward, the reverse currents enter the kink regions due to the grain boundary barrier lowering effect and the grain-boundary traps induced avalanche generation effect. However, the forward currents remain saturation mode with the drain voltage because of less grain boundaries in the drain junction of forward mode. Besides, the drain currents in both modes are close to each other and significantly increase after NH_3 plasma treatment for 4h. The grain-boundary barrier heights are lowered and more electrons are induced to become conduction carriers.

Fig. 5-6 compares the variation of V_{th} with the drain bias in TFT-A with that in TFT-B. As V_{DS} is varied from 5V to 15V, the V_{th} of the TFT-A and the forward mode of the TFT-B remain almost unchanged, but V_{th} in the reverse mode of the TFT-B decreases as V_{DS} increases. This result implies that V_{GS} must be reduced to maintain a constant drain current as V_{DS} increases, because grain boundaries themselves create space charge regions that enhance the local electric fields in the drain junction. V_{th} evaluated above V_{DS}=5V depends strongly on the grain-boundary locations. However, V_{th} at a low drain bias, such as V_{DS}=0.1V, depends strongly on the number of grain boundaries of the channel region, rather than on the grain-boundary locations. The trapping of charges at the grain boundaries also influences the drain depletion length when a gate and drain voltage are applied.

C. Characterization of hot-carrier reliability of ELA poly-Si TFTs

When excimer laser-crystallized poly-Si TFTs, with and without NH_3 plasma treatment, are under static hot-carrier stress, the behaviors of these devices are degraded. The degradation can be characterized by the creation of trap states and the injection of hot carriers into the gate oxide. Fig. 5-7 shows the variations of the threshold voltage and the maximum transconductance of non-hydrogenated TFT-A and non-hydrogenated TFT-B associated with static hot-carrier stress for 10^4s. In particular, the single TFT-B was first stressed in the forward mode for 10^4s and then stressed in the reverse mode for 10^4s. TFT-A, and TFT-B in the forward mode, are robust against the hot-carrier stress, but the same stress strongly degrades the performance of TFT-B in the reverse mode. Hence the hot-carrier reliability of the laser-crystallized poly-Si TFTs depends strongly on the locations of grain boundaries, rather than on the number of grain boundaries of the channel region. Meanwhile, the number of grain boundaries of the drain junction is critical to the hot-carrier reliability of the devices. While the TFT-B undergoes reverse stress for 10^4s, avalanche multiplication occurs through impact ionization in the drain junction, generating very many electron-hole pairs from the initially broken weak Si-Si bonds at grain boundaries of the drain junction and the more recently broken strong Si-Si bonds in the drain junction [26]. The hot carriers induced damage at the grain boundaries of the drain junction, equivalently introducing a serial resistance into the current path, reducing the ON currents, as evidenced by the serious degradation of nonhydrogenated TFT-B in the reverse mode, as shown in Fig. 5-7. However, the ON currents of the devices with large grains in the drain junction, following the same stress for 10^4s, are either slightly increased or almost unchanged in relation to the initial ON currents. Table 5-2 summarizes several important parameters obtained from the device of Fig. 5-7 (a) stressed in both modes for the each stress time.

Additionally, Fig. 5-8 shows the transfer characteristics of nonhydrogenated TFT-A and the forward mode of nonhydrogenated TFT-B treated with the same stress for 10^4s. Meanwhile, the drain avalanche hot holes are injected into the gate oxide by the positive voltage V_{DG}=10V, slightly reducing V_{th} and slightly increasing the ON current, as clearly shown in the insert in Fig. 5-8 (b). The hot holes screen damage at the grain boundaries of the drain junction, as is also observed by stressing another TFT-B in the reverse mode.

The hot-carrier reliability of devices with grain boundaries in the drain junction is further investigated using another single TFT-B, which was first stressed in the reverse mode for 10^4s and then directly stressed in the forward mode for 10^2s.

Notably, a forward stress for 10^2s does not significantly damage the TFT-B because the drain junction contains large grains in the forward mode. The behaviors of the TFT-B in the reverse mode were characterized continuously after the last 10^2s forward stress. As shown in the insert in Fig. 5-9, the V_{th} at V_{DS}=0.1V increases with the stress time, but the V_{th} at V_{DS}=5V decreases as the stress time increases. This result implies that the hot holes injected into the gate oxide and the trap states created at the grain boundaries of the drain junction screen each other as the gate voltage V_{GS} is swept from low to high at a constant drain voltage of V_{DS}=5V. After the stress is applied for 10^4s, the sub-threshold region in which the channel exhibits weak inversion undergoes a parallel shift to lower V_{GS}, because the hot holes injected into the gate oxide shorten the channel. The hot holes in the gate oxide can be neutralized by attracting channel electrons during the forward stress applied for 10^2s [27]. After the hot holes are released from the gate oxide, the sub-threshold region significantly shifts to higher V_{GS}, as shown in Fig. 5-9. This statement can be further supported in Fig. 5-10. The transfer characteristics of another non-hydrogenated TFT-B first stressed in reverse mode for 10^4s and then directly stress in forward mode for 20s are shown in Fig. 5-10 (a) and (b), respectively. During the last forward stress, as shown in Fig. 5-10 (b), the hot holes were gradually released from the gate oxide, resulting in a parallel shift of subthreshold region toward larger V_{GS} without changing OFF and ON currents in forward mode.

This finding implies that a large number of deep states are generated at the grain boundaries of the drain junction after the first reverse stress has been applied for 10^4s. However, the drain currents at large V_{GS} always decline as the stress time increases because the acceptor-like states created at the grain boundaries of the drain junction are introduced into the channel that exhibits deep inversion. A comparison between the OFF currents reveals the donor-like states, as it does the acceptor-like states located near the midgap. When negative V_{GS} is applied, the OFF current of the neutralization of the hot holes increases more slowly than the initial OFF current at V_{DS}=5V, as shown in Fig. 5-9. The donor-like states are positively charged when negative V_{GS} is applied, so the electric field becomes weaker in the drain depletion region. This effect causes the OFF current that flows after the stress has been applied for 10^4s to be less than the initial OFF current at $V_{GS} < -25$V. This phenomenon is consistent with the results obtained by Brown et al. [28].

Furthermore, the curves at V_{DS}=5V in Fig. 5-9, the minimum I_{DS} at its corresponding V_{GS} which represents the flat-band voltage V_{FB} [29], are 1.51×10^{-10} A at $V_{GS}=-4.8$V for the initial curve, 2.06×10^{-10} A at $V_{GS}=-4.1$V for the 10s curve, 2.29×10^{-10} A at $V_{GS}=-5.5$V for the 10^4s curve, and 3.07×10^{-10} A at $V_{GS}=-4.8$V for the curve of hot holes neutralization, respectively. The increase in V_{FB} from -4.8V to－4.1V is due to the trapping of electrons in the acceptor-like trap states. The negatively charged states enhance the electric field in the drain depletion region, leading to the OFF current approaching to maximum values following 10s reverse stress. As the stress time increases to 10^4s, the V_{FB} decreases to－5.5V due to the injection of hot holes into the gate oxide. When negative V_{GS} is applied, the positive charges in the gate oxide effectively shield the electric field which originates from the potential difference between the gate and drain. However, the V_{FB} and the OFF current at V_{DS}=5V in the curve of hot holes neutralization, including the minimum I_{DS}, increase as compared to the 10^4s curve, because the neutralization of the positive charges enhances the electric field again with the application of negative V_{GS}. On the other hand, the ON current accompanied the reduction of transconductance $G_{m\ max}$ can be ascribed to a large number of band tail states created in the upper half of energy gap.

NH_3 plasma treatment can destroy the excellent hot-carrier reliability of devices with large grains in the drain junction. Fig. 5-11 shows the variations of ΔV_{th} and $\Delta G_{m\ max}/G_{m\ max,i}$ with the stress time for devices that have been hydrogenated. One can see that hot-carrier reliability of hydrogenated TFT-B in reverse mode is effectively promoted. The high local electric fields created at grain boundaries of the drain junction can be effectively reduced because atomic hydrogen ties up the dangling and strained bonds during hydrogenation, reducing the number of carriers trapped at the grain boundaries. The Si-H bonds of the shallow tail states are easily bound and are easily broken because they have a small binding energy [17]. Therefore, the behaviors associated with the degradation of devices differ from that of non-hydrogenated devices. Fig. 5-11 exhibits the tendency to degrade. The degradation of devices after hydrogenation becomes independent of the original distribution of the grain boundaries in the channel region. Fig. 5-12 shows the transfer characteristics of hydrogenated TFT-B measured in (a) forward and (b) reverse modes before and after hot-carrier stress was applied for 10^4s. In fact, the hydrogenated devices of TFT-A and TFT-B after being stressed exhibit increased OFF currents, decreased ON currents, and reduced sub-threshold slopes. The mechanism of device degradation involves the breaking of many Si-H bonds, creating the shallow tail states in the upper half of the band gap. Additionally, the hump effect appears in the sub-threshold region, especially after the channel region is asymmetrically damaged by the hot-carrier stress, as shown in Fig. 5-12 (b). This result is also consistent with the observations of hydrogenated TFT-A and hydrogenated TFT-B in forward mode. The hump effect originates in the non-uniformity of the passivation of grain boundaries throughout the channel region. The center of the channel region has different turn-on characteristics from the two sides of the region because the lateral diffusion of hydrogen activates the trap states.

5.4 CONCLUSION

This study reports the effects of grain boundaries on the performance and hot-carrier reliability of the laser-crystallized poly-Si TFTs with and without hydrogenation. The hot-carrier reliability of the devices strongly depends on the locations of grain boundaries rather than on the number of grain boundaries of the channel region. Grain boundaries in the drain junction increase the leakage current; cause the threshold voltage to decline as the drain bias increases; enhance the kink effect in the output characteristics, and strongly degrade the device performance under static hot-carrier stress. These effects are attributable to the generation of high local electric fields from the surface roughness and the trapping of charges at grain boundaries of the drain junction. NH_3 plasma treatment can effectively passivate the grain boundaries that are randomly distributed in the channel region. However, hydrogenation introduces the hump effect in the sub-threshold region, and causes a tradeoff between the electrical characteristics and the hot-carrier reliability of the laser-crystallized poly-Si TFTs.

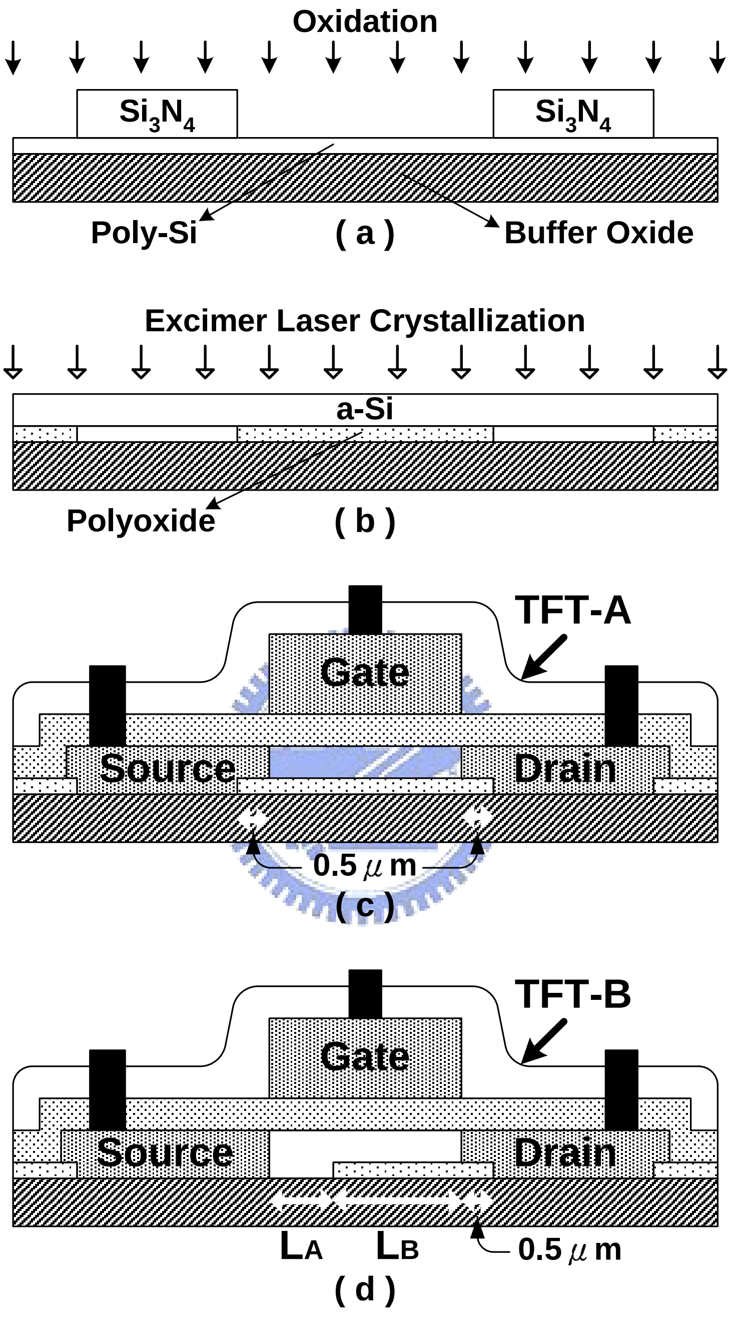
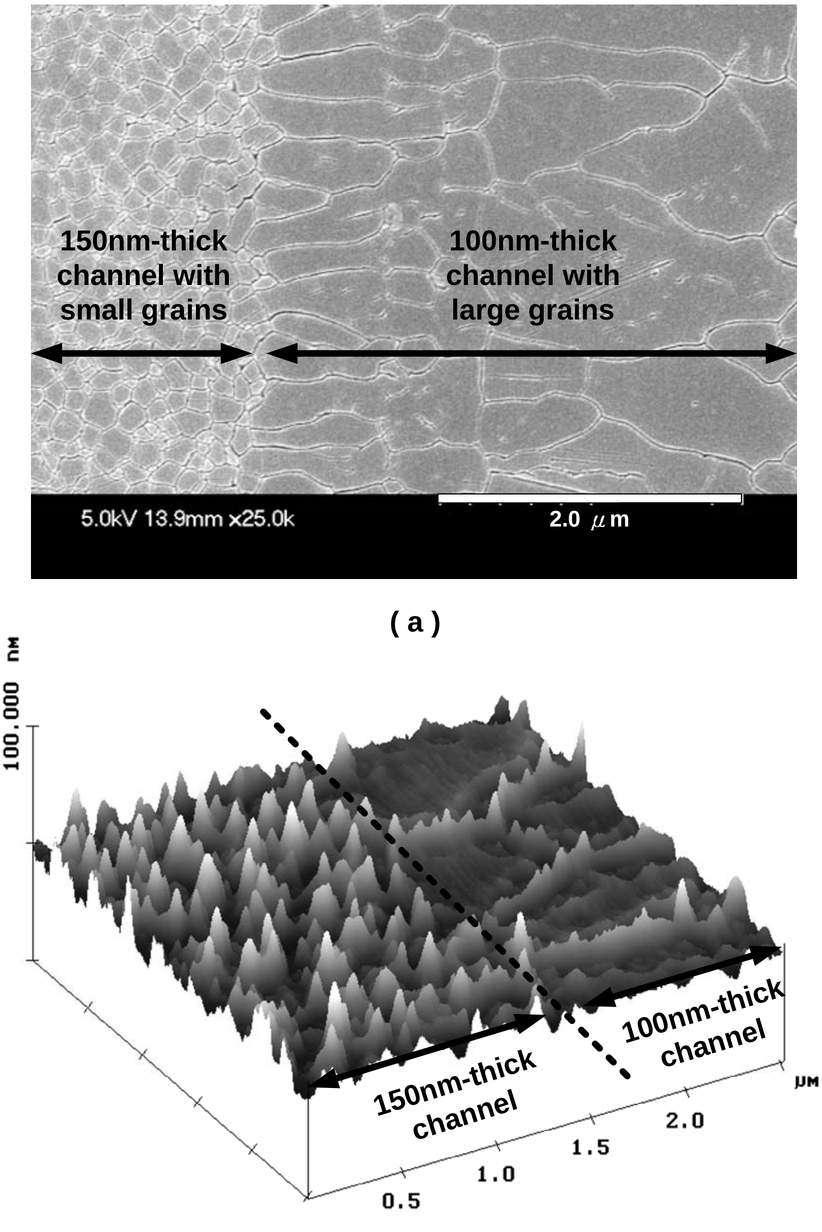


Fig. 5-1 Key process flows for fabricating self-aligned poly-Si TFTs. TFT-A, shown in Fig (c), has large grains throughout its channel region. TFT-B, shown in Fig (d), has large and small grains on both sides of its channel region.



(a)

(b)

Fig. 5-2 (a) SEM photograph of the excimer laser-crystallized poly-Si film after Secco etching and (b) AFM image of the surface roughness of the excimer laser-crystallized poly-Si film near where the 150 nm and 100 nm thick regions are connected.

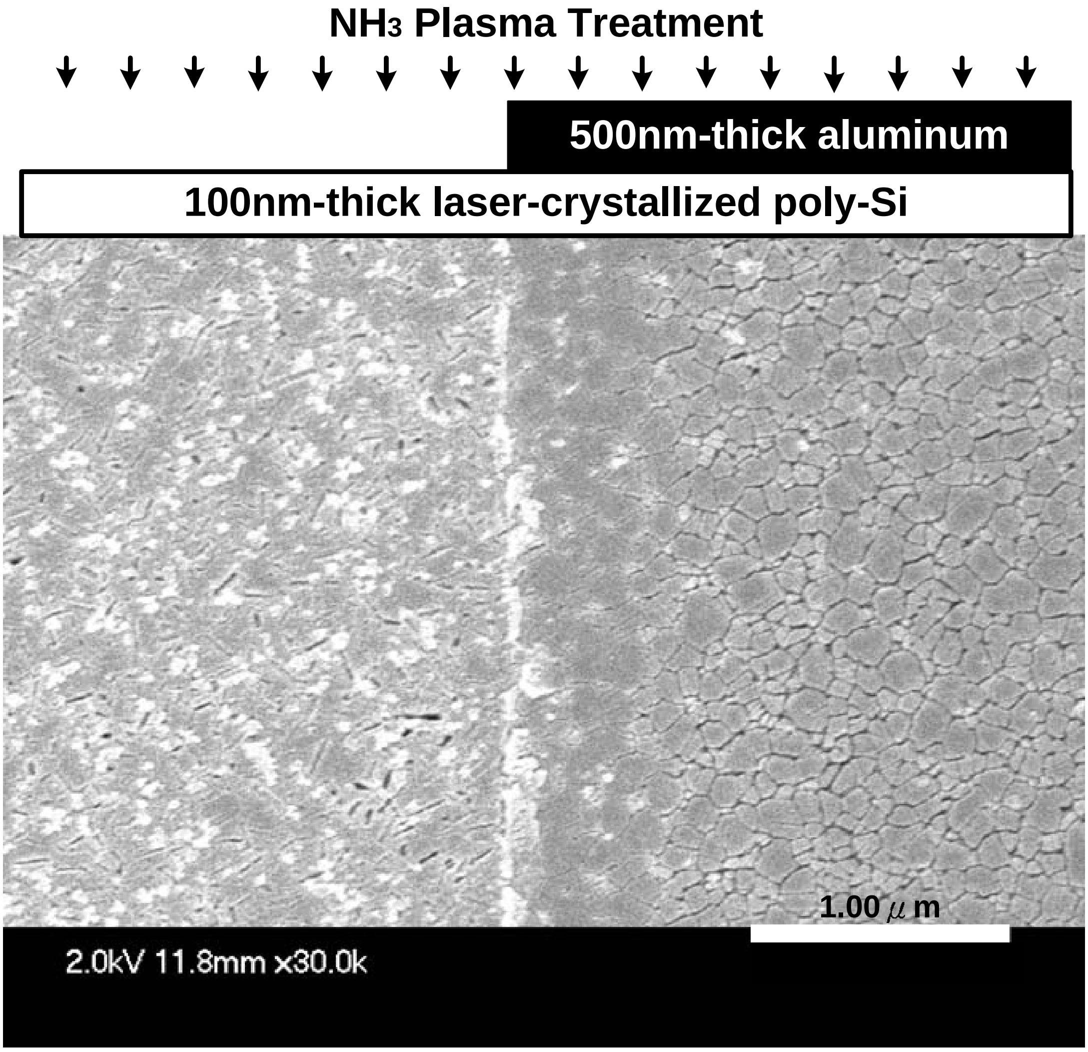


Fig. 5-3 SEM photograph of an excimer laser-crystallized poly-Si film with and without NH_3 plasma treatment after Secco etching. A 100 nm thick laser-crystallized poly-Si film was selectively treated with NH_3 plasma using aluminum patterns as hard masks, shown schematically at the top.

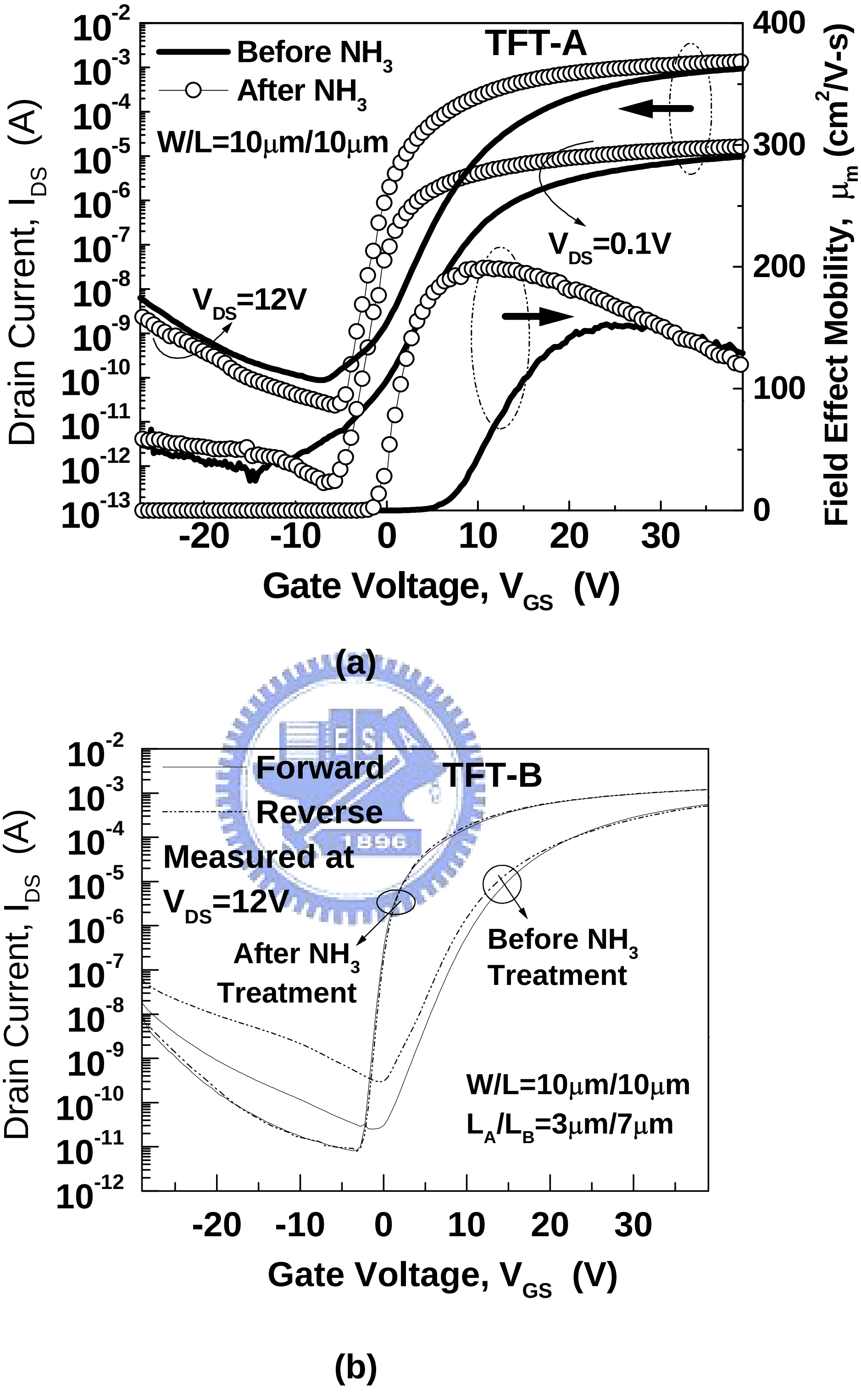
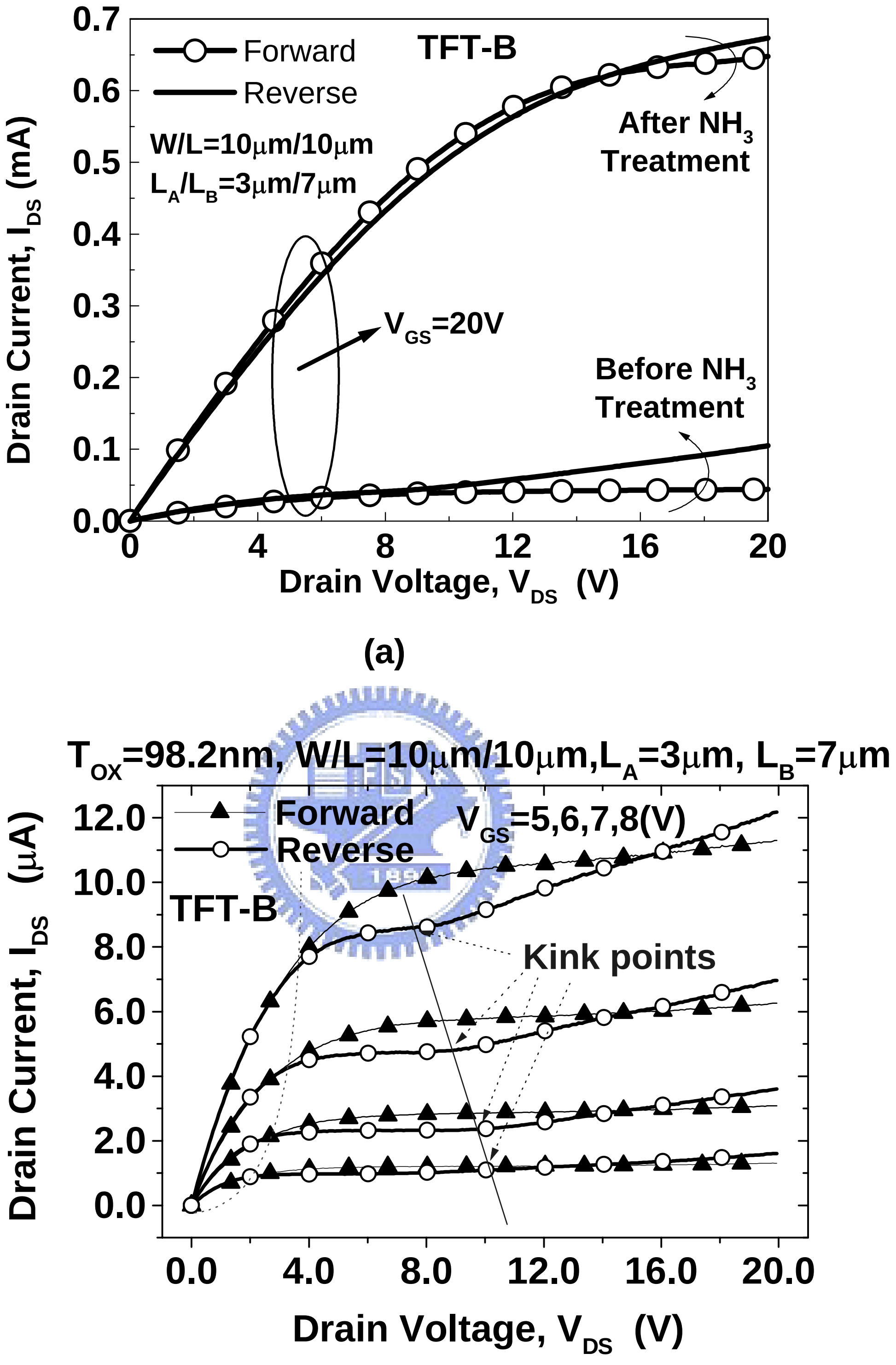


Fig. 5-4 Transfer characteristics of (a) a device of TFT-A measured before and after NH_3 plasma treatment for 2h and (b) a single device of TFT-B measured in forward and reverse modes before and after NH_3 plasma treatment for 4h.

Table 5-1 Summary of values of several important parameters obtained from the devices in Fig. 5-4.

W / L= 10μm / 10μm L_A / L_B= 3μm / 7μm	TFT-A		TFT-B			
	Before NH_3	After 2h NH_3	Before NH_3		After 4h NH_3	
			Forward	Reverse	Forward	Reverse
Threshold voltage at V_{DS}=0.1V (V)	5.51	-0.81	7.74	8.03	-0.38	-0.37
Threshold voltage at V_{DS}=12V (V)	4.04	-1.26	7.91	6.60	-0.36	-0.25
Field-effect mobility (cm^2/V-s)	154	199	101	102	149	148
On/Off current ratio at V_{DS}=12V ($\times 10^7$)	1.12	5.92	2.27	0.18	15.1	15.5



(a)

(b)

Fig. 5-5 Output characteristics of (a) a single TFT-B measured in the forward and reverse modes before and after NH_3 plasma treatment for 4h and (b) a single nonhydrogenated TFT-B measured in forward and reverse modes.

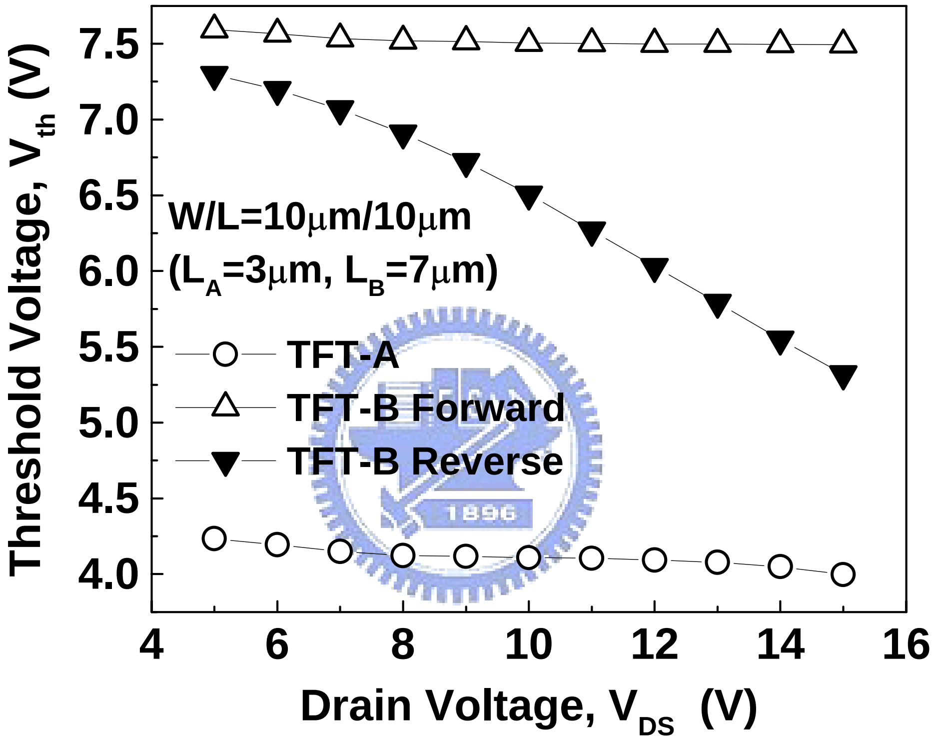
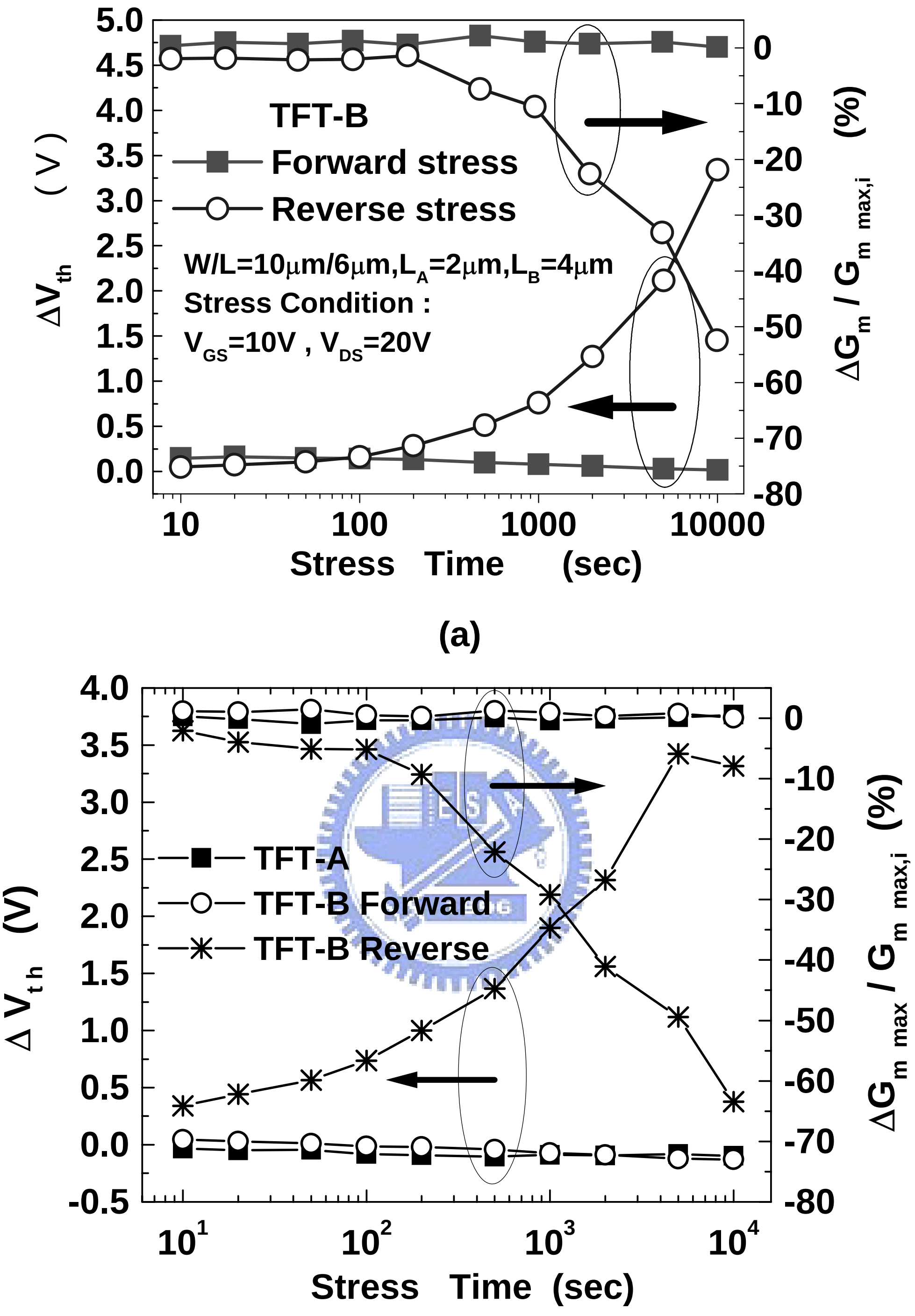


Fig. 5-6 Variations of threshold voltage V_{th} with the drain bias V_{DS} for non-hydrogenated TFT-A and non-hydrogenated TFT-B in both modes.



(a)

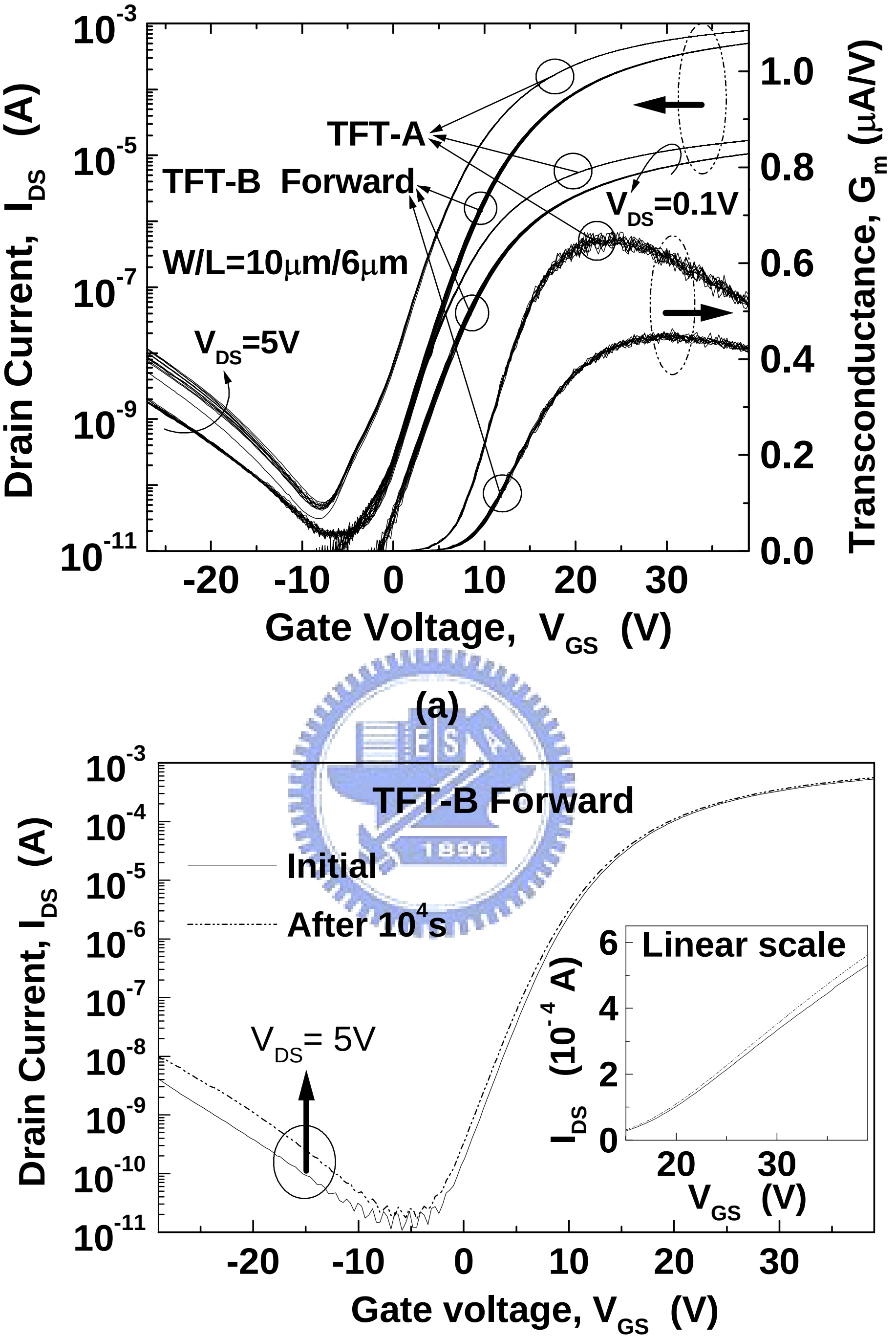
(b)

Fig. 5-7(a) & (b) Degradations of both the threshold voltage and the maximum transconductance of nonhydrogenated devices with stress time. ΔV_{th} and $\Delta G_{m\,max}/G_{m\,max,i}$ were evaluated at V_{DS}=0.1V for the each stress time. The single TFT-B was first stressed in forward mode and then stressed in reverse mode.

Table 5-2 Summary of values of several important parameters obtained from the device of Fig. 5-7 (a) stressed in both modes for the each stress time.

Forward Stress Time（s）	V_{TH}（V）	S（min）（V/DEC）	Gm（max） (nA/V)	I_{ON} / I_{OFF}（$\times 10^6$）
0	8.24902	2.50153	408.75000	21.87007
10	8.39628	2.60531	410.33333	22.31463
20	8.41321	2.61485	412.96667	22.16763
50	8.39913	2.62026	411.80000	22.36367
100	8.39084	2.57205	414.03333	21.01714
200	8.38096	2.62988	411.18333	21.09545
500	8.34752	2.62521	417.78333	21.63309
1000	8.32766	2.64029	413.25000	20.81927
2000	8.30960	2.65830	411.81667	20.44129
5000	8.27786	2.64698	413.18333	19.88340
10000	8.26609	2.66577	409.50000	20.45775

Reverse Stress Time（s）	V_{TH}（V）	S（min）（V/DEC）	Gm（max） (nA/V)	I_{ON} / I_{OFF}（$\times 10^6$）
0	8.22387	2.70475	416.28333	2.59534
10	8.27274	2.70650	408.21667	2.18507
20	8.29787	2.70009	408.61667	2.10669
50	8.32937	2.71565	407.33333	2.05140
100	8.38542	2.73092	407.73333	1.95437
200	8.50867	2.75401	410.60000	1.86242
500	8.73665	2.80913	385.65000	1.72526
1000	8.98498	2.83851	372.40000	1.61939
2000	9.49613	2.90730	322.30000	1.56319
5000	10.33909	3.04985	278.43333	1.37228
10000	11.56534	3.15206	198.03333	1.38774



(a)

(b)

Fig. 5-8 Transfer characteristics of (a) non-hydrogenated TFT-A and TFT-B in forward mode and (b) another non-hydrogenated TFT-B in forward mode before and after hot-carrier stress was applied for 10^4s. Shown in Fig. 5-8 (b), the inset presents a linear scale to show ON currents.

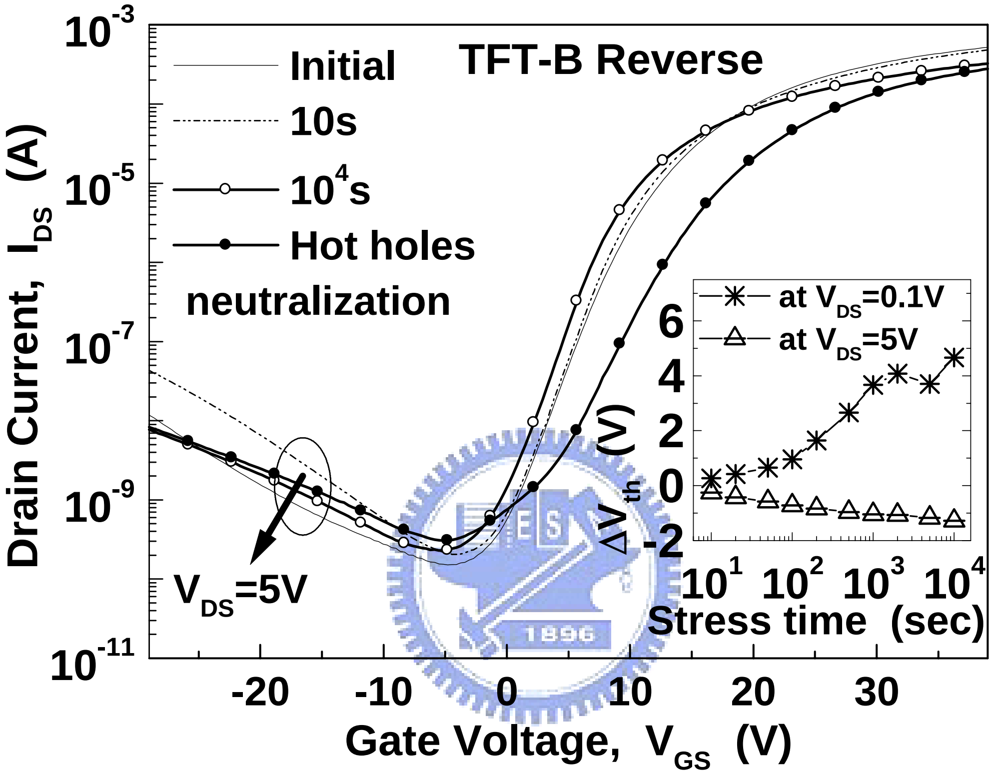


Fig. 5-9 Transfer characteristics of non-hydrogenated TFT-B measured in the reverse mode before and after reverse stress were applied for 10^4s. The curve associated with the neutralization of hot holes was plotted after the hot holes were released from the gate oxide by final forward stress applied for 10^2s. The inset plots ΔV_{th} with the stress time at V_{DS}=0.1V and V_{DS}=5V, respectively.

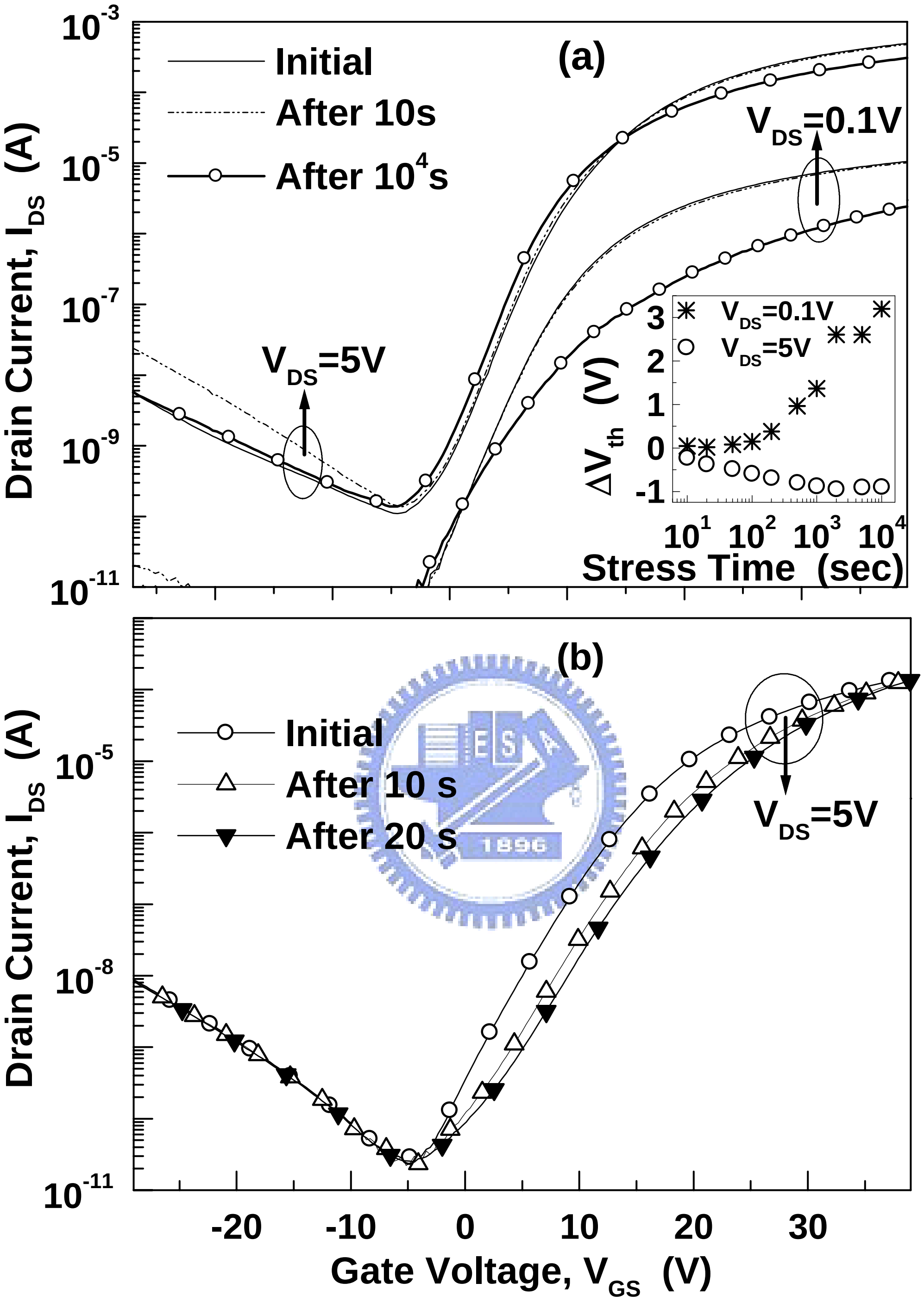


Fig. 5-10 Transfer characteristics of another non-hydrogenated TFT-B first stressed in reverse mode for (a) 10^4s and then directly stress in forward mode for (b) 20s. During the last forward stress, as shown in Fig. 5-10 (b), the hot holes were gradually released from the gate oxide, resulting in a parallel shift of subthreshold region toward larger V_{GS} without changing OFF and ON currents.

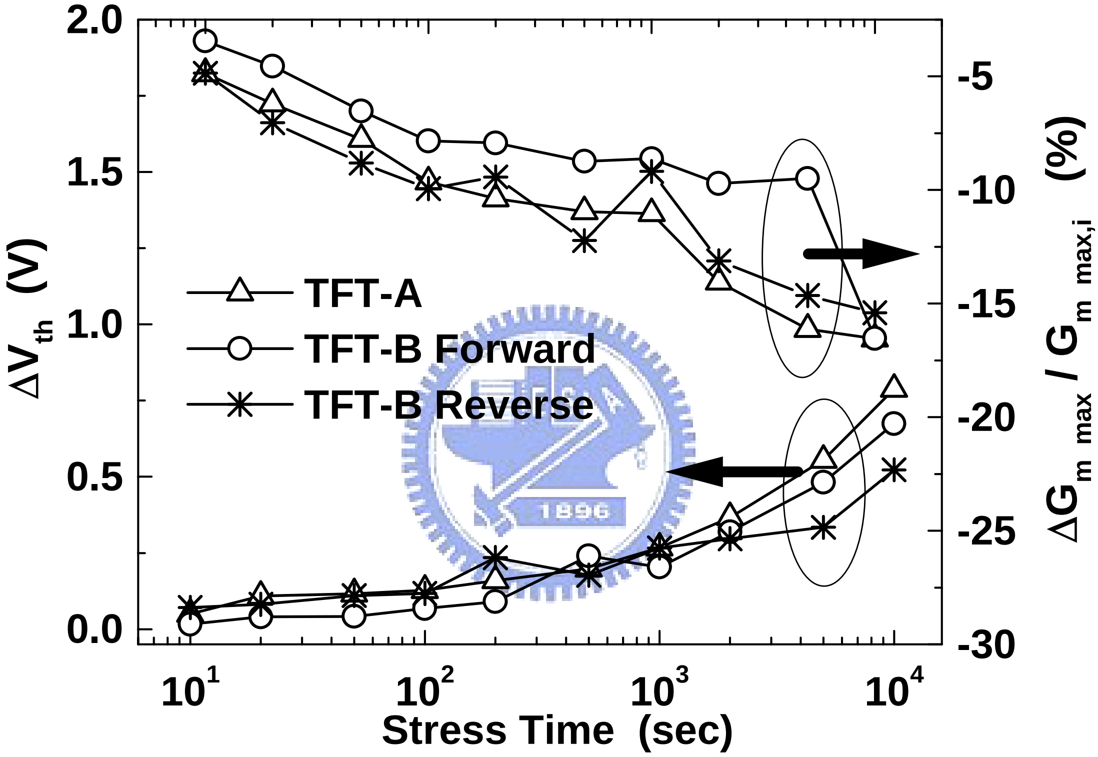
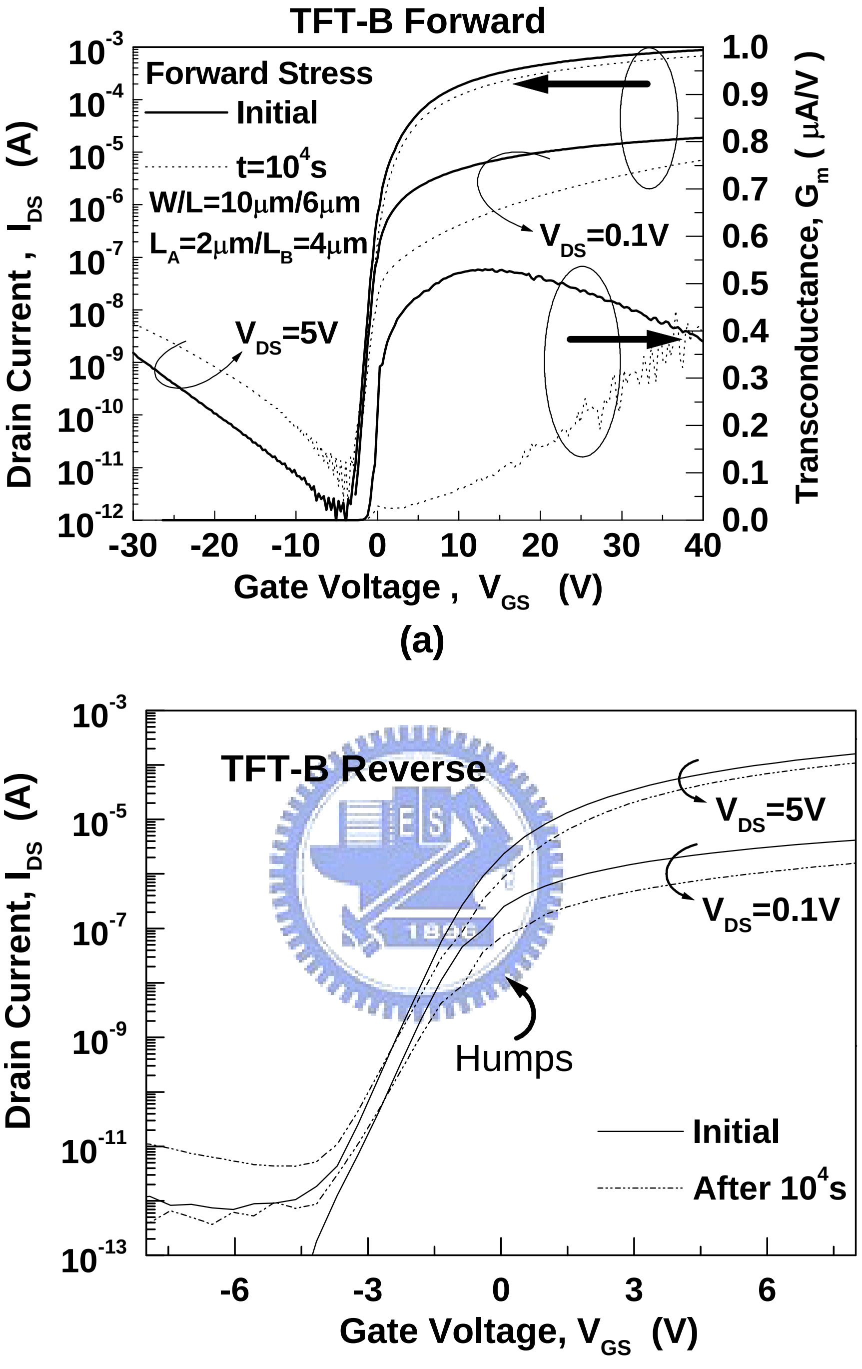


Fig. 5-11 Degradations of both threshold voltage and maximum transconductance of hydrogenated devices with stress time. These devices were treated with NH_3 plasma for 4h, and ΔV_{th} and $\Delta G_{m\ max}/G_{m\ max,i}$ were evaluated at V_{DS}=0.1V for each stress time. Two devices of TFT-B were stressed in forward and reverse modes, respectively.



(a)

(b)

Fig. 5-12 Transfer characteristics of hydrogenated TFT-B measured in (a) forward and (b) reverse modes before and after hot-carrier stress was applied for 10^4s. The devices were treated using NH_3 plasma for 4h. The hump effect in the sub-threshold region is observed before and after the hot-carrier stress is applied.

Chapter 6

Conclusions and Future Works

6.1 CONCLUSIONS

In this thesis, excimer laser crystallized poly-Si TFTs whose grain boundaries are artificially controlled using three individual temperature modulation techniques are fabricated and then characterized. These novel crystallization methods are first reported, and are crucial techniques in the manufacture of LTPS-TFT LCD or OLED. The importance of these techniques in this thesis is concluded as follows.

First, as far as manufacturing cost is concerned, how to reduce the mask counts in TFT array process is critical. Four masks are essential to fabricate top-gated poly-Si TFTs, but no four-mask process associated with a temperature gradient of laser crystallization is proposed to produce lateral-grained poly-Si TFTs. In chapter 2, four-mask-processed poly-Si TFTs are fabricated using excimer laser crystallization of edge-thickened a-Si islands. When the molten silicon films commence solidifying, the grains are enlarged by a thermal gradient established across the channel width. Meanwhile, the surface tension-induced shrinkage effect of multi-pulse excimer laser irradiation on pre-patterned α-Si islands is successfully eliminated through the edge-thickened method. Therefore, field-effect mobility of the TFTs is promoted, and this method can make uniform the performance of TFTs due to a regular arrangement of the channel grains by the lateral modulation of temperature. The proposed TFTs with divided channel units can meet the application of various gate widths, and their performances depend on the grain-boundary control of each channel unit. Hence, how to further control the quality of a channel unit is the major concern of the proposed TFTs.

Second, a novel seeding technique is being developed to produce large single crystal silicon areas. In chapter 3, we have been trying to crystallize the a-Si films into single crystal silicon by the contact seeding technique. Prior to fabricating TFTs on transparent glass substrate, a contact seeding process with silicon substrate is performed to produce laser-crystallized silicon films on buffer SiO_2 layer. However, there have been no the seeded silicon grains observed using this process. The major cause is that the surface of the contacted bulk silicon cannot be melted during excimer laser irradiation. The a-Si film is fully melted on the un-melted silicon so that many clear pinholes or voids appear due to the different adhesions of the molten silicon on buffer SiO_2 and silicon substrate.

Third, a LOCOS-like process is created to fabricate high-performance poly-Si TFTs. In chapter 4, the n- and p-channel poly-Si TFTs fabricated by this process are characterized. High field-effect mobility is obtained when the channel length is cut short. Some effects, such as self-heating and avalanche multiplication, are found due to a floating substrate. We also find that boron activation during 600℃ will introduce many hole traps into the gate oxide when the gate is poly-Si gate. Additionally, in chapter 5, the electrical characteristics of the laser-crystallized poly-Si TFTs with various numbers of grain boundaries throughout the channels and in the drain junction are investigated. We find that there is a great impact on the performance and hot-carrier reliability of laser-crystallized poly-Si TFTs because of grain boundaries located in the drain junction. Different numbers of grain boundaries throughout the channels bring a variation on the devices being operated in the linear mode. Different numbers of grain boundaries in the drain junction bring an impact on the devices being operated in the depletion mode of saturation and OFF states.

High-performance laser-crystallized poly-Si TFTs have been fabricating by several techniques, among them in this thesis crystallizing the edge-thickened a-Si islands, seeding a large single-crystal silicon area, and carrying out a LOCOS-like process.

6.2 FUTURE WORKS

There are some intriguing studies about the fabrication of LTPS TFTs worthy to be further investigated as follows.

1) The continuous wave (CW) laser is difficult to be widely employed because

additional masks are necessary prior to the CW crystallization. We believe that the edge-thickened method in chapter 2 can be applied to fabricate a high-performance poly-Si TFT with a neck to grow a single crystal of Si by appropriately modulating CW laser scanning in the source-drain direction, since the edge-thickened α-Si active islands are very robust against laser-induced distortion. Even if some residual a-Si uncrystallized by laser irradiation are left in the edges following the anisotropic poly-Si plasma etching, the performance of the devices will not be affected due to quite different turn-on characteristics in the edges and out of the edges.

2) The seeding technique proposed in chapter 3 can be further investigated using improved facilities, such as good vacuum chamber, and high energy density laser. If the silicon seeds and the a-Si films are simultaneously melted, large single-crystal silicon areas will be possibly produced. Different surface orientations of device channels affect the performance of devices. Only seeding technique can well control the orientation of laser-crystallized silicon films. On the other hand, choosing a material to match the lattice of laser-crystallized silicon films is worthily tried for this seeding technique.

3) The devices with T-shape gates to release the lateral electric field have not been extensively studied. We think that T-gated poly-Si TFTs are possibly

fabricated using selectively liquid phase deposition (LPD) method. The liquid phase deposited SiO_2 cannot be deposited onto some metal layers, photoresist layer, and silicon nitride (Si_3N_4) layer. The selective characteristics are suitable for creating T-shaped gated device.

4) High quality silicon nitride (Si_3N_4) films have been developing to be deposited below 600 ℃. Using Si_3N_4 as hard masks is easy to realize various TFT structures at low temperature.

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CHAPTER3

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Laser Annealing Techniques for LTPS TFTs and Influence of Grain Boundaries on Electrical Characteristics and Hot-carrier Reliability of Poly-Si TFTs

PUBLICATION LISTS

Journal Papers

1. **Tien-Fu Chen**, Ching-Fa Yeh, and Jen-Chung Lou, "Investigation of Grain Boundary Control in the Drain Junction on Laser-Crystalized Poly-Si Thin Film Transistors," **IEEE Electron Device Lett**., vol. 24, pp. 457-459, July 2003.
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3. **Tien-Fu Chen**, Ching-Fa Yeh, Chun-Yen Liu, and Jen-Chung Lou, "A Novel 4-mask Processed Poly-Si TFT Using Excimer-Laser Crystallization of an Edge-Thickened α-Si Island," **IEEE Electron Device Lett**., vol. 25, pp. 396-398, June 2004.
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2. Ching-Fa Yeh, **Tien-Fu Chen**, Yueh-Chuan Lee, Chien-Hung Liu, Shyue-Shyh Lin, "Smart Dielectrics of Fluorinated silicon Glass Prepared by Liquid Phase Deposition Method" in Proc. **SPIE** Vol. 4592, pp.43-54, 2001.
3. Ching-Fa Yeh, **Tien-Fu Chen**, and Jen-Chung Lou, "Effects of Grain Boundary in the Drain Depletion on Excimer Laser-Annealed Poly-Si TFTs before and after NH_3 Plasma Treatments," in **AMLCD** Tech. Dig., 2003, pp.173-176.
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Patents

1. Ching-Fa Yeh, **Tien-Fu Chen**, 製作複晶矽薄膜電晶體之方法，送審中。
2. Ching-Fa Yeh, **Tien-Fu Chen**, and Jen-Chung Lou, 低溫多晶矽薄膜電晶體主動層之雷射再結晶方法，已經通過經濟部智慧財產局審核，目前公告中。
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