A Low-Dropout Regulator With Smooth Peak Current Control Topology for Overcurrent Protection

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***Abstract*—The proposed low-dropout (LDO) regulator with a smooth peak current control (SPCC) circuit can be simultaneously controlled by using an error amplifier to regulate output voltage and a peak current controller as a means to limit its current level. The SPCC circuit can be switched smoothly between these two control mechanisms by detecting the information of load current and the dropout voltage. Measured results show that overcurrent protection can make the pass device operate as a current source while the load current exceed the peak current level. Moreover, the control mechanism can return to error amplifier control when load current becomes smaller than the limiting current, thus ensuring output voltage to be close to the rated value. Output voltage is stable and varies smaller than 15 mV when a 160 mA load current step or a 2 V supply voltage step is placed on this LDO regulator.**

***Index Terms*—CMOS analog ICs, low-dropout (LDO) regulator, MOSFET ICs, overcurrent protection (OCP).**

I. Introduction

IN THE modern technology, power management is greatly demanded for portable devices, especially when concerning the volume and the power consumption. Low-dropout (LDO) regulators are widely used as power management ICs in portable communication systems [1], since they occupy a small chip area and can convert Li-ion battery voltage to a low-noise and high-precision voltage to noise-sensitive analog blocks for ensuring high performance [2], [3]. Owing to the increased level of the integration in System on Chip (SoC) system, the stability and fast transient response of LDO regulators [4]–[7] are essential over a wide range of load current using high-gain error amplifier with a feedback topology. In addition, the LDO regulators require extremely small quiescent currents to obtain higher current efficiency.

Generally speaking, the design of LDO regulators usually utilizes a pass device, which typically uses a p-type MOSFET for LDO voltage. It aims to provide large load current and an error amplifier to regulate output voltage. However, an instant overload condition may damage the pass device due to large load current and heat not dissipated in the chip. Therefore, the design of overcurrent protection (OCP) function [8], [9] is important and frequently implemented in LDO regulators to prevent overcurrent flowing through the pass device and damaging the chip. The protection functions of the pass device can reduce influence on the SoC system, and thus, allow regulators to safely supply voltage to SoC applications. In general, OCP circuit cutoff the negative feedback loop of the regulator, inhibiting the regulator's capacity to regulate the output voltage [10]. That is, output voltage is decreased to the voltage level, which is equal to the value of load resistance multiplied by the limiting current. Hence, LDO has a lower possibility of being destroyed from the overload current. The proposed OCP topology with the smooth peak current control (SPCC) circuit still reserves the feedback loop, but it likewise lowers negative gain. As a result, the SPCC circuit do not only make the current flow through the pass device in a persistent limiting level, but also smoothly switches the control mechanism between the OCP topology and the error amplifier control.

Manuscript received June 23, 2009; revised August 20, 2009 and October 20, 2009. Current version published May 7, 2010. This work was supported by the National Science Council, Taiwan, under Grant NSC 97–2221-E-009–172. Recommended for publication by Associate Editor U. K. Madawala.

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Digital Object Identifier 10.1109/TPEL.2010.2040197

II. Concept of Proposed OCP

The foldback limit is the most common OCP topology and controls the limiting current level by depending on the output voltage until the pass device is turned off [10]. When load resistance is decreased to cause load current exceed the predefined peak current level, the OCP topology starts to limit the output current. The output voltage drops, as shown in Fig. 1(a), since the load current is larger than the peak current level. Next, the drop of output voltage would reduce the peak current level. This OCP topology then reduces the limiting current level according to the drop of output voltage and allows the pass device operate in the cutoff region. Therefore, when short-circuit fault occurs, the foldback limit expends smaller power consumption because of the small current limit level. However, even if the load current is decreased to a safe region, the error amplifier would be difficulty returning to regulate the LDO regulator due to the small current limit level. As a result, the LDO regulator needs to be restarted to regulate the output voltage.

In addition, when the load current is larger than the peak current level, LDO regulators can be controlled by the error amplifier to regulate the output voltage, as well as OCP topology to limit the current of pass device, as shown in Fig. 1(b). However, the current of pass device and the output voltage are unregulated, since the operation switched between the two control mechanisms. This method may consume more power and reduce efficiency due to a larger average current when the short-circuit fault occurs. As such, the constant current limiting can be used for OCP topology. When the overload happens, the current of pass device can be regulated at a predefined constant level, as shown in Fig. 1(c). However, when the load current is decreased, the error amplifier would replace the constant current limiting mechanism to regulate the output voltage. Meanwhile,

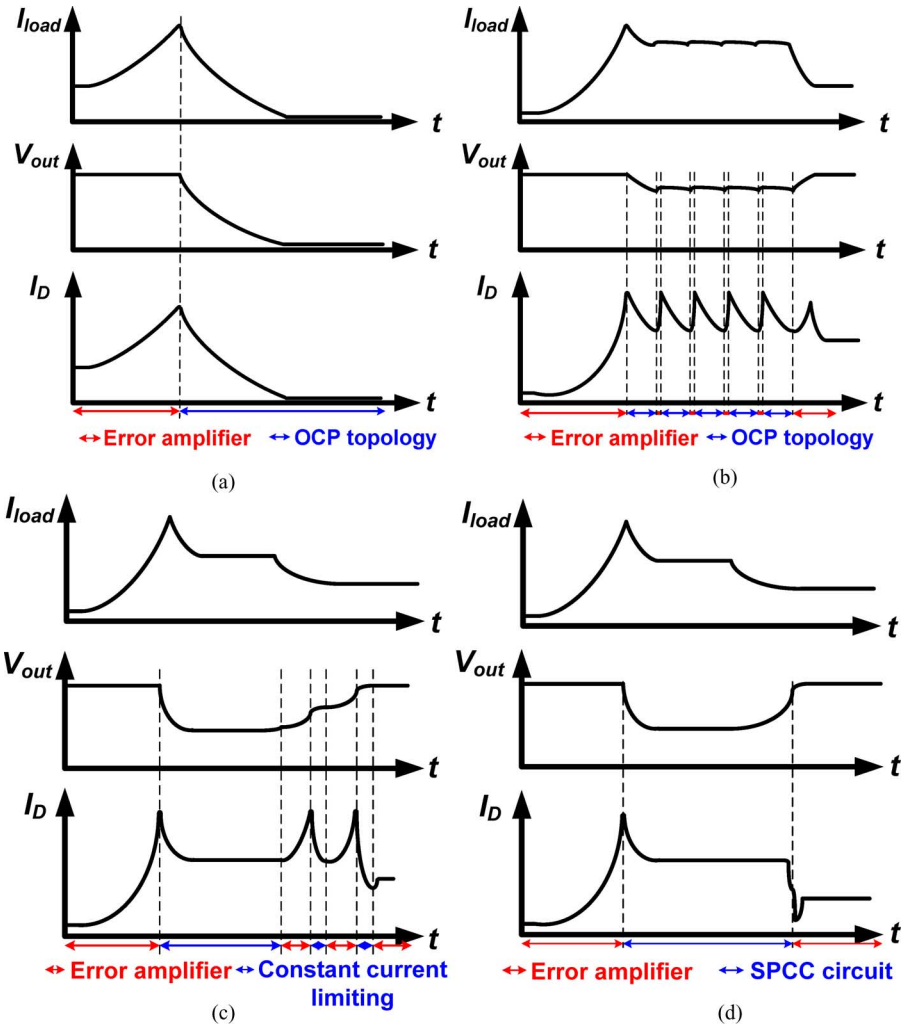

Fig. 1. Control mechanism switches between the error amplifier control and the OCP topology. (a) Foldback limiting decreases the current limit level according to the drop of output voltage. (b) LDO regulator simultaneously controlled by the error amplifier control and the OCP topology causes unregulated the current of pass device and the output voltage. (c) Constant current limiting and the error amplifier will in turn control and make some oscillation before the output voltage reaches to the target voltage. (d) LDO regulator smoothly exchanges the control mechanism between the error amplifier control and the SPCC circuit.

the current of pass device could be quickly pulled up by the error amplifier because the output voltage is smaller than the target voltage. Thus, the constant current limiting mechanism would again take the place of the error amplifier to control the LDO regulator. Therefore, the control mechanism would oscillate between these two control methods and cause large voltage ripple before the output voltage reaches to its rated voltage. In this paper, the proposed SPCC circuit utilizing the drop voltage and the current flowing through the pass device is proposed to determine the proper control mechanism between the error amplifier control and the SPCC circuit. These two control mechanisms can be smoothly exchanged. Adequate waveforms of output voltage, load current, and the current flowing through the pass device are depicted in Fig. 1(d). In other words, the proposed LDO regulator can avoid damage on the chip from the overload as well as smoothly return back to the error amplifier control to obtain a regulated output voltage if the load current is again decreased and is smaller than the current limit level.

The structure of the proposed LDO regulator with the SPCC circuit is illustrated in Fig. 2. An SPCC circuit with the peak

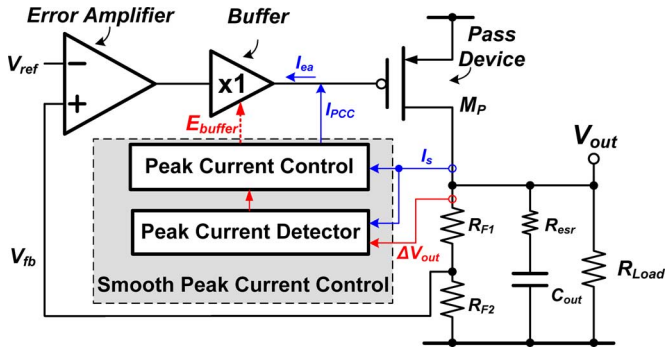

Fig. 2. Structure of proposed LDO regulator with SPCC circuit.

current detector and the peak current control utilizes a sensing current to define peak current level. Meanwhile, the intermediate buffer is utilized to compensate the LDO regulator. In addition, the reference voltage $V_{\rm ref}$ is integrated in the LDO circuit and the signal $E_{\rm buffer}$ operates as a condition indicator. When the sensing current exceeds the peak current level, the signal $E_{\rm buffer}$

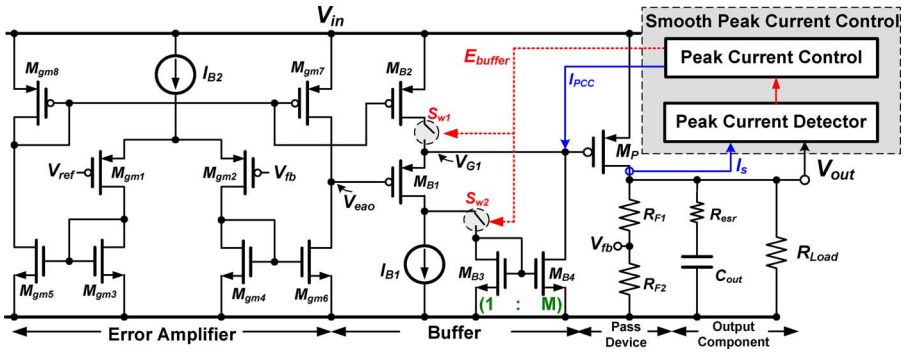

Fig. 3. Schematic of proposed LDO regulator composed of the error amplifier, the buffer, the pass device, and the SPCC circuit.

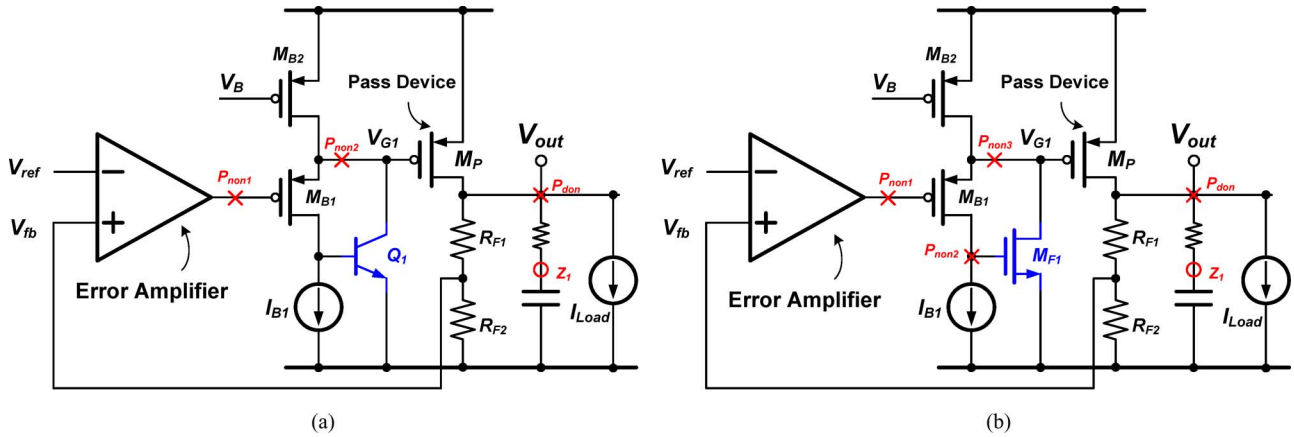

Fig. 4. (a) Traditional buffer utilizes a source follower with a current amplifier by a shunt feedback n-p-n BJT Q_1. (b) Shunt feedback device can be implemented by a n-type transistor M_{F1}, but the feedback loop results in another high-frequency pole $p_{\rm non2}$ near the nondominant pole $p_{\rm non1}$, and thereby, the damping factor is increased and affects the system stability.

generated by the peak current detector would enable the peak current control to source a suitable current $I_{\rm PCC}$. Moreover, the buffer gain would be decreased. Therefore, the gate-source voltage of pass device would be clamped by the negative feedback loop from current sensing technique. Simultaneously, the drop of output voltage will be added into the peak current detector and prevent an unregulated situation. When the load current is decreased, the pass device remains controlled by the peak current control. Until the output voltage is close to the settled voltage and the load current is in the normal region, the signal $E_{\rm PCC}$ will reactivate the buffer stage and disable the peak current control. Then, the error amplifier will take the place of the peak current control to regulate the output voltage. As a result, the two control mechanisms will be smoothly exchanged, and the current of pass device will be decreased to a safety region. This is done to prevent the chip being damaged due to overload condition.

III. Circuit Implementation

A. Structure of LDO Regulator

The proposed LDO regulator composed of the error amplifier, the buffer, the pass device, and the SPCC circuit is illustrated in Fig. 3. When load current is lower than peak current level, the two switches, S_{w1} and S_{w2}, are shorted and the intermediate buffer is enabled to transmit the error signal from the error amplifier to regulate output voltage. The intermediate buffer is utilized to move the pole formed by the output resistance of error amplifier and the capacitance of pass device (M_P) to high frequencies. In addition, the buffer brings in another high-frequency pole. In contrast, the traditional buffer utilizes a source follower with a current amplifier through the use of a shunt feedback n-p-n bipolar junction transistor (BJT) Q_1 [11], as depicted in Fig. 4(a) to minimize the power consumption and size of the source follower. Unfortunately, the generic CMOS process only provides single-well process without permitting the use of n-p-n BJT devices. Therefore, in a single-well CMOS process, the shunt feedback device can be alternately implemented using an n-type transistor M_{F1} [12] as illustrated in Fig. 4(b). However, since the resistance $R_{\rm oea}$ is nearly equal to R_o and the gate capacitances of the transistor M_{B1} and M_{F1} are almost equivalent, the feedback loop would result to the emergence of a high-frequency pole $p_{\rm non2}$ near the nondominant pole $p_{\rm non1}$. Hence, the damping factor is increased and causes the system to become unstable. In the proposed design, the diode connected transistor M_{B3} is used to reduce the resistance at the drain of M_{B1} equal to $1/g_{MB3}$ a value, which is much smaller than R_o. As a result, this nondominant pole is moved to high frequencies, thus ensuring system stability. Moreover, the feed-forward transistor M_{B2} is controlled by the error signal and can enhance

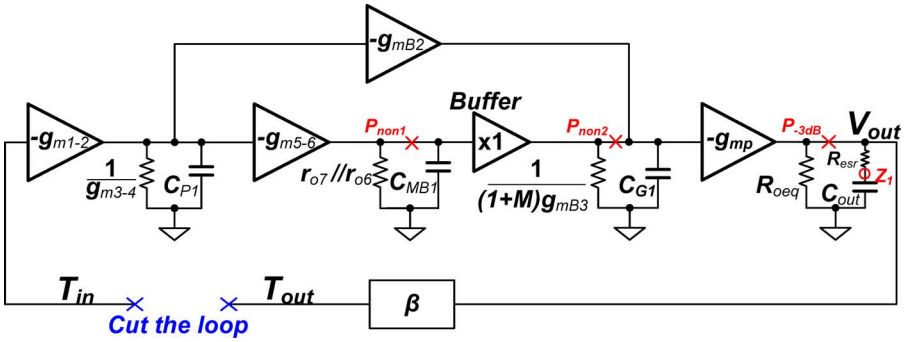

Fig. 5. Small signal circuit of the proposed LDO.

transient response, as well as improve load regulation [13]. The small signal circuit of the proposed LDO as shown in Fig. 5, is used to analyze the stability of the LDO regulator.

Basically, the three poles in the LDO regulator are located at the output voltage ($V_{\rm out}$), the output of the error amplifier ($V_{\rm eao}$), and the gate of pass device (V_{G1}). The expressions of three poles are shown as follows:

$$p_{-3{\rm dB}(V_{\rm out})} = \frac{1}{(R_{\rm oeq}C_{\rm out})} \tag{1}$$

$$p_{{\rm non1}(V_{\rm eao})} = \frac{1}{(r_{\rm oea}C_{M_{B1}})} \tag{2}$$

$$p_{{\rm non2}(V_{G1})} = \frac{1}{(r_{\rm buffer}C_{G1})}. \tag{3}$$

Resistance $R_{\rm oeg}$ is the output equivalent resistance at the output node, $r_{\rm oea}$ (equal to $r_{o6}//r_{o7}$) and $r_{\rm buffer}$ (equal to $1/[(1+M)g_{mB3}]$) indicate the output resistances of the error amplifier and the buffer stage, respectively, $C_{\rm out}$ is the output capacitor. $C_{M_{B1}}$ and C_{G1} are the input capacitances of transistor M_{B1} and pass device M_P, respectively. The g_{m1-2}, g_{m5-6}, g_{mB2}, and g_{mp} refer to the transconductances of input differential stage (M_{gm1} and M_{gm2}), the second stage (M_{gm5} or M_{gm6}), the feed-forward transistor M_{B2}, and pass device M_P, respectively. Finally, β is the feedback factor $R_{F2}/(R_{F1}+R_{F2})$. The closed-loop transfer function *T(s)*, can then be expressed as, (4), as shown at the bottom of this page.

In general, the dominant pole $p_{-3\,{\rm dB}}$ is located at the output node. As earlier mentioned, the output of the buffer has low impedance while capacitance $C_{M_{B1}}$ is much smaller than the output capacitor C_L. Therefore, $p_{\rm non1}$ and $p_{\rm non2}$ are placed at much higher frequencies to achieve a single-pole system compared to the unity gain frequency. In addition, a zero is achieved by the equivalent series resistance (ESR) $R_{\rm esr}$, and the output capacitor. In this design, $R_{\rm esr}$ is equal to the summation of the parasitic resistance of capacitor and the routing resistance from the LDO chip to the external capacitor and its value is very small. Therefore, the zero located at the region near the first nondominant pole $p_{\rm non1}$, can improve the phase margin and stabilize the system accordingly. The $p_{\rm non2}$ is located near the unit-gain frequency and the worst phase margin is approximately equal to 50° even if the LDO operates at the maximum load (200 mA). The Bode plot of the proposed LDO regulator is depicted in Fig. 6.

B. Peak Current Detector

Two control mechanisms are used to control the pass device. The output voltage is regulated by the error amplifier when the load current is lower than the peak current level. On the other hand, if the load current is higher than the peak current level, the pass device will be regulated to source the persistent current through the peak current control and to achieve OCP. The peak current detector shown in Fig. 7 is used to determine the suitable control mechanism. In normal condition, the load current is smaller than the peak current level and the switch M_{S1} is turned off by the output node of the unilateral-hysteresis comparator $Comp_{out}$. Meanwhile, $V_{\rm det}$ follows a load current information since the current sensing signal I_{S1} flows through the resistor R_S. The transistor $M_{\rm sen2}$ is designed to reduce the difference between $V_{\rm out}$ and the drain voltage of $M_{\rm sen1}$, while the cross voltage ($V_{\rm out}-V_{\rm fb}$) is larger than the threshold voltage of $M_{\rm sen2}$ and equal to the gate-source voltage of the transistor $M_{\rm sen2}$. Therefore, the effect of channel length modulation could be decreased. The sampling current I_{s1} is equal to the ratio of the pass device and the sensing transistor $M_{\rm sen1}$. The output node of comparator $Comp_{out}$ enables the peak current control mechanism to avoid an overload condition when $V_{\rm det}$ is higher than the reference voltage $V_{\rm OCP}$, as shown as follows:

$$\frac{1}{K}I_{D(MP)}R_S \geq V_{\rm OCP}. \tag{5}$$

In the formula, R_S is the sensing resistor and K refers to the sensing ratio. The absolute value of resistor suffers variation in different corners and temperatures, and may cause the precision of the OCP mechanism to deteriorate. Hence, in this proposed circuit, the SPCC circuit is expected to regulate the current value to be smaller than the minimum peak current level in variation region caused by environmental variation. When the

$$T(s) = \frac{g_{m1-2}\left[g_{m5-6}(r_{o6}//r_{o7}) + g_{mB2}r_{\rm buffer}\right]g_{mp}(R_{\rm oeq})\left(R_{\rm esr}C_{\rm out}+s\right)}{g_{m3-4}\left(1+(s/p_{-3{\rm dB}})\right)\left(1+(s/p_{\rm non1})\right)\left(1+(s/p_{\rm non2})\right)}. \tag{4}$$

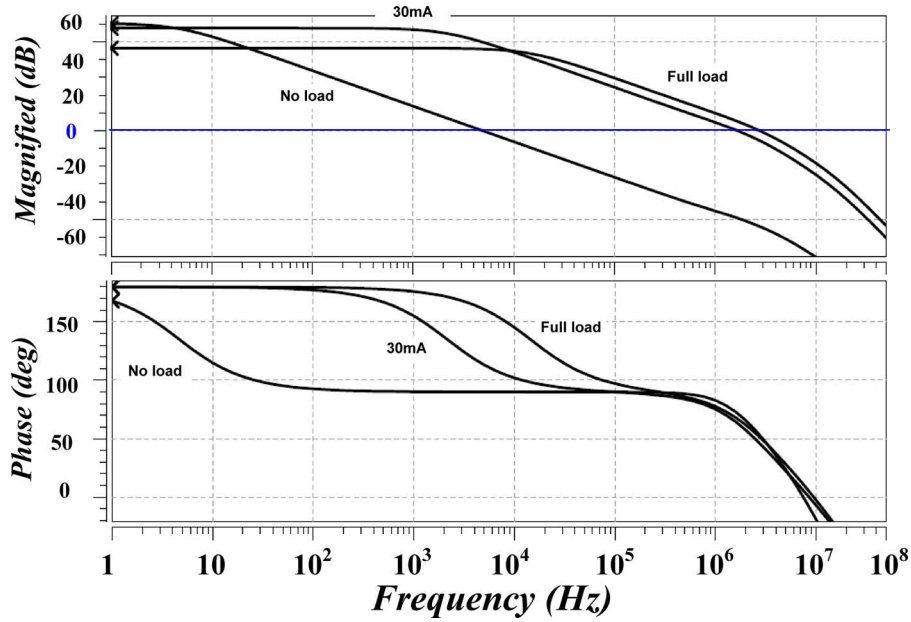

Fig. 6. Bode plot of the proposed LDO regulator.

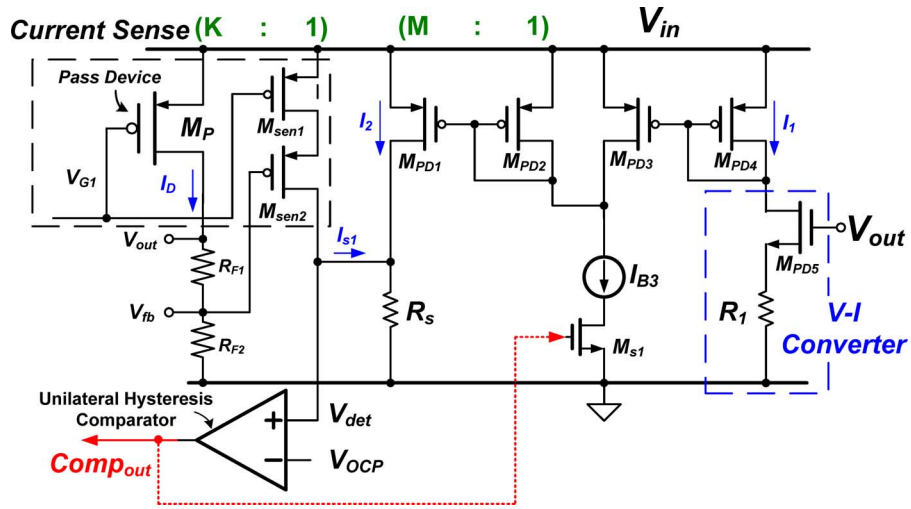

Fig. 7. Proposed peak current detector, which utilizes the output voltage and sensing current to determine, which control mechanism is suitable for LDO circuit.

load current is decreased, the error amplifier may still take the place of the SPCC circuit. The maximum dc current of metal line in this layout should be able to sustain the current value, which is larger than maximum peak current level in variation region. Based on their layout capacities, some dummy resistors are added to all resistors in this proposed LDO regulator with SPCC circuit to reduce the variation.

When the switch M_{s1} is turned on, a drain current of transistor M_{PD2} is generated by subtracting the current I_1, which is converted from the output voltage by the *V–I* converter, from the biasing current I_{B3}. In the current mirror pair, which is composed of M_{PD1} and M_{PD2}, the current I_2 is found to be equal to $M \times (I_{B3} - I_1)$ and flows through the resistor R_S to increase the value of $V_{\rm det}$. Because of the extra current, $V_{\rm det}$ could contain the information of load current and the drop of output voltage. Moreover, the unilateral-hysteresis comparator as shown in Fig. 8(a) is used to ensure that the load current is smaller than the peak current level. When the signal $Comp_{out}$ transits from low to high level, the extra current I_{B1}, which is equal to I_{B2}/k, is added to the positive feedback loop in order to form a hysteresis region as expressed as follows:

$$V_{\rm hy} = \sqrt{\frac{i_{B1}}{\mu_p C_{\rm ox}}}(\sqrt{k+1} - \sqrt{k-1}) \tag{6}$$

μ_p is the mobility of holes and $C_{\rm ox}$ is the oxide capacitance per unit area. When the voltage $V_{\rm det}$ is higher than the voltage $V_{\rm OCP}$, the signal $Comp_{out}$ transits from low to high level. In other words, when the voltage $V_{\rm det}$ is smaller than the value of $(V_{\rm OCP} - V_{\rm hy})$, the signal $Comp_{out}$ would transit from high to low level and the comparator's transfer curve with hysteresis window can be depicted in Fig. 8(b). As a result, the control

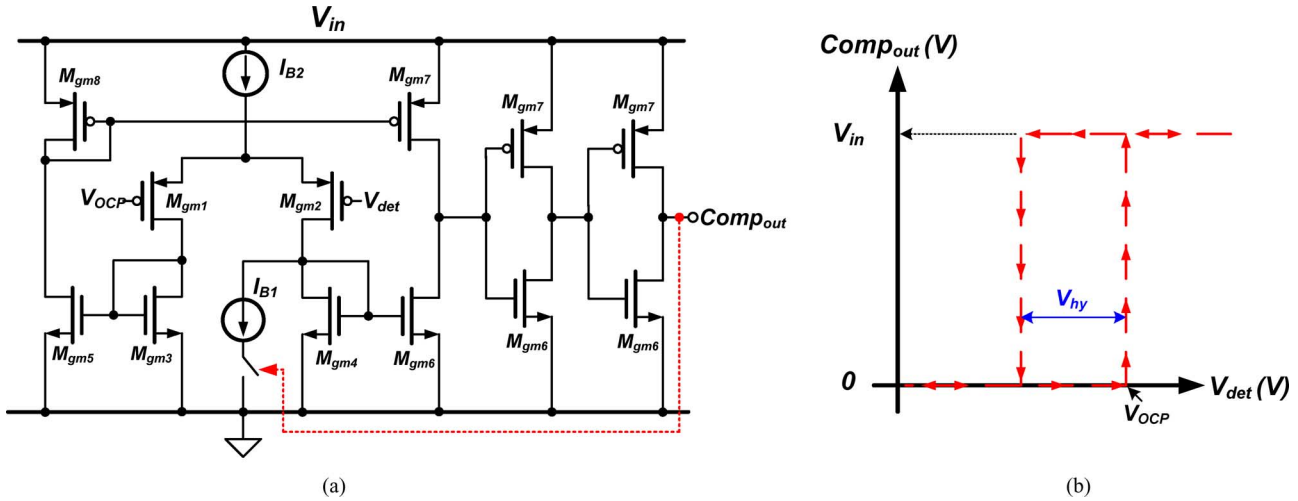

Fig. 8. (a) Unilateral-hysteresis comparator. (b) Comparator transfer curve with an unilateral-hysteresis region.

TABLE I
VALUE OF RESISTOR R_1 CORRESPONDING THE DIFFERENT VOLTAGE

The output voltage	The value of resistor R_1
1.2 V	100 kΩ
1.8 V	250 kΩ
2 V	300 kΩ
3 V	550 kΩ

mechanism is switched back to the error amplifier control to regulate output voltage until voltage $V_{\rm det}$ is smaller than the value of $V_{\rm OCP}$–$V_{\rm hy}$ as shown as follows:

$$\left[M\left(I_{B3}-\frac{V_{\rm out}-V_{{\rm th}(M_{PD5})}}{R_1}\right)+\frac{1}{K}I_{D(MP)}\right]R_S \leq (V_{\rm OCP}-V_{\rm hy}). \quad (7)$$

The $V_{{\rm th}(M_{PD5})}$ is the threshold voltage of the transistor M_{PD5}. In the proposed method, the resistor R_1 is designed to generate the current I_1, which is equal to the biasing current I_{B3}, when the output voltage is close to predefined value. In the equation, R_1 can be designed as a programmable resistor for the different output voltage value to achieve the SPCC when the LDO regulator is used in different applications. The biasing current is designed as 4 μA and the resistor is designed as 250 kΩ when the output voltage is 1.8 V. Table I lists the value of resistor R_1 corresponding the different output voltages when the value of I_{B3} is fixed at 4 μA. The positive temperature resistor is chosen for resistor R_1. Thus, when the temperature is –40 °C and 80 °C, the OCP would happen at 221 and 175 mA, respectively. The ranges of peak current level are from 187 to 218 mA when the process variation influences the resistor. Hence, the constant current level, which is regulated by OCP topology should be smaller than the minimum peak current level for ensuring the error amplifier can replace the OCP topology. The hysteresis region is set at 50 mV. As a result, the LDO regulator, which is controlled by the peak current control, is terminated and returned to the error amplifier control until the load current is smaller than the peak current level and the output voltage is close to the predefined level.

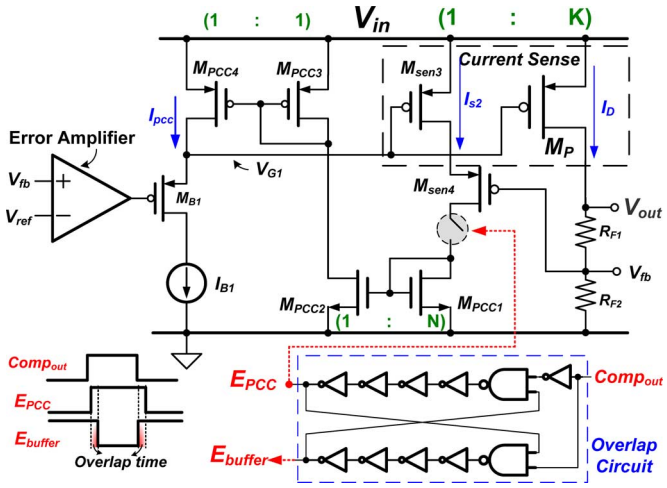

Fig. 9. Proposed peak current control uses the current mirror pairs to clamp the gate-source voltage of the pass device. In addition, the overlap circuit ensures the two control mechanisms can control the LDO regulator at the same time.

C. Peak Current Control Loop

The scheme for peak current control is illustrated in Fig. 9. When load current exceeds peak current level, signal $Comp_{out}$ received from the peak current detector transits from low to high level to disable the buffer circuit in Fig. 3 and enables the peak current control mechanism to suppress the gate-source voltage of the pass device. However, there could be a possibility that the two control mechanisms are turned off at the same time. Therefore, the LDO regulator may source a much larger current, since the gate voltage of the pass device is pulled down by the biasing current I_{B1}. The overlap circuit is used to prevent the two control mechanisms from being turned off at the same time. As a result, the two control mechanisms are simultaneously enabled in a small period when $Comp_{out}$ from the peak current detector transits from low to high level. During this short period,

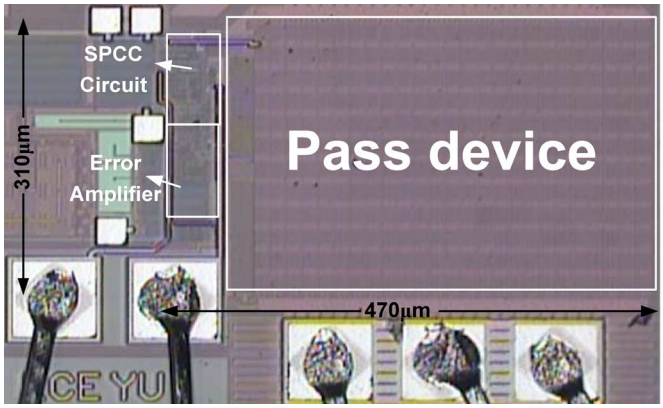

Fig. 10. Chip photograph.

TABLE II
PERFORMANCE OF THE PROPOSED LDO

Fabrication Process	0.35-μm 3.3-V CMOS 2P4M
Chip Area	0.146mm^2(470μm×310μm)
Supply Voltage (V_{in})	2 - 4.5V
Output Voltage (V_{out})	1.8V
Maximum Load Current	200mA
Capacitor	C_{Load} > 1μF, R_{esr} ≈ 0.05Ω
Line Regulation	6mV/V
Load Regulation	90μV/mA
Quiescent Current	30μA
Dropout Voltage (Load current @ 200mA)	200mV
Settling Time (0mA → 160mA) (160mA → 0mA)	1.8μs 6.5μs

the LDO regulator is mainly regulated by the error amplifier because of high-gain characteristics. The current $I_{\rm PCC}$ is equal to the bias current I_{B1} because signal $E_{\rm buffer}$ is utilized to open the two switches (S_{w1} and S_{w2}), as shown in Fig. 3, after this short period. Moreover, $I_{\rm PCC}$ is generated by the closed-loop of the peak current control, which is composed of two current mirror pairs ($M_{\rm PCC1}$ and $M_{\rm PCC2}$) and ($M_{\rm PCC3}$ and $M_{\rm PCC4}$) as depicted in Fig. 9. Thus, the current $I_{\rm PCC}$ is approximately equal to $I_{\rm load}/(K \times N)$. As a result, $I_{\rm load}$ will be clamped and equal to the bias current I_{B1} multiplied by ($K \times N$) according to the current mirror pairs. In addition, the transistor $M_{\rm sen4}$ is utilized to suppress the channel length modulation effect for improving the accuracy of the sensing current. In cases, where the current of pass device is regulated by the peak current control, the transistor M_{B2} in Fig. 3 could not transmit an error signal. The super source follower is also disabled and ultimately, the gain of buffer stage is decreased. Therefore, the buffer circuit cannot correctly pass the error signal to the gate of pass device. Similarly, the error amplifier loses control of the pass device and the output voltage starts to drop. When the voltage drops greatly, the error amplifier allows the transistor M_{B1} operate in a deep linear region (similar to a resistor) due to high gain by the error amplifier. When the load current decreases and becomes smaller than the clamped current, the limiting current regulated by peak current control pulls up the output voltage. Until the $V_{\rm out}$ is approximately equal to 1.75 V, the transistor M_{B1} operates nearly in the saturation region. In addition, the signal $Comp_{out}$ from the peak current detector will reactivate the buffer stage, and then, disable the peak current control. Consequently, the error amplifier takes the place of the peak current control to regulate the output voltage.

IV. MEASURED RESULTS

The proposed LDO regulator with the SPCC circuit was fabricated by 0.35-μm 3.3-V CMOS technology. The threshold voltages of n-MOSFET and p-MOSFET are 0.55 and −0.65 V, respectively. The chip micrograph is shown in Fig. 10 with a chip area of 310 × 430 μm^2. Table II shows the performance of the proposed LDO with the SPCC circuit.

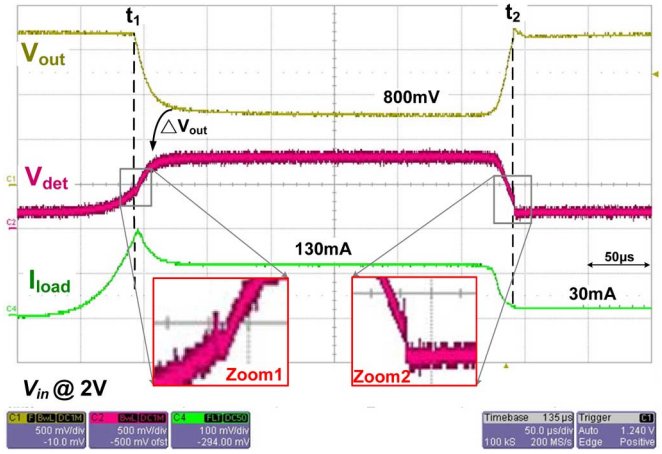

Fig. 11. OCP is activated when the load current is larger than the peak current level and the drop of output voltage will be added into the voltage $V_{\rm det}$. In addition, the load current is limited at 130 mA and the output voltage is about 800 mV, made by the current limiting level is multiplied by load resistance.

In this design, the input voltage range of the LDO regulator varies from 2 to 4.5 V and the output voltage of the proposed LDO regulator is regulated at 1.8 V. The dropout voltage is 0.2 V when the load current is raised to 200 mA. The chosen output capacitor should be higher than 1 μF to form a dominant pole at low frequencies to ensure the stability of the LDO regulator. The ESR is approximately equal to 50 mΩ. The maximum drain current of the pass device is designed to be at 200 mA. When the load current exceeds 200 mA, the SPCC circuit would reduce the drain current of pass device to be approximately equal to 130 mA. Fig. 11 shows the SPCC circuit taking the place of the error amplifier control to regulate the source current. In this experimental environment, the external power transistor is used as an active load resistance to adjust the load current. At time t_1, the load current is larger than 200 mA and the peak current detector enables the peak current control and decreases the gain of buffer stage in the proposed LDO regulator. Therefore, the drain current of pass device is decreased by the peak current control to the limited current level about 130 mA. While the output voltage drops to 800 mV, is obtained by multiplying the limit current level by load resistance. The $V_{\rm det}$ is raised

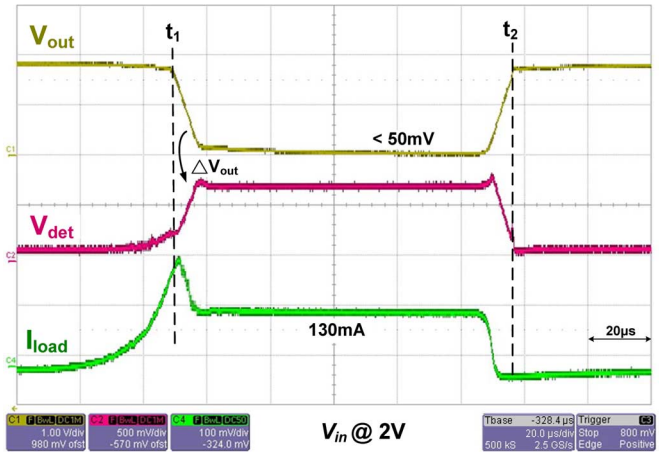

Fig. 12. Load current is limited at 130 mA to protect the chip when the short-circuit fault happens within 30 μs. The output voltage is smaller than 50 mV.

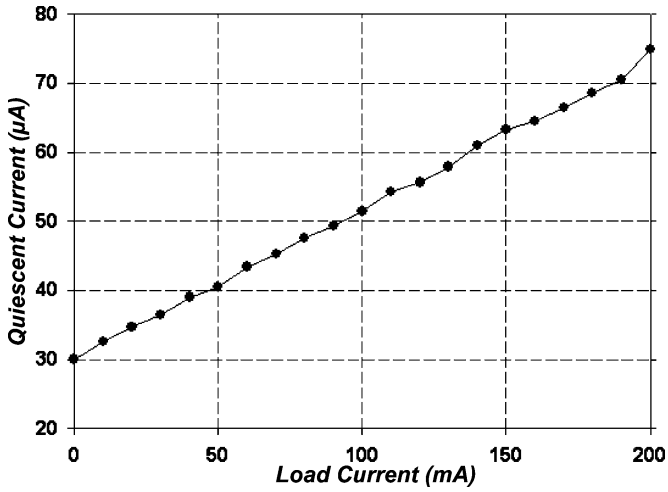

Fig. 13. Measured quiescent current versus load current.

because the drop of output voltage is added. Zoom1 shows the details at time t_1. Thus, when the load current is decreased, the limited current level pulls up the output voltage, the voltage $V_{\rm det}$ is decreased because of the reduction in the drop of output voltage. When the output voltage is close to 1.75 V at time t_2 and the drain current of pass device remains regulated at 130 mA, the voltage $V_{\rm det}$ becomes smaller than $V_{\rm OCP}$–$V_{\rm hy}$. The peak current detector reactivates the buffer stage, and then, disables the peak current control. Therefore, the voltage $V_{\rm det}$ instantly decreases a voltage level because the information sent by the voltage drop is removed as shown in Zoom2. The voltage $V_{\rm det}$ completely presents the load current information when the SPCC is disabled. Therefore, instead of the peak current control, the LDO regulator is regulated by the error amplifier control to provide a steady output voltage. Fig. 12 shows the peak current control can regulate the current at a value of 130 mA, the output voltage is kept smaller than 50 mV when the short-circuit fault transpires within 30 μs. As a result, the proposed circuit can prevent the chip and the SoC system from being damaged by larger current and short-circuit fault, as well as allowing smooth switches in the control mechanism between the error amplifier and SPCC circuit.

Fig. 13 shows the measured quiescent current at the different load currents. Owing to the current sensing technique, the quiescent current increases with load current. Moreover, the quiescent current is 30 and 75 μA when the load current is in a no-load and full-load condition, respectively. Load transient response of the proposed LDO is shown in Fig. 14 when the load current is changed from 0 to 160 mA with a rising/falling time of 0.1 μs. The overshoot and undershoot voltages mainly result from *IR* drop across the ESR, which is formed by the parasitic resistance of capacitor and the routing from the LDO regulator to the external capacitor. The variation of the output voltage $V_{\rm out}$ during the transient period is smaller than 50 mV while using the 1 μF ceramic output capacitor. The steady state voltage error is 15 mV and the output voltage is stable within 2 μs when the load current changes from no load to 160 mA. The LDO regulator was also subjected to line transient response

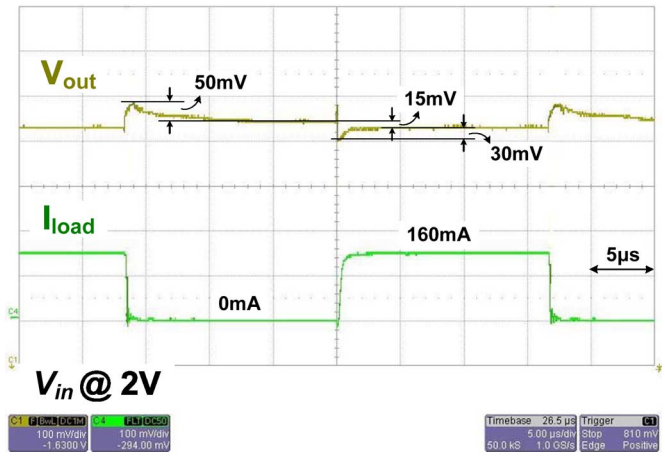

Fig. 14. Measured load regulation when the load current changes from 0 to 160 mA, and *vice versa*.

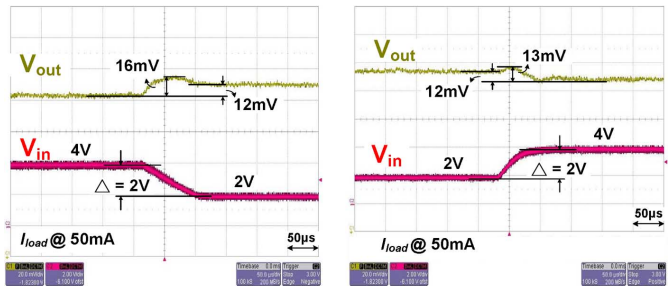

Fig. 15. Measured line regulation when the supply voltage changes from 4 to 2 V, and *vice versa*.

to evaluate the effect of battery voltage as shown in Fig. 15. The 2-V input variation with a rising/falling time of 60 μs results in a 12 mV steady-state variation at the output voltage when the load current is 50 mA. Thus, the output voltage of the proposed LDO regulator remains stable over a wide input voltage range.

V. Conclusion

This proposed LDO regulator has the characteristics of stable operation and fast transient response over wide ranges of load current and supply voltage. In addition, owing to its capability of detecting the information from load current and the drop of output voltage, the proposed SPCC integrated in an LDO regulator can smoothly switch the two control mechanisms, which can then function as error amplifier control used to regulate the output voltage and the peak current control for limiting the current level.

Acknowledgment

The authors would like to thank to Chunghwa Picture Tubes, Ltd. and Richtek for their assistance. And this work was supported by the MediaTek Fellowship.

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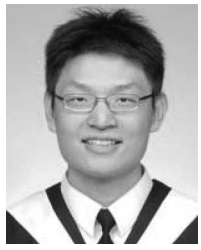

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