國　立　交　通　大　學

電子工程學系 電子研究所

博 士 論 文

氮化處理與氟摻雜對二氧化鉿堆疊式閘極介電層金氧半場效電晶體其電性特性與可靠性影響

Effects of Nitridation and Fluorine Incorporation on the Electrical Characteristics and Reliabilities of MOSFETs with HfO_2/SiON Gate Stack

研 究 生：盧文泰

指導教授：黃調元 博士

中 華 民 國 九十四 年 九 月

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國 立 交 通 大 學

電子工程學系 電子研究所

博 士 論 文

A Dissertation

Submitted to Department of Electronics Engineering and
Institute of Electronics
College of Electrical and Computer Engineering
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for the Degree of
Doctor of Philosophy
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中 華 民 國 九十四 年 九 月

推薦函

事由：推薦電子研究所博士班研究生 盧文泰 君提出論文，以參加國立交通大學博士論文口試。

說明：本校電子研究所博士班研究生盧文泰，已完成電子研究所規定之學科及論文研究訓練。有關學科部分，盧君已修畢電子所訂之所需學分數，且通過資格考試。有關論文研究部分，盧君已完成『氮化處理與氟摻雜對二氧化鉿堆疊式閘極介電層金氧半場效電晶體其電性特性與可靠性影響』論文初稿，博士論文內容中已有數篇論文發表或送審於國際學術期刊，玆列舉如下：

[1] "The characteristics of hole trapping in HfO_2/SiO_2 gate dielectrics with TiN gate electrode," ***App. Phys. Lett***, Vol. 85, pp. 3525-3527, 2004.

[2] "Effects of low-temperature NH_3-treatment on the characteristics of HfO_2/SiO_2 gate stack," ***Journal of Electrochemical Society***, accepted to be published.

[3] "Effects of low temperature NH_3 treatment on HfO_2/SiO_2 stack gate dielectrics fabricated by MOCVD system," in the 2004 ***Joint International Meeting*** (including ***the 206th Meeting of The electrochemical Society***), held 2004 fall in Honolulu, October 3-October 8, 2004.

[4] "Improvements on the electrical characteristics of pMOSFETs with HfO_2 gate stacks by Post-Deposition N_2O plasma treatment," submitted to ***Jpn. J. Appl. Phys.***.

[5] "Improved Reliability of HfO_2/SiON Gate Stack by Fluorine Incorporation," submitted to ***IEEE Electron Device Lett.***.

[6] "Impact of Fluorine-incorporation on the Reliability and Plasma Charging Damage of PMOSFETs with HfO_2/SiON Gate Stack," submitted to ***2005 IEEE International Electron Devices Meeting***, Hilton Washington.

綜上所述，盧君已具備國立交通大學電子研究所應有之教育及訓練水準，因此推薦並請准予盧君參加國立交通大學電子研究所博士論文口試。

國立交通大學電子研究所教授　　黃調元　　黃調元 博士

國 立 交 通 大 學

論文口試委員會審定書

本 校 電 子 工 程 學 系 電 子 研 究 所 博 士 班 盧 文 泰 君

所提論文 氮化處理與氟摻雜對二氧化鉿堆疊式閘極介電層金氧半場效電晶體其電性特性與可靠性影響

合於博士資格標準、業經本委員會評審認可。

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中 華 民 國 九十四 年 九 月 七 日

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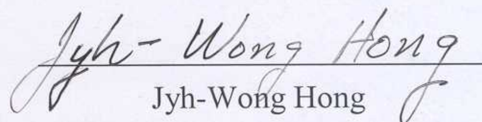
Date : Sept. 7, 2005

We have carefully read the dissertation entitled **Effects of Nitridation and Fluorine Incorporation on the Electrical Characteristics and Reliabilities of MOSFETs with HfO_2/SiON Gate Stack** submitted by **Wen-Tai Lu** in partial fulfillment of the requirements of the degree of DOCTOR OF PHILOSOPHY and recommend its acceptance.

Jenn-Gwo Hwu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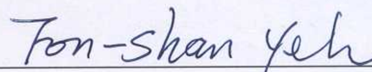
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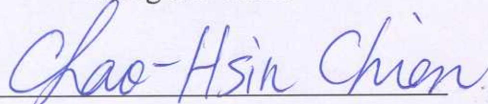
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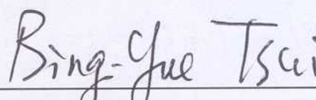
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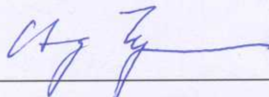
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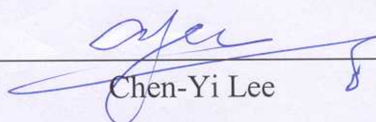
Chairman : 
Chen-Yi Lee

氮化處理與氟摻雜對二氧化鉿堆疊式閘極介電層
金氧半場效電晶體其電性特性與可靠性影響

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博士論文

摘要

隨著 CMOS 技術急速的微縮到奈米技術點，傳統閘極介電層二氧化矽層將達到其物理與電性限制。主要的問題是的量子效應引發無法接受的大量的載子直接穿隧電流(Direct Tunneling Current)穿隧超薄二氧化矽層。為了可以有效的抑制此漏電流，高介電常數的閘極介電層材料會被使用來取代傳統的二氧化矽層而可以維持在相同的等效電性氧化層厚度(EOT)下增加實際介電層膜的厚度。在本論文中，我們對於具有二氧化鉿堆積式閘極介電層之金氧半元件與電晶體，研究不同氮化處理，如沉積前的不同氣體電漿處理、沉積後的 N_2O 氣體電漿處理、後沉積低溫氨氣處理及氟併入到閘極介電層，對二氧化鉿堆積式閘極介電層其電性特性(如電荷捕捉)及固定偏壓電應力(constant voltage stress)、負偏壓不穩定(negative bias-temperature instability，NBTI)，AC 電性應力(AC stress).. 等可靠性議題。此外，我們也針對目前文獻很少發表有關於高介電層材料，其電漿損害效

應做了深入探討，及其對於 NBTI 效應之影響和氟對於漿損害效應的改善影響。我們也對於目前高介電層材料的另一大問題，由於快速電荷捕捉所引起的電壓不穩定(Threshold voltage instability)，架設了可以對這些快速缺陷(Fast Transient Charge Trap, FTCT)作探討的單一脈波 I_d&V_g 量測(Single-Pulsed I_d&V_g)。

首先，我們探討了我們利用氨氣及一氧化二氮高密度電漿來處理矽基板表面，形成一層薄的含氮的介面層，及與一般傳統的二氧化矽介面層或是直接沉積 HfO_2 薄膜在矽基板上的閘極介電層，他們在電性上和可靠度上的差異，結果顯示經過高密度電漿處理過後的介面層電性較差，且漏電流仍然未達到我們要的標準，必須經由傳統的快速升溫回火來修補這些損害，所以修補後呈現出較小的漏電流、較小的磁滯、較小的頻率分散、較大的崩潰電壓。而就可靠度來說，經由氨氣電漿處理的試片會有最大的崩潰時間、崩潰電荷，以及最好的特性存活時間，所以用氨氣來作為表面處理的氣體是很好的選擇！我們發現對於由氮化鈦作為電極的電容，在二氧化鉿薄膜裡面主要的捕捉電荷機制是電洞捕捉而不是電子捕捉。而這種行為可以用捕獲面積模型來適當敘述。特別的是，平帶電壓平移是由於陷阱填補而不是陷阱產生.而電洞捕捉為主要機制可以歸因於電洞由基板注入的機率遠大於電子由閘極注入的機率而這是因為氮化鈦電極的功函數造成電洞具有較短的穿透路徑。

其次，我們提出一個改善二氧化鉿電性特性的後沉積低溫氨氣處理方法。於二氧化鉿介電層沉積後，但於後沉積退火前，使用低溫 (~400 ℃) 氨氣對二氧化鉿介電層做氮化處理，我們發現並有低溫氨氣處理的試片呈現出較好 *C-V* 特性、較小的頻率分散、較低的漏電流、崩潰電場等等。此外，低溫氨氣處理的試片也呈現出較少的二氧化鉿本體內部缺陷(bulk trap)，且對於電壓應力抵抗能力也明顯被改善，即使於高溫的 700℃的 PDA。最後，我們發現經過電壓應力後，漏電流主要是由於電洞的 SILC 所主導。

此外，我們也嘗試使用一氧化二氮氣體對二氧化鉿作電漿氮化處理，來改善二氧化鉿閘極介電層的品質。我們發現一氧化二氮電漿氮化處理後，可以得到諸

如較低閘極漏電流、較高電導頂峰值(higher peak of transconductor)、較佳次臨界擺幅(substhreshold swing)、較低界面缺陷、和較低二氧化鉿本體缺陷等優點。我們也發現，在固定電壓應力(CVS)、及負偏壓-溫度應力(NBTI)的可靠性測試中，不管是否經過 N_2O 處理，電晶體之退化，主要是由於本體中之捕捉行為，而非界面缺陷的增加。且經氮化處理後，原本呈現捕捉電洞之行為，會轉變成捕捉電子。在動態應力(dynamic AC stress)可靠性測試下，我們發現，關閉時間(off-time)時釋放電洞之行為，及因開啟時間(on-time)太短，而來不及捕捉電洞，二者均須加以考量，方能解釋動態應力下臨界電壓漂移之行為。透過載子分離(carrier separation)量測，我們得以釐清，崩潰究竟是發生於二氧化鉿本體內部或是界面層。

最後，本論文中，我們探討氟對具有 HfO_2/SiON 閘極介電層之 p 型電晶體其可靠性的影響。利用氟摻雜在源極/汲極摻雜過程前，然後藉由接下來的高溫摻雜活化過程使氟原子擴散到通道和閘極介電層中去形成氟的併入。發現導入氟對所製造的元件其基本特性沒有明顯的改變，但在固定電壓應力(CVS)和負偏壓-溫度應力(NBTS)測試時，觀察到有氟併入的元件有較低的界面狀態產生和較少的電荷捕捉，因而改善元件的穩定性和可靠性。其次，則是探討電漿效應對具有 HfO_2/SiON 閘極介電層之 p 型電晶體電性與其對 NBTI 可靠性的影響，以及氟併入對這些結果的影響也有深入探討。我們發現不論在 NBTS 前後，界面狀態密度均會隨天線面積比而增加。且負偏壓-溫度應力 (NBTS) 所導致的臨界電壓漂移，也會因受到電漿充電損傷而更加惡化，且其會造成嚴重的電洞缺陷。更重要的是,電漿充電效應會使在二氧化鉿內的的電洞捕捉現象的惡化比界面產生的缺陷更嚴重。這和傳統以二氧化矽為閘極之 p 型通道電晶體為電子捕捉是不同的。利用氟併入可有效增加對電漿充電損傷的免疫，因此降低具有大天線面積比之元件在 NBTS 時的嚴重電洞捕捉現象。氟併入仍然維持相同的臨界電壓漂移與界面狀態密度產生的活化能，分別為 0.08eV 與 0.12eV。實驗結果發現，AC 電性應力下，臨界電壓漂移會從 DC 電性應力下的負漂移轉變成的正漂移。這可能是因

為在 AC 電性應力一週期裡的 on time 時有較少的電洞捕捉及 off time 時有較多電洞被釋放。此外，AC 電性應力下，界面狀態密度產生不易受頻率與 duty cycle 影響且電洞捕捉現象是一主要的劣化原因。

Effects of Nitridation and Fluorine Incorporation on the Electrical Characteristics and Reliabilities of MOSFETs with HfO_2/SiON Gate Stack

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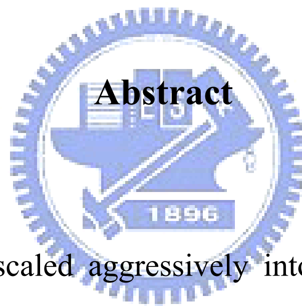

Abstract

As CMOS devices are scaled aggressively into nanometer regime, SiO_2 gate dielectric is approaching its physical and electrical limits. The primary issue is the intolerably huge leakage current caused by the direct tunneling of carriers through the ultrathin oxide. To substantially suppress the leakage current, high-k materials are recently employed by exploiting the increased physical thickness at the same equivalent oxide thickness (EOT). In this dissertation, the electrical characteristics of pMOSFETs with HfO_2/SiON gate stack subjected various Nitridation, i.e., pre-deposition plasma treatments, post-deposition N_2O plasma Nitridation, low temperature NH_3 Nitridation, and incorporated with Fluorine were discussed. The related reliabilities, including CVS stress, NBTS, dynamic unipolar AC stress, and charge traping, were comprehensively investigated. In addition, the characteristics of

plasma charging damage of the HfO_2 high k film few reported and the impact of plasma charging damage on NBTI effects also were studied in detail. Moreover, we also investigate the threshold voltage instability in high k film, due to fast charge trapping at Fast Transient Charge Trap (FTCT), by using the single pulse I_d-V_g measurement.

First, we investigated the effects of various pre-deposition plasma treatments (NH_3 and N_2O) on Si surface to form an interfacial layer before deposition HfO_2 gate dielectric. In order to significantly reduce gate leakage current, a good quality interfacial layer is essential before deposition of high k film. However, our results show that samples with various gas plasma pre-treatments still result in poor electrical properties and the leakage current does not meet device criterion. A conventional RTA is found to be necessary to repair the damage in the interfacial layer. Samples with plasma pre-treatment and RTA anneal depict lower leakage current, smaller hysteresis and frequency dispersion, and higher breakdown voltage. In addition, NH_3 pre-treatment also results in longer time to breakdown, larger charge to breakdown and better characteristics life time. The samples with conventional RTA show much lower leakage current, lower frequency dispersion, and smaller hysteresis than as-deposited, spike RTA and no RTA samples because of a thicker interfacial layer. Therefore, RTA is still an essential process after pre-treatment to densify nitrided interfacial layer. We also found that the dominant charge trapping mechanism in the high-k gate stack is hole trapping rather than electron trapping. This behavior can be well described by the distributed capture cross section model. In particular, the flatband voltage shift (ΔV_{fb}) is mainly caused by the trap filling instead of the trap creation. The dominant hole trapping can be ascribed to a higher probability for hole tunneling from the substrate, compared to electron tunneling from the gate, due to a

shorter tunneling path over the barrier for holes due to the work function of the TiN gate electrode.

Second, we proposed a post-deposition low-temperature (~ 400°C) NH_3-treatment on the HfO_2/SiO_2 gate stacks with TiN gate electrode. Our results indicate that samples subject to the LTN treatment exhibit superior *C-V* characteristics, less frequency dispersion, and lower gate leakage. In addition, the defect density in the bulk and the immunity against trap generations are significantly improved, especially for samples with subsequent 700°C PDA. Moreover, we find that the trap-assisted hole tunneling mechanism is responsible for the increase in gate leakage current after constant voltage stress.

Next, we used post-deposition N_2O plasma treatment to improve the characteristics of pMOSFETs with HfO_2/SiON gate stack. We have found that the improvements include many aspects, such as the reduced leakage current, the better subthreshold swing, the enhanced normalized tranconductance, and the higher driving current. Those were ascribed to the lower interface states and bulk traps, confirmed by various type of charge pumping measurement. In evaluation of the reliability, it was found that the degradation caused by the voltage stress and NBTI was dominated by the charge trapping in the bulk of HfO_2 films rather than interface states generation no matter whether the N_2O plasma treatment was employed or not. In addition, it was observed that the N_2O plasma treatment did significantly improve the charge trapping

characteristics and the electron trapping is the main mechanism during stressing, which was opposite to the hole trapping observed in the case without the N_2O plasma treatment. Under dynamic AC stress, both the off-time de-trapping and the lack of hole trapping due to short on-time are required to explain the behavior of threshold voltage degradation. Finally, through the help of carrier separation experiments, we have clarified whether the breakdown originates in the bulk or the interfacial layer.

Finally, we investigate the effects of fluorine (F) incorporation into HfO2/SiON gate stack on the reliabilities of pMOSFETs with HfO2/SiON gate stack. Fluorine was incorporated before the source/drain implant step, which was subsequently diffused into the gate stack during later dopant activation. We found that F introduction only negligibly impacts the fundamental electrical properties of the fabricated transistors. In addition, under constant voltage stress (CVS) and negative bias temperature stress (NBTS), lower generation rates of interface states and charge trapping are observed for devices with F incorporation, thus enhances high-k devices' stability and reliability. Next, effects of plasma charging and fluorine incorporation were also explored thoroughly. We find that the interface-state density is increased for devices with large antenna ratio, both before and after the BTS. It is clearly shown that the threshold voltage shift during negative bias-temperature stressing (NBTS) is deteriorated by plasma charging damage, causing severe hole traps, which is different from that

observed in traditional pMOSFETs with SiO_2 gate dielectric where electron trapping is dominant. More importantly, we also found that hole trappings are aggravated in HfO2 film as compared to interface trap generation by plasma charging. Fluorine incorporation would effectively improve plasma charging immunity, thus reducing the severe hole trapping under NBTS for devices with large antenna area ratios. F incorporation is effective in suppressing hole trapping as well as interface trap generation, thus improving threshold voltage instability. Furthermore, fluorine incorporation maintains almost the same activation energies of threshold voltage shift is 0.08 eV and that of interface trap generation is 0.14 eV for both devices. Fluorine is found to be able to electrically passivate traps without changing the NBTI mechanism. The experimental results of dynamic AC stressing show that threshold voltage shifts toward more negative voltage in DC stress, but shifts toward more positive voltage under AC unipolar stress. This is believed to be due to less hole charge trapping during on-time of a AC cycle and more hole charge de-trapping during off-time of a AC cycle. The interface trap generation depends weakly on both frequency and duty cycle. Instead of interface trap, the bulk trap of HfO_2 eventually plays a preponderant role during AC stress.

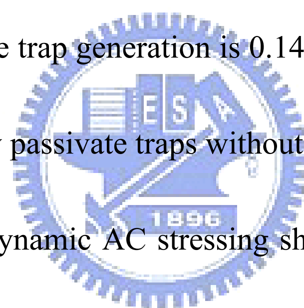

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Fig. 6.31 V_{th} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different duty cycle (a) w/o F sample (b) with F sample.
Fig. 6.32 N_{it} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different duty cycle (a) w/o F sample (b) with F sample.
Fig. 6.33 (a) Frequency dependence of $\triangle N_{it}$, stressed at 25 °C, V_g =−4 V under duty cycle = 50% (b) Duty Cycle dependence of $\triangle N_{it}$, stressed at 25 °C, V_g =−4 V under unipolar 10KHz.

Fig. 6.34 Frequency dependence of $\triangle V_{th}$, stressed at 25 °C, $V_g = -4$ V under duty cycle = 50% (b) Duty Cycle dependence of $\triangle V_{th}$, stressed at 25 °C, $V_g = -4$ V under unipolar 10KHz.

Fig. 6.35 The transistor is used in an inverter circuit with the gate receiving a single pulse from the pulse generator. The voltage is measured at the transistor drain and converted to drain current because the load resistance value is known.

Fig. 6.36 (a) Example data of the pulsed I_d-V_g where $\triangle V_t$ is measured at 50% of the maximum I_d on a W/L = 10/1 μm transistor. (b) Example data of the pulsed I_d versus time on a W/L = 10/1 μm transistor where the 'droop' at the top is associated with the drop of pulsed I_d-V_g at V_g = 2.5 V.

Fig. 6.37 A new single pulsed I_d-V_g method to improve the noises and parasitic capacitance of conventional method (Fig. 6.35).

Fig. 6.38 Single Pulse I_d-V_g characteristics for different rising and falling time of (a) 20 μs (b) 15 μs (c) 6 μs illustrating increased trapping (Vt shift) with increased rising and falling time for pMOS. The included pMOS DC ramp I_d-V_g result demonstrates the effect of hole charge trapping during the slower measurement, except electron trapping.

Chapter 7

Fig. 7.1 The schematic of metal antenna transistor and definition of Antenna Area Ratio (AAR).

Fig. 7.2 Wafer maps of (a) negative and (b) positive potential values recorded by CHARM-2 sensors.

Fig. 7.3 N_{it} of PMOS devices with and without F incorporation (a) before sintering (b) after sintering as a function of device location.

Fig. 7.4 V_{th} of PMOS devices with and without F incorporation (a) before sintering (b) after sintering as a function of device location.

Fig. 7.5 Cumulative probability of the (a) threshold voltage (V_{th}) and (b) interface trap (N_{it}).

Fig. 7.6 Output characteristics for fresh devices with AAR of 1K and 60K.

Fig. 7.7 Threshold voltage shift as a function of stress time, stressed at 25 °C, $V_g = -4$ V (a) linear scale (b) logarithm scale.

Fig. 7.8 (a) Interface trap shift and (b) total trap shift as a function of stress time, stressed at 25 °C, $V_g = -4$ V.

Fig. 7.9 Drain current degradation in a saturation regime of stress time, stressed at

25 °C, V_g = −4 V.
Fig. 7.10 Threshold voltage shift as a function of stress time, stressed at 125 °C, V_g = −3.5 V (a) linear scale (b) logarithm scale.
Fig. 7.11 (a) Interface trap generation and (b) total trap density as a function of stress time, stressed at 125 °C, V_g = −3.5 V.
Fig. 7.12 Drain current degradation in a saturation regime of stress time, stressed at 125 °C, V_g = −3.5 V.
Fig. 7.13 Threshold voltage shift as a function of stress time under BTS at different stress temperature, V_g =−3.5 V. AAR is 60K (a) linear scale (b) logarithm scale.
Fig. 7.14 (a) Interface trap generation and (b) total trap density as a function of stress time under BTS at different stress temperature, V_g = −3.5 V. AAR =60K.