Chapter 1
Introduction

1. 1 General Background

Recently, CMOS devices have been aggressively scaled into sub-100 nm regime in order to enhance the device's performance and increase the integrated circuit functionality. The accelerated downsizing rule of the transistor feature size is to scale the vertical and horizontal dimensions simultaneously. With the downsizing, the gate oxide thickness of MISFETs should be reduced. However, the continuous shrinking of gate dielectrics faces several limitations. According to the SIA roadmap [1], the SiO_2 gate dielectric film thickness should be scaled down to 1.3 nm for 65nm technology node. Such an ultra-thin SiO_2 film consists of only a few atomic layers, causing a considerably large direct-tunneling current through the film, as dictated in Equation (1-1), and in turn resulting in significant increase of power consumption. The direct tunneling current which depends on physical film thickness will cause an intolerable level of off-current, resulting in huge power dissipation and heat.

$$I_{DT} \propto [\exp - \sqrt{\frac{2mq\phi}{\left(h/2\pi\right)^2}} T_{phys}] \qquad (1\text{-}1)$$

As shown in **Fig. 1.1**, we can see that when the gate oxide thickness scales down to 2 nm, the leakage current will exceed the limit of $1A/cm^2$ set by the allowable stand-by power dissipation. Further scaling of oxide thickness to below 2nm, the direct tunneling current will increase exponentially, causing intolerable power consumption. [2] In addition, reliability issues become a serious concern for such a thin SiO_2 dielectric. To circumvent these problems, high-k dielectrics have been investigated extensively as possible replacement to the SiO_2 film as gate insulators [3]. By using gate dielectrics with higher dielectric, electrically equivalent oxide thickness (EOT) in order to maintain the same gate capacitance can be obtained with a thicker physical thickness. Therefore, the

quantum direct tunneling gate leakage current can be significantly reduced, as shown in **Fig. 1.2.**

Selecting a gate dielectric with a higher permittivity than that of SiO_2 is a clearly indispensable to extend the lifespan of the famous Moore's law. As to how high the dielectric constant should be, one needs to consider the following Equation (1-2):

$$t_{high-k} = \frac{k_{high-k}}{k_{ox}} t_{eq} = \frac{k_{high-k}}{3.9} t_{eq} \quad (1\text{-}2)$$

Although it seems that the **κ** value should be as high as possible. However, it should not be too high, otherwise it could result in degradation of the electrical properties due to increased fringing field from the gate to the source/drain of the transistor [4]. On the same token, the **κ** value should not be too low, otherwise it defeats the whole purpose of substituting for high **κ** materials. A case in point is Al_2O_3, with its mediocre κ value of only 8~10, it is not suitable as the ultimate choice of high **κ** material to replace SiO_2, albeit it may serve as a short-term band-aid solution. Similarly, oxynitride and nitride/oxide stacked dielectrics [4-9] are considered to be potential candidates for 0.13 μm and 90 nm technology nodes due to their compatibility with the existing ULSI processing and no contamination issues. They are expected to serve only as near-term improvised replacement for the gate dielectric. However, the mediocre dielectric constant can not provide sufficient physical thickness to reduce the gate leakage current for 65 nm technology. Therefore, searching a dielectric material with a sufficiently high dielectric constant to permanently replace SiO_2 is urgent and indispensable.

There are several requirements for high-k dielectrics aiming at replacing conventional SiO_2 or oxynitride [10, 11]:

(1) Thermodynamically stable in direct contact with Si [12], with thin interfacial layer (if this layer can not be avoided) to preserve the capacitance of gate stack after processing, as shown in **Table.1.1**.

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(2) Higher energy band-gap with conduction band offset (ΔE_c) > 1eV or valence band offset (ΔE_v) > 1eV to reduce the thermal emission of carriers. Too low a

bandgap will lead to intolerably large gate leakage (leakage current ~exp(-$\triangle E_c$)) [3]. The offset of conduction band and valence band relevant to Si for several gate dielectrics are shown in **Fig. 1.3** [13].

(3) Suitably high k value (12~60),

A suitable k value is critical. Those with not high enough k value could not satisfy eq (1) to lower the leakage by increasing the physical thickness. Those with too large a k value, in general, suffer from poor thermal stability and large fringing field. The energy gap is shown in **Fig. 1.4**. In general, the energy gap is inversely proportional to the dielectric constant.

(4) Low leakage current ($< 1 mA/cm^2$ at V_G-V_{FB} = 1 V),

(5) low interface state density ($D_{it} < 10^{11}$ /cm^2 eV^{-1}),

(6) Hysteresis < 20 mV,

(7) Film morphology (amorphous is desirable) and stable process compatibility,

In the VLSI process, the thermal budget is an important concern since high temperature processing changes dielectric phase, and once the polycrystalline forms from amorphous; the large grain boundaries would serves as leakage path, and induce large leakage current.

(8) Good gate electrode compatibility,

(9) Stable process compatibility (especially high temperature source/drain anneal).

(10) Less mobility degradation.

(11) Low charge trapping

(12) No Fermic level pinning effect for high-k film contacting with gate electrode, i.e., tunable work function of gate electrode.

Some of the promising high-k candidates include ZrO_x [14-15], HfO_x [16-17], Zr–silicate [14], [18], and Hf–silicate [18-19], all have demonstrated EOT scalability (12 Å) with low leakage current. Currently, Hf-based gate dielectrics are the most promising candidate among all potential high-k dielectrics with many advantages as follows: (1) suitable permittivity (22~25), (2) acceptable band alignment (>1.4eV), (3) a large bandgap of 5.6eV (4) high free energy of reaction with Si, (5) high heat of formation, and (6) superior thermal stability with poly-Si.

1.2 Organization of the Dissertation

This dissertation consists of eight chapters. The main topics are focused on the physical and electrical characteristics of oxynitride, hafnium oxide, and hafnium silicate.

In **Chapter 1**, the research background, the motivation and rationale of the dissertation are reviewed and elucidated.

In **Chapter 2**, we investigated the effects of different surface nitridation treatments on the electrical characteristics of HfO_2 gate stacks. In addition, the reliability and the characteristics of charge trapping in HfO_2 film were investigated. We observed that the hole trapping rather than electron trapping dominates in the HfO_2/SiO_2 gate stack during constant voltage stressing (CVS). We also found that hole trappings follow the charge filling model in HfO_2 films.

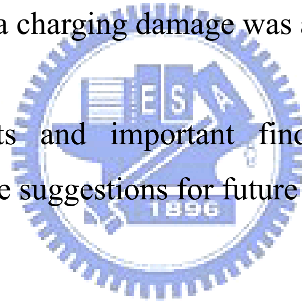
In **Chapter 3**, we demonstrated that the method of low temperature NH_3 nitridation (LTN) can effectively improve the film quality of HfO_2 gate stack dielectrics.

In **Chapter 4**, we investigated the effects of post-deposition N_2O plasma treatment on electrical characteristics of pMOSFETs with HfO_2/SiON gate stack dielectrics. We observed that N_2O plasma treatment can effectively improve the film quality of pMOSFETs with HfO_2/SiON gate stack dielectrics. Although charge pumping (CP) measurement was a powerful technique to evaluate the interface states and bulk traps presented in the high-k films, we proposed that to precisely measure the bulk traps at a lower frequency, it is better to measure charge pumping current (I_{cp}) and source/drain current (I_{ds}) simultaneously and confirm that I_{cp} and I_{ds} are the same value.

In **Chapter 5**, we clarified the breakdown mechanism in HfO_2 or interfacial layer by carrier separation measurement. Moreover, we also discussed the reliability issues, such as dynamic AC stress and negative bias temperature instability (NBTI).

In **Chapter 6**, we investigated the effects of fluorine incorporation on the electrical characteristics of pMOSFETs with HfO_2/SiON gate stack. To fully understand the effects of fluorine incorporation on pMOSFETs with HfO_2/SiON gate stack, systematic experiments and measurements were performed in this study. Some basic electrical properties such as the components in the gate leakage current and their mechanisms, and some reliability issues such as constant voltage stress (CVS), negative bias temperature stress (NBTS) and dynamic AC stress of the devices with or without fluorine were explored and discussed.

In **Chapter 7**, we presented the results on evaluating the plasma charging damage for pMOSFETs of HfO_2/SiON gate stack, both with and without fluorine incorporation. We used the NBTI characterization as a sensitive method for characterizing the antenna effects in device with HfO_2/SiON, which is particularly attractive in light of the fact that conventional indicators are becoming inadequate as oxide is scaled down. The effect of fluorine incorporation on plasma charging damage was also investigated.



Finally, the major results and important findings of this dissertation were summarized in **Chapter 8**. Some suggestions for future work were also given.

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▲ = Not a solid at 1000K

■ = Radioactive

(1) = Failed reaction Si + MO_x → M + SiO_2

(2) = Failed reaction Si + MO_x → MSi_x + SiO_2

(3) = Failed reaction Si + MO_x → M + MSi_xO_y

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
▲ H																	▲ He
Li	Be											▲ B	▲ C	▲ N	▲ O	▲ F	▲ Ne
(1) Na	Mg											Al	Si	▲ P	▲ S	▲ Cl	▲ Ar
▲ K	Ca	Sc	(2) Ti	(1) V	(1) Cr	(1) Mn	(1) Fe	(1) Co	(1) Ni	(1) Cu	(1) Zn	(1) Ga	(1) Ge	▲ As	▲ Se	▲ Br	▲ Kr
▲ Rb	Sr	Y	Zr	(1) Nb	(1) Mo	■ Tc	(1) Ru	(1) Rh	(1) Pd	▲ Ag	(1) Cd	(1) In	(1) Sn	(1) Sb	(1) Te	▲ I	▲ Xe
▲ Cs	(3) Ba	£	Hf	(1) Ta	(1) W	(1) Re	(1) Os	(1) Ir	▲ Pt	▲ Au	▲ Hg	▲ Ti	(1) Pb	(1) Bi	■ Po	■ At	■ Rn
■ Fr	■ Ra	¥	■ Rl	■ Ha	■ Sa	■ Ns	■ Hs	■ Mt									

£	La	Ce	Pr	Nd	■ Pm	(1) Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
¥	■ Ac	■ Th	■ Pa	■ U	■ Np	■ Pu	■ Am	■ Cm	■ Bk	■ Cf	■ Es	■ Fm	■ Md	■ No	■ Lr

Table 1.1 Metal oxides thermodynamically stability in direct contact with silicon [12].

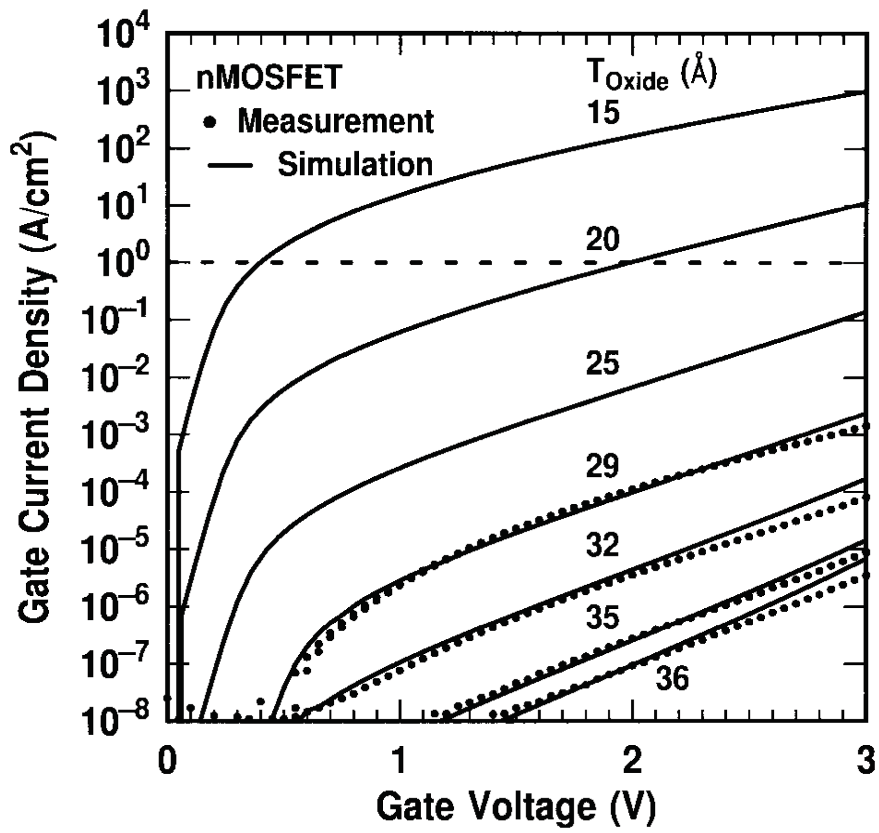


Fig. 1.1 Measured and simulated I_g-V_g characteristics under inversion condition for nMOSFETs. The dotted line indicates the 1A/cm^2 limit for the leakage current. [2]

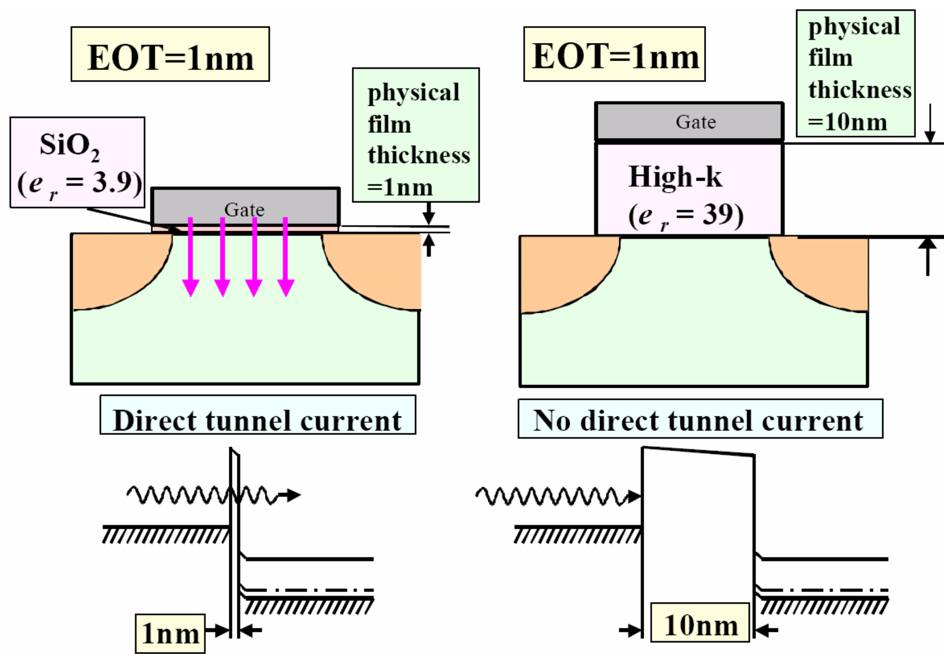


Fig. 1.2 By using high k material to suppress gate direct tunneling current.

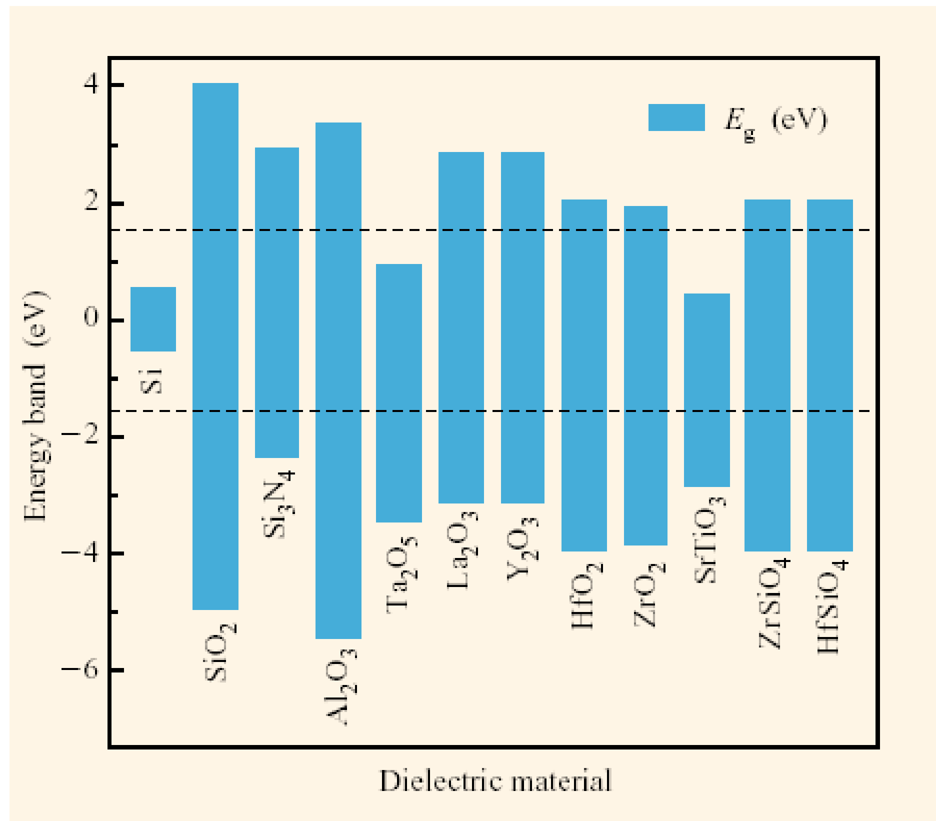


Fig 1.3 Bandgap and band alignment of high-k dielectric with respect to silicon. The dash line represents 1eV above/below the conductive/valence bands

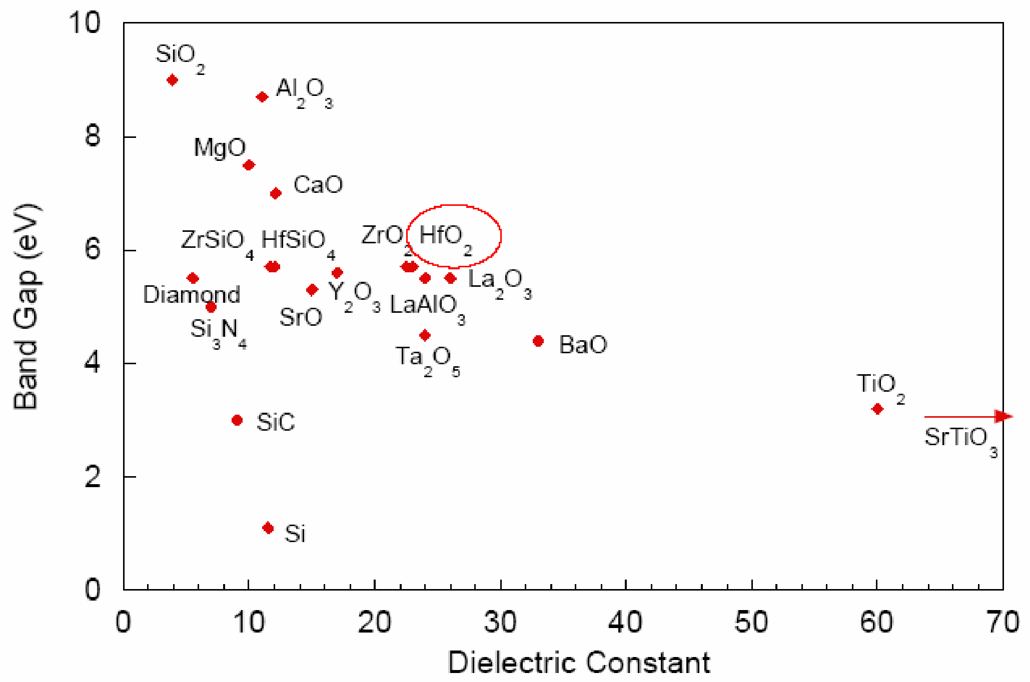


Fig. 1.4 Several high-k gate dielectric materials with their bandgaps and dielectric constants.[3]

Chapter 2
The Effects of Surface Pre-deposition Treatments on the Properties of HfO_2 Thin Films

2. 1 Introduction

As the dimensions of complementary metal oxide semiconductor (CMOS) devices are scaled into the nanometer regime, the equivalent oxide thickness (EOT) of the gate dielectric decreases steadily to thinner than 1nm (~several atom layers). In such thickness range, the gate leakage current under normal operation bias becomes intolerably large due to the quantum direct tunneling effect. Due to their thicker physical thickness while maintaining the same EOT and gate capacitance compared to thermal oxide, high-k materials have capability to drastically reduce this direct tunneling gate leakage current. Recently, high-k materials such as ZrO_2, HfO_2 and their silicates have been extensively studied [1]-[2]. Even though excellent characteristics in terms of interface state density, reliability and leakage current have been demonstrated, there are still many issues that need to be tackled before they can be used as the gate dielectrics in future device generations. Poly depletion is one of the challenging issues. To effectively solve the poly depletion problem, other gate electrodes such as metal gate must be used to replace the poly-Si gate electrode. Considering the thermal stability of the new materials, metals that are rather inactive in contact with high-k materials such TiN, Pt, are often regarded as the potential

candidates. In this work, we will use TiN as the gate electrode.

The unavoidable formation of interfacial low-k layer during deposition of high-k dielectrics is another critical issue, which will set a limit on pursuing the lowest EOT value for the application of high-k dielectrics. Previously, the formation of this interfacial layer, ascribed to the oxygen diffusion through the high-k layer during deposition of high-k dielectrics or subsequently high thermal processes, is thought to be SiO_2-like [3]-[4]. In order to suppress the oxygen diffusion through the high-k layer during deposition of high-k dielectrics, we adopt an additional nitrogen-based gas plasma treatment prior to the deposition of the HfO_2 films to form an ultra thin interfacial layer. Although there are many methods to form an ultra-thin nitride film such as furnace growth or plasma deposition, plasma nitridation is preferred because of its low thermal budget and high throughput. In this thesis, high density plasma (HDP) was used for the thin nitrided interfacial layer formation prior to the deposition of HfO_2 film. Conventional oxide RTA and spike oxide RTA with different temperatures are adopted to densify the nitrided film and hopefully to reduce the hysterisis effect.

We find that the samples with plasma surface pre-treatment show much lower gate leakage current, higher breakdown voltage and higher effective breakdown field, due to incorporated nitrogen in the interfacial layer [5]. However, formation of thin Si_3N_4 on Si surface will result in higher interface charges [6], which may in turn lead to higher hysteresis and reduced channel mobility. In order to reduce the hysteresis, it is observed that the "conventional" RTA is essential to density the film quality. For time-to-breakdown and charge-to-breakdown characteristics, NH_3 and N_2O plasma pre-treatments show improved and degraded performance over RTO control, respectively.

2. 2 Experimental

N-type MIS capacitors were fabricated on p-type (100)-oriented silicon wafers with 8~10 Ω-cm nominal resistivity. After standard RCA clean process with HF-last dip process, three surface treatment (i.e. pre-treatment) methods were performed prior to film deposition. We used NH_3 and N_2O plasma to nitridate silicon surface, immediately followed by conventional N_2 RTA at three various temperatures (900°C, 950°C, 1000°C), and we also used spike RTA at 800°C in O_2 ambient to form about 1nm interfacial oxide. After surface pre-treatment, HfO_2 film of approximately 5 nm was deposited by atomic vapor deposition (AVD^{TM}) in an AIXTRON Tricent® system at a substrate temperature of 500°C, followed by 500°C N_2 RTA for 30sec. A 500nm TiN electrode was sputtered and patterned to form gate electrodes, followed by 600℃ post-mteal deposition anneal for 30 sec. Then, all samples were sputtered with aluminum on the backside, and received a forming gas anneal at 400°C for 30 min.

For physical analysis, high-resolution transmission electron microscopy (HRTEM) was employed. For electrical analysis, a precision LCR meter, HP 4284, was used for *C-V* measurements, while a semiconductor parameter analyzer, HP 4156A, was used for *I-V* measurements. The capacitance-equivalent-thickness (CET) and flatband voltage of gate dielectric were extracted from the capacitance under accumulation mode by using UCLA's *CVC* method [7].

2. 3 Physical and Electrical Characteristics

2. 3. 1 *C-V* and *J-V* characteristics

Fig. 2.1 (a) shows the high frequency 100 KHz *C-V* curves of the samples with NH_3 pre-treatment followed by ""conventional" N_2 RTA at 900°C, 950°C, 1000°C and without RTA, respectively. **Fig. 2.1** (b) shows the corresponding J_g-V_g curves.

Without surface NH_3 pre-treatment, the capacitance shows severe distortion, which may be due to extremely high gate leakage current. This seems to suggest that the surface pre-treatment is necessary for the preparation of High-k films. When the RTA temperature increases, the capacitance value decreases, thus lowers the EOT. As a result, the gate current is reduced significantly with increasing RTA temperature. **Fig. 2.2** shows HRTEM images of as-deposited samples which received NH_3 pre-treatment and "conventional" N_2 RTA annealing at 900°C, 950°C, 1000°C, respectively. We found that the interfacial layer thickness increases with increasing temperature. As a result, EOT increases with increasing interfacial layer thickness, so the leakage current dramatically decreases. From the HRTEM, we can see that owing to RTA treatment, interfacial layers become thicker. Care should be exercised to maintain a thin EOT of high-k films for CMOS applications.

Fig. 2.3 (a) shows the high frequency 100 KHz *C-V* curves of the samples with NH_3 pre-treatment followed by N_2 "spike" RTA at 900°C, 950°C, 1000°C and without RTA, respectively. The corresponding J_g-V_g curves are shown in **Fig. 2.3** (b). From these results, we clearly observe that the "spike" RTA subsequent to NH_3 pre-treatment causes serve *C-V* and J_g-V_g degradations, especially at high temperature of 1000°C, compared to the "conventional" RTA following the NH_3 pre-treatment. This may be due to severe thermal stress resulting from the high ramp-up and ramp-down rates in "spike" RTA processing.

When the pre-treatment gas is changed from NH_3 to N_2O plasma treatment, the results of N_2O pre-treatment with "conventional" or "spike" N_2 RTA show similar trend to NH_3 pre-treatment with "conventional" or "spike" N_2 RTA (**Figs. 2.4 to 2.5**). These results indicate the surface pre-treatment seems to be necessary for the preparation of high-K films. In addition, the gate current is significantly decreased

with increasing RTA temperature, due to a thicker interfacial layer. **Fig. 2.6** shows comparisons of *C-V* and J_g-V_g characteristics of the samples with NH_3 and N_2O plasma pre-treatments with "conventional" and "spike" N_2 RTA at 900°C. Irrespective of N_2O or NH_3 treatment, the leakage current for the samples with "conventional" N_2 RTA is nearly 3 orders of magnitude lower than that with "spike" N_2 RTA. This indicates that the N_2 RTA treatment following the interfacial layer formation by plasma pre-treatment can effectively improve the interfacial layer quality.

Ideally the capacitance as determined from *C-V* measurements should not be frequency dependent at the high frequency range (i.e., above 100 kHz). In a typical capacitor, two mechanisms cause frequency dispersion. The first one is series resistance effect and the other is interface traps. The former effect mainly shows up in the accumulation region while the latter affects the transition in the depletion region. For radio frequency (RF) application of metal-insulator-metal (MIM) capacitors with high-k dielectrics, frequency dispersion is an index for quality. Therefore, frequency dispersion is addressed in the following sections.

The dispersion percentage is defined as:

$$\text{Frequency Dispersion} \equiv \frac{\text{C (@10 KHz)-C (@1 MHz)}}{\text{C (@10 KHz)}} \times 100\% \qquad (2\text{-}1)$$

Fig. 2.7 shows frequency dispersion percentage for all conditions. It can be seen that "conventional" RTA can improve frequency dispersion, and the improvement becomes even more significant with increasing temperature. In contrast, "spike" RTA does not improve frequency dispersion at all.

One of the important features in the *C-V* characteristics of MOS devices is hysteresis, which can be employed to evaluate the electrical quality of the dielectrics. The requirement for the high-k gate dielectric applications is that the hysteresis

window must be less 20 mV. Detailed mechanism responsible for the hysteresis in the high-k films has not been fully understood yet. Inner interface traps is commonly suspected as the main cause of the hysteresis [8].

First of all, *C-V* hysteresis is measured by sweeping the gate voltage from inversion to accumulation (i.e., forward sweeping) and then sweeping backward from accumulation to inversion. **Fig. 2.8** shows the hysteresis windows for all conditions in our experiments. Hysteresis seems to be improved by using conventional N_2 RTA following the interfacial layer formation, while spike RTA does not. The formation of interfacial layer by using NH_3 plasma treatment shows better hysteresis characteristics.

2. 3.2 Reliability

In the following, we will discuss the reliability issues of HfO_2 films with three different processing conditions, including N_2O pre-treatment followed by 900°C N_2 RTA, NH_3 pre-treatment followed by 900°C N_2 RTA, and spike rapid thermal oxide (~1.1nm) as interfacial layer. It should be noted that the sample with thermal oxide interfacial layer is grown by spike rapid thermal anneal (RTA) at 800 °C in an O_2 ambient (i.e., RTO interfacial layer). All samples have approximately equal equivalent oxide thickness (EOT) and lower gate leakage current, compared to the control.

Figs. 2.9 (a) & (b) show typical *J-V* curves and Weibull plots for the samples with three different pre-treatments, respectively. All samples have similar EOT values (~2.4nm). It can be seen that samples with either N_2O or NH_3 pre-treatment show comparable leakage characteristics, which are much lower than the RTO interfacial layer sample. This can be explained by HRTEM images shown in **Fig. 2.10**. As shown in **Fig.2.10**, N_2O and NH_3 pre-treatments result in a thicker interfacial layer than the RTO control (i.e., 1.5nm, 1.84nm *vs*. 1.1nm). The samples with plasma pre-treatments

may incorporate N atoms into the interfacial layer, resulting in a higher k value of interfacial layer. Due to a thicker interfacial layer, the gate leakage current is reduced. **Fig. 2.11** shows Weibull plot of the effective breakdown field ($E_{BD\,(eff)}$). The samples with plasma pre-treatments indeed have higher $E_{BD\,(eff)}$ than the RTO control, due probably to a thicker interfacial layer.

Fig. 2.12 exhibits the time-to-breakdown characteristics for three samples. We can see that the sample with NH_3 pre-treatment has the longest breakdown time, while the sample with N_2O pre-treatment the shortest. **Fig. 2.13** shows the charge-to-breakdown (Q_{BD}) of the samples under −4.8V stress voltage. NH_3 pre-treatment depicts higher Q_{BD} value than either RTO or N_2O pre-treatment.

Fig. 2.14 shows the predicted 10-year lifetime for the samples with different I.L. treatment methods (RTO, N_2O, NH_3), all with the same post-treatment annealing (900°C). It can be found that NH_3 pre-treatment shows higher operation voltage (around −3.58V).

So for reliability concerns, NH_3 pre-treatment is better than N_2O pre-treatment. A possible reason may be due to the NH_3 plasma being more uniform in HDP system than N_2O plasma.

2. 4 Characteristics of Hole Trapping in HfO_2/SiO_2 Gate Stack with TiN Electrode

In order to investigate the charge trapping in HfO_2, the smallest hystresis for HfO_2 / SiO_2 stack sample (RTO interfacial layer ~ 30mV) was used for analysis. **Fig. 2.15** (a) shows a set of *C-V* curves of a MOS capacitor measured after different CVS times. The stress voltage was – 3.5 V, i.e., gate injection polarity. It is clearly observed that the *C-V* curve gradually shifts toward negative gate voltage with increasing stress

time. This tendency indicates that hole trapping, rather than electron trapping, is the predominant process in the gate stack during stressing. However, the negative flatband voltage shift (ΔV_{fb}) may arise from the emergence of positive bulk trapped charges and/or interface charges. To clarify the mechanism responsible for the hole trapping, the conductance of the capacitor is plotted against measuring voltage over several decades of stress time, as shown in **Fig. 2.15** (b). It is found that the conductance peak value only changes slightly with stress time. This suggests that charge trapping at the interface states does not play any significant role in flatband voltage shift for the HfO_2/SiO_2 gate stack during CVS [9]. Thus, we conclude that the flatband voltage shift is mainly caused by hole trappings in the bulk of HfO_2 layer, rather than at the SiO_2/Si interface. This result seems to contradict with most previous works, in which electron trappings in the high-k stacks were shown to be the dominant mechanism responsible for the threshold and flatband voltage shifts [10]-[13].

To gain further insight into the trapping mechanism, we assume that the hole trapping is attributed to filling of pre-existing traps in the high-k dielectrics without the creation of additional trap centers, and employ the so-called distributed capture cross section model or stretched exponential model [13]-[14] to describe the trapping behavior in our high-k gate stacks. The stretched exponential equation is given by

$$|\Delta V_{fb}| = |\Delta V_{max}| \bullet (1 - exp(- t/\tau_0)^{\beta}), \qquad (3\text{-}1)$$

where $|\Delta V_{max}|$, τ_0, β are fitting parameters which are related to the total trap density. Here, τ_0 represents the characteristic time constant of the distribution, and $|\Delta V_{max}|$ denotes the maximum shift in $|\Delta V_{fb}|$ that occurs after prolonged stressing. **Figs. 2.16** (a) and (b) shows the dependence of ΔV_{fb} on injected charge density and stress time, respectively. It can be clearly seen that the fitting curves (i.e., solid curves) match very well with experimental data (i.e., symbols) over several decades of injected

charge density and stress time, respectively. In addition, $|\Delta V_{fb}|$ saturates at longer stress time when the magnitude of the stress voltage is higher than |–3.5V|. These features support our assumption of filling existing hole traps in the high-k gate stacks. Since the parameter β is a measure of the distribution width, the value of around 0.184 for all stressing conditions indicates that hole traps in the high-k gate stacks possess larger distributed capture cross section than that of electron traps (c.f., $\beta \sim 0.32$) [12], while σ_0 is nearly independent of voltage and its value is about 1.5×10^{-14} cm^2. Moreover, it is worthy to note that $|\Delta V_{fb}|$ increases again as the N_{inj} is larger than 2×10^{20} cm^{-2} s at $V_g = -4.2$ V. This phenomenon is thought to be due to additional traps creation.

Disregarding the success of the distributed capture cross section model in describing the flatband voltage shift during CVS, it is still necessary to explain why the hole trapping is more likely to take place in our high-k gate stacks. We believe this can be explained by the resultant band diagram of the TiN/HfO_2/SiO_2 gate stack system under $V_g = -4.2$ V stress, as illustrated in **Fig. 2.17**. The parameters, including physical thickness, band offsets and voltage drops across the individual insulators were determined based on our TEM analyses (as shown in **Fig. 2.10** (a)) and the work function of TiN (~ 4.8 eV) was adopted from previous researches [15]-[16]. From the band diagram, it can be seen that the probability of hole tunneling from the substrate is much higher than that of electron tunneling from the gate because of the shorter tunneling distance. Therefore, the leakage current is dominated by hole injection. To reinforce this argument, the characteristics of the gate current density (J_g) as a function of injected charge density (N_{inj}) for different CVS conditions were monitored and shown in **Fig. 2.18**. It can be seen that the leakage current decreases with increasing stress time for various applied voltages. This is consistent with hole dominance in the gate stack because only the trapped holes can cause leakage increase

if the hole current is the dominant component.

In order to investigate the detrapping characteristics of filled holes, we used opposite polarity of stress to detrap the hole charge in the HfO_2 film. It is found that positive voltage (V_g = +3.6 V) does not change the flatband voltage, indicating the positive voltage does not cause damages and charge trapping, as shown in **Fig. 2.19** (a). Therefore, we first apply a –3.6 V on capacitor for 1000s, causing some hole charges to be trapped in HfO_2 film. Then, we apply a +3.6 V for 1000s in an effort to de-trap the hole charges. As shown in **Fig. 2.19** (b), it is observed that the trapped charges can not be totally detrapped even after a duration of 1000s by positive voltage. This implies that hole trapping efficiency is more efficient than hole detrapping efficiency.

2.5 Pre-Existing Charges and Current Transport Mechanism

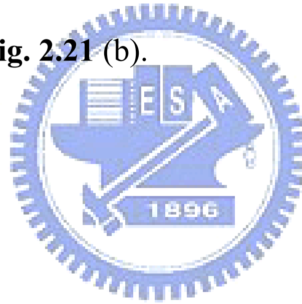
In **Fig. 2.20 (a)**, the *J-V* curves of fresh devices are measured under various temperatures from 25 to 150°C. The current remains essentially constant with increasing temperature. This indicates that the gate leakage current is not related to the traps. However, from previous sections, we know that flatband voltage shifts toward negative gate voltage, and the leakage current reduces under constant voltage stress. Besides, charge trapping is a filling behavior. Therefore, we first stress the sample under –4 V, 600s stress, and measure the *J-V* curves. It can be obviously seen that the current now increases with increasing measuring temperature. This again proves that the traps are latent and can be activated by applying a stress. Furthermore, traps which are passivated during processing are activated; meanwhile, the amount of holes which fill the pre-exiting traps (i.e., as-fabricated traps) is dependent on the stressing time.

Next, we investigate the current transport mechanism. The current from

Frenkel-Poole emission is of the form:

$$J=B*E\exp\left[\frac{-q(\phi_B-\sqrt{qE/\pi\varepsilon_i\varepsilon_{HfO_2}})}{k_BT}\right] \quad (3\text{-}2)$$

where B is a constant in terms of the trapping density in the HfO_2 film, φ_B is barrier height , E is the electric field in HfO_2 film, ε_i is free space permittivity, ε_{HfO2} is HfO_2 dielectric constant, k_B is Boltzmann constant, T is the temperature measured in Kelvin. **Fig.2.21** (a) shows ln (J/E) as a function of 1000/T with different V_{stack} (=V_g-V_{fb}), and the linearity indicates that the conduction mechanism of leakage current after stress follows Frenkel-Poole emission. We found the dielectric constant of HfO_2 can be calculated and the value is 15.6. The value is very close to the estimated value from HRTEM image, which is 14.7. Moreover, the calculated barrier height for holes is around 0.42 eV, as shown in **Fig. 2.21** (b).



2.6 Summary

In this chapter, the characteristics of the AVCVD-deposited HfO_2 films with pre-treatment by NH_3 or N_2O and subsequently subjected to “conventional” N_2 RTA or “spike” N_2 RTA are presented. The samples with conventional RTA show much lower leakage current, lower frequency dispersion, and smaller hysteresis than as-deposited, spike RTA as well as no RTA samples because of a thicker interfacial layer. Therefore, RTA is still an essential process after pre-treatment to densify nitrided interfacial layer. HRTEM images reveal that even though “conventional” N_2 RTA can effectively decrease the leakage current, the formation of an interfacial layer could defeat the whole purpose of achieving thin EOT. In contrast, spike RTA does not seem to be a proper method to densify nitride film because of large thermal stress.

We have also investigated the reliability issues of HfO_2 samples subjected to NH_3

or N_2O HDP plasma surface pre-treatments, and compared with those of HfO_2 control samples with conventional oxide interfacial layer. The samples with plasma surface pre-treatment show much lower leakage current, higher breakdown voltage and higher effective breakdown field, due to incorporated nitrogen in the interfacial layer. For time-to-breakdown and charge-to-breakdown characteristics, NH_3 and N_2O plasma pre-treatments show improved and degraded performance over RTO control, respectively.

Next, we have studied hole trapping characteristics in HfO_2/SiO_x gate dielectrics stack. We have proposed that hole trapping occurs through filling of pre-existing hole traps in HfO_2 film, and we have successfully employed continuous capture cross section model to fit our experimental data. The fitting results match well with experimental data, and the fitting parameter β possesses larger distributed capture cross section than that of electron traps. We have also proposed an energy band diagram to illustrate our viewpoint.

Finally, we have studied the current transport mechanism responsible for the leakage current in HfO_2 films. Since the pre-existing (latent) traps were passivated during processing so that the leakage current in the virgin sample is almost independent of the measuring temperature. When we applied a stress to the thin film, these traps will be activated and the samples depict leakage characteristics of Frenkel-Poole emission.

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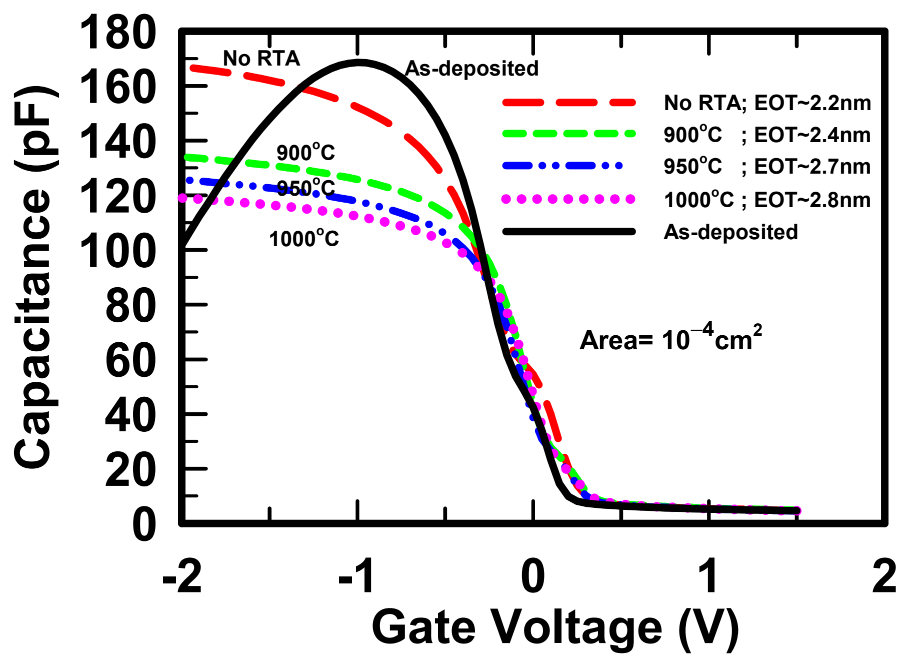
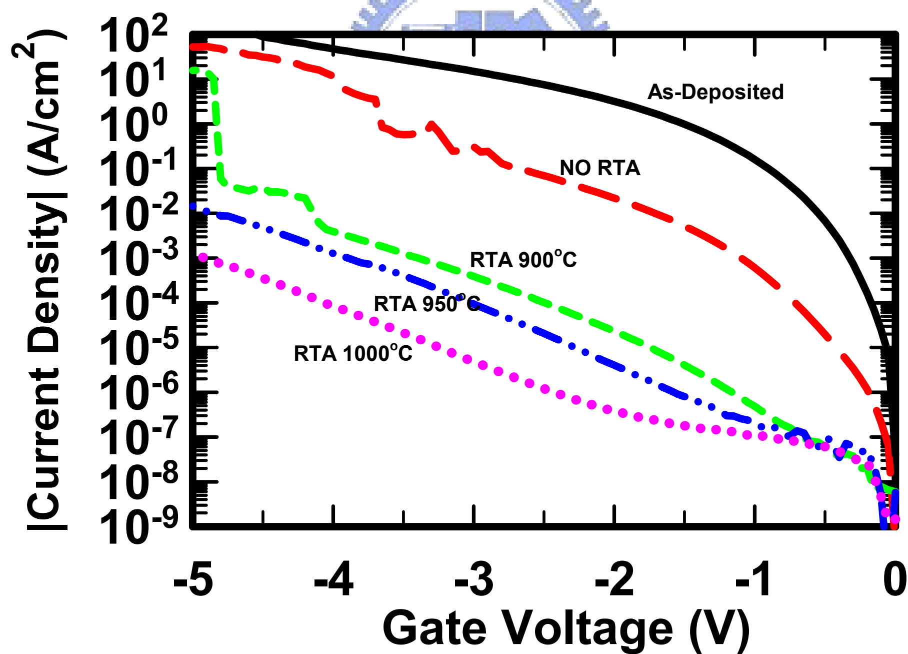


(a)



(b)

Fig. 2.1 (a) C-*V* and (b) *J*-*V* curves of **NH_3** pre-treatment with different N_2 **conventional** RTA temperature.

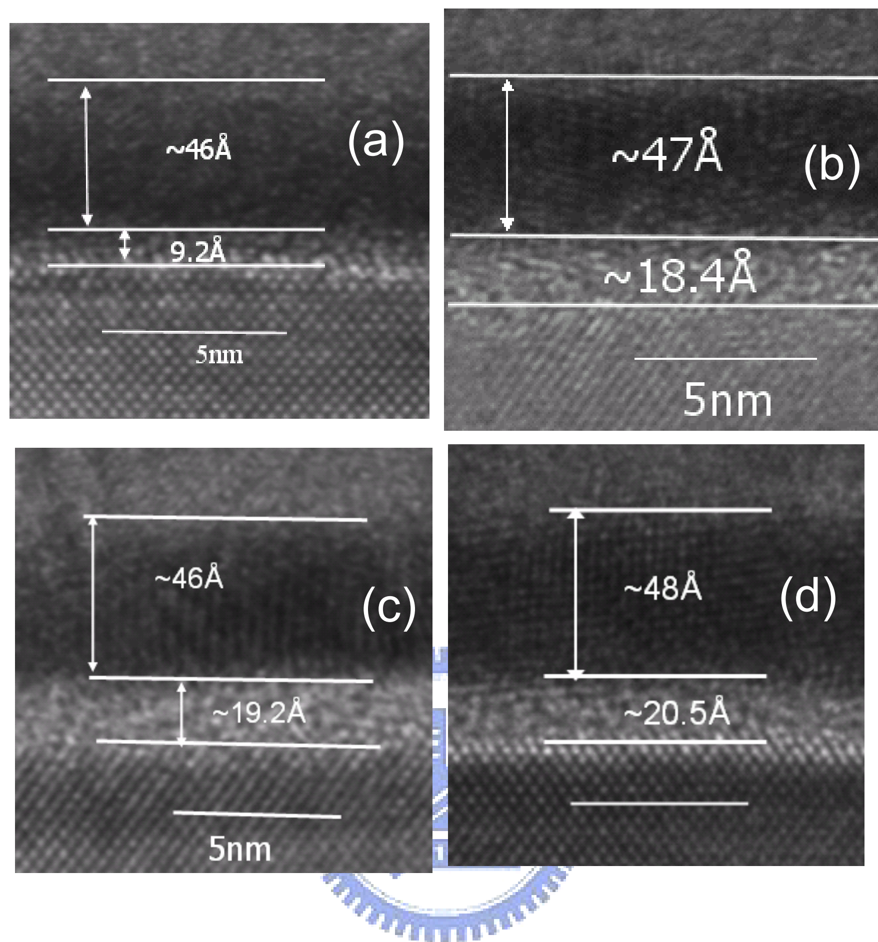
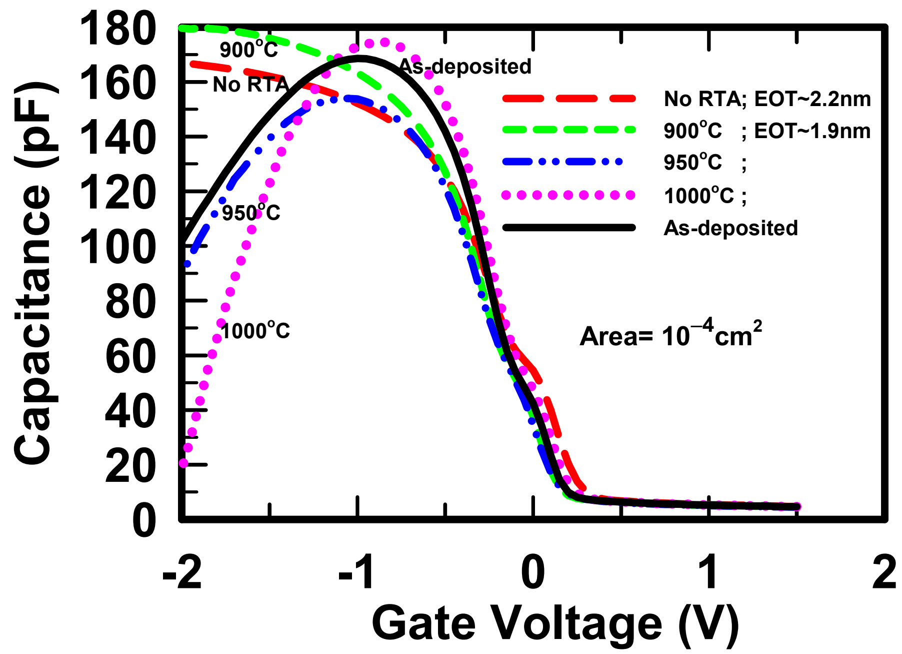
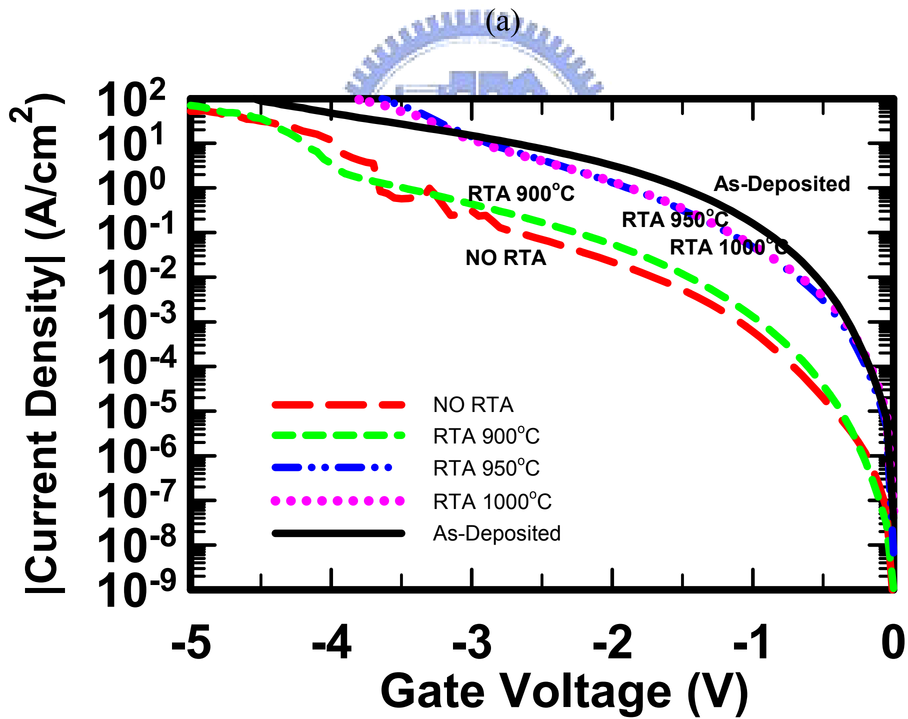


Fig. 2.2 The HRTEM images show the (a) as-deposited sample, and the sample with NH_3 pre-treatment and **conventional** N_2 RTA at (b) 900℃ (c) 950℃ (d) 1000℃ annealing.

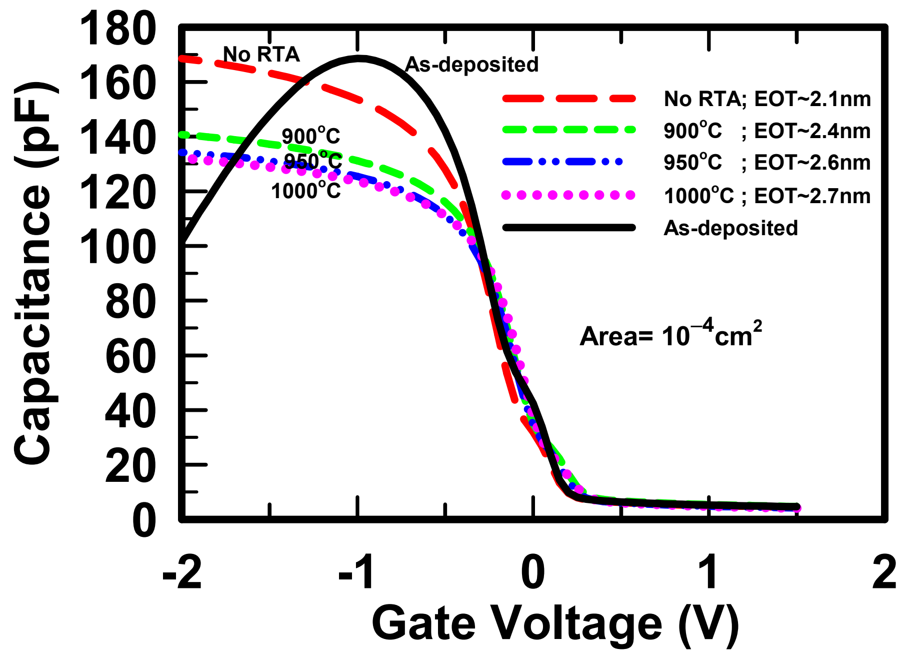


(a)

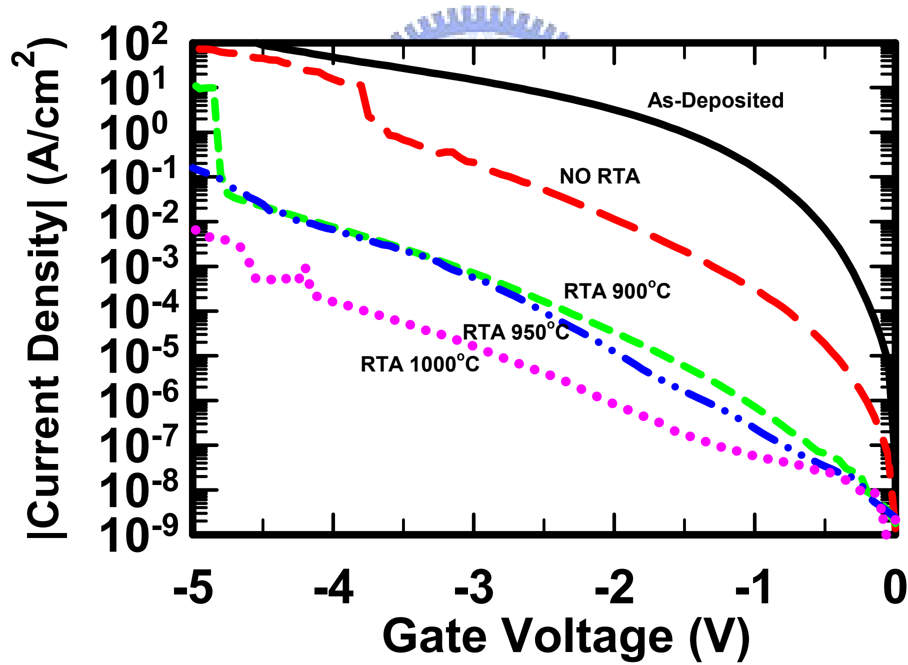


(b)

Fig. 2.3 The (a) *C-V* and (b) *J-V* curves of **NH_3** pre-treatment with N_2 **spike** RTA temperature.

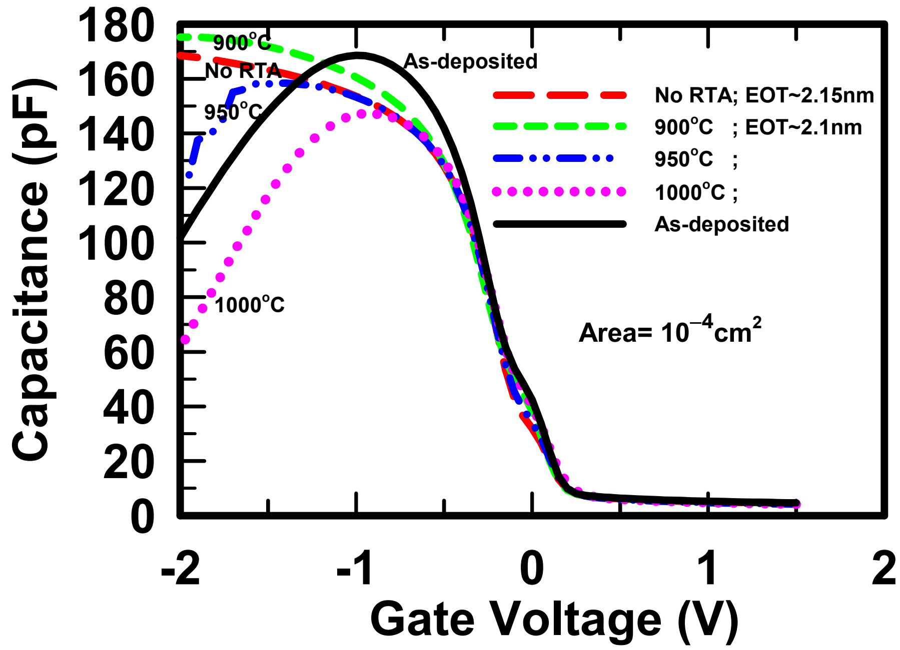


(a)

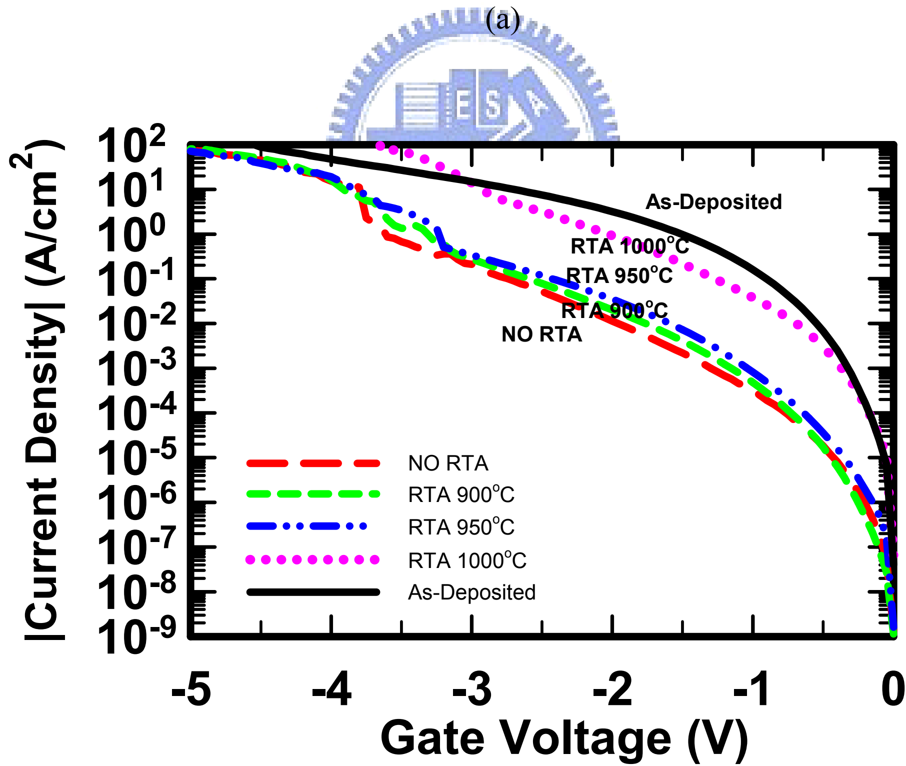


(b)

Fig. 2.4 The (a) *C-V* and (b) *J-V* curves of **N_2O** pre-treatment with N_2 **conventional** RTA.

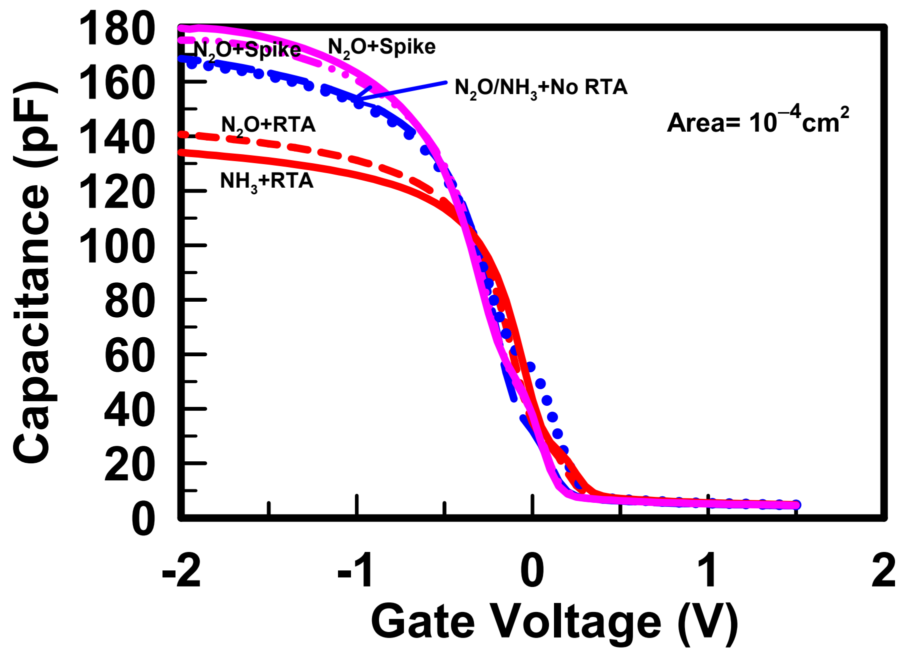


(a)

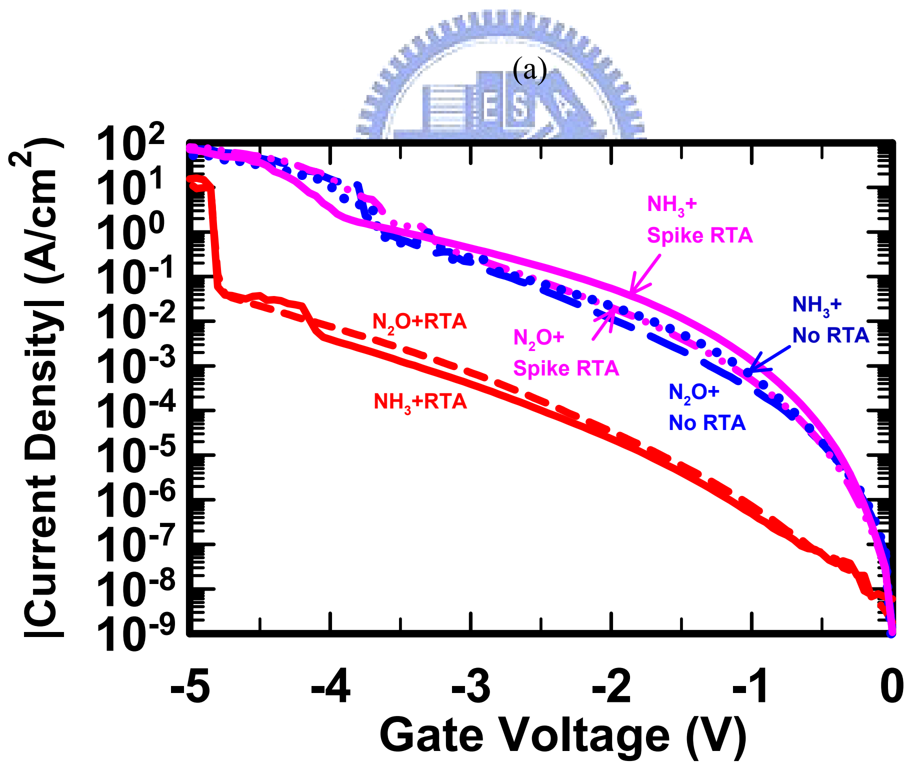


(b)

Fig. 2.5 The (a) *C-V* and (b) *J-V* curves of $\mathbf{N_2O}$ pre-treatment with N_2 **spike** RTA.



(a)



(b)

Fig. 2.6 The (a) *C-V* and (b) *J-V* curves of 900℃ N_2 annealing with N_2O/NH_3 plasma pre-treatment by conventional RTA and spike RTA.

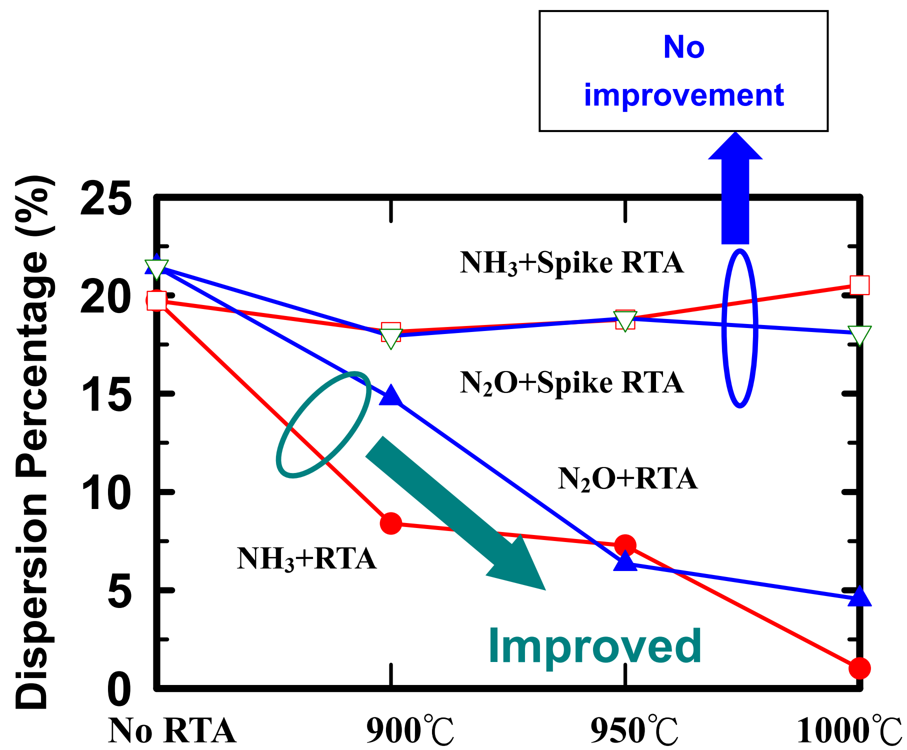


Fig. 2.7 Frequency dispersion as a function of various RTA temperature for N_2O and NH_3 pre-treatment samples.

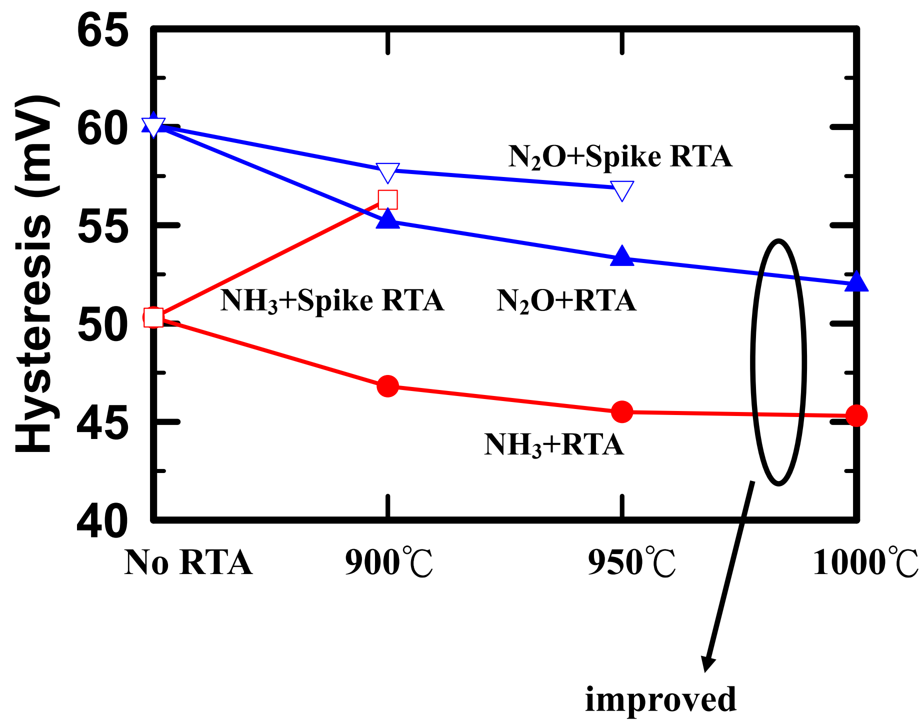
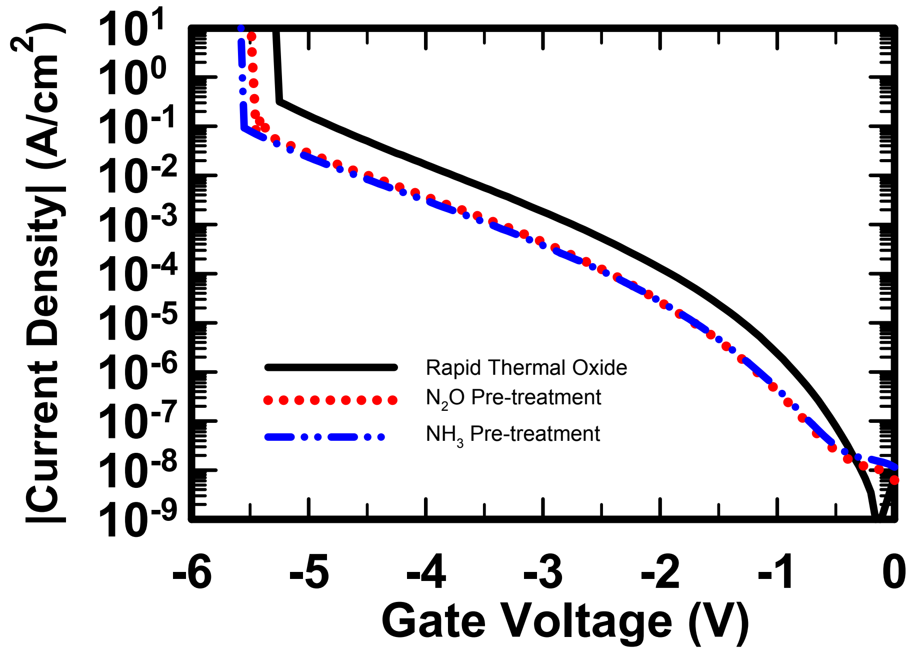
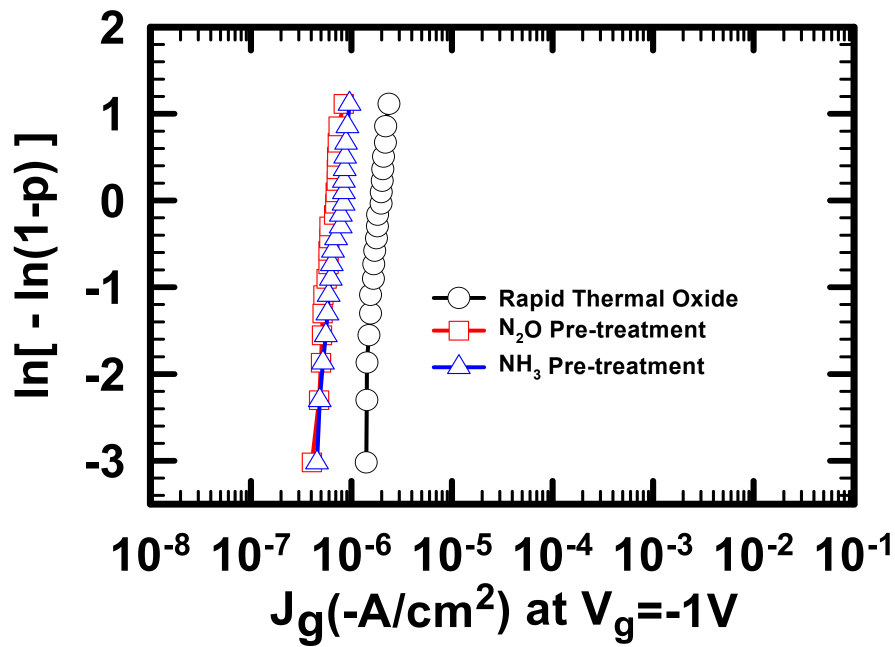


Fig. 2.8 Hysteresis seems to be improved by using conventional N_2 RTA following the interfacial layer formation. The formation of interfacial layer by using NH_3 plasma treatment shows the better hysteresis characteristics.



(a)



(b)

Fig. 2.9 (a) The *J-V* characteristics with different I.L (RTO, N_2O, NH_3) treatment method at same post-treatment annealing (900°C). (b) The Weibull plot shows the gate current densities at Vg= −1V with different I.L. treatment method (RTO, N_2O, NH_3).

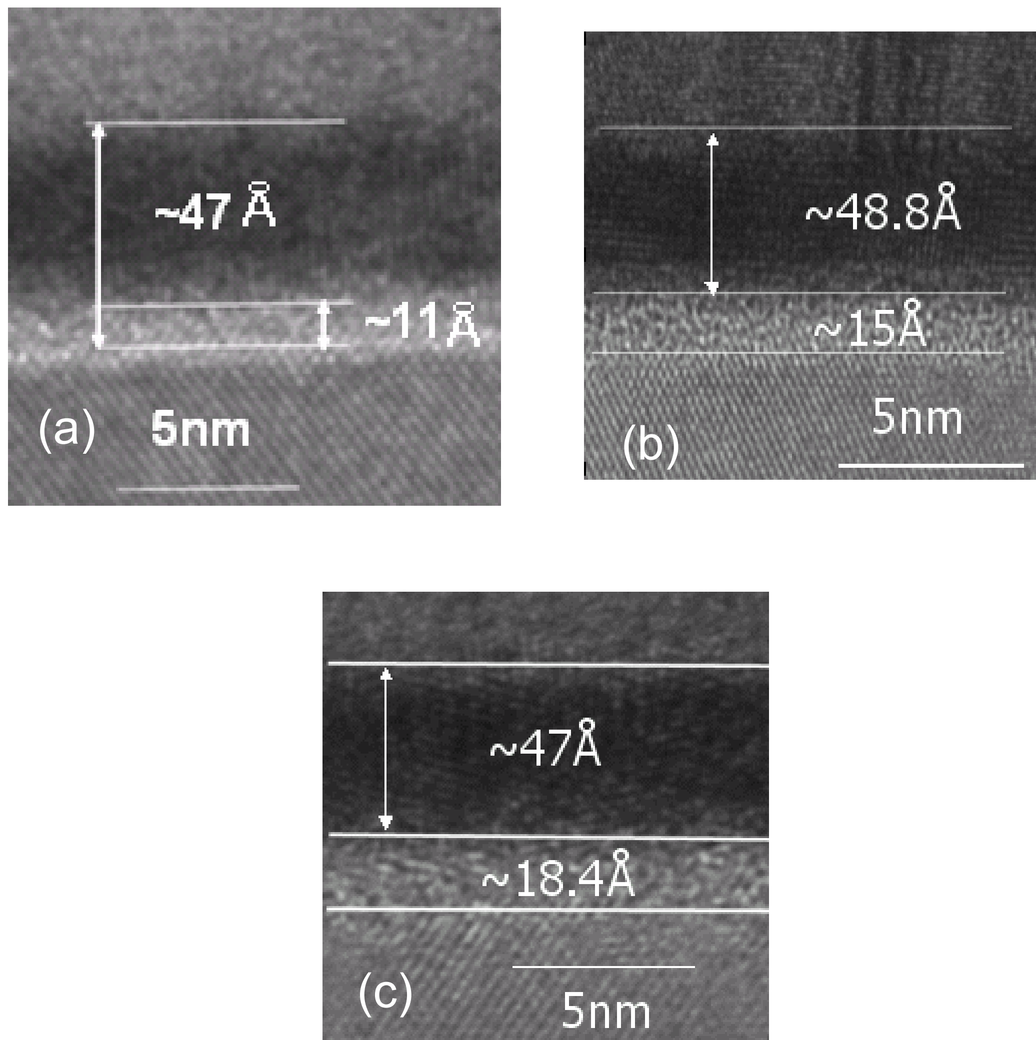


Fig. 2.10 The TEM images of the HfO_2 with (a) RTO I.L.(b) N_2O pre-treatment and 900℃ N_2 RTA annealing. (c) NH_3 pre-treatment and 900℃ N_2 RTA annealing.

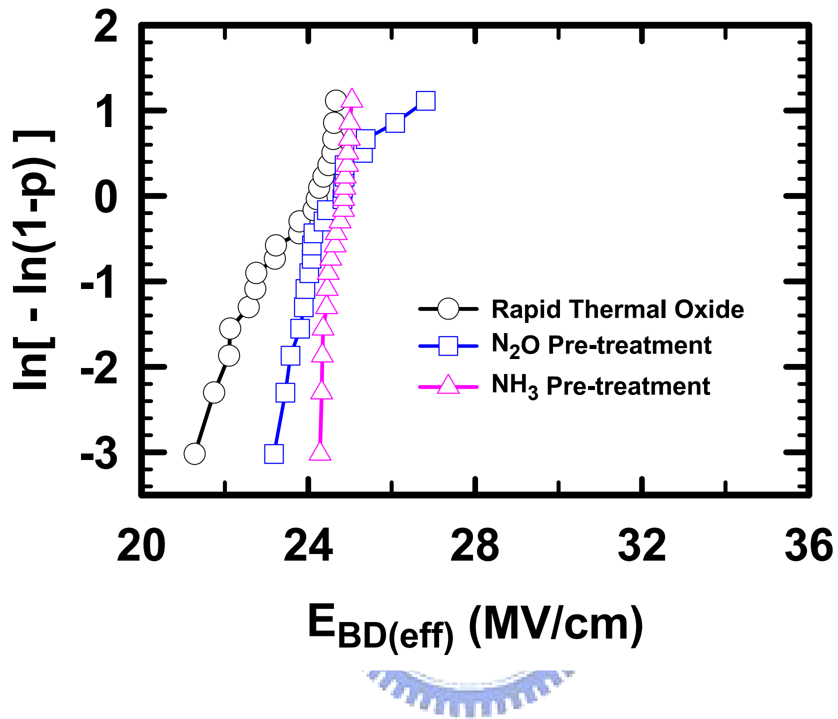
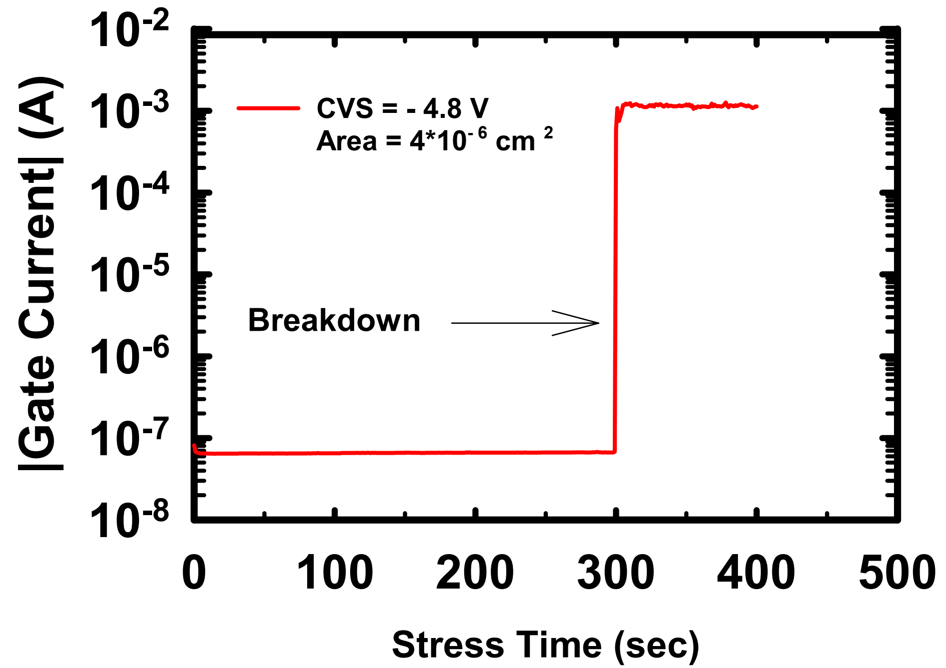
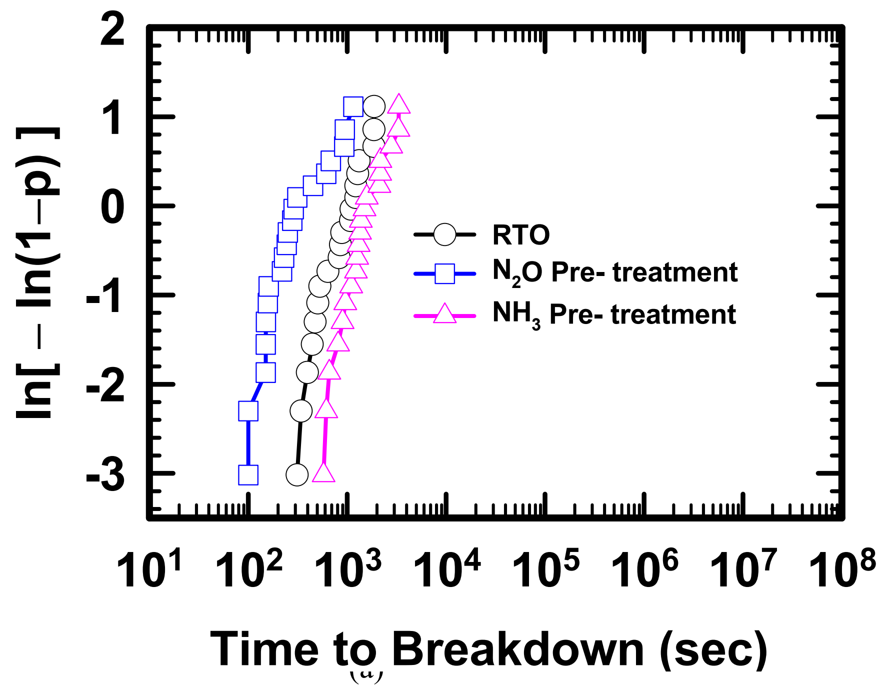


Fig. 2.11 The Weibull plot shows the effective breakdown field with different I.L. treatment method (RTO, N_2O, NH_3) at same post-treatment annealing (900°C).





(b)

Fig. 2.12 (a) Definition of breakdown for the sample under constant voltage stress (b)The Weibull plot shows the time to breakdown under constant voltage stress with different I.L. treatment method (RTO, N_2O, NH_3) at same post-treatment annealing (900°C).

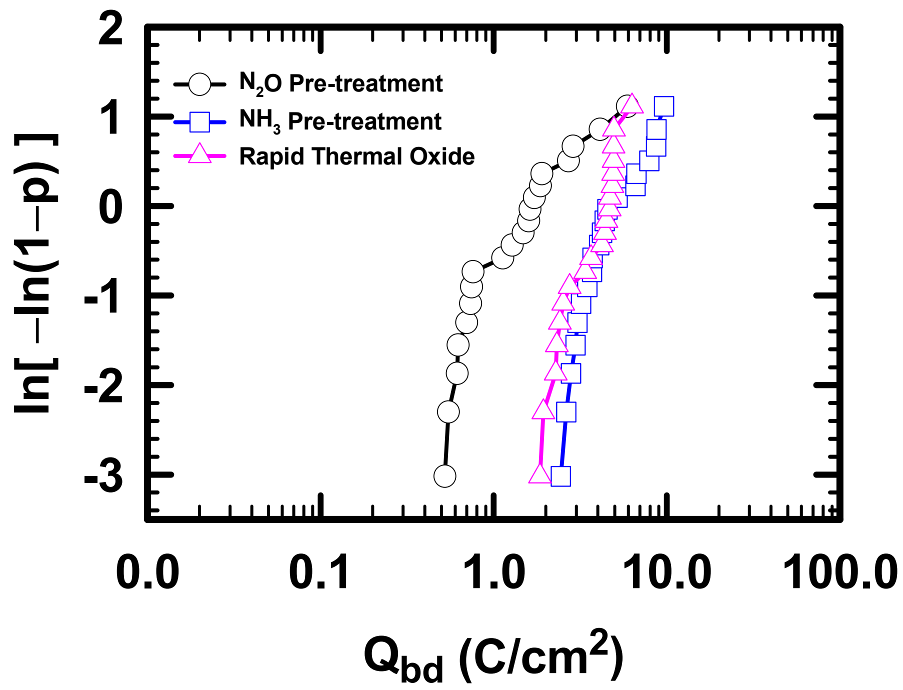


Fig. 2.13 The Weibull plot shows the charges to breakdown under −4.8V stress voltage with different I.L. treatment method (RTO, N_2O, NH_3).

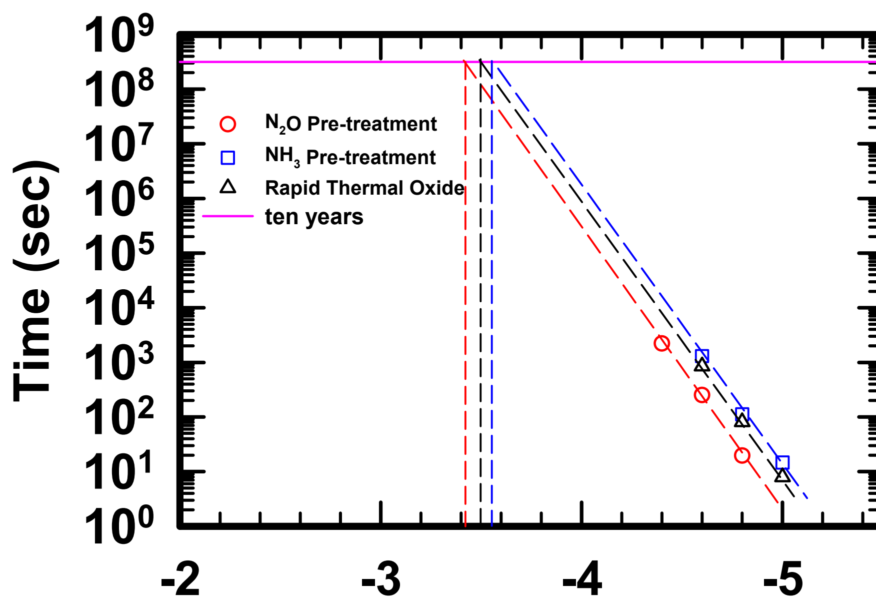
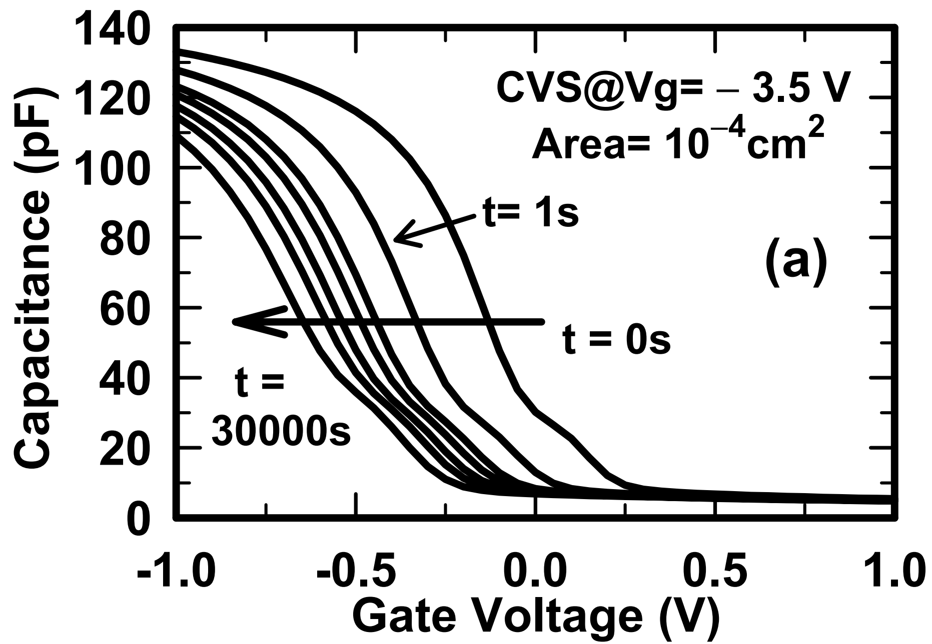


Fig. 2.14 10-year lifetime projection for the samples with different I.L. treatment method (RTO, N_2O, NH_3) at same post-treatment annealing (900°C).



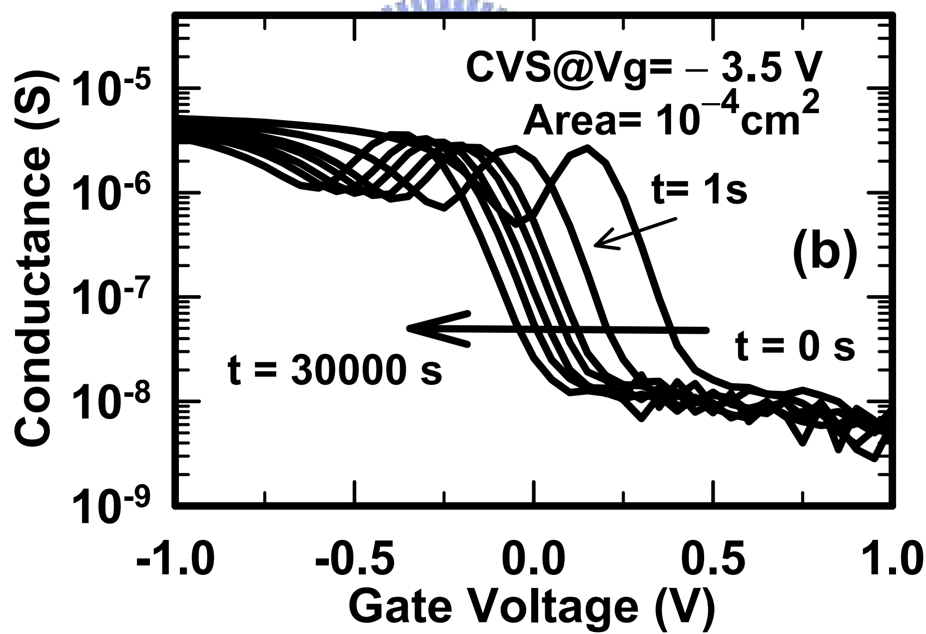
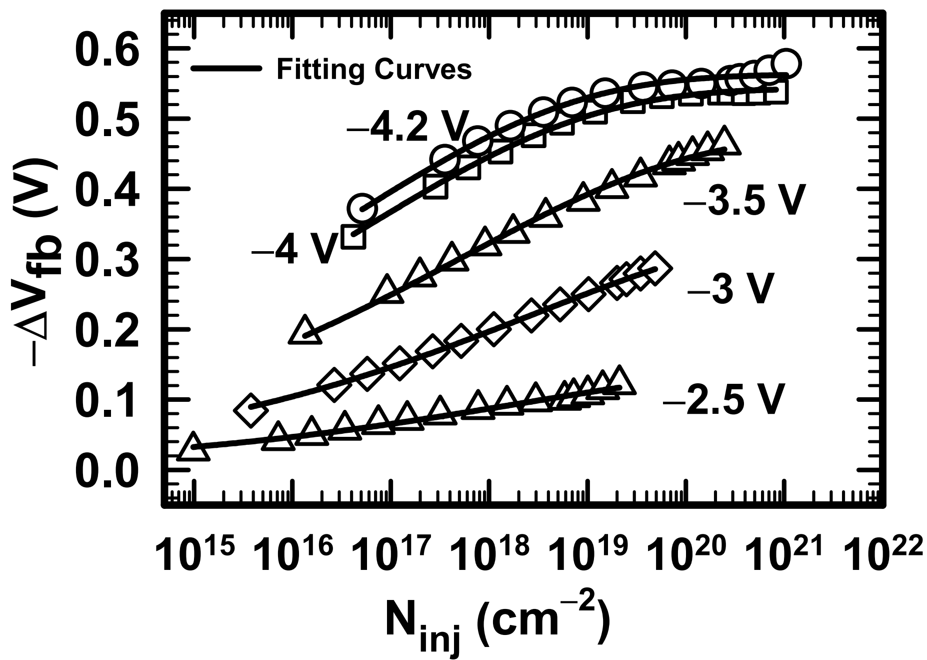
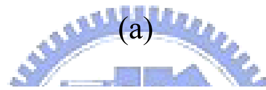
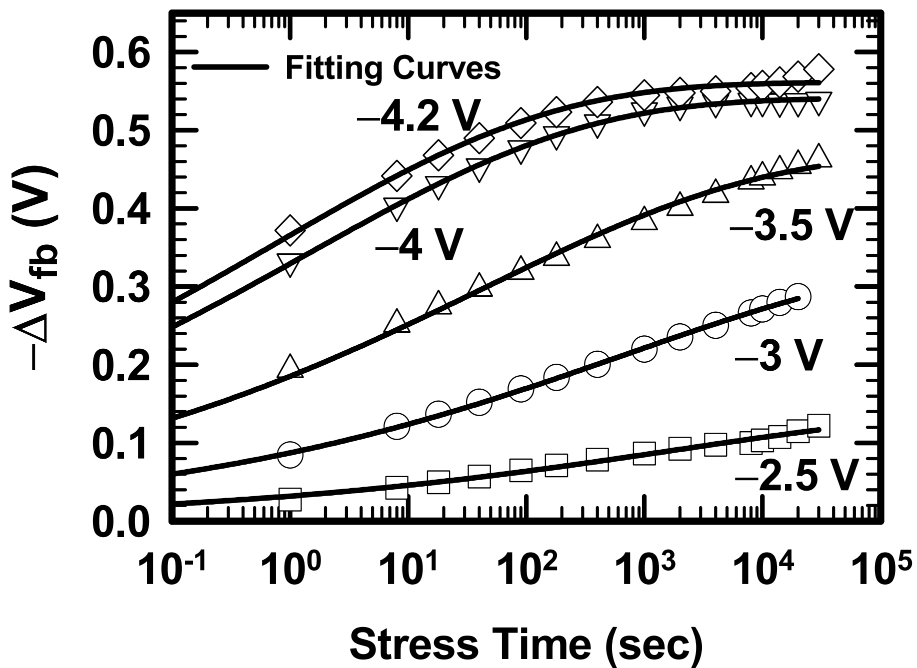


Fig. 2.15 (a) *C-V* curves and (b) *G-V* curves measured at 100 kHz with increasing stress time as a parameter. The stress voltage (V_g) was – 3.5 V. The curve labeled t = 0 s corresponds to the data before stressing.



(a)





(b)

Fig.2.16 Dependence of flat band voltage on (a) injected charge density (b)stress time at various stress voltages; symbols are measured data; solid curves are fitting curves.

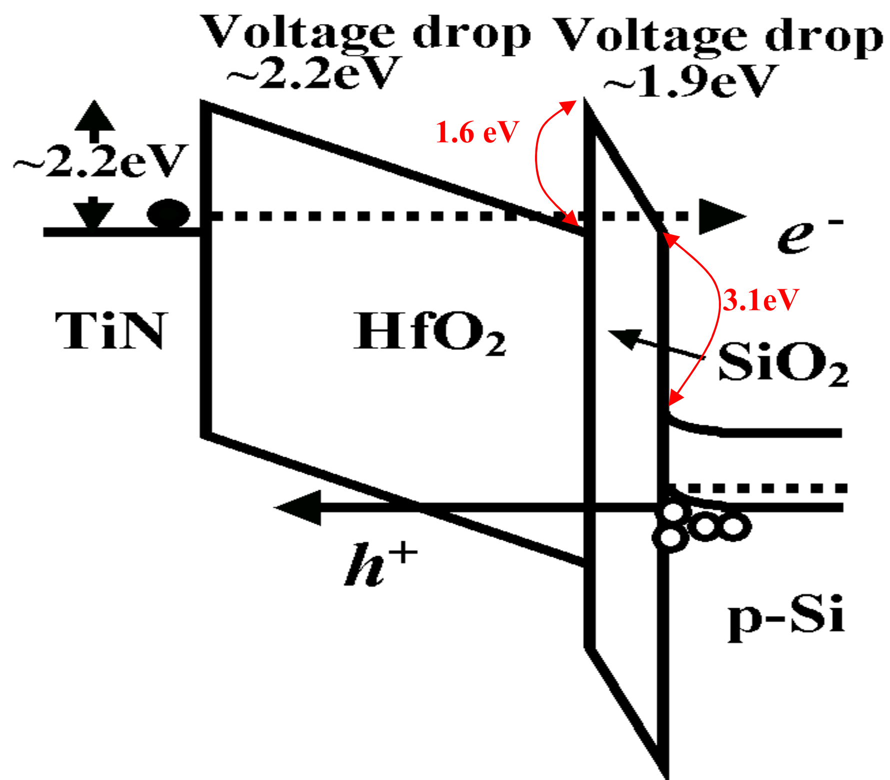


Fig. 2.17 Energy diagram of HfO_2/SiO_2 gate stack capacitor with mid-gap TiN metal gate electrode under constant voltage stress ($V_g = -4.2$ V).

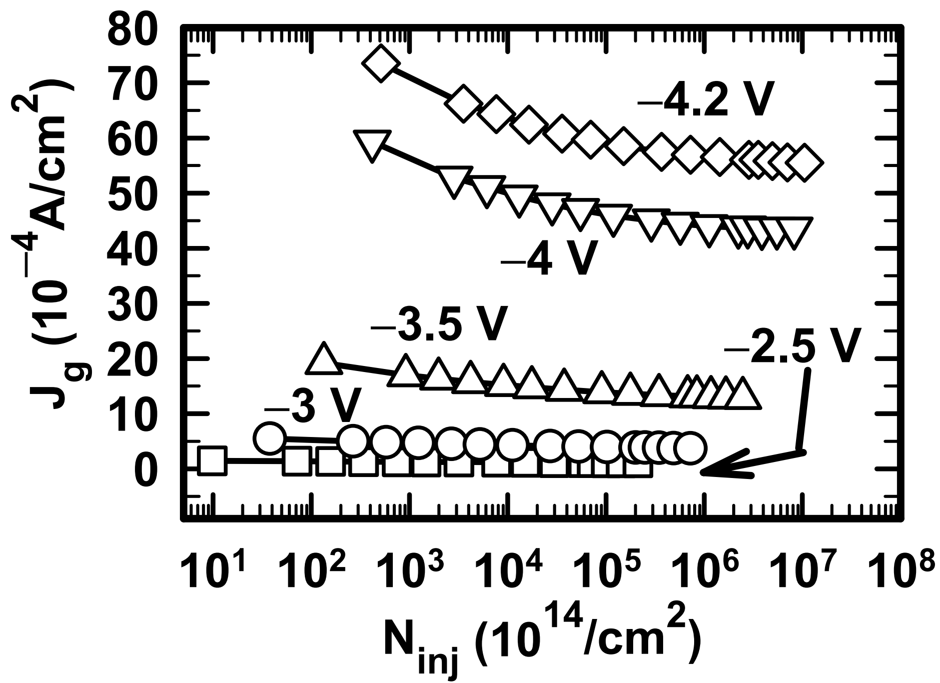
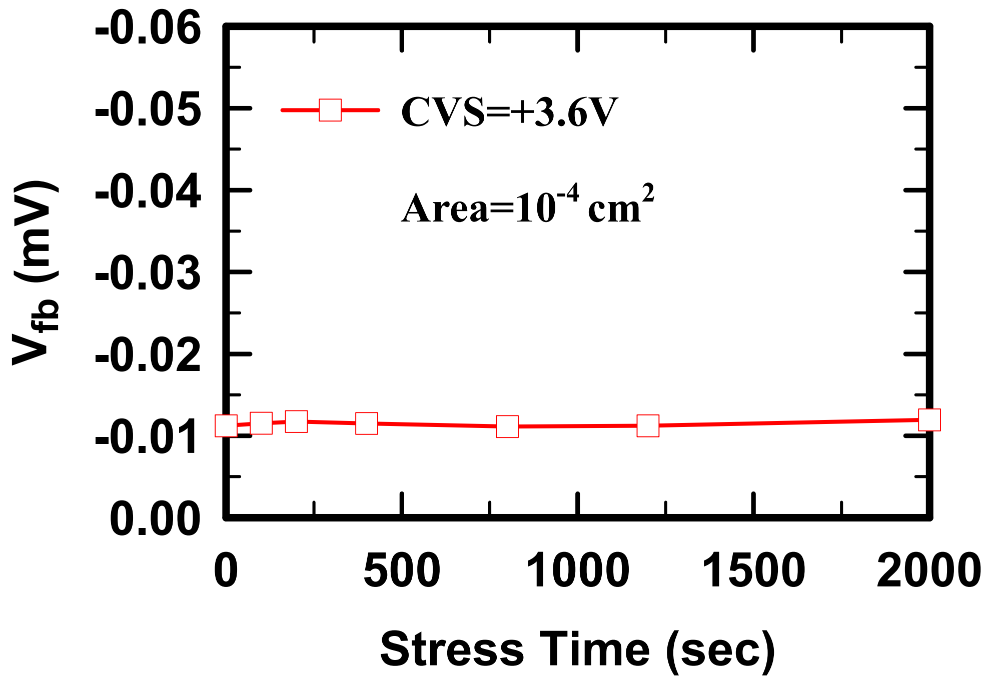
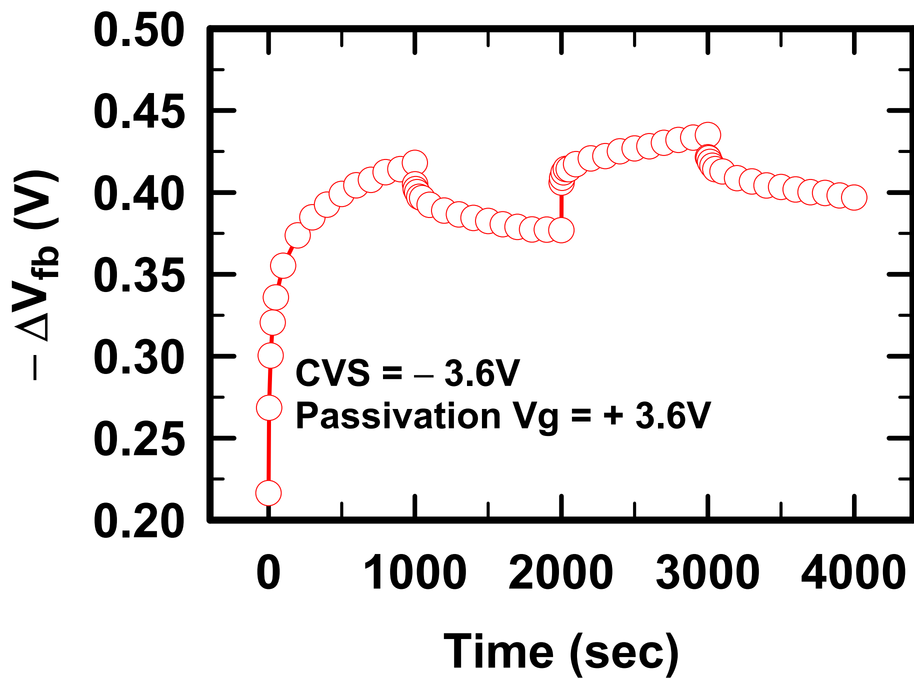


Fig. 2.18 Gate current density as a function of injection charge density for various stress voltages.

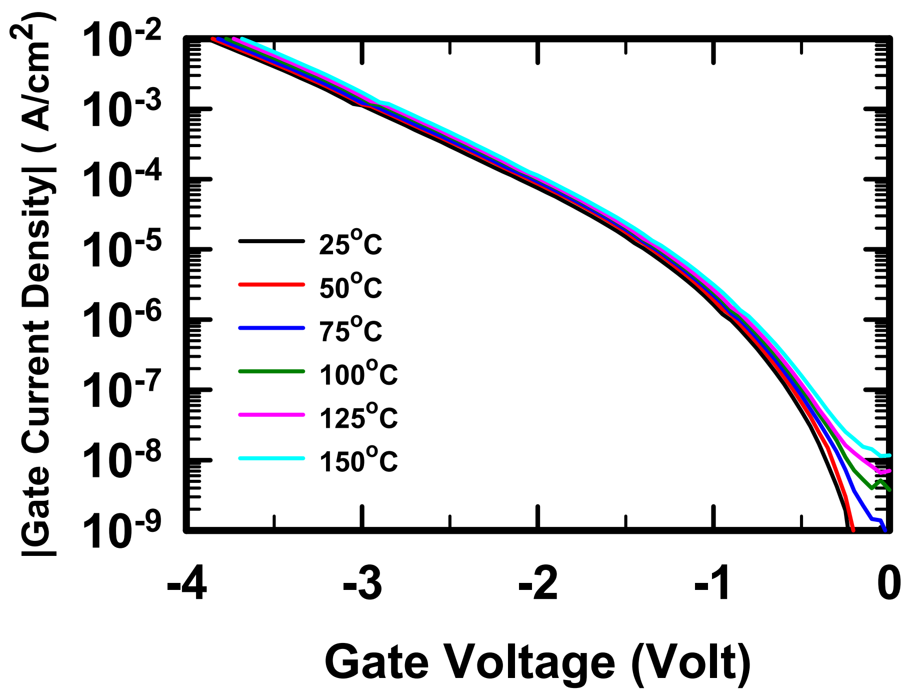


(a)

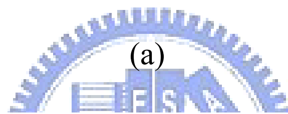


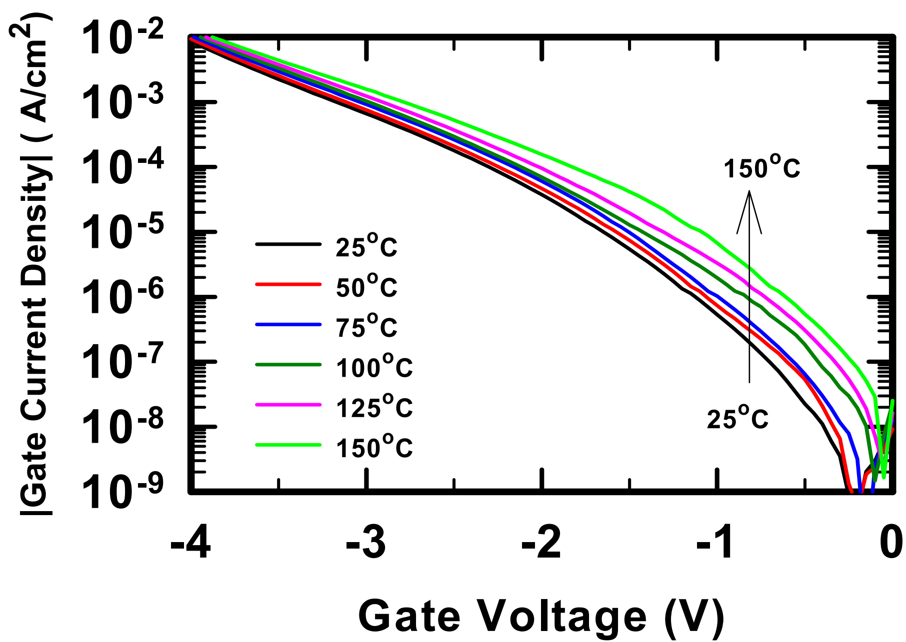
(b)

Fig. 2.19 (a) Flat band voltage versus stress time under positive constant voltage stress, and (b) Flat band voltage shift versus stress time under dynamic stressing with stress and passivation duration both 1000 sec.



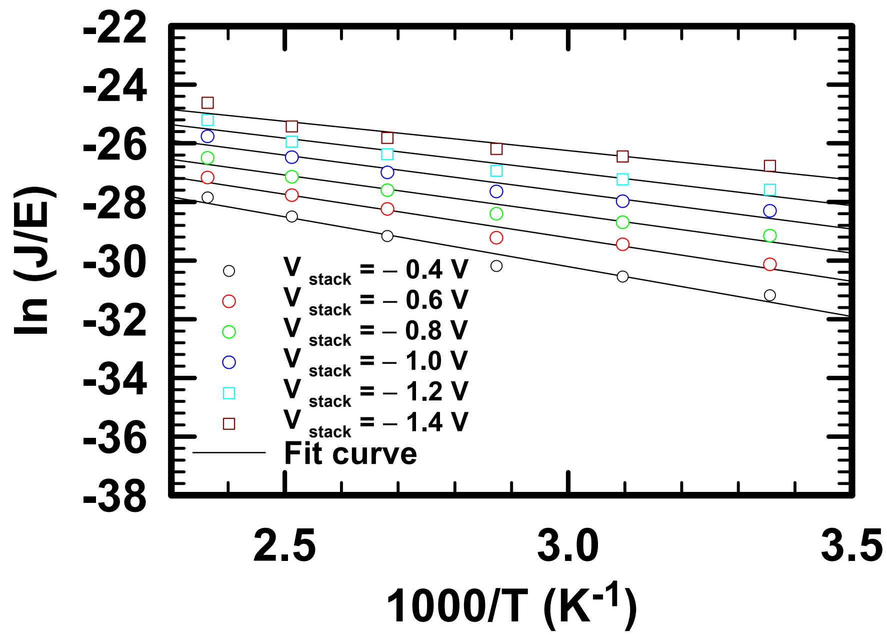
(a)





(b)

Fig. 2.20 (a) The *J-V* curves measurement under various temperatures from 25℃ to 150℃ (a) before and (b) after stress of – 4.0V 600s.



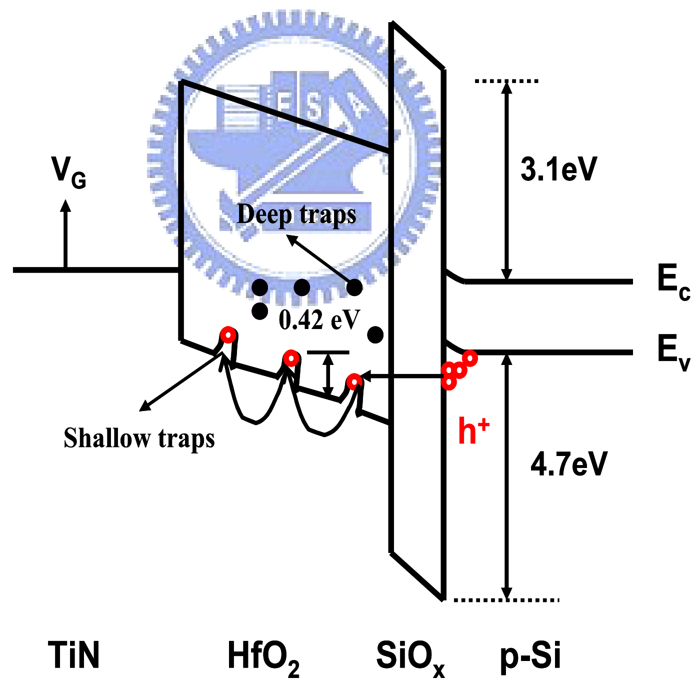


Fig. 2.21 (a) ln (*J/E*) v.s. 1000/T under different HfO_2/ SiO_x stack voltage, and the symbols are experiment data and the solid line are fit curve. (b) Energy band diagram of HfO_2/SiO_x stack to illustrate the conduction mechanism of Frankel-Poole emission.