Chapter 3

Effects of low-temperature NH_3-treatment on the characteristics of HfO_2/SiO_2 gate stack

3.1 Background and Motivation

For aggressively scaling devices into nanometer regime, the concomitant thinning of SiO_2 gate dielectric has been approaching its physical and electrical limits. The main hurdle encountered is the intolerably huge leakage current caused by the direct quantum tunneling of carriers through these ultra thin oxides. Recently, high-k materials are extensively studied to take advantage of their capability of maintaining the drive current while substantially suppressing the leakage current due to the increased physical thickness at the same equivalent oxide thickness (EOT). Among them, HfO_2 is highly attractive owing to its relatively high dielectric constant (~25), sufficiently large band gap (~ 5.9 eV), suitable tunneling barrier height for both electrons and holes (>1 eV), and thermal compatibility with contemporary CMOS processes.

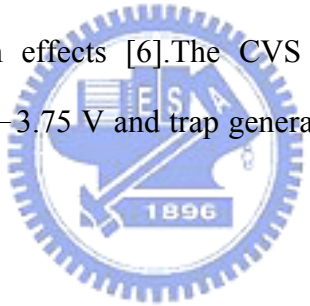
Nitridation of the Si surface by high-temperature (600~700°C) NH_3-treatment prior to the deposition of the high-k gate dielectrics has been shown to be effective in not only suppressing the undesirable interfacial layer formation, which is helpful in minimizing the EOT value, but also preventing the boron penetration [1]-[2].

However, nitrogen can readily diffuse through the high-k films and pile up at the interface at such high temperatures, resulting in higher densities of the interface states and near-interface bulk traps, which in turn lead to a larger hysteresis and channel mobility degradation [2]-[5]. In this study, therefore, we used the LTN process immediately after the deposition of HfO_2 thin films to suppress the diffusion of nitrogen in order to achieve high-quality gate dielectrics with low defect densities both at the interface and in the bulk without causing significant increase in EOT. We found that the incorporation of LTN treatment does not cause additional growth of the pre-existing interfacial layer during subsequent high temperature annealing step. Further, the LTN treatment also improves the electrical properties of the HfO_2/SiO_2 gate stack, including lower interface defect density, and less frequency dispersion. Moreover, the LTN treatment can remarkably reduce the trap generation in the HfO_2/SiO_2 gate stacks when subjected to high stressing conditions, and the increase of the gate leakage with subsequent higher temperature PDA.

3.2 Experimental

Metal-oxide-semiconductor (MOS) capacitors were fabricated on p-type (100)-oriented silicon wafers with resistivity of 8~10 Ω-cm utilizing conventional local oxidation of silicon (LOCOS) isolation. After HF-last dipping, a thin oxide layer of approx. 1.5nm was grown in an O_2 ambient at 800°C, at a ramping rate of 200 °C/sec, by rapid thermal annealing (RTA). Next, an HfO_2 film of approximately 4 nm was deposited at a substrate temperature of 500°C by atomic vapor deposition (AVD^{TM}) in an AIXTRON Tricent® system. Prior to the PDA treatment, some samples were subjected to the LTN treatment in a pure NH_3 ambient at a substrate temperature of 400°C for 5 minutes in 30 mbar ambient. Then, all wafers were

subjected to the PDA treatment, either at 600°C or 700°C, in a N_2 ambient for 60 sec. A 200nm TiN electrode was subsequently sputtered and patterned to form the gate electrodes. Afterwards, aluminum was sputtered on the wafer backside to form backside electrode. In order to clearly study the effects of LTN, no other anneal treatments were performed after backside electrode formation. High resolution transmission electron microscopy (HRTEM) was used to monitor the physical thickness of the gate stacks. For electrical analysis, an Agilent 4284, a precision impedance meter, was used for *C-V* measurement, and a semiconductor parameter analyzer, Agilent 4156A, was used for current-voltage (*I-V*) measurements and constant voltage stress (CVS). The EOT values of the gate stacks were estimated from 100 kHz *C-V* measurements, using the North Carolina State University CVC method without considering quantum effects [6].The CVS estimation was performed at constant voltage stress V_g = −3.75 V and trap generation rate was evaluated at V_g = −1 V.



3.3 Results and Discussion

Fig. 3.1 (a) –(d) show HRTEM images for the 500°C-deposited HfO_2/SiO_2 gate stacks after various post-deposition treatments. Specifically, **Fig. 3.1** (a) shows the as–deposited film. **Fig. 3.1** (b) shows the film subjected to a 600°C PDA. **Fig. 3.1** (c) shows the film subjected to a 700°C PDA, and **Fig. 3.1** (d) shows the film with LTN treatment and 700°C PDA. We can clearly see that the physical thickness of the interfacial oxide layer does not change significantly even after the high-temperature 700°C-PDA. This indicates that the interfacial thermal oxide is rather stable and is not affected by the LTN. On the other hand, it is observed that the extent of crystallization in the HfO_2 film becomes more apparent with increasing PDA temperature. In

contrast, the film undergoing the LTN treatment prior to the high-temperature PDA of 700°C, as shown in **Fig. 3.1** (d), does not show any evidence of crystallization.

Fig. 3.2 (a) shows the high-frequency (100kHz) *C-V* characteristics of all samples subject to various post-deposition conditions. It is observed that the distortion that occurs in the *C-V* curves can be significantly suppressed with increasing PDA temperature. The origin of the hump near 0 V in the *C-V* curves is believed to be closely related to the presence of fast interface states, since their positions are located in the depletion region [7]. The incorporation of LTN treatment can substantially lower the PDA temperature needed to smoothen the distortion. Moreover, another benefit of the LTN treatment is its capability of suppressing the increase in EOT value even after undergoing high-temperature PDA. This is speculated to arise from an increase in the overall k value of the gate stack because extremely low thermal budget causes less low-k interfacial layer formation [8]. The frequency dispersion rate is displayed in **Fig. 3.2** (b). For the samples without LTN, the frequency dispersion rate worsens upon increasing PDA temperature, while the samples with LTN only depict slight increase with increasing PDA temperature. This trend suggests that there are more defects presented in the HfO_2/SiO_2 gate stack without LTN [9].

The hysteresis widths for the annealed HfO_2/SiO_2 gate stacks with and without LTN are shown in **Fig. 3.3**. Obviously, the LTN treatment leads to smaller hysteresis. Due to the serious distortion in the *C-V* curves for the as-deposited samples with/without LTN, as well as the 600°C-PDA-annealed sample without LTN, their hysteresis values can not be precisely determined and are not shown.

Fig. 3.4 displays the gate leakage current density as a function of gate voltage for the as-deposited and PDA-annealed HfO_2/SiO_2 gate stacks, both with and without LTN. The magnitude of leakage current density increases monotonically for the samples without LTN with increasing PDA temperatures. This trend is thought to be

caused by the crystallization of HfO_2 thin films at higher PDA temperatures [10]. Similar to the previous results, the LTN can effectively suppress the leakage current increase after high-temperature PDA, because nitrogen incorporation can help to improve the thermal stability of HfO_2 and increase the crystallization temperature.[1-4]

Fig. 3.5 shows the dependence of gate leakage current density on the measuring temperature for the HfO_2/SiO_2 gate stacks annealed at 700°C PDA, without (**Fig. 3.5** (a)) and with (**Fig. 3.5** (b)) LTN treatment. Without LTN treatment, the conduction mechanism in the resultant gate dielectrics is related to Frenkle-Poole emission or trap-assisted tunneling [11]-[12]. While the conduction mechanism with LTN treatment is more likely to be related to Fowler-Nordheim conduction, since the variation of the gate leakage with varying measuring temperature is significantly suppressed. This result strongly suggests that there are fewer defects in the LTN-treated sample, which might be owing to less grain boundaries as a result of better thermal stability and/or the passivation of incomplete bonds in the bulk by the nitrogen atoms [13].

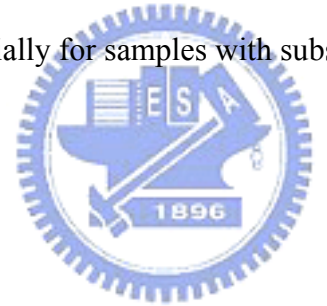
The Weibull distributions of the dielectric breakdown voltage for the HfO_2/SiO_2 gate stacks are shown in **Fig. 3.6**. It is evident that with nitrogen incorporation, the LTN samples exhibit higher breakdown voltages. More importantly, the samples subjected to the combination of LTN and 700°C PDA exhibit the highest breakdown voltage among all splits, while those without LTN display increasingly severe degradation in the breakdown voltage as the PDA temperature increases. Again, we hypothesize that the bond network of the HfO_2 film is strengthened by the nitrogen incorporation during high temperature PDA process, similar to the case in SiO_2. On the other hand, the weakness caused by the high temperature annealing for the samples without LTN echoes the fact that the crystallization of HfO_2 will create more grain boundaries and those boundaries can be easily broken during high field stress.

Fig. 3.7 shows the *J-V* characteristics for the samples subjected to 700°C PDA during constant voltage stress (CVS). The stress voltage was – 3.75 V. It is clearly observed that the gate leakage current increases over stress time at low voltage region. In order to clarify the mechanism responsible for the gate leakage increase after constant voltage stress the *C-V* curves of a MOS capacitor were measured after different CVS times (**Fig. 3.8**). Here, it has to be noted that the CVS was periodically interrupted to measure the *J-V* and *C-V* characteristics. One observes that the *C-V* curve gradually shifts toward negative voltage as the stress time progresses. This tendency indicates that hole trapping occurs during constant voltage stress. **Fig. 3.9** (a) illustrates the energy band diagram of the gate stack under V_g = — 3.75 V stress, i.e., gate injection. The parameters, including physical thicknesses, band offsets, and the voltage drops across the individual insulators were determined based on our TEM analyses and the work function of TiN (~ 4.8 eV) reported in previous researches [14]-[15]. It can be seen that the probability of hole tunneling from the substrate is much higher than that of electron tunneling from the gate because of the shorter tunnel distance. Therefore, it is reasonable to assume that the leakage current is dominated by the hole injection. For the reason that the hole tunneling current will be impeded by the hole trapping inside the gate stack, the evolution of gate leakage current under CVS will decrease, not increase. Therefore, we conclude that the trap-assisted hole tunneling mechanism is responsible for the increase in gate leakage current, as shown in **Fig. 3.9** (b). Certainly, it belongs to the stress-induced-leakage current (SILC) in the high-k gate stack. SILC is an important concern in scaling of the gate oxide thickness because it can decrease DRAM refresh times, degrade EEPROM data retention, and deteriorate MOSFET off-state power dissipation. It is known that the trap generation rate is an index for SILC [16]. **Fig. 3.10** shows the comparison of the trap generation rate for different samples under CVS of V_g = — 3.75V. Clearly,

the LTN can significantly reduce the trap generation rate and, especially, the sample with a higher temperature PDA of 700°C still exhibits extremely low trap generation rate.

3.4 Summary

The effects of post-deposition low-temperature (~ 400°C) NH_3-treatment on the characteristics of the HfO_2/SiO_2 gate stacks with TiN gate electrode were investigated in this work. Our results indicate that samples subject to the LTN treatment exhibit superior *C-V* characteristics, less frequency dispersion, and lower gate leakage. In addition, the defect density in the bulk and the immunity against trap generations are significantly improved, especially for samples with subsequent 700°C PDA.



References

[1] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi and A. Nishiyama, *Tech. Dig. – Int. Electron Devices Meet.*, **2002**, 849.

[2] H.-J. Cho, C. Y. Kang, C. S. Kang, R. Choi, Y. H. Kim, M. S. Akbar, C. H. Choi, S. J. Rhee, and J. C. Lee, 2003 *Semiconductor Device Research Symposium*, IEEE, p. 68 (2003).

[3] Y. Morisaki, T. Aoyama, Y. Sugita, K. Irino, T. Sugii, and T. Nakamura, *Tech. Dig. – Intl. Electron Devices Meeting.*, **2002**, 861.

[4] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo, and A. Nishiyama, *Tech. Dig. – Intl. Electron Devices Meeting.*, **2001**, 459.

[5] R. Choi, C. S. Kang, B. H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J. C. Lee, in 2001 *symposium on VLSI Technology*, IEEE, NJ, p.15 (2001).

[6] J. R. Hauser and K. Ahmed, in *AIP Conference Proceedings,* American Institute of Physics*,* **449**, 235 (1998).

[7] V. K. Bhat, K. N. Bhat, and A. Subhramanyam, *J. Electron. Mater*. **29**, 399 (2000).

[8] C. S. Kang, H.-J. Cho, K. Onishi, R. Choi, Y. H. Kim, R. Nieh, J. Han, S. Krishnan, A. Shahriar, and J. C. Lee, *Tech. Dig. – Int. Electron Devices Meet.*, **2002**, 865.

[9] S. Ramanathan, C. -M. Park, and P. C. McIntyre, *J. Appl. Phys*., **91**, 4521 (2002).

[10] L. Kang, K. Onishi, Y. Jeon, B. H. Lee, C. Kang, W.-J. Qi, R. Nieh, S. Gopalan, R. Choi, and Jack C. Lee, *Tech. Dig. – Int. Electron Devices Meet.*, **2000**, 39.

[11] M. Houssa, M. Tuominen, M. Naili, V. Afanas'ev, A. Stesmans, S. Haukka, and M. M. Heyns, *J. Appl. Phys*., **87** 8615 (2000).

[12] T. Yamaguchi, H. Satake, N. Fukushima, and A. Toriumi *Tech. Dig. – Int. Electron Device Meet. Tech. Dig.,* **2000***,* 19.

[13] M. Koyama, H. Satake, M. Koike, T. Ino, M. Suzuki, R. Iijima, Y. Kamimuta, A. Takashima, C. Hongo, and A. Nishiyama, *Tech. Dig. – Int. Electron Devices Meet.*, **2003**, 931.

[14] J. Westlinder, T. Schram, L. Pantisano, E. Cartier, A. Kerber, G. S. Lujan, J. Olsson, and G. Groeseneken, *IEEE Electron Device Lett*., **24***,* 550 (2003).

[15] G. S. Lujian, T. Schram, L. Pantisano, J. C. Hooker, S. Kubicek, E. Rohr, J. Schuhmacher, O. Kilpela, H. Sprey, S. D. Gendt, and K. D. Meyer, Proc. ESSDERC. 2002.

[16] D. J. DiMaria and E. Cartier, *J. Appl. Phys*., **78**, 3883, (1995).

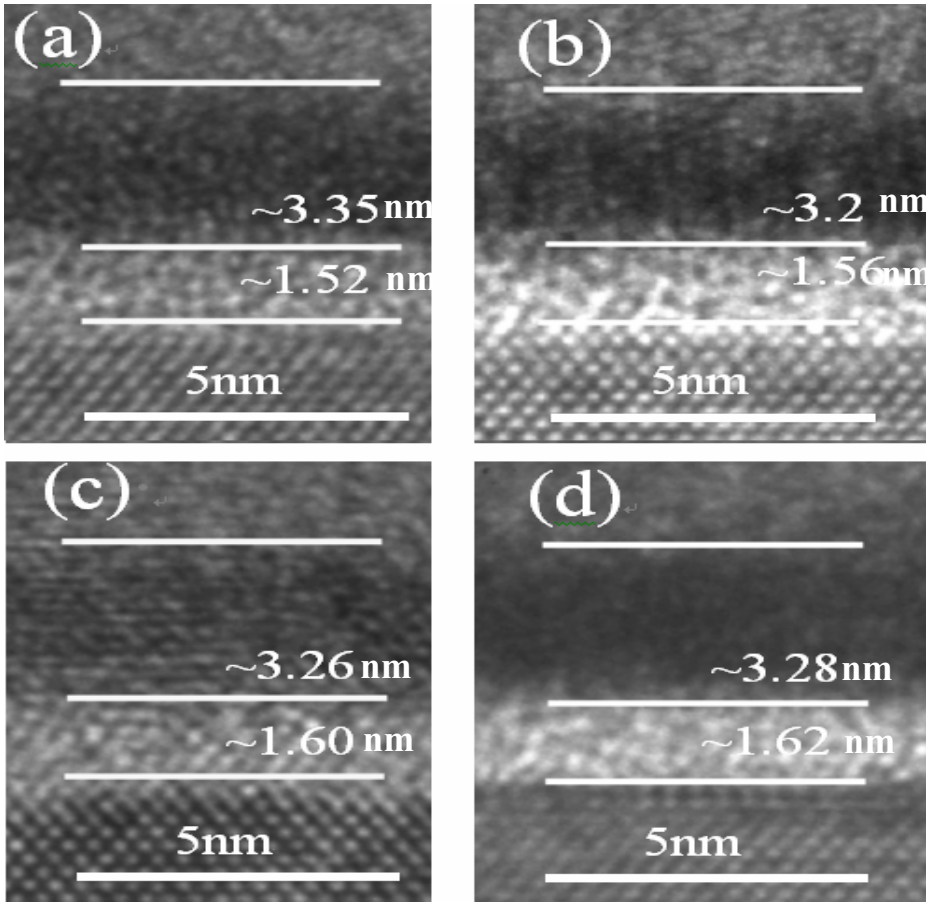


Fig. 3.1 Cross-sectional HRTEM images of the HfO_2/SiO_2 gate stacks (a) for as deposited film; (b) annealed at 600°C; (c) annealed at 700°C; (d) annealed at 700°C and subjected to LTN treatment.

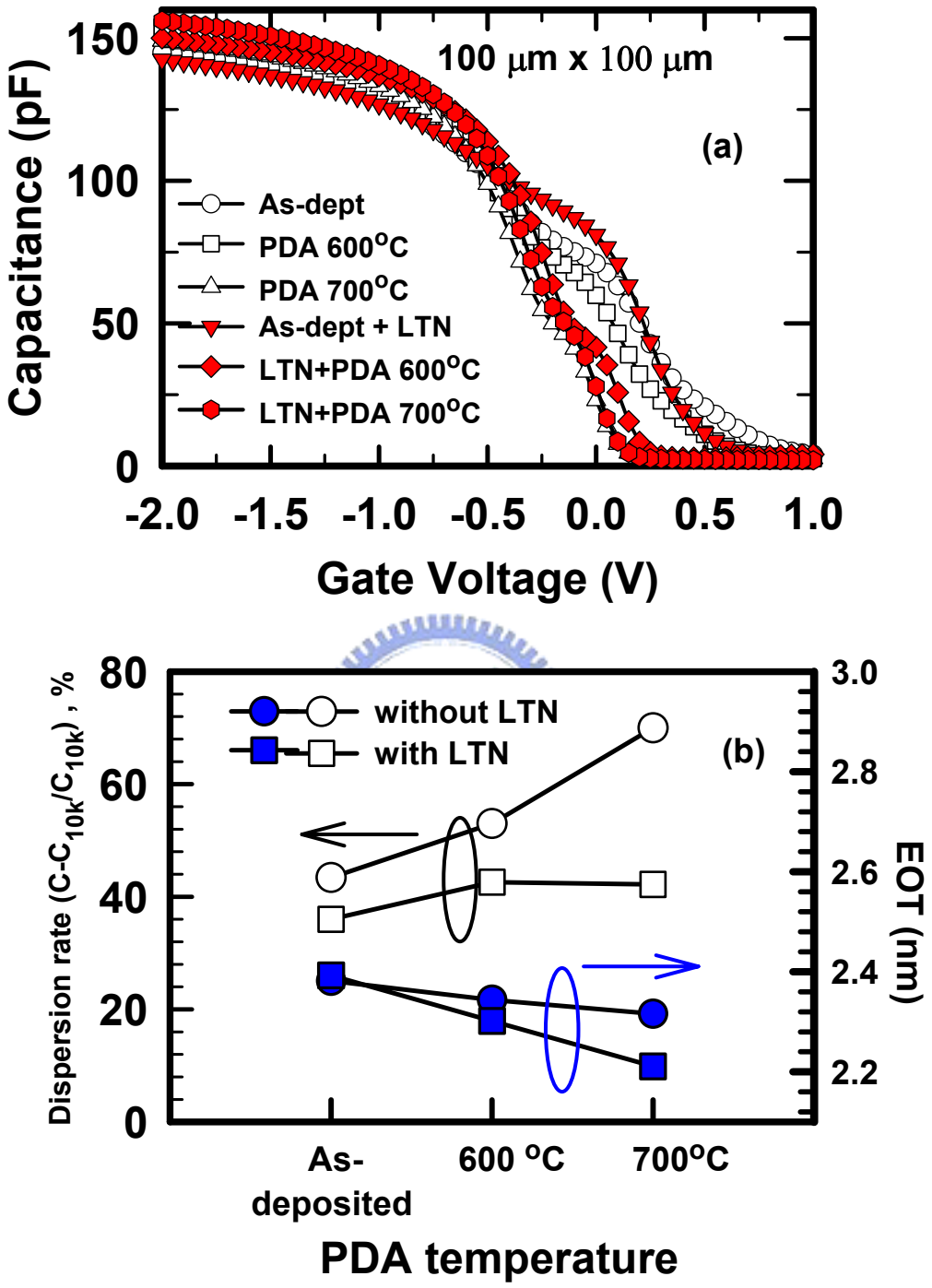


Fig. 3.2 (a) *C-V* characteristics and (b) frequency dispersion rates and EOT values of the HfO_2/SiO_2 gate stacks with/without LTN for various temperatures PDA.

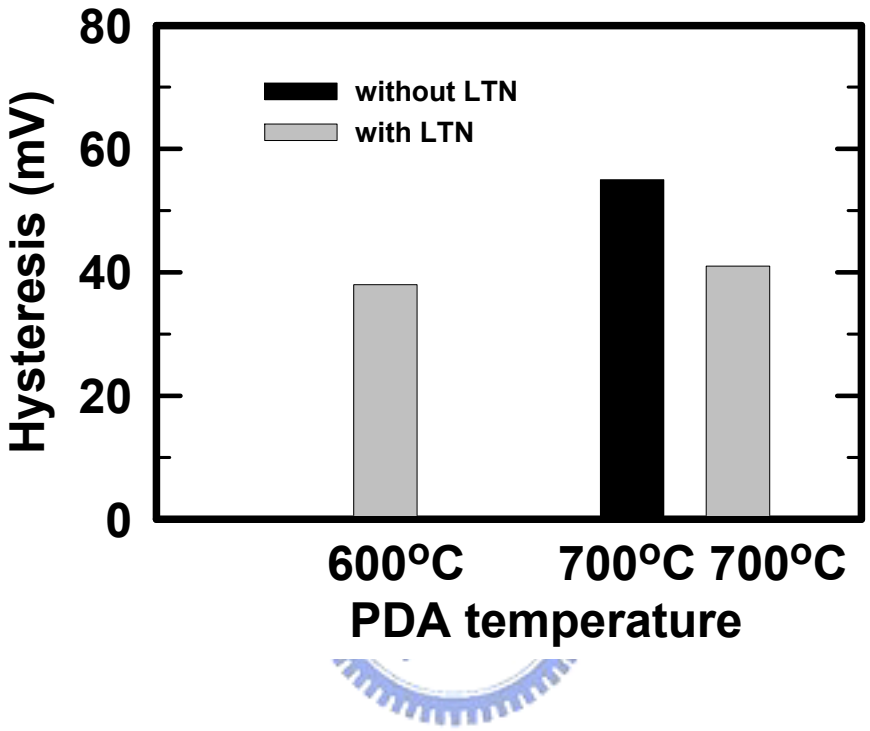


Fig. 3.3 Plot of hysteresis as a function of the PDA temperature of the HfO_2/SiO_2 gate stacks with/without LTN.

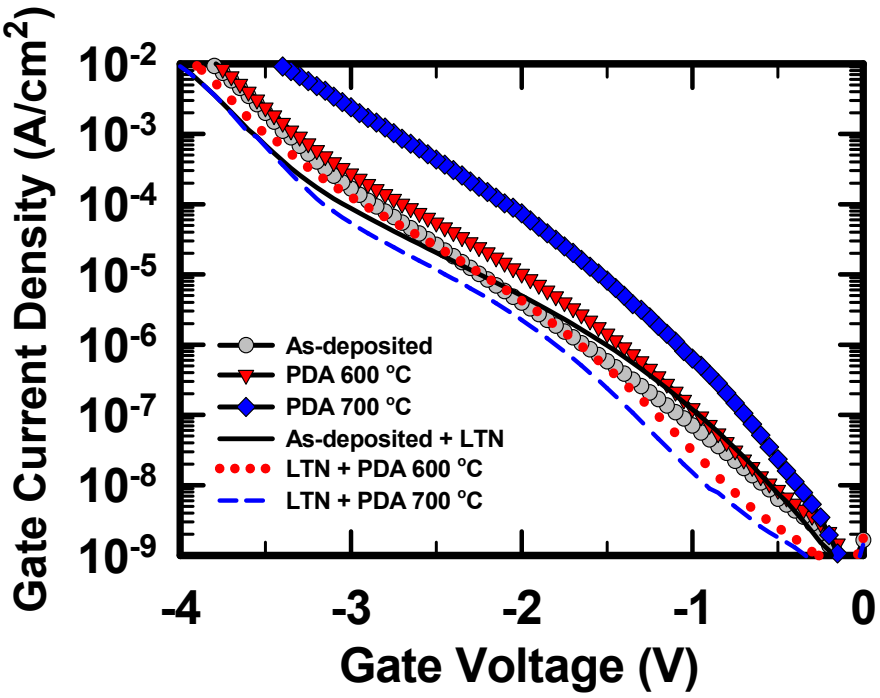


Fig. 3.4 *J-V* characteristics of HfO_2/SiO_2 gate stack with/without LTN for various PDA temperature treatments.

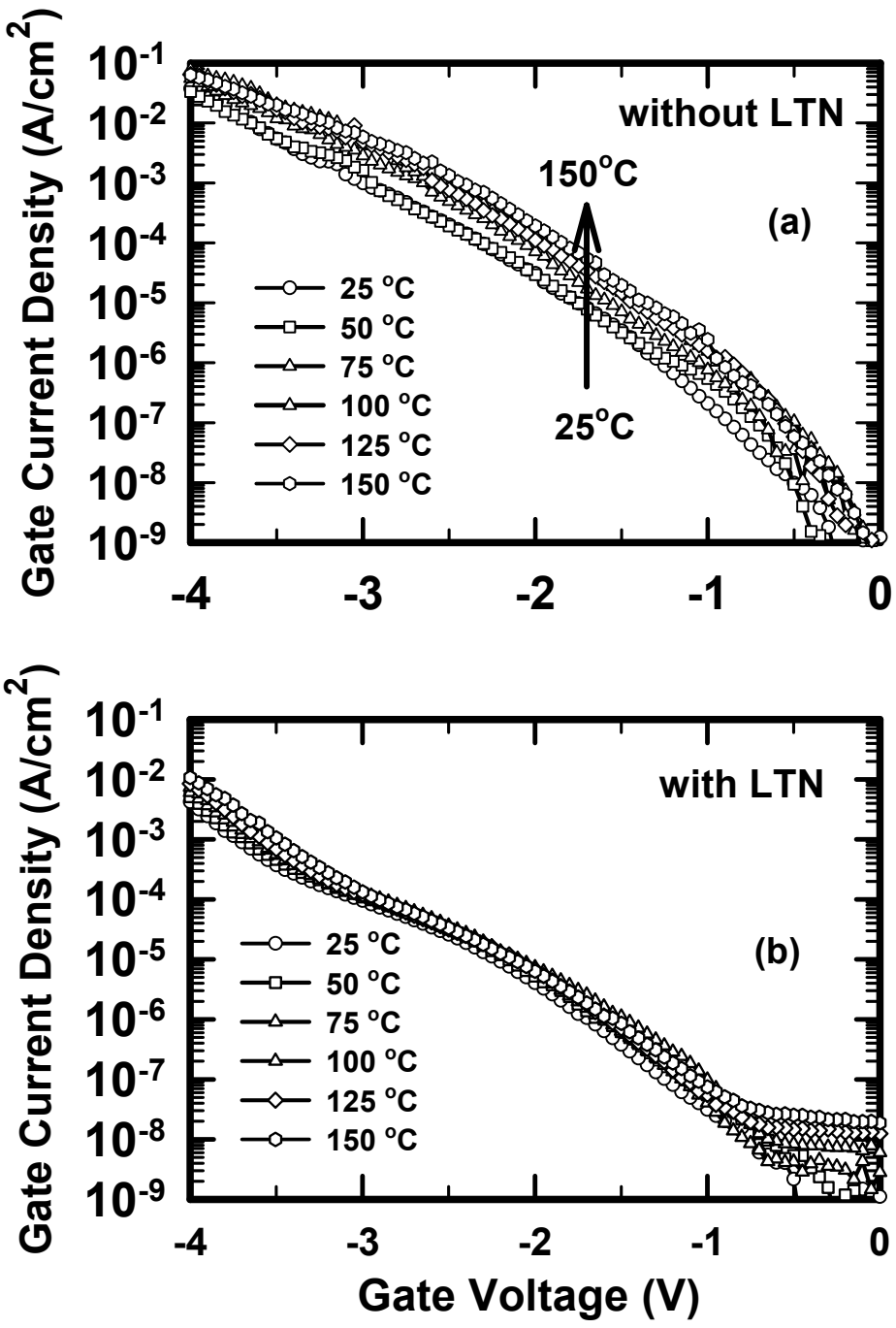


Fig. 3.5 Dependences of gate leakage current density on temperature for the 700°C-PDA-treated HfO_2/SiO_2 gate stacks with or without LTN.

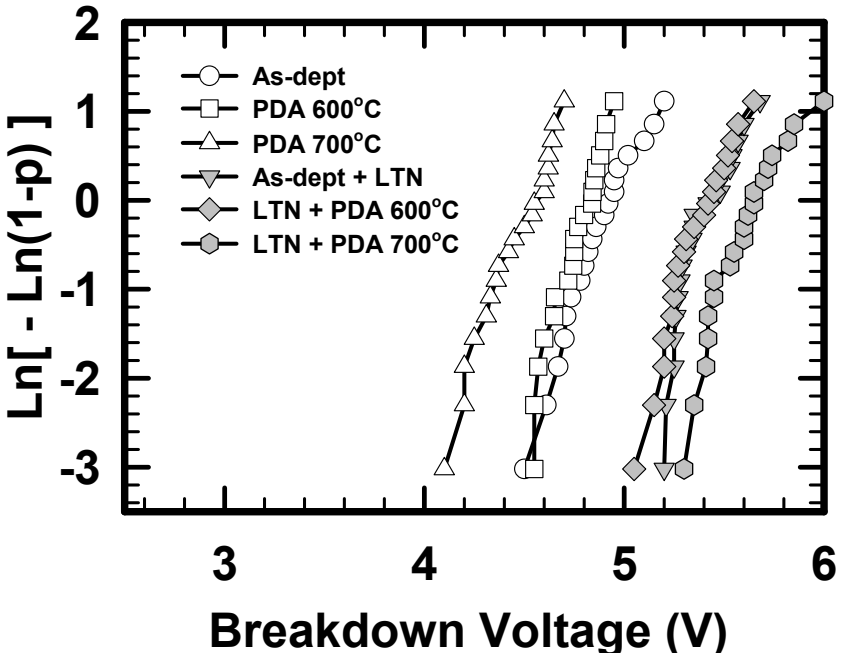


Fig. 3.6 Weibull distributions of dielectric breakdown voltage for the HfO_2/SiO_2 gate stacks, with/without LTN, with various temperatures PDA treatments.

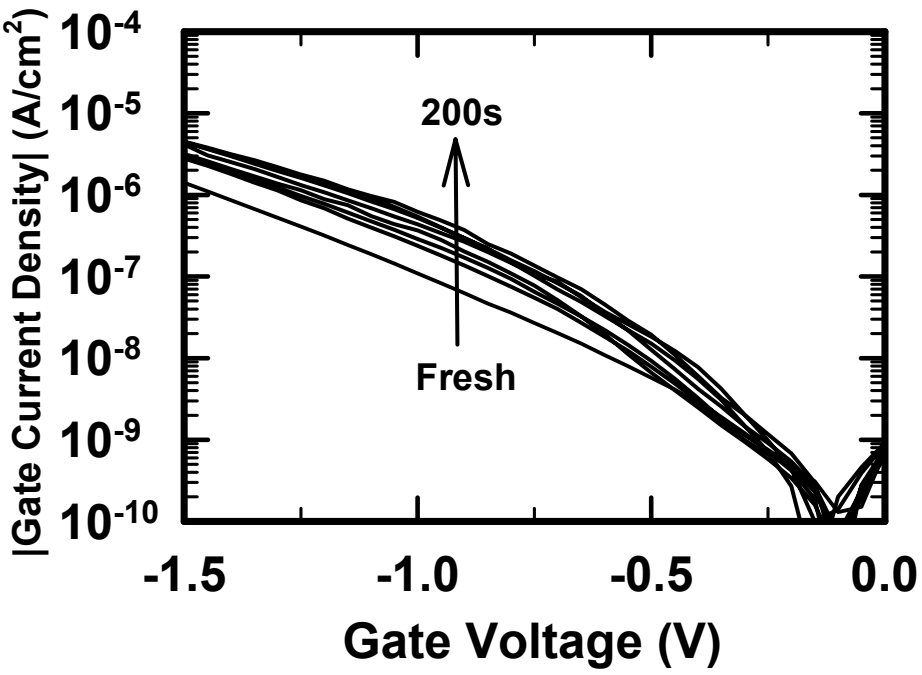


Fig. 3.7 *J-V* characteristics as a function of stress time under constant voltage stress (V_g = −3.75 V) for the 700°C- PDA-treated HfO_2/SiO_2 gate stacks without LTN.

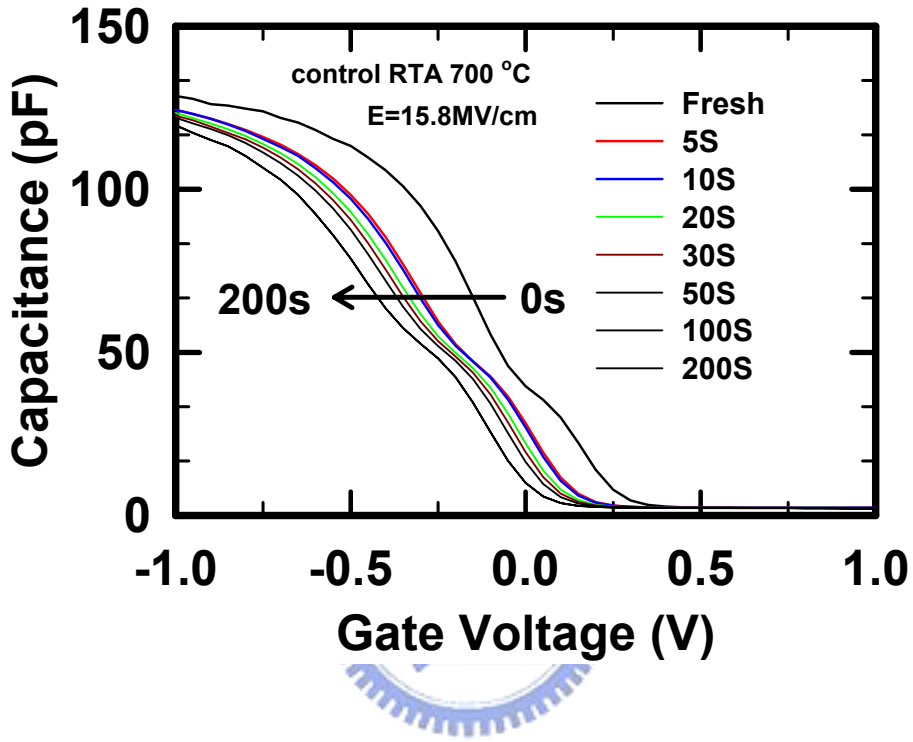


Fig. 3.8 *C-V* curves measured at 100 kHz with stress time as a parameter under constant voltage stress (V_g = −3.75 V) for the 700°C-PDA-treated HfO_2/SiO_2 gate stacks without LTN.

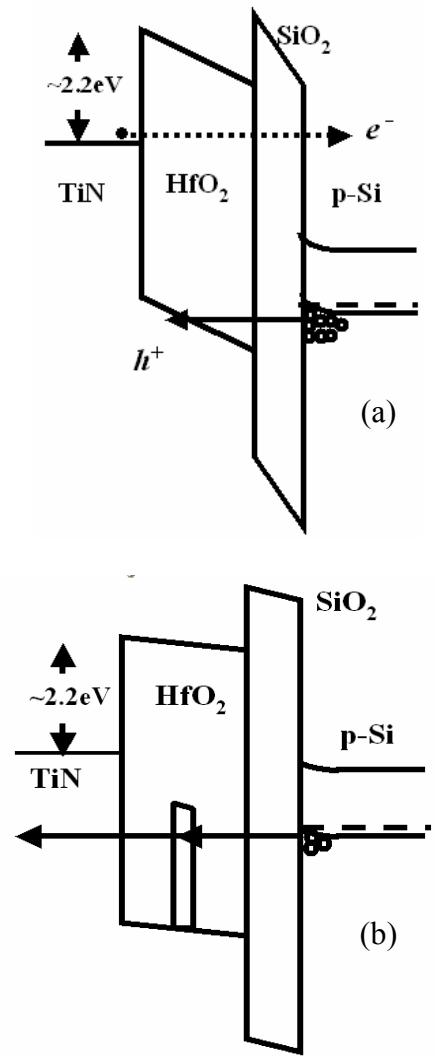


Fig. 3.9 (a) Schematic energy band diagram of the gate stack under $V_g = -3.75$ V stress (b) trap-assisted hole tunneling mechanism responsible for the increase in gate leakage current.

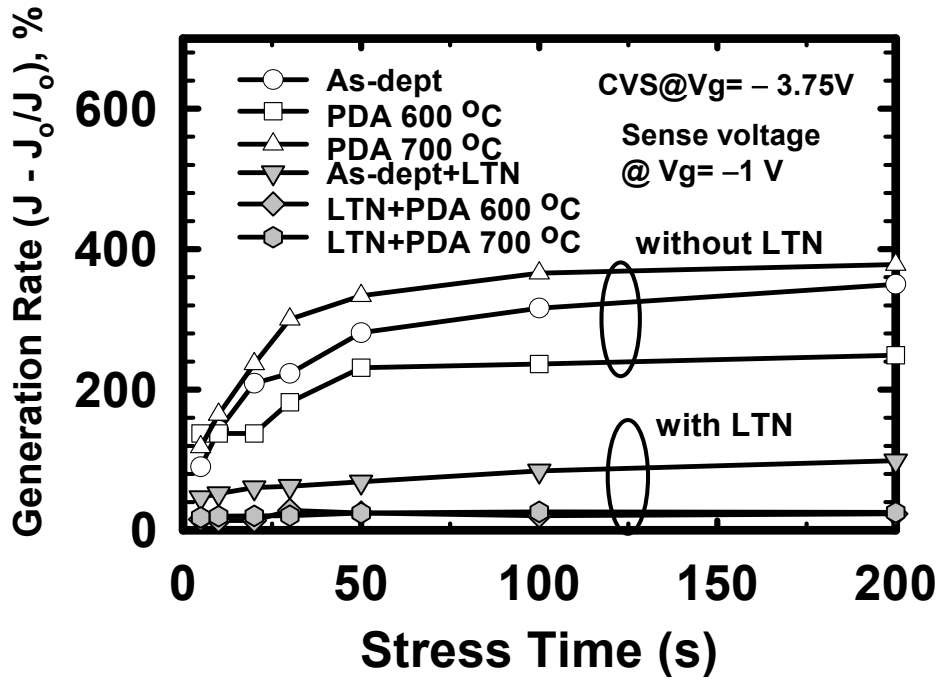


Fig. 3.10 Trap generation rate of the HfO_2/SiO_2 gate stacks with/without LTN under constant voltage stress ($V_g = -3.75$ V).

Chapter 4
Effects of Post-Deposition N_2O Plasma Treatment on the Electrical Characteristics of pMOSFETs with HfO_2 Gate Stacks

4.1 Background and Motivation

High dielectric constant (high-k) materials such as ZrO_2-based [1], HfO_2-based [2], and Al_2O_3-based [3] metal oxide insulators, are under intensive investigation for the gate dielectric application in metal–oxide–semiconductor field-effect transistors (MOSFETs) because they can substantially suppress the intolerable leakage current issue [4] faced by the ultrathin thermal oxide while maintain the driving current due to the thicker physical thickness with the same equivalent oxide thickness (EOT). Among these candidates, HfO_2 has received considerable attention due to its relatively high dielectric constants (~25) [5], wide band gaps, suitable tunneling barrier height for both electrons and holes (>1 eV) [6], and good thermal stability when they are in direct contact with silicon or polysilicon [7]. However, there are still a number of fundamental issues, which include abundant fixed charges, channel mobility degradation, large number of charge traps, and threshold voltage instability [8]-[12]. All of these should be tackled before they can eventually replace conventional SiO_2 or oxyntrides in Si-based CMOS production.

Charge trapping is an important concern for CMOS devices with HfO_2 gate

dielectrics, due to the large amount of bulk traps presented in the HfO_2 films. Their presence can result in the reliability degradation [8], mobility degradation [13]-[17] and threshold voltage instability [8]-[12]. In order to improve the film quality, a variety of nitridation techniques were used to incorporate nitrogen into the high-k films [14], [18]-[20]. In this work, we utilized the N_2O plasma treatment following the HfO_2 deposition, which possesses the advantage of low thermal budget for preventing the HfO_2 films from crystallization during processing. It was found that the post-deposition N_2O plasma treatment can not only effectively improve the electrical characteristics of the pMOSFETs with HfO_2 gate stack, such as lower bulk traps and interface states, enhanced mobility, and higher driving current, but also reduce the gate leakage current substantially.

Recently, it has been reported that the charge pumping (CP) technique can be used to qualify the bulk traps in the high-k films [12]-[21]. In the basic CP measurement, the CP current (or substrate current) is measured by applying a pulse train to the gate electrode of a transistor, with the source, drain, and body grounded. In general, the bulk traps can be directly determined from the CP current at a low frequency. However, the leakage current often occurs at such a low frequency. Therefore, to measure the bulk traps accurately, the influence of the leakage current on the CP current shall be carefully taken into account. In this work, we found that the leakage current contributes significantly to the substrate current in pMOSFETs, rather than to the source/drain current in the case of nMOSFETs [21].

In this study, we found that an enormous amount of trapped charges, rather than interface states, was generated during the voltage stress, causing device degradation. More importantly, we found that by employing the N_2O plasma treatment, the device degradation can be significantly suppressed. Furthermore, we found that the main trapping species will switch from holes to electrons when this treatment was

employed. In order to further investigate the phenomenon, the carrier separation technique [22]-[23] was performed and the results indicate that the dominant carrier type in the gate current determine the polarity of trapping.

4.2 Experimental

The pMOSFETs were fabricated on n-type (100) 150 mm wafers. After conventional LOCOS isolation, standard RCA cleaning with a final HF-dip was performed, followed by the growth of an intentional 0.6nm interfacial oxyntride layer (SiON) using rapid thermal processing in a NO_2 ambient at 700°C. Subsequently, a nominal 3nm HfO_2 layer was deposited by atomic vapor deposition (AVD) using an AIXTRON Tricent® system at a substrate temperature of 500°C. The physical thicknesses of the SiON layer and HfO_2 film were measured by the optical n&k analyzer. After deposition of the HfO_2 films, some samples were subjected to an additional N_2O-gas plasma treatment at the substrate temperature of 300°C. Then, all samples were annealed in a N_2 ambient at 600°C for 30s in order to improve the film quality. A 250nm polycrystalline silicon (poly-Si) layer was directly deposited by low pressure chemical vapor deposition (LPCVD) on top of the HfO_2 films, and then the gate electrode patterning was implemented through lithography and etching processing. Subsequently, the extension and deep source/drain were formed by implantation, which was activated at 950°C with rapid thermal annealing (RTA) for 20s in a N_2 atmosphere. After passivation, contact holes formation, Al metallization and patterning, the forming gas annealing at 400°C was finally performed for 30minutes to complete device fabrication.

Current-Voltage (*I-V*) and capacitance–voltage (*C–V*) characteristics were evaluated using an HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate

dielectrics was obtained from high-frequency (100 kHz) capacitance-voltage (*C-V*) curves at strong inversion (EOT $=\varepsilon_{SiO_2}/C_{inv}$) without considering the quantum effect. In order to reduce the unstable fast destrapping effect [24] during voltage stress ($V_g - V_{th} = -2.2$ V), a small positive voltage (1V) for 15sec was applied before *I-V* and CP measurements without causing any extra damage for the gate stacks. The purpose of this step is to more accurately estimate the density of slow traps without complications due to the interval between the stress and measurement. Thus, the density of slow traps can be monitored during stressing.

4.3 Results and Dissusions

Fig. 4.1 shows the gate leakage currents of the pMOSFETs with HfO_2/SiON gate stack under (a) inversion and (b) accumulation modes, respectively. It can be clearly observed that with post-deposition N_2O plasma treatment, the leakage current is significantly suppressed for both polarities. In particular, the reduction under normal operation condition, i.e., inversion mode, is nearly two orders of magnitude lower. **Fig. 4.2** shows the high frequency (100 kHz) *C-V* characteristics of the HfO_2 gate stacks. We can see that the hump of *C-V* curve appearing in the depletion for the control sample is considerably suppressed by the post-deposition N_2O plasma treatment due to the reduced interface states density. Moreover, the EOT values estimated from the strong inversion region are around 1.88nm and 2.15nm for the samples without and with N_2O plasma treatment, respectively. The thicker interfacial layer is one of plausible reasons that can explain the reduced gate leakage current. The other plausible mechanism, i.e., the reduction of bulk traps in HfO_2 films via N_2O plasma treatment will be further discussed with the results from the carrier separation measurement later.

Figs. 4.3 (a) and (b) show HRTEM images for the HfO_2/SiON gate stacks

without and with N_2O plasma treatment, respectively. We can clearly see that the physical thickness of the interfacial oxide layer increases for the samples with N_2O plasma treatment, due to the fact that the diffused ionic oxygen into/through the HfO_2/SiON gate stack can easily react with Si substrate [25] during the N_2O plasma treatment. The radical oxygen or nitrogen may also improve the film quality and result in reduced bulk traps [26]. On the other hand, it is observed that the extent of crystallization in the HfO_2 film is more apparent for the sample without the N_2O plasma treatment. This may be due to the increased crystalline temperature when the nitrogen is incorporated in the HfO_2 films.

Typical I_d-V_d characteristics of the pMOSFETs with and without N_2O plasma treatment as a function of gate overdrive are shown in **Fig. 4.4**. We found that the driving current is substantially enhanced by the N_2O plasma treatment even though the EOT value is about 0.3nm thicker than that of the sample without N_2O plasma treatment. **Figs. 4.5** (a) and (b) depict typical I_d-V_g curves and normalized transconductance (G_m×EOT) and transconductance of p-MOSFETs, respectively. Consistent with results shown earlier, the subthreshold swing (S) can be reduced from 98 mV/dec to 93 mV/dec, along with 77% gain in normalized transconductance peak value by introducing N_2O plasma treatment. The improvements are believed to be due to not only a better interface quality but also reduced bulk trap density. Moreover, the thicker interfacial layer will benefit the inversion charge layer mobility due to less Coulomb scattering [27]. This will be confirmed later by the CP current measurement. From the above results, we conclude that post-deposition N_2O plasma treatment can considerably enhance the electrical characteristics of pMOSFETs with HfO_2 gate stack in terms of gate leakage current, subthreshold swing, normalized transconductance, and the overdrive current despite the slightly increased EOT value (0.3 nm thicker).

In order to gain further insight into the origins of the benefits by this post deposition process, the CP measurement and the carrier separation technique were performed. It is well known that the CP measurements are widely used to characterize the quality of the interface in the MOSFET devices, which involves the measurement of the substrate current by applying the voltage pulse train to the gate electrode of the transistor, with the source, drain, and body grounded. However, during measurement, the CP current (or substrate current) could be affected by the gate leakage current [24], [28], especially at lower frequencies and with thinner oxides. Therefore, to accurately analyze the interface states or bulk traps in the dielectrics from the CP results, we need to carefully address the leakage current issue. In this work, we employed three conventional types of voltage pulse train applying to the gate electrode, i.e., fixed amplitude sweep, fixed base sweep, and fixed peak sweep, as demonstrated in **Fig. 4.6** [21]. The arrow in the figure indicates the voltage sweep direction during the CP measurement. The results for the devices with HfO_2 gate stack without N_2O plasma treatment, measured with different pulse trains at various frequencies, are shown in **Fig. 4.7**. The current measured at the substrate terminal is denoted as the CP current (I_{cp}) while that measured at the tied source/drain terminals is referred to as I_{DS}. In addition, the interface states density N_{it} is determined by the $N_{CP}=I_{CP}/(A\times f\times q)$ and $N_{DS}=I_{DS}/(A\times f\times q)$, where A is the area of the gate electrode, f is the frequency of the signal at the gate electrode, and q is the charge of electron. **Fig. 4.7** (a) clearly shows that N_{CP} traces identically with N_{DS} over the sweeping voltage range, and both depict negligible frequency dependence, especially at higher frequencies when the fixed amplitude sweep is utilized. This is thought to come from the poor control over the charge exchange (charge/discharging) for the bulk traps in the HfO_2 dielectrics for the chosen amplitude [21]. Therefore, the fixed amplitude sweep at higher frequencies is a suitable approach for qualifying the interface states.

However, the situations in the other two approaches are quite different, as shown in **Fig. 4.7** (b) and **Fig. 4.7** (c). Recently, the CP measurement had been frequently employed to qualify the level of bulk traps [12], [21] in the HfO_2 dielectrics using the fixed base sweep and/or the fixed peak sweep, as indicated in **Fig. 4.6** (b) and **Fig. 4.6** (c), respectively. In the case of the transistors with SiO_2 gate oxide (close to ideal case), the I_{CP} measured from the fixed amplitude sweep is almost identical to that from the fixed peak or base sweep, and it is equal to the I_{DS}. This implys that the CP current is completely attributed to the recombination of the interface states. However, for the dielectrics with inferior quality, it is commonly seen that the measured I_{CP} increases with increasing amplitude and decreasing frequency of the gate pulse, when using the fixed base or peak sweep. This may arise from carrier trapping/distrapping of the bulk traps in the high-k films [12], [21]. In order to avoid the complication of the geometry effect [29], as shown in **Fig. 4.8**, on the CP measurement, the small devices (<10um) shall be used [30]. Our devices have the channel length of 3 μm. In other words, the geometry effect can be excluded. Therefore, when the measured I_{CP} and I_{DS} currents are not the same, there must be some extra components contributing to the I_{CP} if the presence of bulk traps is not the culprit. Nonetheless, the results for the fixed base sweep in **Fig. 4.7**. (b) displays even more remarkable deviation between N_{CP} and N_{DS} at larger positive V_{gh} with lower frequencies, which obviously can not be accounted for by the presence of bulk traps. Because if this is caused by the recombination from the charging/discharging of the bulk traps in the high-k dielectrics, the increment of I_{CP} and I_{DS} should be the same due to the requirement of equal amount of carriers of opposite polarities for the recombination. Therefore, we believe the drastic difference between N_{CP} and N_{DS} with increasing amplitude is ascribed to the larger leakage current. In addition, when the entire CP gate voltage waveform lies at lower V_{gh}<−0.5V region (i.e., close to the

inversion region), the difference in the I_{CP} and I_{DS} is negligible. This indicates that the relatively small leakage current level under the inversion mode as compared to that under accumulation mode (shown in **Fig. 4.1**) has no influence on the I_{CP} and I_{DS}. In order to further confirm our speculation, the fixed peak sweep (**Fig. 4.6** (c)) is also performed. The results are shown in **Fig. 4.7** (c). The discrepancy between I_{CP} and I_{DS} occurs when the frequency is lower than 100 kHz. Clearly, the I_{CP} at the higher gate voltages (V_{gl}>−0.5V) increases when the frequency is lowered. On the other hand, I_{DS} exhibits no frequency dependence. In this voltage region, the entire CP gate voltage waveform can only drive the pMOSFET in the accumulation mode, I_{CP} and I_{DS} both should be negligible in theory. Nevertheless, I_{CP} actually increases when the frequency is lower than 100 kHz. Therefore, no matter which technique is used, i.e., the fixed peak or the base sweep, we observe that when the CP waveform is located at the accumulation region, I_{CP} will be larger than I_{DS} especially at lower frequencies. The reasonable culprit for this phenomenon is the contribution of the considerably large gate leakage current at higher positive gate voltages, caused by the tunneling of electrons from the substrate, as illustrated in the **Fig. 4.8**. This suggests that in order to precisely analyze the bulk traps in the dielectrics using the fixed base or peak sweep from the CP measurement, we need to monitor the substrate current and source/drain current simultaneously. This is necessary to clarify the influence of leakage current, especially at lower frequencies or when the leakage current is considerably large. Similar results also can be observed for the samples with N_2O plasma treatment, which is not shown here. It should be noted that in our case the leakage current is found to only contribute to the I_{CP} in pMOSEFETs. This is in contrast to report by other group who demonstrated that the leakage current would contribute to the I_{DS} in nMOSFETs [21]. According to the tunneling front model [31]-[32] for SiO_2 films, the traps located ~1.1nm away from the interface can

exchange charges with silicon at a time constant of 1μs at zero electric field. Thus, when using the fixed base sweep at a relatively low frequency of 5 kHz, it can detect deeper than 1.1nm, and increasingly deeper into HfO_2 film with increasing amplitude. As a consequence, we used the fixed base sweep at a relatively low frequency of 5 kHz to estimate the behavior of the bulk traps in the HfO_2 films.

Following the above argument, the densities of interface states measured using the fixed amplitude sweep for the pMOSFETs with and without post-deposition N_2O plasma treatment as function of the peak voltage are shown in **Fig. 4.9**. The results are quite consistent with those in subthreshold swing, as shown in **Fig. 4.5**. This may be due to the fact that the oxygen radicals from the plasma can react with Si substrate, resulting in slight thicker EOT and improving the quality of the interface [33]. Moreover, **Fig. 4.10** highlights N_{CP} and N_{DS} determined from the fixed base sweep at the frequency of 5 kHz for the devices with and without post-deposition N_2O plasma treatment. The lower N_{CP} and N_{DS} values and lower slope of N_{CP} and N_{DS} versus voltage for the devices with post-deposition N_2O plasma treatment indicate that this process can not only effectively improve the interface quality but also reduce the bulk traps in the HfO_2 gate stack [26].

The transistors I_d-V_g curves are measured for monitoring the threshold voltage shift (ΔV_{th}) during a constant gate overdrive (V_g–V_{th}) of –2.2V for the devices with/without post-deposition N_2O plasma treatment. Time evolutions of ΔV_{th} as a function of injected charge fluence are shown in **Fig. 4.11**. In order to minimize the fast unstable charge detrapping effect, a small positive gate voltage (1V) for 15 sec was applied prior to the I_d-V_g and CP current measurements to discharge the fast unstable trap as far as possible. This step enables us to investigate the response solely from the stable slow traps in HfO_2 gate stacks. We then clearly observe that the main mechanism responsible for the ΔV_{th} changes from hole trapping to electron trapping,

and the degradation is improved after the post-deposition N_2O plasma treatment. Therefore, the improved V_{th} degradation properties for samples with N_2O plasma treatment may be due to the reduction of crystalinity of the HfO_2 film, resulting from nitrogen incorporation. To further elucidate the degradation mechanism during voltage stress, the interface states generation (ΔN_{it}) and the effective bulk trap density (ΔN_{ot}), which is calculated from ΔV_{th} assuming the charge is trapped at the interface between the dielectric and the substrate, are plotted as a function of the injection charge density (N_{inj}), as shown in **Fig. 4.12**. N_{inj} is calculated by integrating the gate current density, which is monitored throughout the stress. Apparently, ΔN_{ot} is found to be significantly larger than the ΔN_{it}, suggesting that the degradation of the constant gate overdrive stress is dominated by the charge trapping in the bulk of HfO_2 films instead of the generation of interface states, no matter whether the treatment is performed or not.

To gain better insight into the opposite polarity charge trapping during stress for devices with and without N_2O plasma treatment, the carrier separation measurement [22]-[23] was performed. This is to investigate the carrier conductions in the HfO_2/SiON gate stacks, in which the p^+ polysilicon gate is negatively biased, with the source/drain and n-Si substrate grounded. The current measured at the source/drain terminals is denoted as $I_{DS,C}$, while the other currents measured at the gate and substrate terminals are referred to as $I_{G,C}$ and $I_{B,C}$, respectively. The measured results for the sample without N_2O plasma treatment are shown in **Fig. 4.13**. It can be seen that gate current is dominated by the $I_{DS,C}$ current. In order to clarify the current mechanism of carrier transportation, the dependence of $I_{G,C}$, $I_{B,C}$, and $I_{DS,C}$ on substrate bias is investigated under inversion region. $I_{G,C}$ current strongly depends on the substrate bias, and the dependence of $I_{DS,C}$ on the substrate bias is consistent with that of $I_{G,C}$, as shown in **Fig. 4.14**. However, $I_{B,C}$ current slightly changes with the

substrate bias. This suggests that the hole current is dependent on the inversion charge concentration, while electron current is independent of inversion charge concentration, implying that $I_{DS,C}$ is composed of hole flow coming from the S/D regions, and I_B is composed of electrons coming from the gate electrode, as shown in **Fig. 4. 15**.

Fig. 4.16 shows the results of carrier separation of HfO_2/SiON gate stacks without N_2O plasma treatment under inversion region. One can see that, the magnitude of $I_{DS,C}$ is obviously lower than $I_{B,C}$, which is opposite to the trend in the case without N_2O plasma treatment. Similarly, from the current components of substrate bias dependence for the post-N_2O plasma-treated sample (**Fig. 4.17**); the source/drain current is still dependent on the inversion charges in the channel, while the substrate current is not. Therefore, $I_{B,C}$ current is responsible for the observed electron trapping because it is mainly composed of electron tunneling from the gate electrode. We attribute this switch to the increase of the interfacial layer after N_2O plasma treatment, which then leads to a substantial reduction of $I_{G,C}$ as compared to that in the case without N_2O plasma treatment, since $I_{DS,C}$ is significantly suppressed, as shown in **Fig. 4.16**. Since the tunneling probability of hole carriers is strongly dependent on the interfacial layer thickness, the gate leakage reduction for the sample with N_2O plasma treatment may therefore be ascribed to the increase of interfacial layer. The thicker interfacial layer results from the diffused ionic oxygen into/through the HfO_2/SiON gate stack that can easily react with Si substrate [25] during the N_2O plasma treatment. This result is consistent with the results of TEM. The radical oxygen or nitrogen may also improve the film quality, resulting in reduced bulk traps [26].

Fig. 4.19 and **Fig. 4.20** show the temperature dependence of gate leakage current, source/drain current and substrate current for the HfO_2/SiON gate stacks with and without N_2O plasma treatment, both under inversion region and accumulation region,

respectively. For both samples, gate current increases with increasing temperature, except at the range of V_g=0V to −3.5V for the sample without N_2O plasma treatment. This implies that the conduction mechanism of gate current is trap-related, i.e., trap assisted tunneling (TAT), Frenkel-Poole, etc. Since the gate current is composed of both electron current and hole current, we need to separately determine the mechanisms of carrier conduction in the HfO_2/SiON dielectrics with or without N_2O plasma treatment.

Fig. 4.21 and **Fig. 4.22** show the Frenkel-Poole plot for the source/drain current (hole) and substrate current (electron) of the sample without N_2O treatment in the inversion region, respectively. The current from Frenkel-Poole emission is of the form:

$$J = B \times a \times E_{eff} \times \exp\left(\frac{-q(\phi_B - \sqrt{aqE_{eff}/\pi\varepsilon_{HfO2}\varepsilon_0})}{kT}\right);\ B = q\mu N_T\ ,\ \mathrm{a} = \frac{\varepsilon_{SiO2}}{\varepsilon_{HfO2}} = \text{constant}$$

$$\Rightarrow \quad \ln(J/E_{eff}) = \frac{q\sqrt{aq/\pi\varepsilon_{HfO2}\varepsilon_0}}{kT}\sqrt{E_{eff}} - \left[\frac{q\phi_B}{kT} + \ln(aB)\right]$$

$$\text{or} \quad \ln(J/E_{eff}) = E_{act} \times \left(\frac{q}{kT}\right) + \ln(aB)\ ;\quad E_{act} = -(\phi_B - \sqrt{aqE_{eff}/\pi\varepsilon_{HfO2}\varepsilon_0})$$

where B is a constant related to the trapping density and carrier mobility in the HfO_2 film, ϕ_B is barrier height, E_{eff} is the effective electric field in the SiO_2 film, ε_0 is the free space permittivity, ε_{HfO2} is the dielectric constant of HfO_2, k is Boltzmann constant (1.38×10^{23} J/K), E_{act} is a field dependent effective activation energy and T is the temperature measured in Kelvin. From arrhenius plot of E_{act} [i.e., $\ln(J/E_{eff})$ vs. (q/kT)], we can obtain E_{act} and aB. Then, barrier height ϕ_B and dielectric constant ε_{HfO2} of HfO_2 can be calculated from the intercept of y axis and the slope of the fitting curves in the E_{act} vs. $\sqrt{E_{eff}}$ plot according to $E_{act} = q\sqrt{aq\pi\varepsilon_k\varepsilon_0}(\sqrt{E_{eff}}) - q\phi_B$.

From **Fig. 4.21** and **Fig. 4.22**, linear relationships were observed, suggesting that

the conduction mechanism for the high-voltage I_{SD} and I_B are indeed Frenkel-Poole-type in nature. The caculated parameters for the hole and electron barrier heights are around 0.75eV and 0.92eV, respectively, for the sample without N_2O treatment. Results for post-N_2O plasma samples are shown in **Fig. 4.23** and **Fig. 4.24**. Again, linear relationships were seen, suggesting that F-P is the likely mechanism for both I_{SD} and I_B. The barrier heights are about 0.91eV and 0.92eV for electrons and holes, respectively, for the N_2O-treated sample. Note that the barrier height for holes has changed from 0.75eV for the control to 0.91eV for the N_2O-treated sample, indicating that the trap position has moved closer to the valence band of the poly Si gate after post-N_2O plasma treatment. The band diagrams are shown in **Fig. 4.25** and **Fig. 4.26** for the sample without and with post-N_2O plasma treatment, respectively.

The ε_{HfO2} value is calculated from F-P fitting to be around 9.3 for the control sample and around 9.6 for the sample with N_2O treatment. The value is slightly lower than the estimated value from HRTEM image, which is 13.4 for control sample and 14.6 for the sample with N_2O treatment assuming ε_k for I.L is 3.9.

4.4 Summary

The improvements in the electrical characteristics of the p+-poly-gated pMOSFETs with HfO_2/SiON gate stacks employing post-deposition N_2O plasma treatment have been demonstrated, for the first time, in this work. We have found that the improvements include many aspects, such as reduced leakage current, better subthreshold swing, enhanced normalized tranconductance, and higher driving current. These improvements are ascribed to the lower interface states and bulk traps, as confirmed by various types of charge pumping measurements. Although CP

measurement has been known to be a powerful technique for the evaluation of interface states and bulk traps in the high-k films, we found that in order to accurately measure the bulk traps at a lower frequency, charge pumping current (I_{cp}) and source/drain current (I_{ds}) need to be measured simultaneously to confirm that both are of the same value. Noted that the effect of the leakage current on the CP measurement in pMOSFETs is rather different from that in nMOSFETs, where the leakage current will not contribute to the substrate current, but to the source/drain current. In evaluating device reliability, it is found that the degradation caused by the voltage stress is dominated by the charge trapping in the bulk of HfO_2 films rather than interface states generation, no matter whether the N_2O plasma treatment is employed or not. In addition, it is observed that the N_2O plasma treatment significantly improves the charge trapping characteristics, and the electron trapping is the main mechanism during stressing, which is opposite to the hole trapping observed in the samples without N_2O plasma treatment.

References

[1] R. Nieh, S. Krishnan, H. J. Cho, C. S. Kang, S. Gopalan, K. Onishi, R. Choi, and J. C. Lee: Symp. VLSI Tech. Dig., 2002, p.186.

[2] R. Choi, K. Onishi, C. S. Kang, S. Gopalan, R. Nieh, Y. H. Kim, J. H. Han, S. Krishnan, H. J. Cho, A. Shahriar, and J. C. Lee: Int. Electron Device Meet. Tech. Dig., 2002, p. 613.

[3] S. Saito, Y. Shimamoto, S. Tsujikawa, H. Hamamura, O. Tonomura, D. Hisamoto, T. Mine, K. Torii, J. Yugami, M. Hiratani, T. Onai, and S. Kimura: Symp. VLSI Tech. Dig., 2003, p. 145.

[4] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong: Proc. IEEE **89** (2001) 259.

[5] M. Balog, M. Schieber, M. Michman, S. Patai: Thin Solid Films. **41**(1977) 247.

[6] J. Robertson: J. Vac. Sci. & Technol. B **18** (2000) 1785.

[7] K. J. Hubbard, D. G. Schlom: J. Mat. Res. **11** (1996) 2757.

[8] S. Zafar, A. Callegari, E. gusev, and M. Fischetti: J. Appl. Phys. **93** (2003) 9298.

[9] M. Krishnan and V. Kol'dyaev, Proc. 40th *Int. Reliability Physics Symp*, Texas, 2002, p. 421.

[10] W. J. Zhu, T. P. Ma, S. Zafar, and T. Tamagawa: IEEE Electron Device Lett. **23** (2002) 597.

[11] E. P. Gusev and C. P. D'Emic: Appl. Phys. Lett. **83**, 5223 (2003).

[12] A. Kerber, E. Carter, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke: Proc. 41th *Int. Reliability Physics Symp*, Texas, 2003, p. 41.

[13] E. Gusev, D. A. Buchanan, E. Cartier: Int. Electron Device Meet. Tech. Dig., 2001, p. 451.

[14] H. -J. Cho, C. Y. Kang, C. S. Kang, R. Choi, Y. H. Kim, M. S. Akbar, C. H. Choi,

S. J. Rhee, and J. C. Lee: *IEEE Semiconductor Device Research Symposium*, 2003, p. 68.

[15] Y. Morisaki, T. Aoyama, Y. Sugita, K. Irino, T. Sugii, and T. Nakamura: Int. Electron Devices Meet. Tech. Dig., 2002, p. 861.

[16] M. Koyama, K. Suguro, M. Yoshiki, Y. Kamimuta, M. Koike, M. Ohse, C. Hongo, and A. Nishiyama: Int. Electron Device Meet. Tech. Dig., 2001, p. 459.

[17] R. Choi, C. S. Kang, B. H. Lee, K. Onishi, R. Nieh, S. Gopalan, E. Dharmarajan, and J. C. Lee: Symp. VLSI Tech. Dig., 2001, p. 15.

[18] M. Koyama, A. Kaneko, T. Ino, M. Koike, Y. Kamata, R. Iijima, Y. Kamimuta, Takashima, M. Suzuki, C. Hongo, S. Inumiya, M. Takayanagi and A. Nishiyama: Int. Electron Devices Meet. Tech. Dig., 2002, p. 849.

[19] K. Onishi, S. K. Chang, R. Choi, Hag-Ju Cho; Gopalan, S, R. E. Nieh, S. A. Krishnan, and J. C. Lee: IEEE Trans. Electron Devices **50** (2003) 384.

[20] H. -J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan, J. C. Lee: Int. Electron Device Meet. Tech. Dig., 2001, p. 655.

[21] A. Kerber, E. Carter, L. Pantisano, M. Rosmeulen, R. Degraeve, G. Groeseneken, H. E. Maes, and U. Schwalke: Microelectronic Engineering. **72** (2004) 267.

[22] W. Y. Loh, B. J. Cho, M. S. Joo, M. F. Li, D. S. Chan, S. Mathew, and D. L. Kwong: Int. Electron Device Meet. Tech. Dig., 2003, p. 927.

[23] S. Takagi, M. Takayanagi, and A. Toriumi: Int. Electron Device Meet. Tech. Dig., 1999, p. 461.

[24] P. Masson, J. Autran, and J. Brini: IEEE Electron Device Lett. **20** (1999) 92.

[25] S. J. Chang, J. S. Lee, J. F. Chen, S. C. Sun, C. H. Liu, U. H. Liaw, B. R. Huang IEEE Electron Device Lett. **23** (2002) 643.

[26] R. Degraeve, F. Crupi, D. H. Kwak, and G. Geoeseneken: Symp. VLSI Tech. Dig., 2004, p. 140.

[27] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier: J. Appl. Phys. **90** (2002) 4587.

[28] Steve S. Chung, S.-J. Chen, C.-K. Yang, S.-M. Cheng, S.-H. Lin, Y.-C. Sheng, H.-S. Lin, K.-T. Hung, D.-Y. Wu, T.-R. Yew, S.-C. Chien, F.-T. Liou, and Frank Wen: Symp. VLSI Tech. Dig., 2002, p. 74.

[29] G. Van den bosch, G. Groeseneken, and H. E. Maes: IEEE Electron Device Lett. **14** (1993) 107.

[30] R. J. Carter, E. Cartier, A. Kerber, L. Pantisano, T. Schram, S. De Gendt, and M. Heyns: Appl. Phys. Lett. **83**, 533 (2003).

[31] Oldhman, T. R., A. J. Lelis, and F. B. MeLean: IEEE Trans. Nuci., Sci., 1986. **33**. p. 1203.

[32] Dumin, D. J. and J. R. Maddux: IEEE Trans. Electron Dev., 1993. **40**(5), p. 986.

[33] S. Tsujikawa, T. Mine, Y. Shimamoto, O. Tonomura, R. Tsuchiya, K. Ohnishi, H. Hamamura, K. Torii, T. Onai, and Jiro Yugami: Symp. VLSI Tech. Dig., 2002, p. 202.

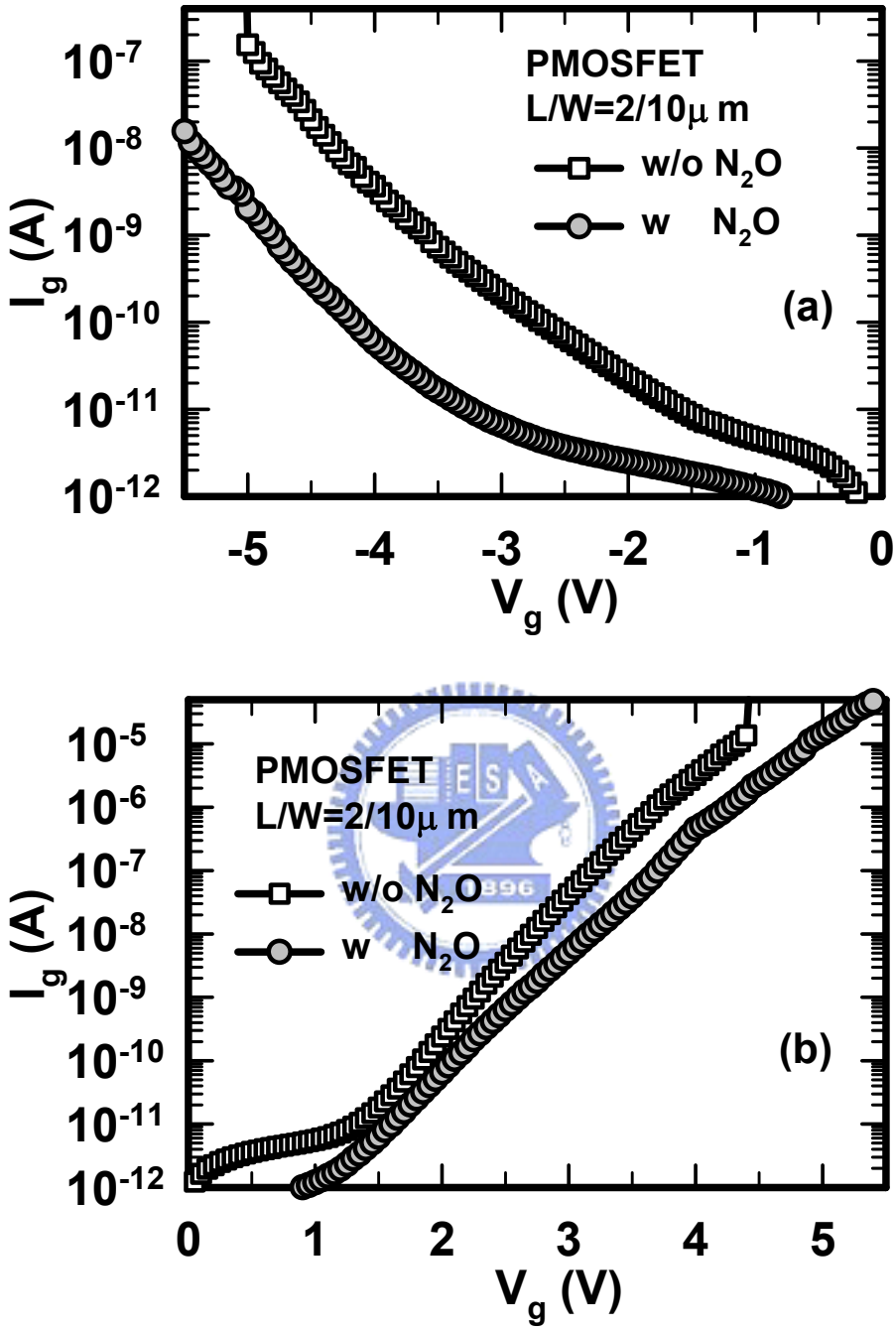


Fig. 4.1 Gate leakage current of p^+ poly-gated pMOSFETs with HfO_2/SiON high-k gate stacks subjected to N_2O plasma treatment or no additional treatment was shown under (a) inversion and (b) accumulation region, respectively.

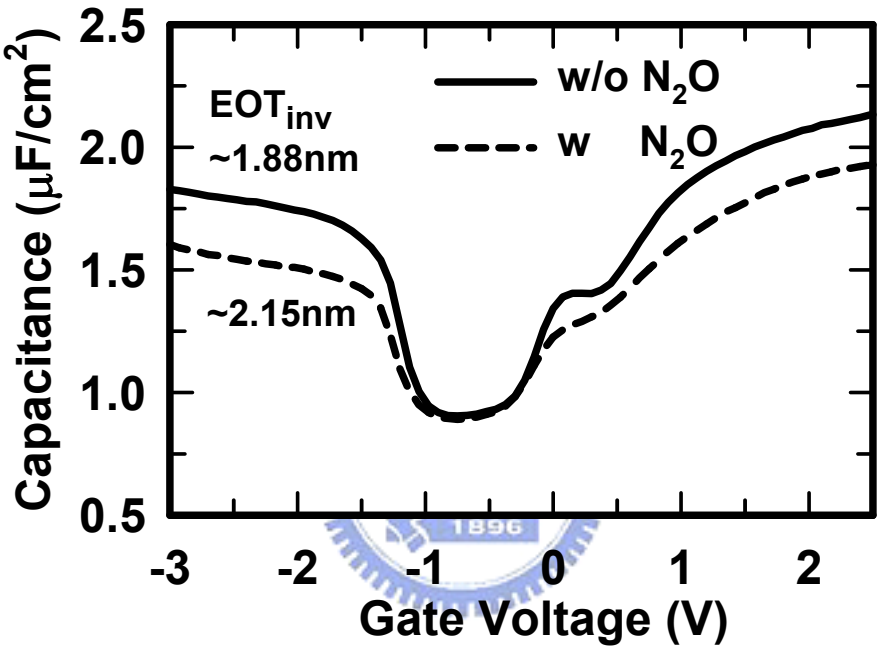


Fig. 4.2 Capacitance–voltage (*C–V*) characteristics measured at 100 kHz for the HfO_2/SiON high-k gate stacks with/without N_2O plasma treatment. The equivalent oxide thickness (EOT) was determined by measuring the maximum inversion capacitance.

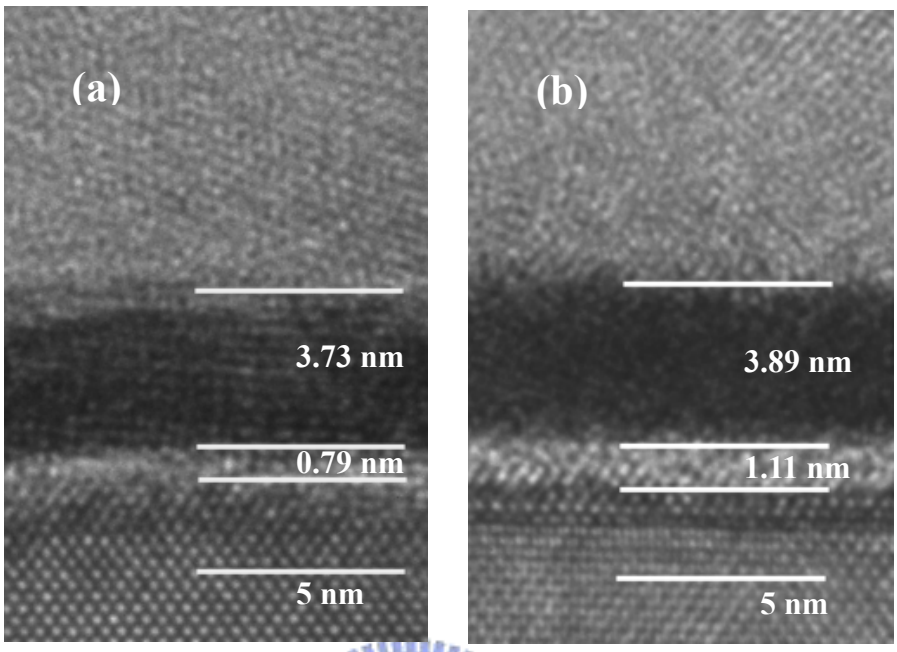


Fig. 4.3 Cross-sectional HRTEM images of the HfO_2/SiO_2 gate stacks (a) without (b) with N_2O plasma treatment.

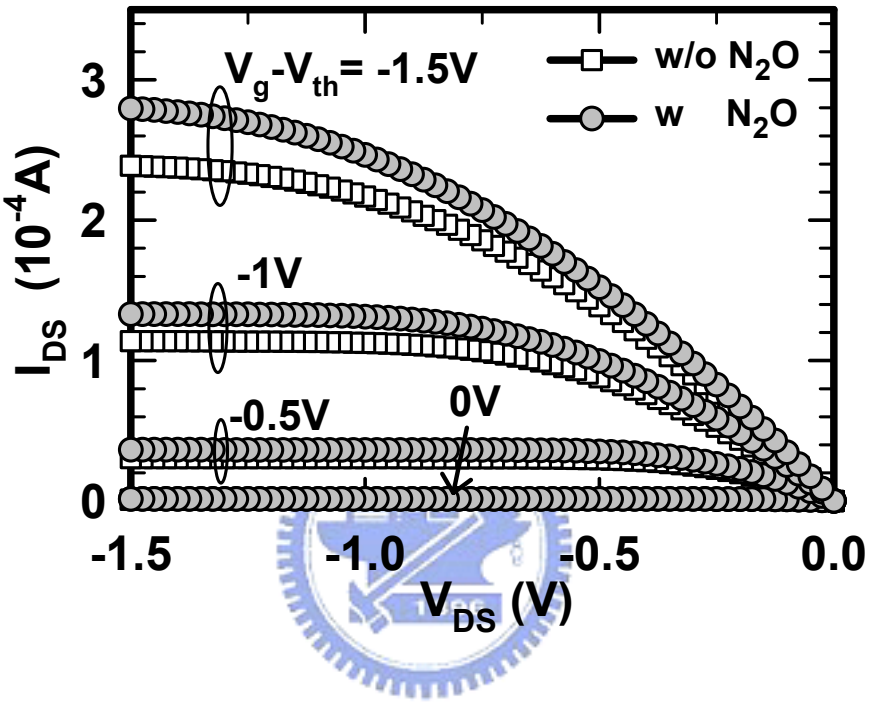


Fig. 4.4 I_d-V_d characteristics of pMOSFETs with HfO_2 gate stacks with/without N_2O plasma treatment.

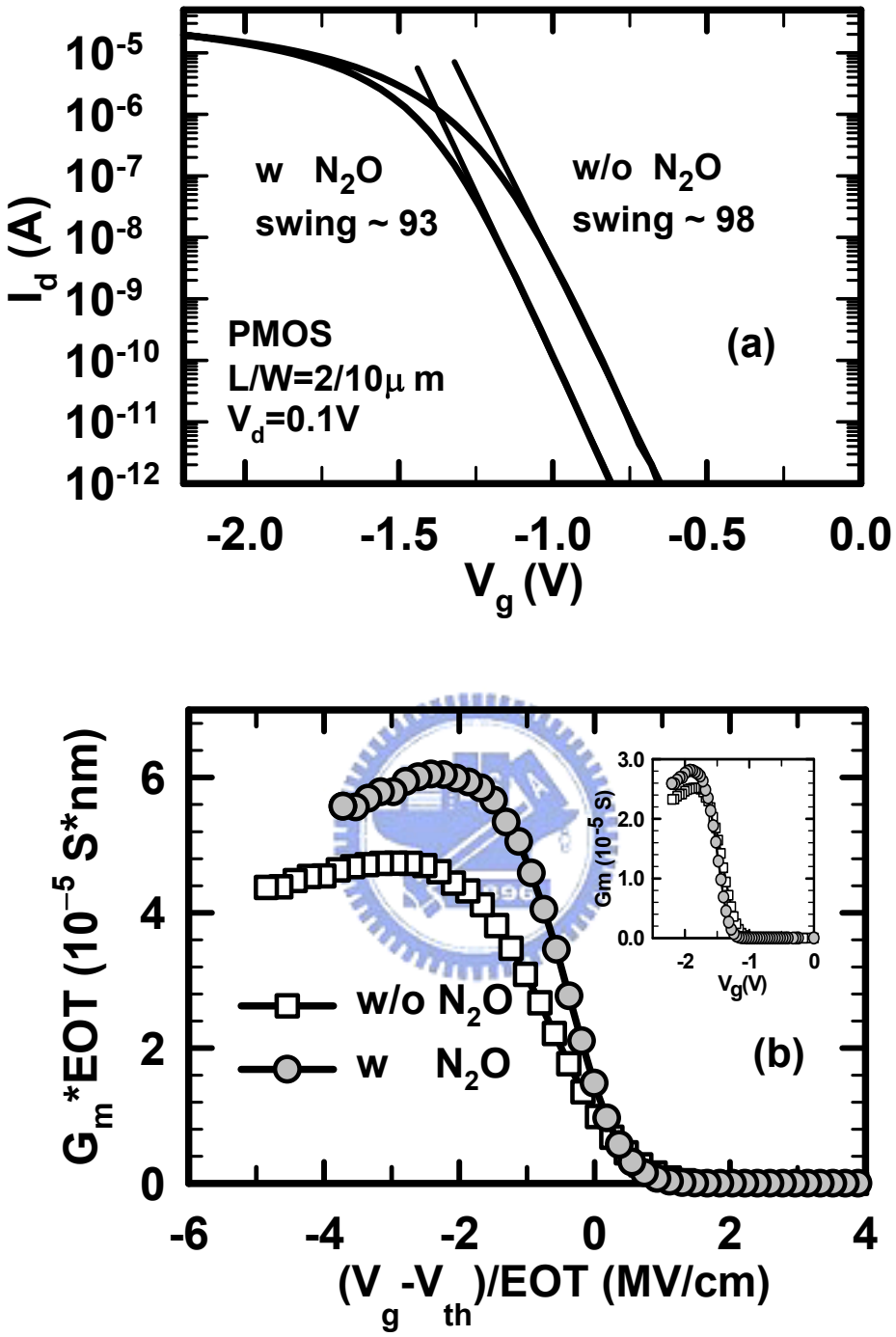


Fig. 4.5 (a) I_d-V_g characteristics and (b) normalized transconductance characteristics of pMOSFETs with HfO_2 gate stack with/without N_2O plasma treatment.

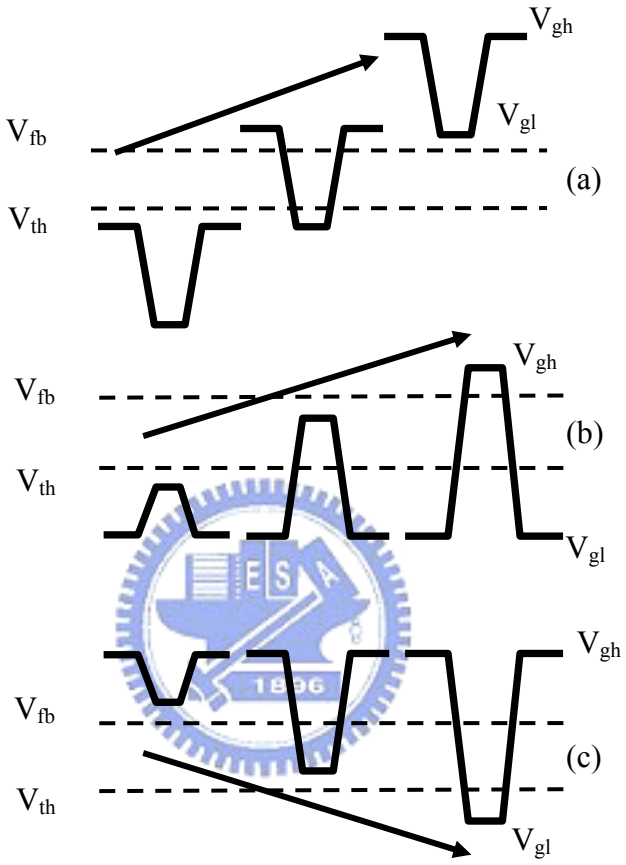


Fig. 4.6 Schematic illustrations for the charge pumping (CP) measurement with (a) fixed amplitude sweep (b) fixed base sweep (c) fixed peak sweep. The arrows indicated the sweep direction.

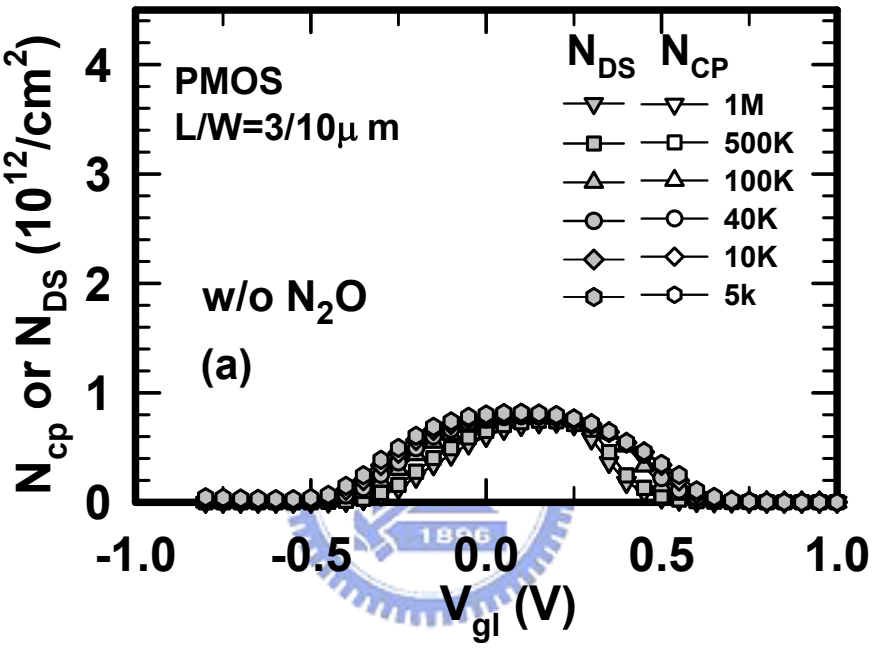


Fig.4.7 Results of the charge pumping (CP) measurements with (a) fixed amplitude (b) fixed base sweep (c) fixed peak sweep as a function of the frequency of gate pulse for the pMOSFETs with HfO_2 gate stack with/without N_2O plasma treatment.

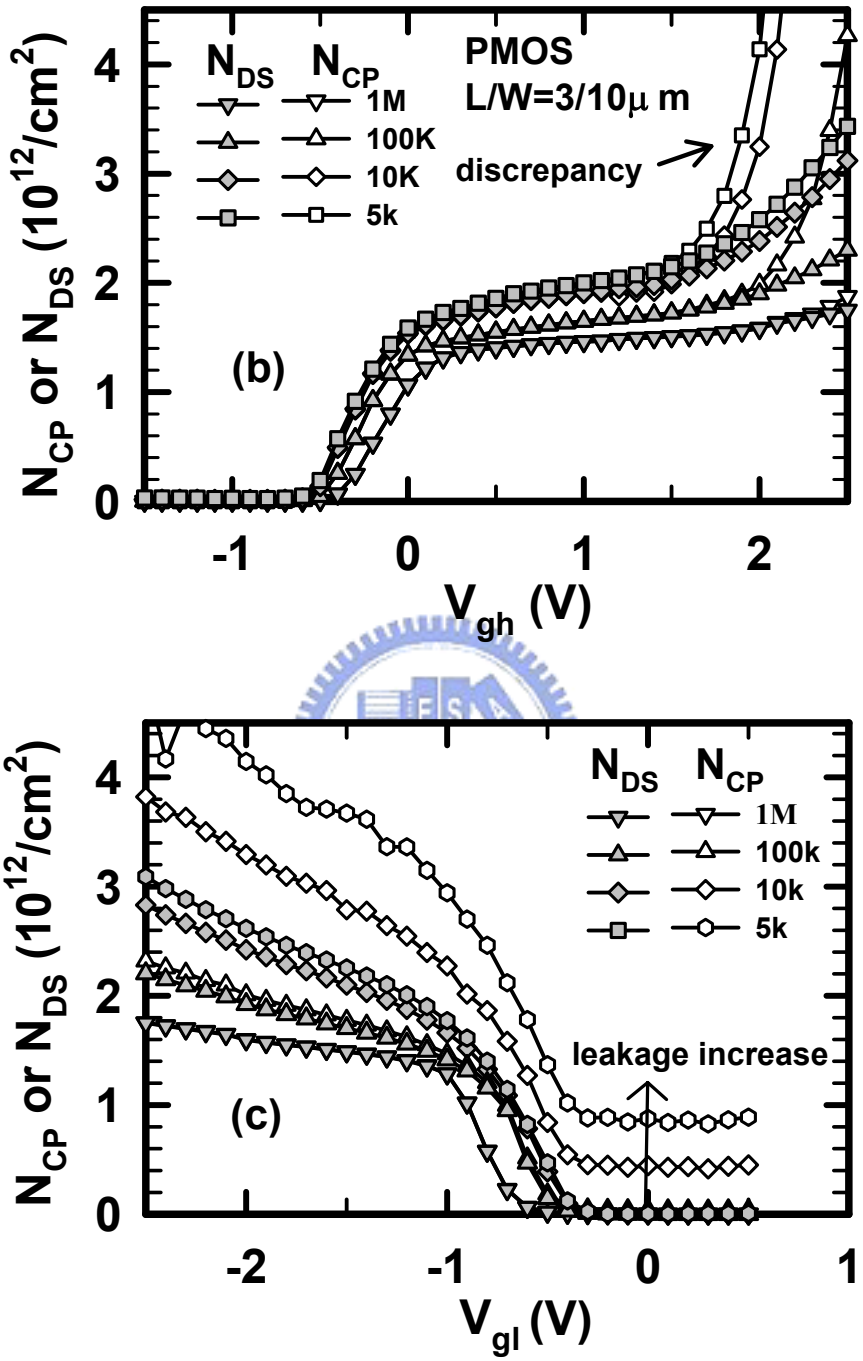


Fig.4.7 Results of the charge pumping (CP) measurements with (a) fixed amplitude (b) fixed base sweep (c) fixed peak sweep as a function of the frequency of gate pulse for the pMOSFETs with HfO_2 gate stack with/without N_2O plasma treatment.

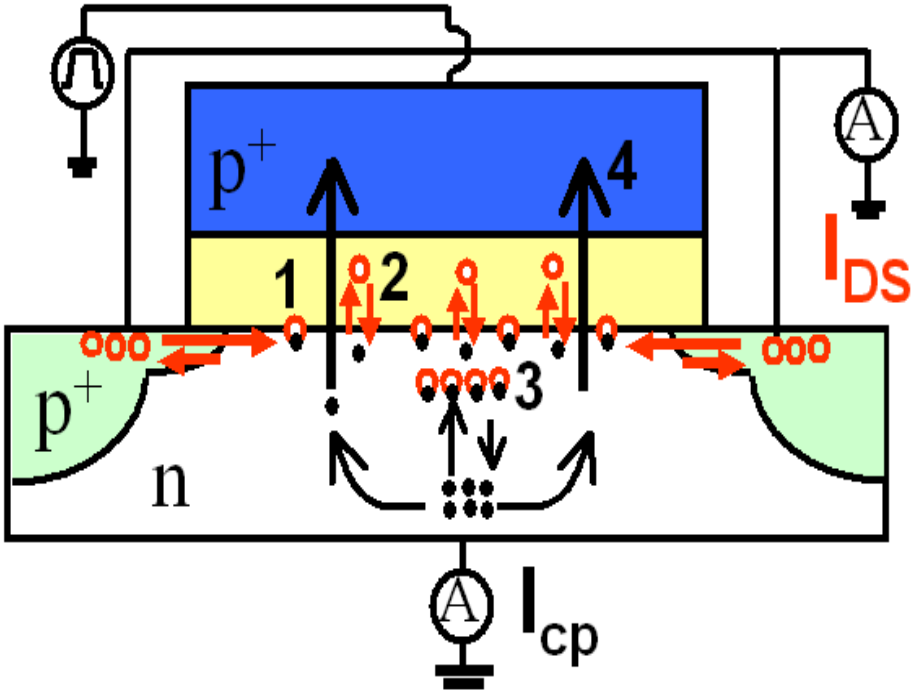


Fig. 4.8 Possible current contributions in a CP measurement with high-k gate dielectrics. Beside the recombination current due to interface states (1), the charging and discharging of bulk defects (2), recombination of inversion carriers due to geometry effect (3), the gate current contribution (4) and minority carrier diffusion (not shown) need to be considered.

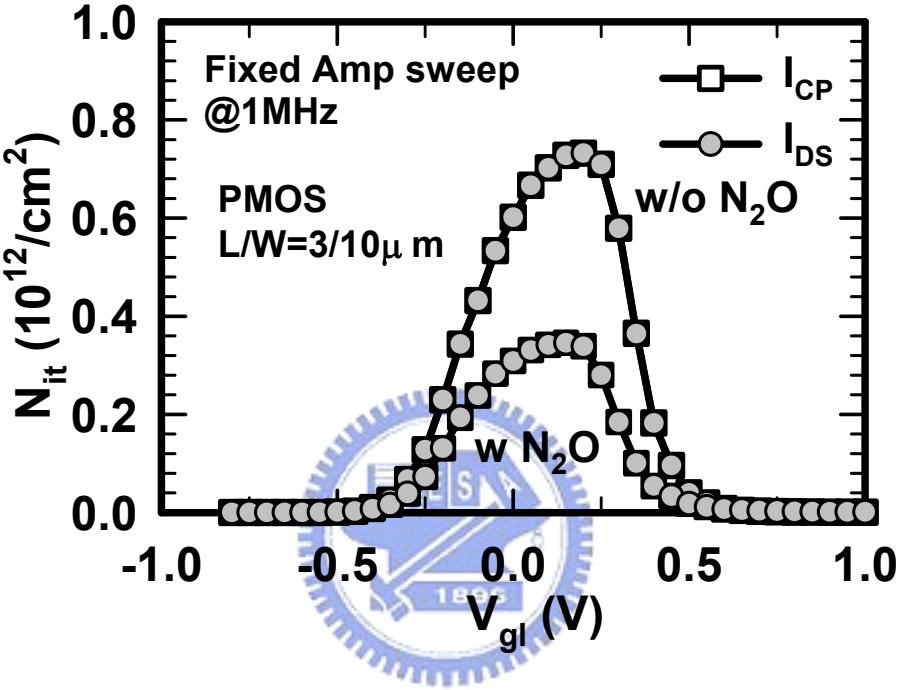


Fig. 4.9 Interface states density as a function of V_{gl} for the HfO_2 gate stacks with/without N_2O plasma treatment measured by fixed amplitude sweep at frequency of 1 MHz.

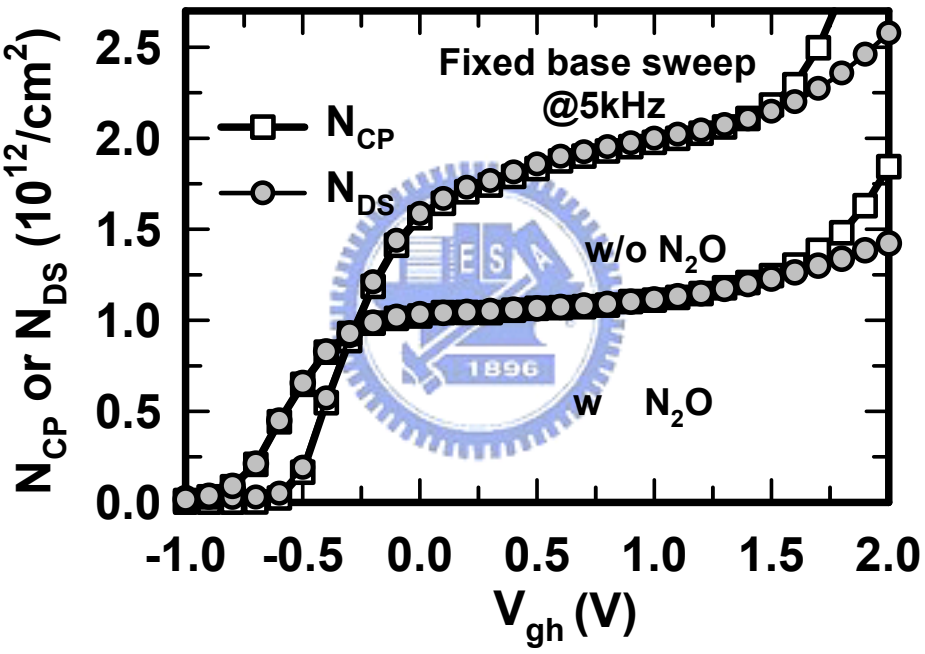


Fig. 4.10 N_{CP} and N_{DS} were determined from the CP current and source/drain current measured by fixed base sweep at 5 kHz. Lower bulk traps were obtained by applying N_2O plasma treatment.

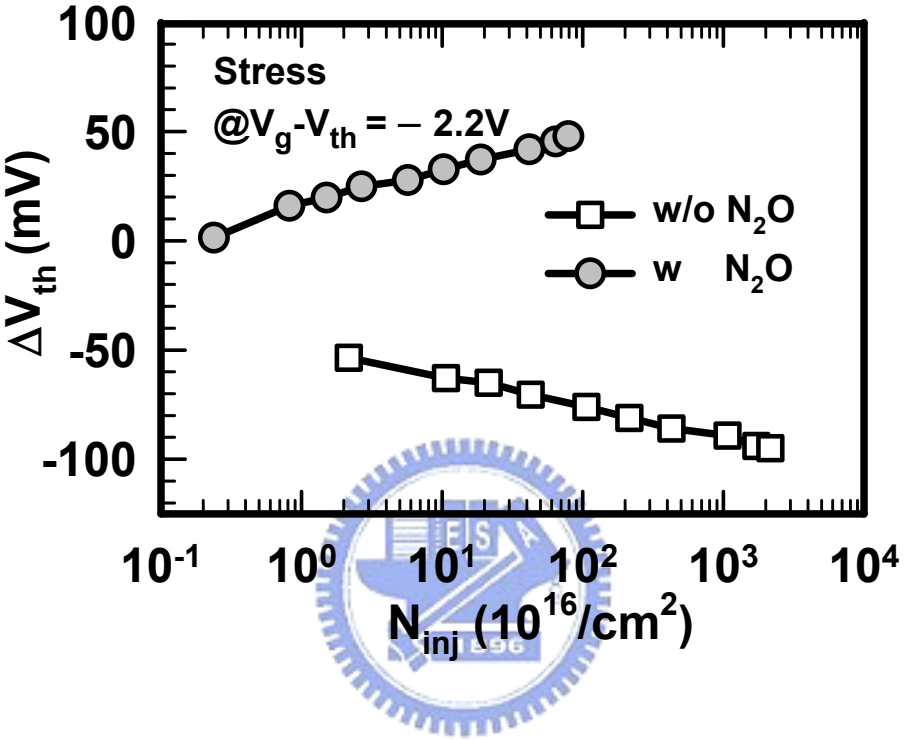


Fig. 4.11 Dependence of threshold voltage shift ($\triangle V_{th}$) on injected charge densities (N_{inj}) under constant gate overdrive voltage of $V_g - V_{th} = -2.2V$ (open symbol) and $V_g - V_{th} = -2.6V$ (solid symbol).

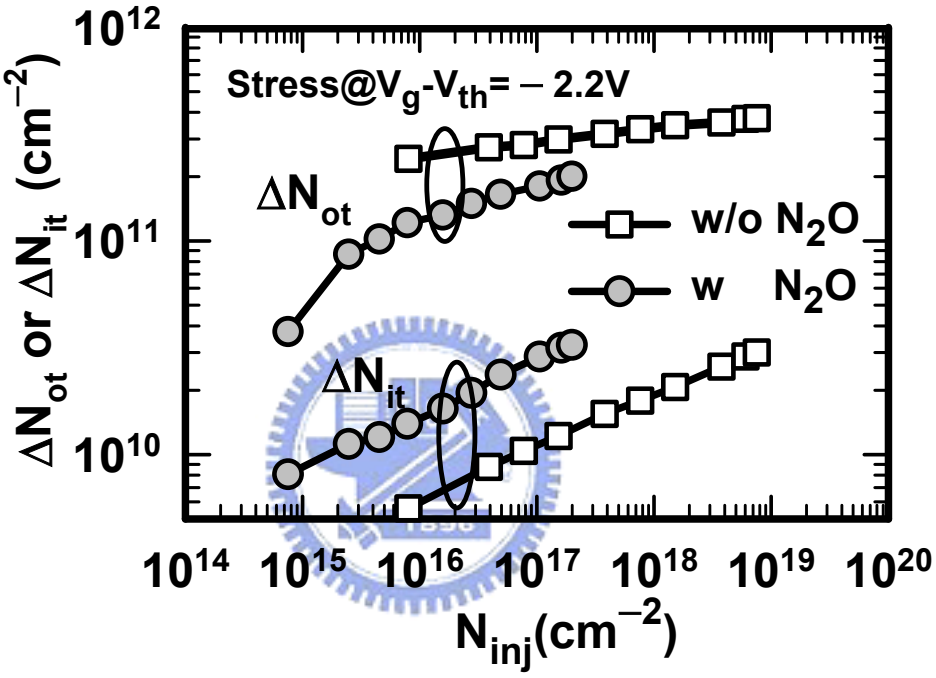


Fig. 4.12 Dependence of generated interface state densities ($\triangle N_{it}$) and trapping charges ($\triangle N_{tot}$) on injected charge densities (N_{inj}) under constant gate overdrive stress voltage of $V_{go}=V_g-V_{th}= -2.2V$ (open sympol) and $V_{go}=V_g-\text{-}V_{th}= -2.6V$ (solid sympol).

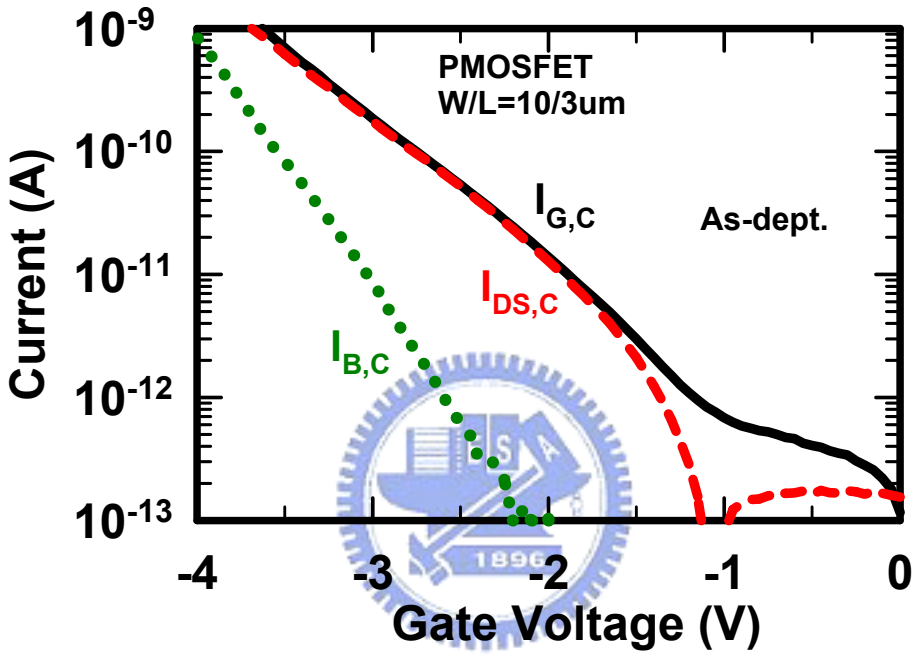


Fig. 4.13 The results of carrier separation of HfO_2/SiON gate stacks without N_2O plasma treatment under inversion region. Gate current is dominated by hole current.

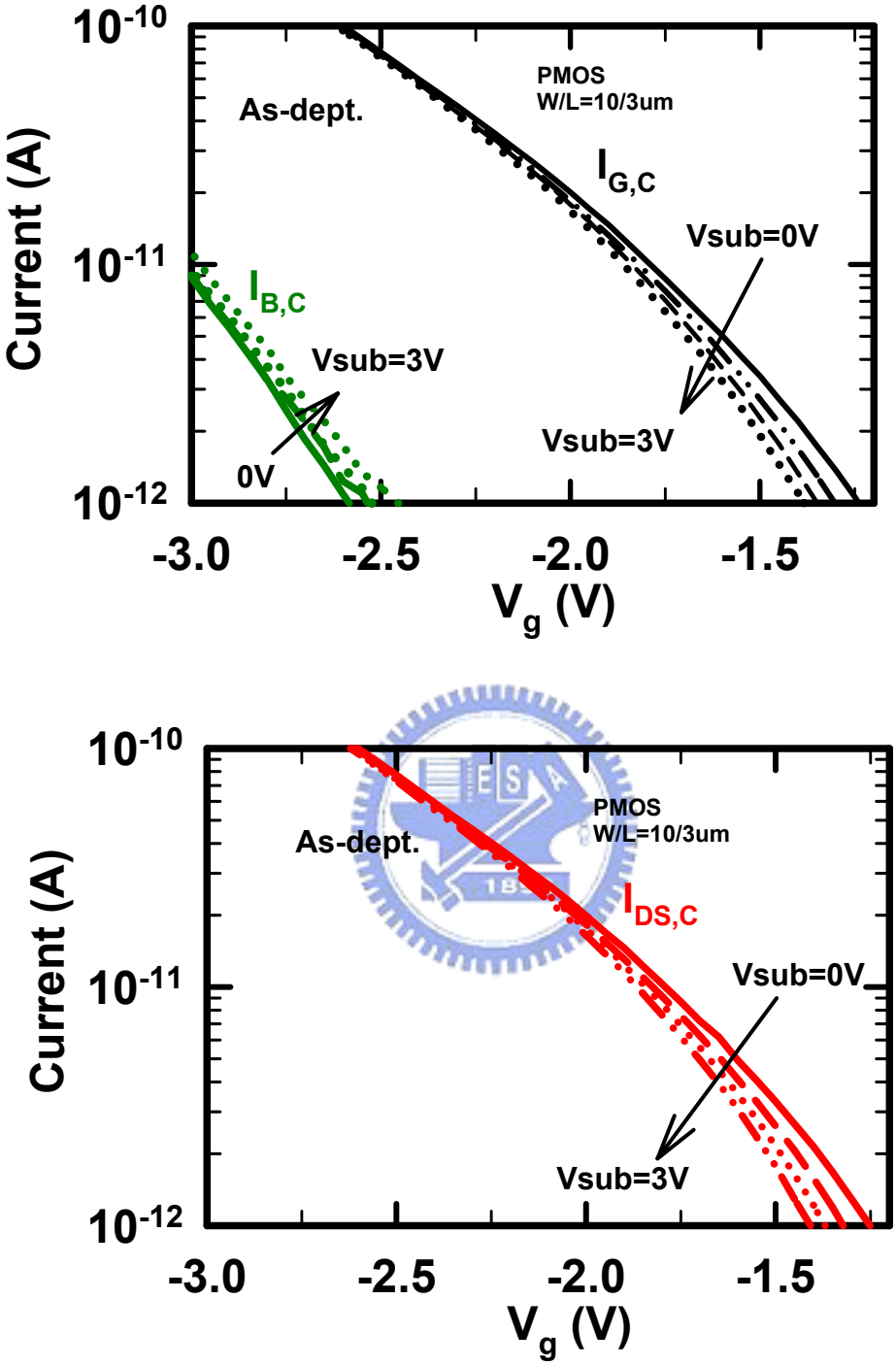


Fig. 4.14 Dependence of (a) I_G , I_B and (b) I_{DS} current on substrate bias for HfO_2/SiON high-k gate dielectrics without post-N_2O plasma treatment.

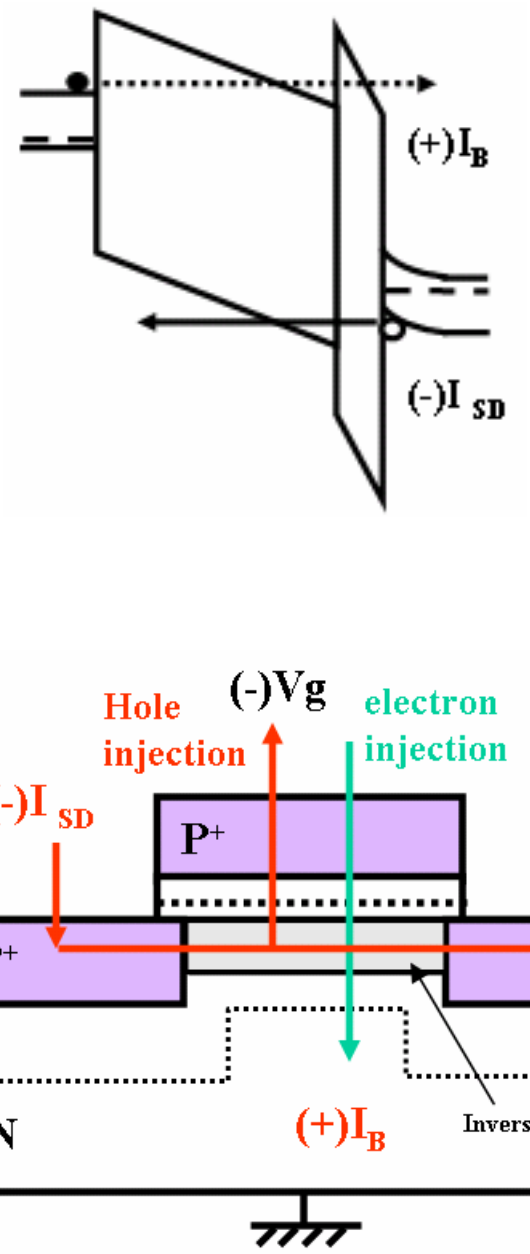


Fig. 4.15 (a) The current components of asymmetric band diagrams (b) The flows of current components of the HfO_2/SiON gate stacks at inversion region are shown.

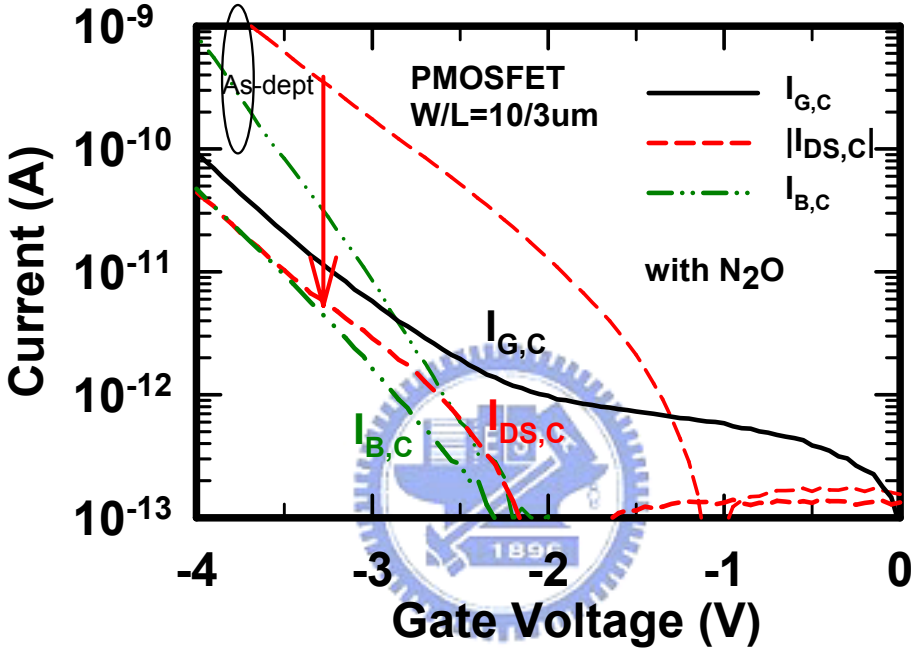


Fig. 4.16 The results of carrier separation of HfO_2/SiON gate stacks with N_2O plasma treatment under both inversion and accumulation regions.

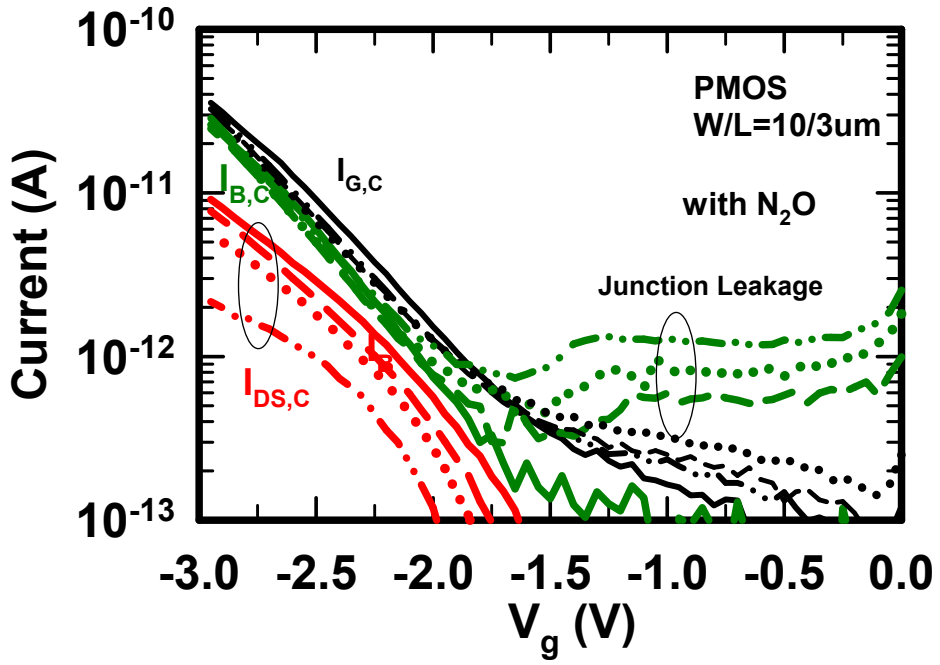
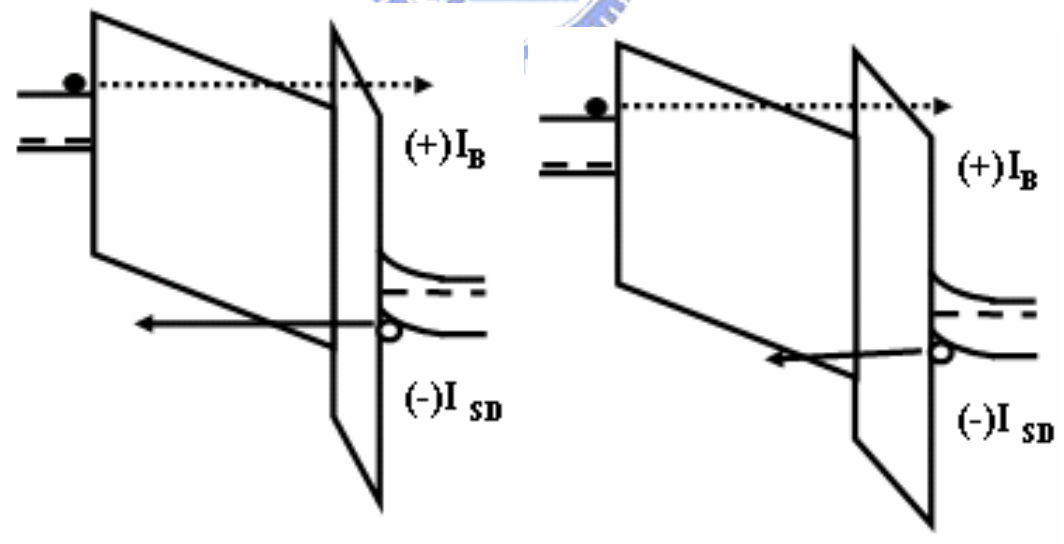


Fig. 4.17 Dependence of I_{SD}, I_G, and I_B on substrate bias for HfO_2/SiON high-k gate dielectrics with post-N_2O plasma treatment.



As-deposited with N_2O treatment

Fig. 4.18 Dependence of carrier separation results of I_{SD}, I_G, and I_B on substrate bias of HfO_2/SiON high-k gate dielectrics (w/ post-N_2O plasma treatment).

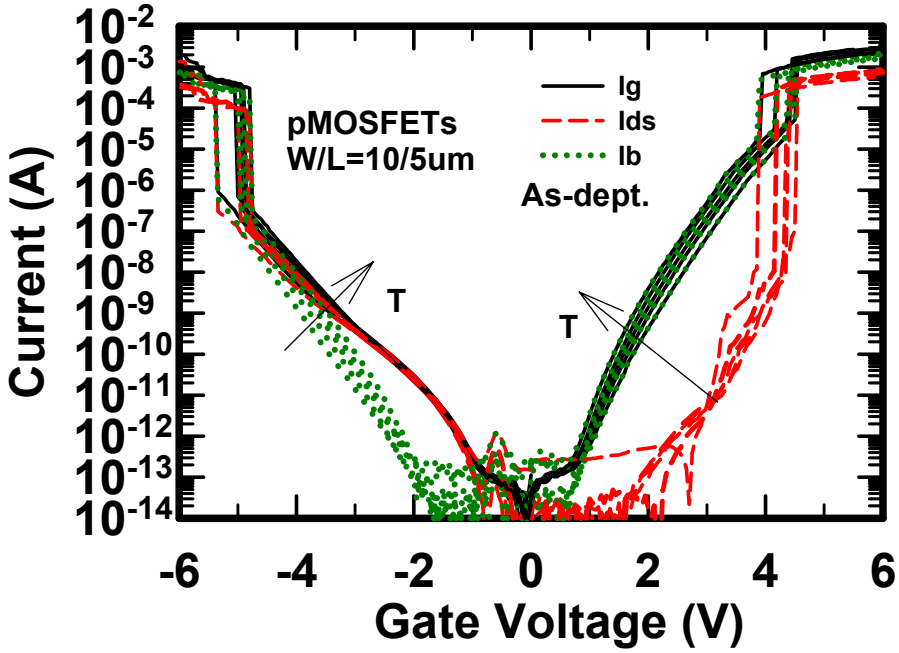


Fig. 4.19 Carrier separation results versus gate voltage for fresh devices at various temperatures of As-dept. samples.

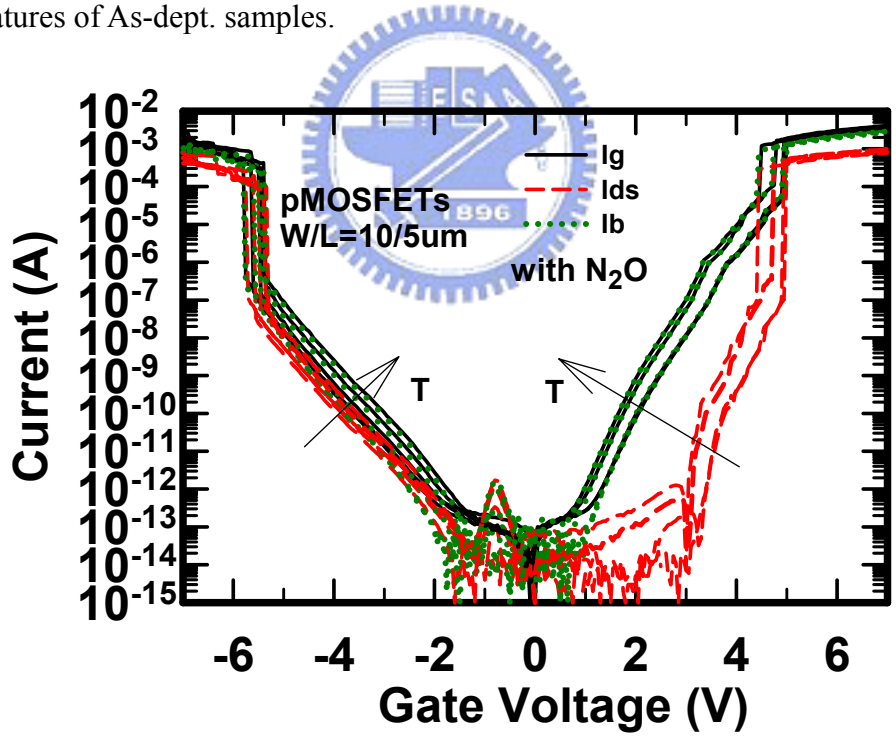


Fig. 4.20 Carrier separation results versus gate voltage for fresh devices at various temperatures of post-N_2O plasma treatment samples.

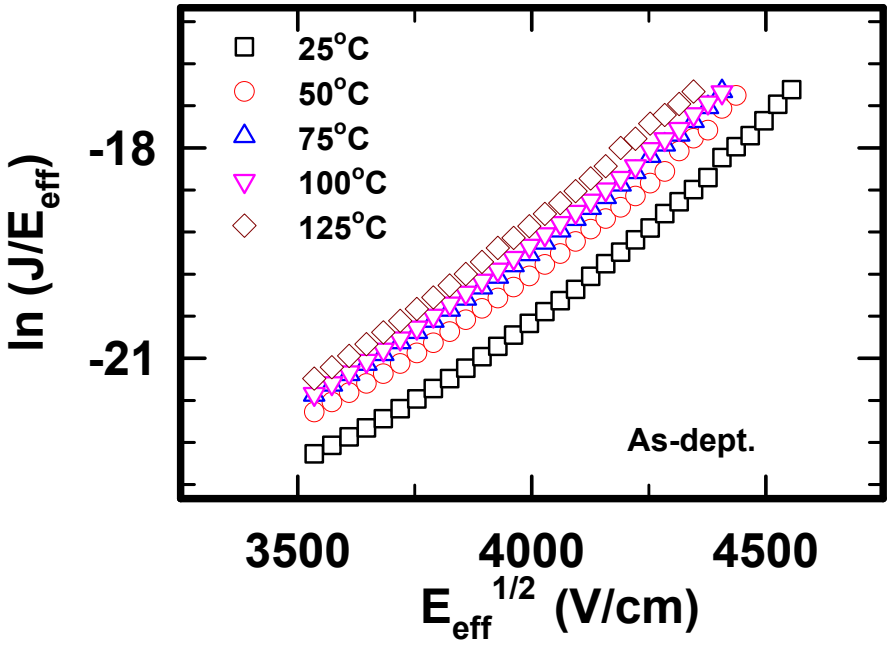


Fig. 4.21 Frenkel-Poole plot for the source/drain current in the inversion region, good fitting curves can be observed (solid line) for the As-dept. sample.

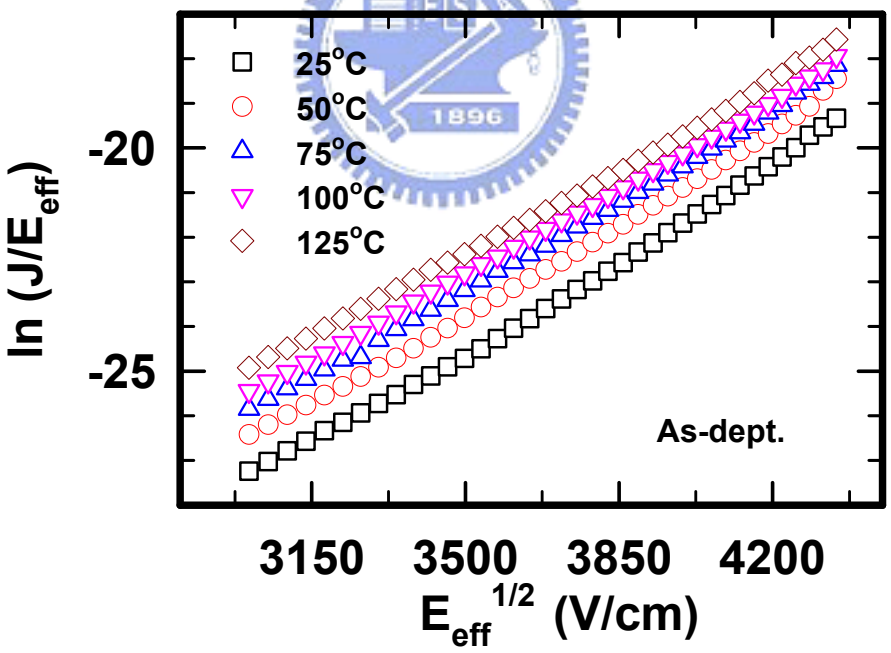


Fig. 4.22 Frenkel-Poole plot for the substrate current in the inversion region, good fitting curves can be observed (solid line) for the As-dept. sample.

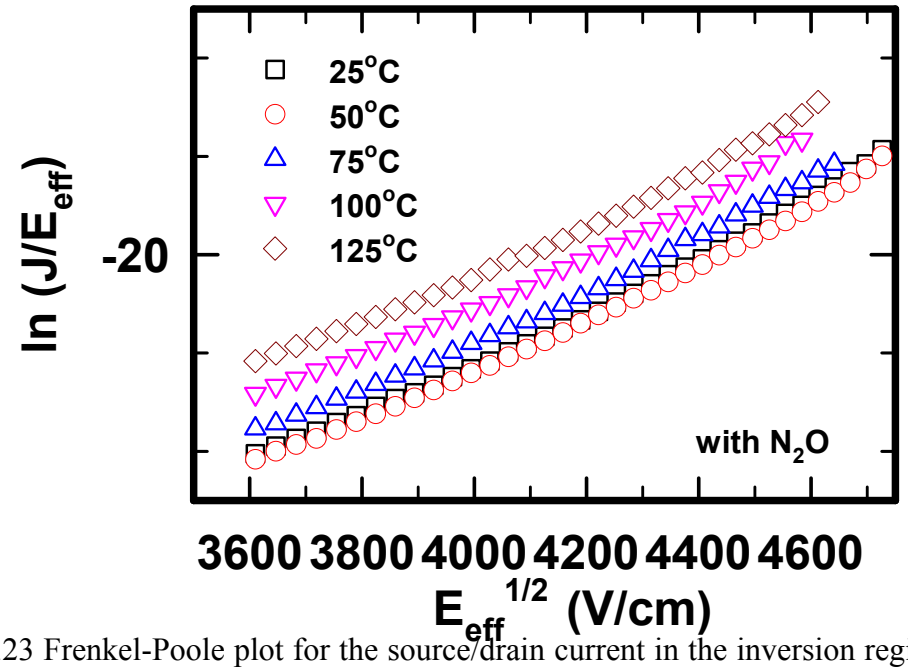


Fig. 4.23 Frenkel-Poole plot for the source/drain current in the inversion region, good fitting curves can be observed (solid line) for the post-N_2O plasma treatment sample.

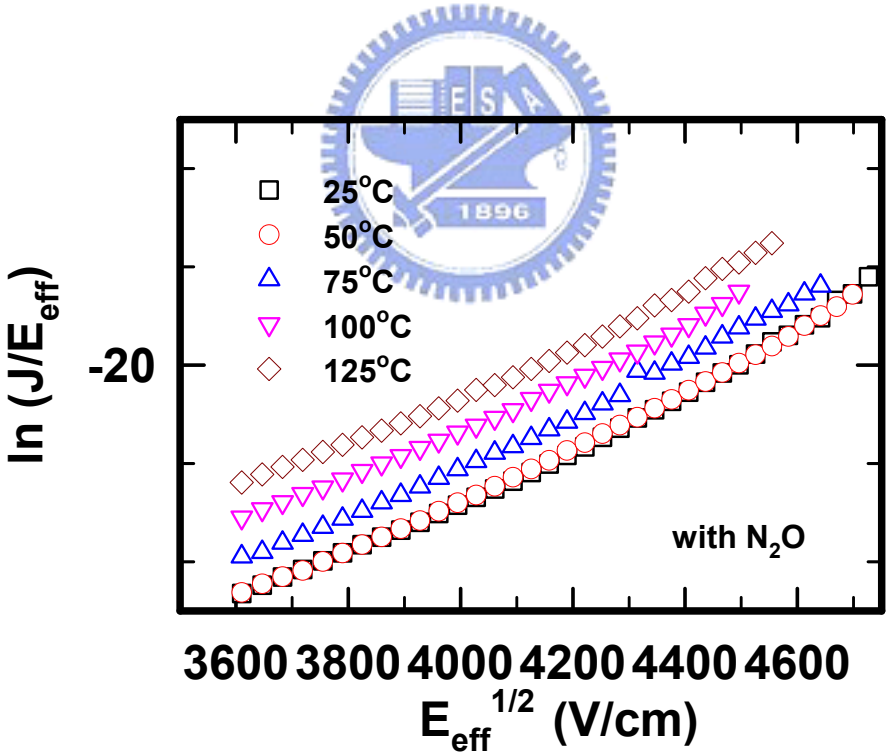


Fig. 4.24 Frenkel-Poole plot for the substrate current in the inversion region, good fitting curves can be observed (solid line) for the post-N_2O plasma treatment sample.

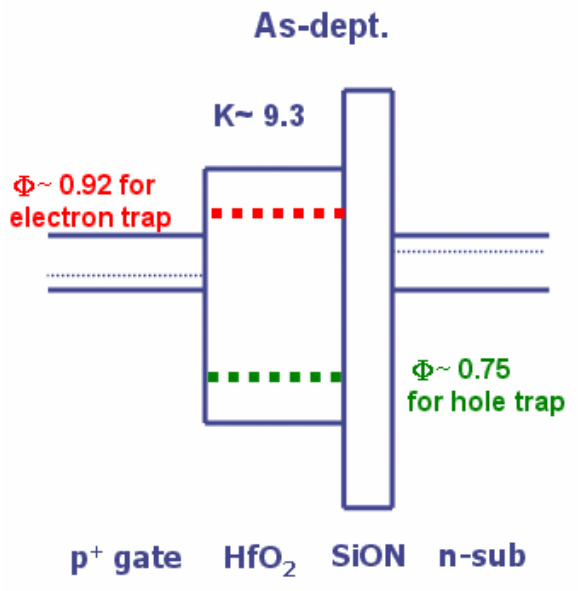


Fig. 4.25 Energy band diagram for HfO_2/SiON gate stacks without N_2O plasma treatment to illustrate the conduction mechanism of Frenkel-Poole emission.

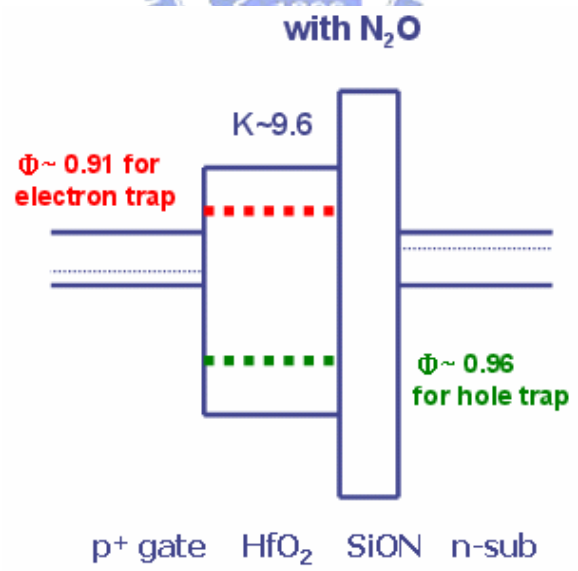


Fig.4.26 Energy band diagram for HfO_2/SiON gate stacks with N_2O plasma treatment to illustrate the conduction mechanism of Frenkel-Poole emission.