Chapter 5
Impacts on the Reliability of HfO_2/SiON Gate Stacks by Post-Deposition N_2O Plasma Treatment

5.1 Introduction

As CMOS devices are scaled aggressively into nanometer regime, SiO_2 gate dielectric has been approaching its physical limit due to the intolerably huge leakage current caused by the direct quantum tunneling of carriers through the ultra-thin oxide. HfO_2 is one of the most promising candidates among high-k materials to replace SiO_2. Even though HfO_2 films have been shown to be scalable down to below 1nm, there still exist several issues that need to be tackled before its acceptance to the mainstream ULSI technologies.

In this chapter, we focus on the study of reliabilities of the high-k dielectric, and address several topics including appropriate measurement setup for high k gate dielectrics, where the breakdown taking place (i.e., in the bulk or IL?), the behaviors observed in dynamic AC and NBTI stresses. The detailed experimental are shown previously in Chapter 4.

5.2 Results and Discussion

5.2.1 Appropriate Measurement Setup for High-k Gate Dielectrics

During reliability evaluation processing, no matter which technique is used, e.g. constant voltage stress (CVS) or negative bias temperature stress (NBTS), the stressing has to be interrupted periodically in order to conduct I_d-V_g and charge pumping measurements for determining the generated interface states density and the threshold voltage shift. As

described in Chapter 4, charge pumping measurement with fixed amplitude sweep at high frequency (1 MHz) is used to determine interface state density based on the recombination current measured by I_{cp} at the substrate terminal. During measurement, pulse trains are applied to the gate electrode. However, this procedure is somewhat similar to the dynamic stress (AC stress), and will cause extra degradation in the high-k films. In an attempt to more precisely single out the degradation caused by the constant voltage stress alone, it is necessary to pre-test the parameter setup, and make sure that no extra damage is done to the film, especially at high temperature. During the charge pumping measurement, the magnitude (ΔV_A) of every single pulse in the train has to be large enough to cause the recombination current. This means that the amplitude of the pulse has to exceed the flat band voltage and threshold voltage of the transistor. However, the amplitude should not be too large to avoid unnecessary stressing of the transistor during measurement. The I_d-V_g measurement conditions also have to be carefully chosen in order not to cause similar unwanted effect.

High-k materials, considered as a candidate to likely replace the conventional SiO_2 or oxynitride gate insulators in the future, do not possess the ideal quality for the gate dielectric as SiO_2 uniquely does. This is due to the a large amount of bulk traps in the high k gate dielectrics, which possess continuous capture cross section and include fast transient charge trapping traps, slow traps, permanent traps. For high-k gate dielectric, there is a serious issue about V_{th} instability. It is shown that the magnitude of the V_{th} instability in the conventional MOSFETs with HfO_2/SiON gate stack is strongly dependent on the details of the measurement sequence. We believe that the origin of the V_{th} instability stems from the fast charging and discharging of pre-existing defects near HfO_2/SiON interface as well as in the bulk of the HfO_2 layer. Therefore, conventional stressing and sensing experiments used to evaluate V_{th} stability can not fully qualify the film, because of fast de-trapping after stress, and it also means that the V_{th} instability will be underestimated.

Fig. 5.1 (a) illustrates DC I_d-V_g characteristics for the sample without N_2O plasma

treatment. First, we measure forward-1 (0 V ~ −2 V) for the "Forward 1", then measure reverse-1 (−2 V ~ 0 V) for the "Reverse 1" as first cycle. Then, we repeat this sweeping cycle again. We find V_{th} shifts toward negative gate voltage after first cycle, which indicates that net positive charges are trapped in the gate dielectric layer as the devices were measured. In addition, V_{th} recovers to some degree during the second cycle. However, V_{th} does not fully recover to its initial value, indicating that some positive charges remain in the gate dielectrics. These behaviors indicate that both fast trapping and de-trapping charges have taken place in the HfO_2 during device's parameters sensing measurement, which could obviously lead to the misjudgment of threshold voltage shift. However, when the starting sweeping voltage of I_d-V_g characteristics is changed to 1V, full recovery is obtained, as shown on **Fig. 5.1** (b). This indicates that even with a very small voltage range, i.e., from 0V to -2V, charge trapping effect can be detected during the transistor's parameters sensing measurements, which could obviously lead to the misjudgment of threshold voltage shift. When the sweeping cycle range of I_d-V_g characteristics shifts to more negative gate voltage range (i.e., [1V↔-2V; 1V↔-2.1V; 1V↔-2.2V;….; 1V↔-2.8V;]), we can see that the magnitude of V_{th} instability increases with sweeping range, and full recovery of the characteristics can be obtained, as shown in **Fig. 5. 2**.

The fast trapping/de-trapping characteristics during sensing measurements are similar for the samples with N_2O treatment, but the species for trapping changes from holes to electrons. (**Fig. 5.3** and **Fig. 5.4**). In addition, positive starting voltage of I_d-V_g measurements can de-trap both holes and electrons, resulting in full recovery of the characteristics. Therefore, to neutralize the effects of fast traps [1-5], a small positive gate voltage (V_g=1V) which is opposite to stress voltage, is applied for 15 seconds, prior to I_d-V_g and charge pumping measurements. This procedure will serve to minimize the fast unstable charge trapping/de-trapping effect during constant gate override stress.

5.2.2 Breakdown Characteristics of HfO(N)/SiON Gate Stack by Using

Carrier Separation Method

Dielectric degradation and breakdown are the two most important concerns in the high-k devices, whose characteristics are influenced by defects and fixed charges in the high-k films. The breakdown characteristics of high-k films are significantly different from those of conventional SiO_2 gate insulator. Since it is inevitable to form an IL layer at the high-k/Si interface when the high-k film is deposited on Si substrate, it is essential to consider at least two-layer stacked structure for high-k gate dielectrics. Moreover, it is noted that the electric field across the interfacial layer is larger than that across the high-k dielectric film. Therefore, it is crucial to understand the relationship of leakage and breakdown in the HfO_2/SiON gate stacks. In this work, using the carrier separation measurement technique, we are able to distinguish two different breakdown mechanisms, i.e., high-k bulk-initiated breakdown and an interfacial-layer-initiated breakdown. The carrier type and conduction mechanism for samples both with and without N_2O plasma treatment have been addressed in Chapter 4.

Fig. 5.5 shows the evolution of I_G, I_{SD}, and I_B under negative constant voltage stress. It is noted that a large stress voltage is applied to ensure that traps are generated during stressing. This is important because with small stress bias, charge filling instead of trap generation becomes the dominant trapping mechanism in high-k films. The period during which the gate current is almost constant as constant voltage stress is applied is called "stress induced leakage current (SILC) condition", since SILC is generated during this duration. The soft breakdown (SBD) in the HfO_2/SiON gate stacks is clearly defined as a sharp drop of the gate current. In order to identify the dominant carrier type after the electrical stress, the carrier separation experiments during SILC and after SBD were performed. The increment of I_B is larger than that of I_{SD}, indicating that the breakdown has taken place in the bulk. The results of I_G, I_B, and I_{SD} of carrier separation during SILC and after SBD for the sample without N_2O plasma treatment are shown in **Figs. 5.6** (a), (b), (c), correspondingly. At SILC condition, comparing **Figs. 5.6** (b) and (c), the increase in electron current is about an order of

magnitude larger than the increase in the hole current. This indicates that both electron and hole traps are created during the SILC duration, and the generation rate for electron traps is higher than that of holes. However, during SILC duration, the gate current is still dominated by the hole current, flowing from the S/D region. The speculated locations of generated traps during the SILC are shown in **Fig. 5.7** (a). Further, considering the situation in SBD, we find that I_B increases significantly for the V_G sweeping range from 0V to –3V. Therefore, we speculate that there does exist a breakdown phenomenon from the viewpoint of electron current; the electron path through the bulk after breakdown is as shown in **Fig. 5.7** (b). However, for I_{SD} (hole current), the leakage increases rapidly as $|V_G|>|V_{th}|$, and becomes comparable to I_B at $|V_G|>2.5V$. This indicates that the breakdown is more likely to occur at the interfacial layer, because holes have to tunnel through IL only at higher voltages, as shown in **Fig. 5.7** (b). In addition, the dominant component of the gate current has switched from hole current during SILC duration to electron current after SB.

The same procedure was repeated to examine samples with post-N_2O plasma treatment. The results of I_G, I_B, and I_{SD} extracted from carrier separation technique during SILC and after SBD for the sample with N_2O plasma treatment are shown in **Figs. 5.8** (a), (b) and (c), respectively. At SILC condition, comparing **Figs. 5.8** (b) and (c), the increase in hole current is much larger than the increase in the electron current. This indicates that both electron and hole traps are created during the SILC duration; while the generation rate for hole traps is higher than that of electron, which is contrary to the result of the sample without N_2O plasma treatment. After SBD occurrence, I_G is mainly contributed by I_B for the entire V_G sweep range, which means that the breakdown path for the electrons has been formed in the high-k film, as shown in **Fig. 5.9**. From **Fig. 5.8** (c), we can see that I_{SD} current increases slightly even when $|V_G|<|V_{th}|$, indicating a bulk breakdown path in the high-k film, as shown in **Fig. 5.9** (b). This is consistent with the higher hole trap generation rate in the sample with N_2O plasma treatment. At even higher voltages of above $|–2.5V|$, I_{SD} is almost as large as I_B, indicating that

IL has been also broken down after the occurrence of SBD. The results were reexamined, as shown in **Fig. 5.9** (b).

5.2.3 Dynamic AC Stress

For CMOS operation, V_{DD} and GND signals are generally supplied to turn on and off the device, which means that AC gate bias is frequently used. However, in the reliability test of gate dielectric, DC stress is commonly used for convenience. The prediction from DC results in an unrealistically pessimistic device lifetime. While AC stress gives a more realistic and correct insight into the device lifetime. It is reported that the threshold voltage shift is indeed reduced under dynamic stress [6-8].

Fig. 5.10 shows the schematic setup of dynamic AC stress for the HfO_2/SiON gate stacks with and without N_2O plasma treatment. During the AC stress, AC square wave pulse from pulse generator is applied to the gate electrode; while the other three terminals are grounded. For a fair comparison, the cumulative 'on-time' under the AC unipolar stress is defined as the 'stress time' and the duty cycle is fixed as 50% for all samples. The stress condition is at a gate overdrive $V_{go}=V_g-V_{th}= -2.2V$.

Fig. 5.11 shows the interface state generation for the HfO_2/SiON gate stacks without N_2O plasma treatment under unipolar AC stress at various frequencies. It can be seen that the generated N_{it} on the order of 10^{10} is essentially independent of frequency. In contrast, the threshold voltage shift shows strong frequency dependence, as shown in **Fig. 5.12**. Under DC stress with $V_{go}= -2.2V$, positive charges trapped in the gate dielectric are observed. However, under AC stress, trapped positive charges are reduced with increasing stress frequency. When the frequencies are higher than 10k Hz, the specie of charge trapping actually becomes negative charges, as shown in **Fig. 5.13**, rather than positive charges. This suggests that both electrons and holes are trapped in the high-k film. Because of the unipolar stress (i.e., $V_{go}= -2.2V$ during stressing cycle, $V_g=0V$ during relaxation cycle), negative charges being trapped

during off-time is unlikely to happen. Therefore, simultaneous trapping of positive and negative charges during on-time may be a reasonable explanation. Since the cumulative "on-time" and "off-time" are the same in two cases, there exits two possible explanations for frequency dependence on threshold voltage shift. First, it is believed that the de-trapping of trapped positive charges could happen during the off-time period. Second, the period of AC stress frequency may be too short for positive charge trapping to occur in the pMOSFETs with HfO_2/SiON gate dielectrics.

Next, the off-time characteristics (or reduced on-time for trapping carrier) were studied by verifying three duty cycles, i.e., 25%, 50%, 75%. **Fig. 5.14** shows that generated interface state densities are also independent of duty cycles and frequencies. **Fig. 5.15** shows ΔV_{th} under AC stress with (a) 10 kHz, (b) 100 Hz, and (c) 10 Hz. For all different frequencies, we can find that a shorter duty cycle shows smaller negative threshold voltage shift, implying that longer off-time (i.e., shorter duty cycle) de-traps more positive charges. In addition, the difference of ΔV_{th} between duty cycle of 25% and 75% decreases with increasing stress frequency. This indicates that the on-time during the AC stress cycle may be too short for hole trapping since holes populating at the gate stack/substrate interface take longer time to tunnel through the interfacial layer into the high-k film. Therefore, we consider that there are two plausible mechanisms for hole trapping. First, it is believed that the de-trapping of trapped positive charges could happen during the off-time period. Second, the period of AC stress frequency may be too short for positive charge trapping to occur in the HfO_2/SiON gate dielectrics.

Fig. 5.16 shows the generated interface states as a function of stress time at various stress frequencies. It can also be seen that changing the frequency does not significantly affect the generated interface state density for the samples with post-N_2O treatment. The same trend of frequency dependence on the threshold voltage shift has been observed for the post-N_2O plasma samples, as shown in **Fig. 5.17,** besides the trapping of negative charges under DC

stress, which is due to higher electron current than hole current. Due to the thicker interfacial layer for the post-N_2O plasma samples, the tunneling time for hole through the interfacial layer increases, making holes more difficult to be trapped in the high-k film during the on-time of an AC frequency cycle. Therefore, the more positive threshold voltage shift occurs as the AC frequency is increased. Moreover, changing duty cycle produces the same effect on the control samples for the threshold voltage shift and generated interface state density (shown in **Fig. 5.18**).

5.2.4 NBTI in HfO_2/SiON Gate Stacks

It is well-known that for the SiO_2-based gate dielectrics, high voltage stress on the gate electrode of MOSFETs could lead to flatband or threshold voltage shift, in particular at elevated temperatures. This phenomenon is called bias temperature instability (BTI). Most of BTI researches on the SiO_2 dielectric are focused on the negative BTI, because of aggravated degradation as compared with that in positive BTI [9]. Besides, Kimizuka et al. have shown that as the gate oxide thickness is scaled down to the range of 3.5nm, NBTI in pMOSFET could become the bottleneck limitation to the SiO_2 scaling than hot carrier instability (HCI) in nMOSFETs [9]. NBTI of pMOSFETs is an important reliability issue for both digital and analog applications. Despite the many works on NBTI in order to keep NBTI at bay, including better modeling and improved processes, the basic root cause mechanism is still not fully understood. Ogawa et al. proposed a model based on their experimental results [10].

$$Si_3 \equiv SiH + p^+ \Leftrightarrow Si_3 \equiv Si* + H^+ \qquad \text{Reaction-limited} \qquad (5.1)$$

$$Si_3 \equiv SiH \Leftrightarrow Si_3 \equiv Si* + H_i \qquad \text{Diffusion-limited} \qquad (5.2)$$

$$O_3 \equiv SiH + p^+ \Leftrightarrow O_3 \equiv Si* + H_i \qquad (5.3)$$

$$(H^+, H_i)_{\text{interface}} \Leftrightarrow (H^+, H_i)_{\text{bulk}} \qquad (5.4)$$

It can be seen that the model can be separated into reaction-limited and diffusion-limited

processes [11-12]. The reaction-limited process is dependent on the number of holes near the interface available to interact with Si-H bonds. Once the reaction-limited process is equilibrated, the diffusion-limited process is dependent on the rate of diffusion of hydrogen away from the interface.

Figs. 5.19 (a) and (b) show I_d, G_m-V_g characteristics before and after V_{go}= −1.5V stress for 1000 sec at room temperature and 125°C, respectively. A parallel shift of I_d-V_g curve can be seen, which indicates that less $\triangle N_{it}$ is generated. Negligible G_m degradation also can be observed. For confirmation, the generated interface state densities versus stress time are depicted in **Fig. 5.20**. We can recall that the fresh N_{it} value is on the order of $8x10^{11}$ /cm^2, which means that the amount of $\triangle N_{it}$ is relatively small, compared to N_{it}. $\triangle N_{it}$ is shown to obey the power-law, and the index is 0.24, exactly the same value as that in the conventional SiO_2, indicating that $\triangle N_{it}$ follows the reaction-diffusion model. **Fig. 5.21** shows that $\triangle V_{th}$ increases with increasing temperature. **Fig. 5.22** shows the time evolution of $\triangle N_{it}$ and $\triangle N_{tot}$ under BTS stress at 125°C. $\triangle N_{tot}$ is larger than $\triangle N_{it}$ by more than an order of magnitude, signifying that the bulk traps in HfO_2, rather than interface state density generation, is responsible for the transistor degradation [13].

After a gate overdrive stress of −2V for 1000 seconds at either room temperature or 125°C, the resultant I_d and G_m-V_g are shown in **Figs. 5.23** (a) and (b), respectively. At room temperature, I_d depicts only a parallel shift after 1000 seconds stress, and G_m peak shows less than 5% degradation. Similar trend is observed for the high temperature case. However, the threshold voltage shift for BTS at elevated temperature (125°C) is significantly smaller than that at room temperature. **Fig. 5.24** shows the generated interface state densities as a function of stress time at various stress temperatures. We can clearly see that the interface state densities are degraded as the stress temperature increases and $\triangle N_{it}$ still depicts the power-law, and the index is 0.24. **Fig. 5.25** displays the threshold voltage shift dependence on stress time under various stress temperatures. It can be seen that $|\triangle V_{th}|$ seems to reduce when the stress

temperature increases. According to the reaction-diffusion model of NBTI, the threshold voltage shift ($|\triangle V_{th}|$) should keep increasing because of the increasing positive charge trapping related to hydrogen species. Unfortunately, it does not follow the predicted trend in our samples. There are two possibilities: one is the increased electron trapping that can overcompensate the hole trapping, and the other is the occurrence of recombination of hole trappings. **Fig. 5.26** clarifies the culprit of threshold voltage shift, whether it stems from the oxide traps or the interface states. At low temperature, $\triangle N_{tot}$ is about two orders of magnitude larger than $\triangle N_{it}$, indicating that trapping in the HfO_2 bulk can be a very critical issue. However, I_d degradation curve in **Fig. 5.27** reveals that the recombination of hole trapping is the root cause of **Fig. 5.26**, as the I_d degradation should be worsen if the amount of total traps increases. The recombination occurrence can be explained by the rapidly increasing electron current as the temperature rises, while the hole current remains the same, as shown in **Fig. 5.28**.

By changing the stress voltage to V_{go}= –2.5V, a parallel shift is still obtained and the subthreshold swing shows a slight increase after stress at 125℃, as shown in **Fig. 5.29** (a) and (b), respectively. From **Fig. 5.30**, we can find that trapping effect in high-k bulk is still an order of magnitude larger than $\triangle N_{it}$, indicating that reaction-reaction model may not be suitable for HfO_2/SiON gate stacks, due to the preponderant bulk traps, compared to interface traps. As shown in **Fig. 5.30**, the power-law index in the relationship between $\triangle V_{th}$ and stress time increases (i.e., from 0.06 at low temperature to 0.15 at 125°C). Because at larger stress voltage, the valence band of the Si substrate shifts closer to the hole traps, located at Φ_B~0.75eV, as already mentioned in Chapter 4. So holes become easier to jump and get trapped.

Fig. 5.38 and **Fig. 5.39** compare the control sample and the sample with N_2O plasma treatment under V_{go}= –2.5V at 125°C. The improvement can be achieved after post-N_2O plasma treatment, especially at higher temperature.

In conclusion, $\triangle N_{it}$ follows the reaction-diffusion model with a power-law index of 0.25, because our IL is still SiON in nature. In addition, bulk traps always dominate the degradation of HfO_2/SiON, which means that trapping effect is larger than hydrogen species effect. **Fig. 5.40** shows that under dynamic stress, the recovery of $\triangle N_{it}$ is observed, and shows no dependence on the relaxation voltage. **Fig. 5.41** shows that the trapped charges can be de-trapped by the relaxation voltage.

5.3 Summary

Several types of reliability testing have been performed, including dynamic stress, evaluation of bulk or IL breakdown, and NBTI. It is found that the post-N_2O plasma treatment may not be beneficial because of the resulting higher electrons trapping under AC stress, even though it exhibits several advantages as discussed in Chapter 4. Bias temperature instability shows that leakage current could affect the threshold voltage shift behavior. Our data also confirm that two different mechanisms exist in HfO_2/SiON gate stacks, i.e., trapping and the NBTI. And the effect of trapping is larger than the reaction-diffusion effect.

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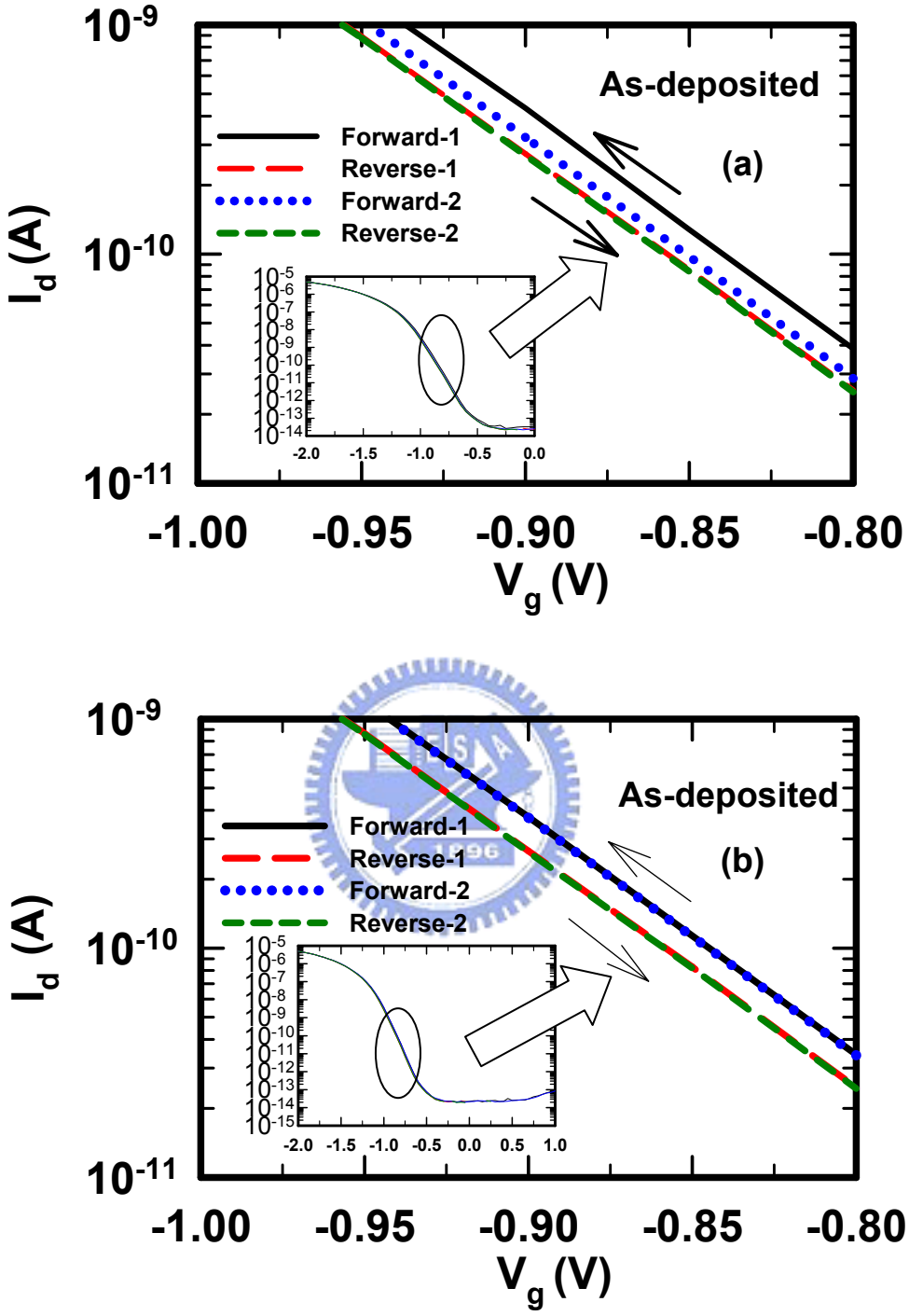


Fig. 5.1 Repetitive I_d-V_g traces for HfO_2/SiON high-k gate dielectric using measurement sequence (a) [V_g=0V ↔ V_g=–2V], (b) [V_g=1V ↔ V_g=–2V]. (w/o post-N_2O plasma treatment).

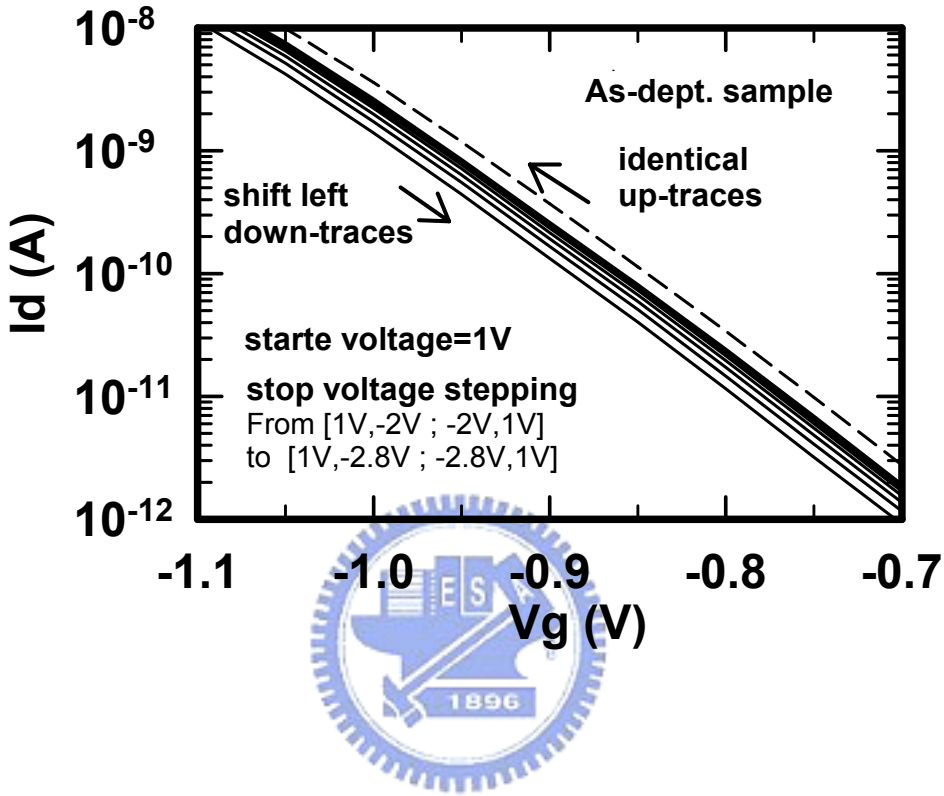


Fig. 5.2 Repetitive I_d-V_g traces for HfO_2/SiON high-k gate dielectric using measurement sequence of [V_g=1V ↔ –2V], [V_g=1V ↔ –2.2V], … , to [V_g=1V↔–2.8V] (w/o post-N_2O plasma treatment).

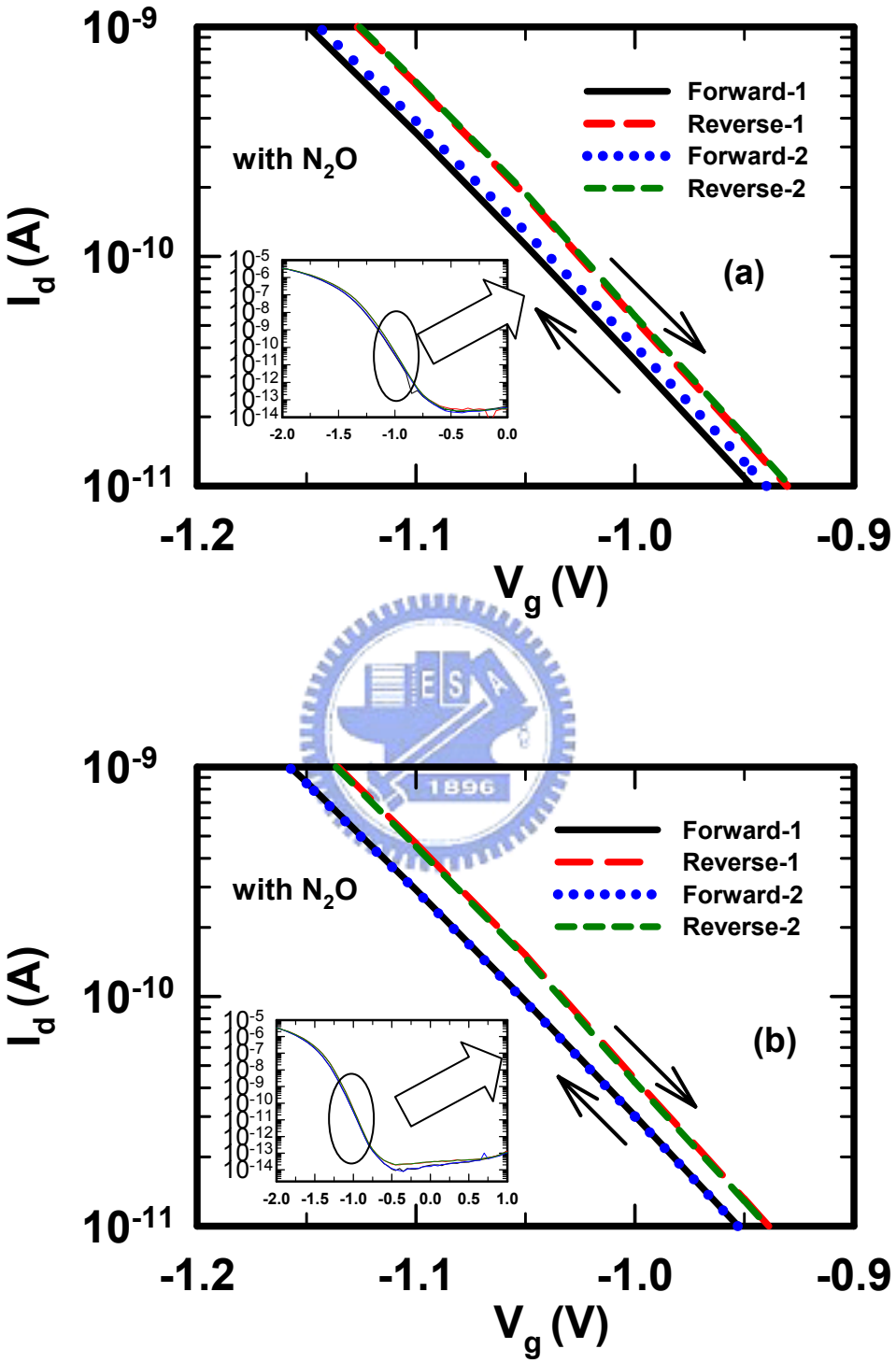


Fig. 5.3 Repetitive I_d-V_g traces for HfO_2/SiON high-k gate dielectric using measurement sequence (a) [V_g=0V↔−2V], (b) [V_g=1V↔−2V]. (with post-N_2O plasma treatment).

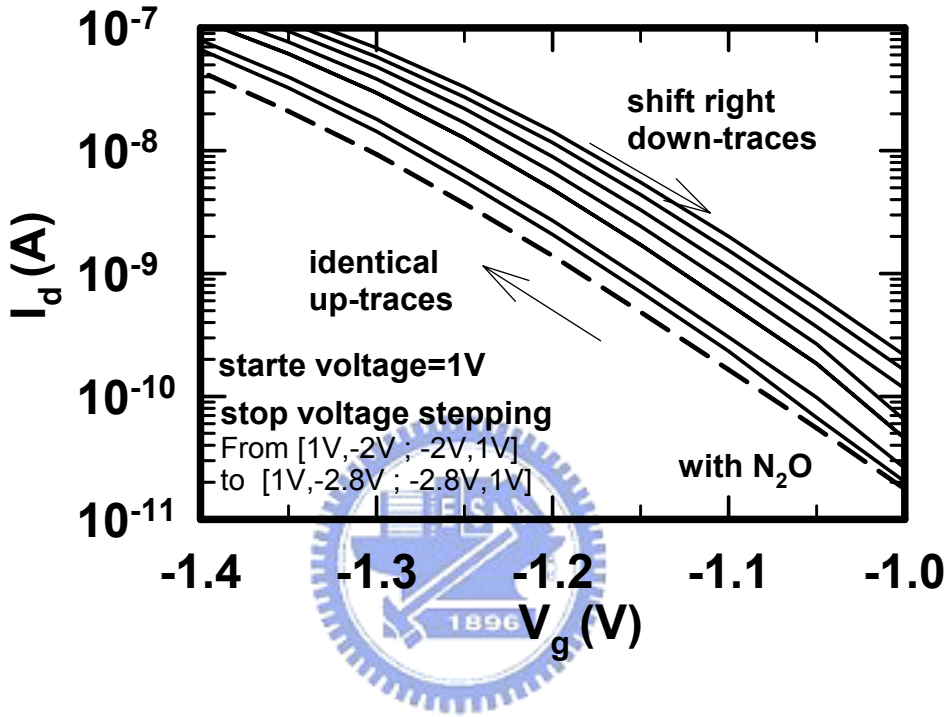


Fig. 5.4 Repetitive I_d-V_g traces for HfO_2/SiON high-k gate dielectric using measurement sequence of [V_g=1V ↔ –2V], [V_g=1V ↔ –2.2V], … , to [V_g=1V↔–2.8V] (with post-N_2O plasma treatment).

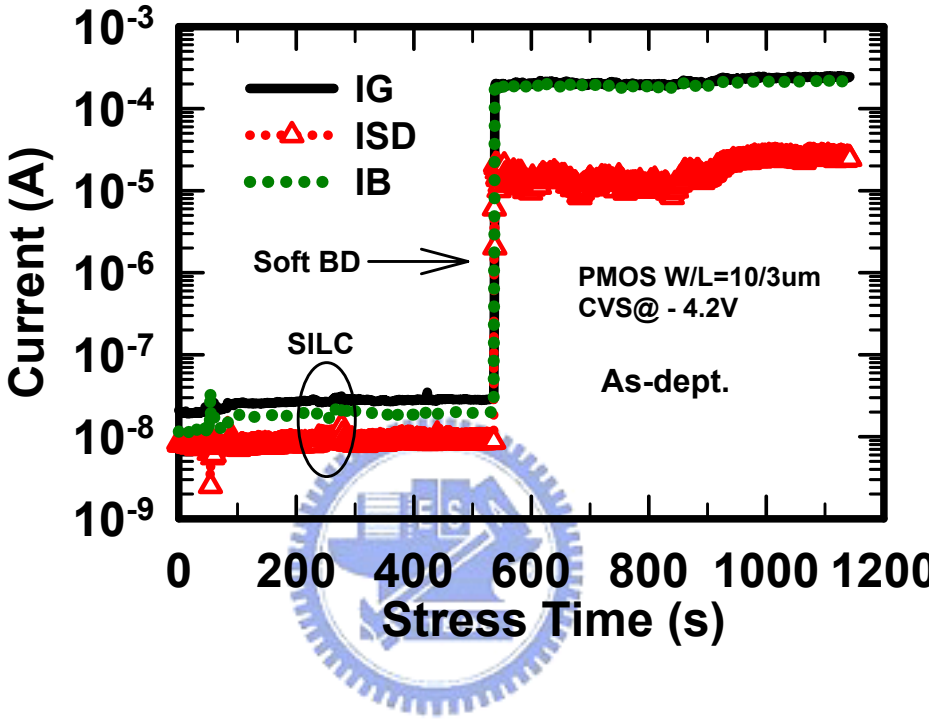


Fig. 5.5 Evolutions of three kinds of current, gate current (I_G), S/D current (I_{SD}), and the substrate current (I_B) under negative constant voltage stress of –4.2V (w/o post-N_2O plasma treatment).

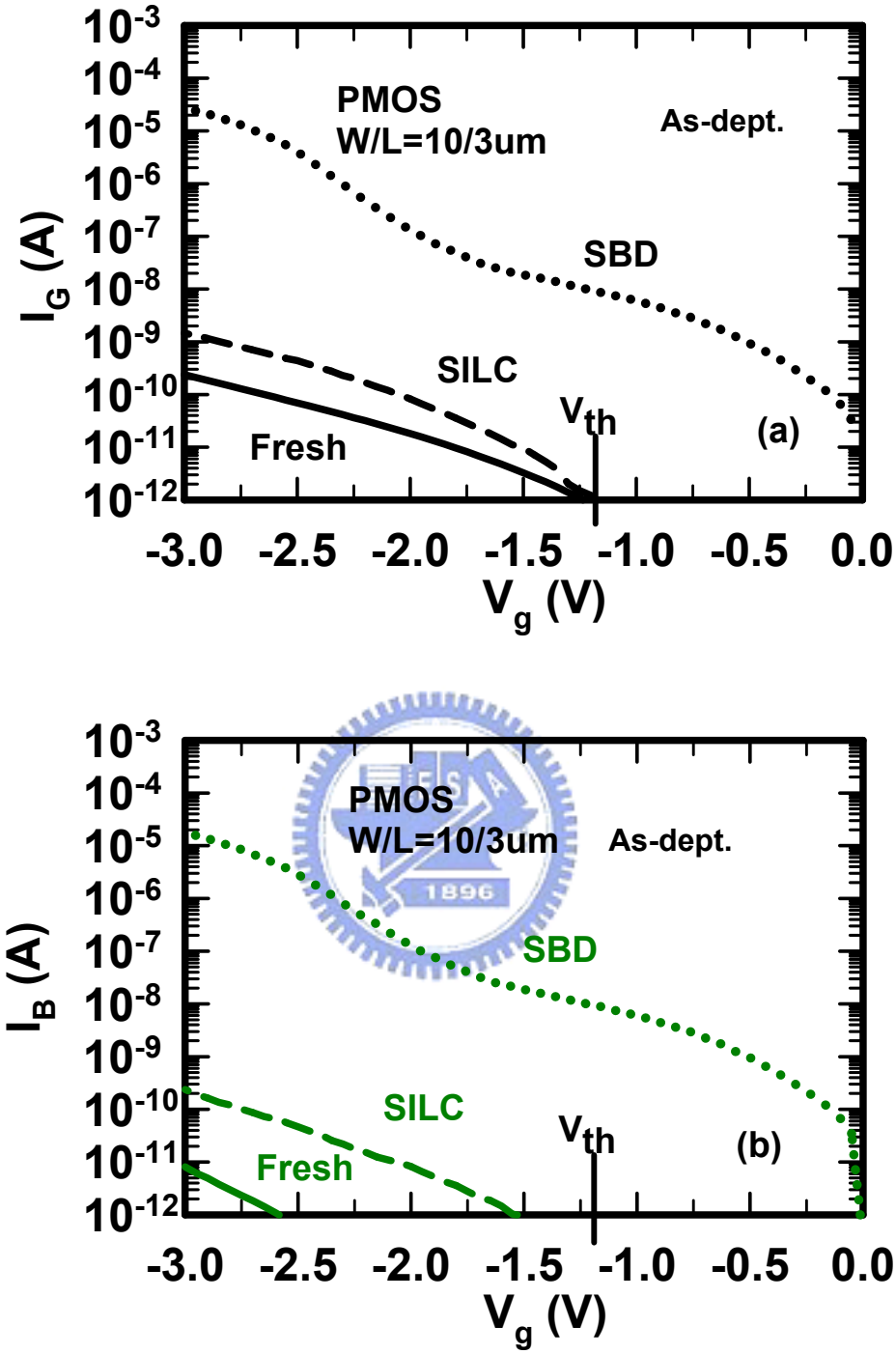


Fig. 5.6 Current of (a) I_G, (b) I_B, (c) I_{DS} versus gate voltage for Fresh, SILC, and SBD conditions (w/o post-N_2O plasma treatment).

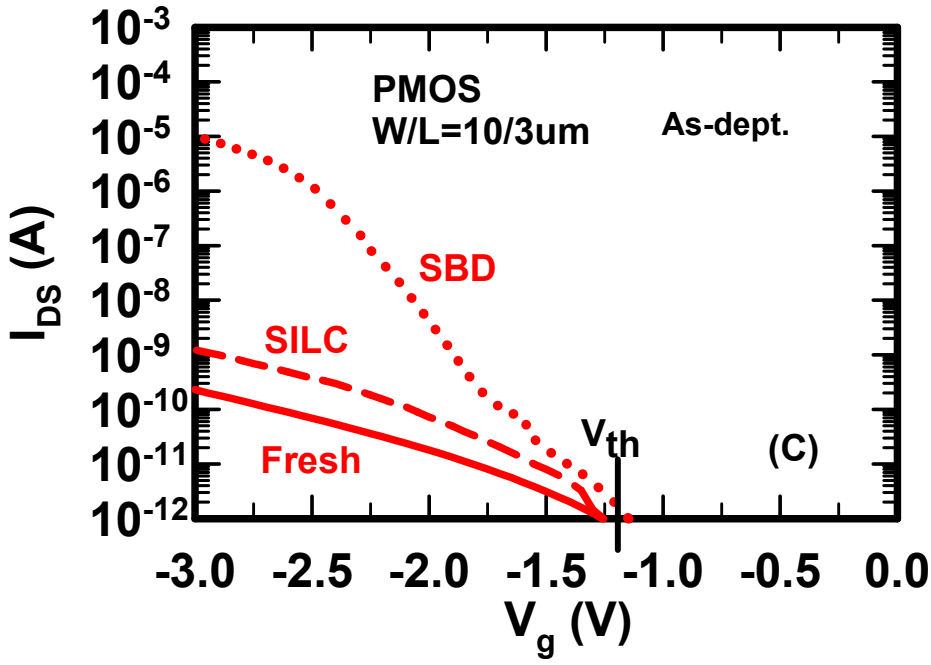


Fig. 5.6 Current of (a) I_G, (b) I_B, (c) I_{DS} versus gate voltage for Fresh, SILC, and SBD conditions (w/o post-N_2O plasma treatment).

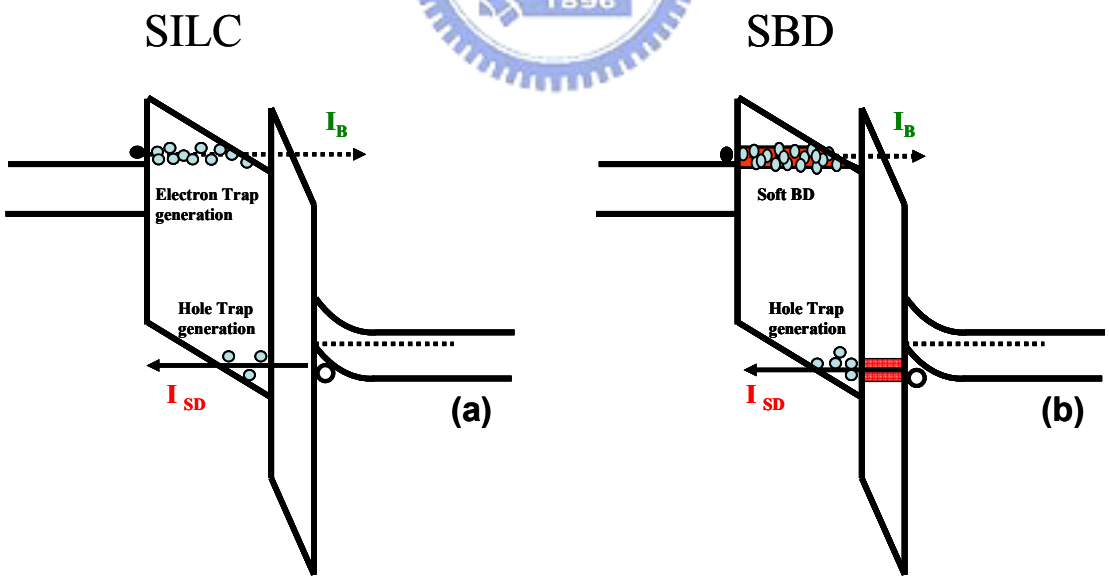


Fig. 5.7 Illustrations of damage situations under SILC (a), and after SBD (b) (w/o N_2O treatment).

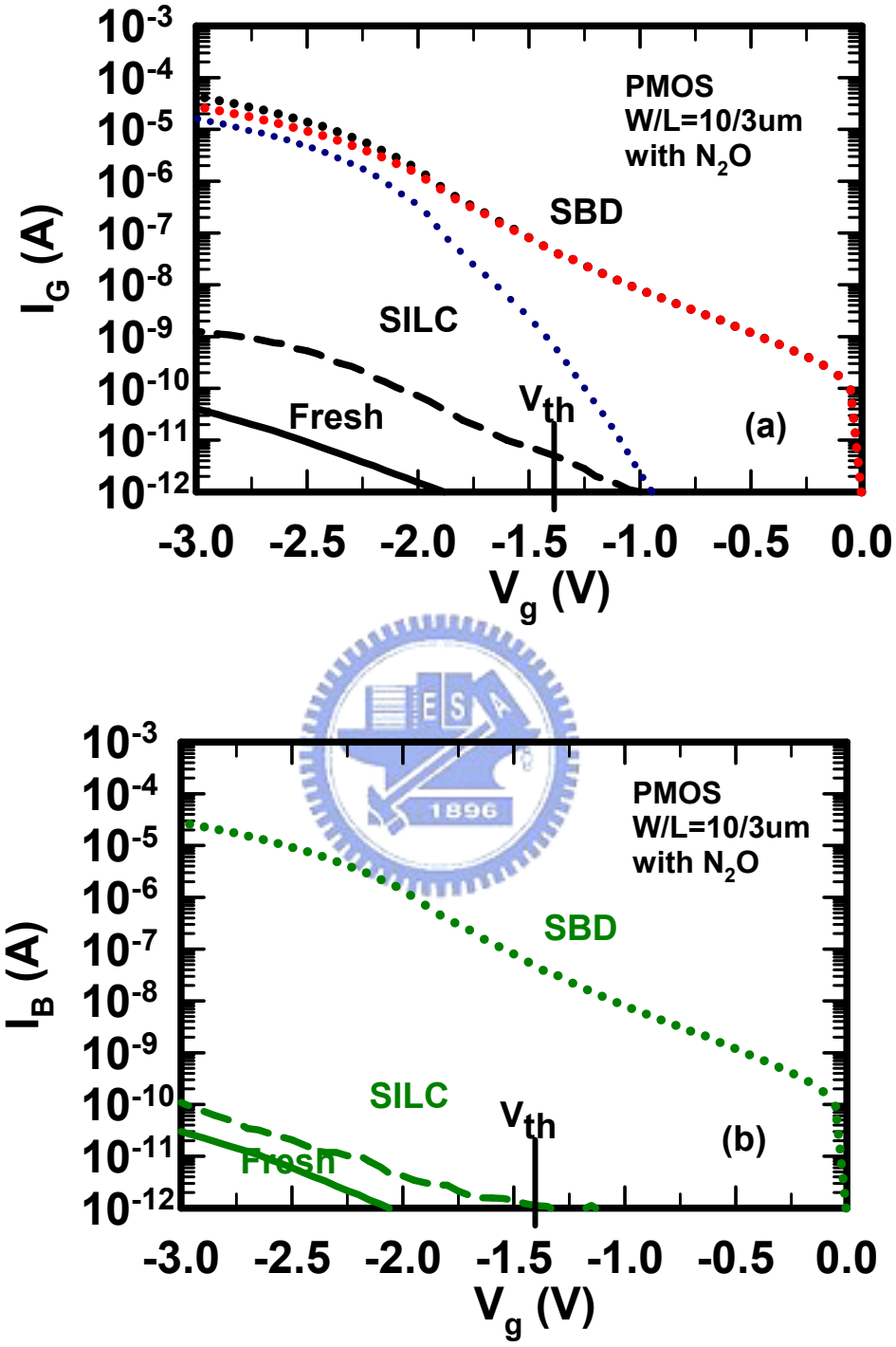


Fig. 5.8 Current of (a) I_G, (b) I_B, (c) I_{DS} versus gate voltage for Fresh, SILC, and SBD conditions (without post-N_2O plasma treatment).

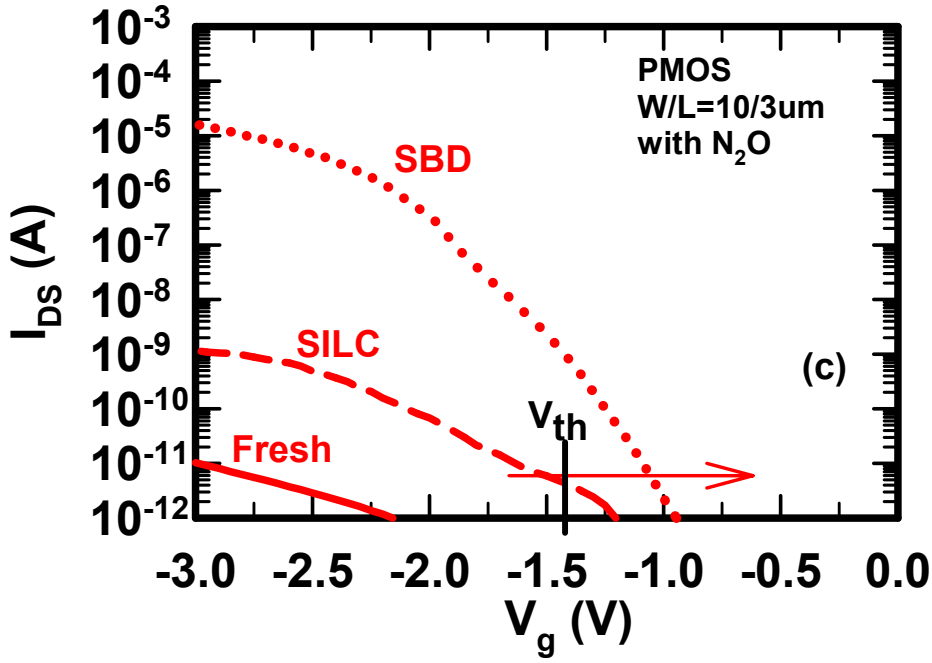


Fig. 5.8 Current of (a) I_G, (b) I_B, (c) I_{DS} versus gate voltage for Fresh, SILC, and SBD conditions (w/o post-N_2O plasma treatment).

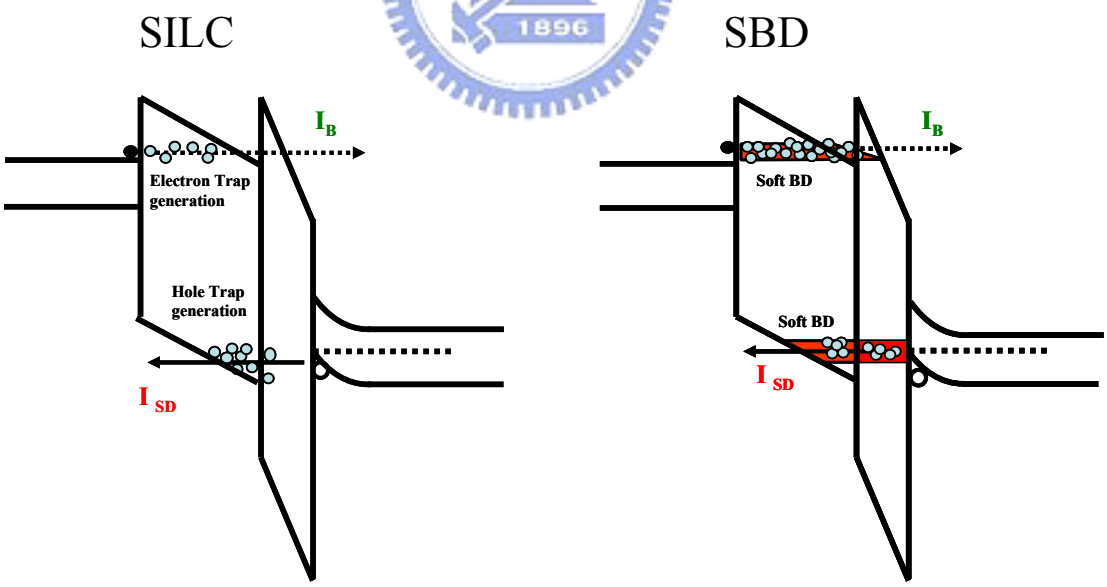


Fig. 5.9 Illustrations of damage situations under SILC (a) and after SBD (b) (without post-N_2O plasma treatment).

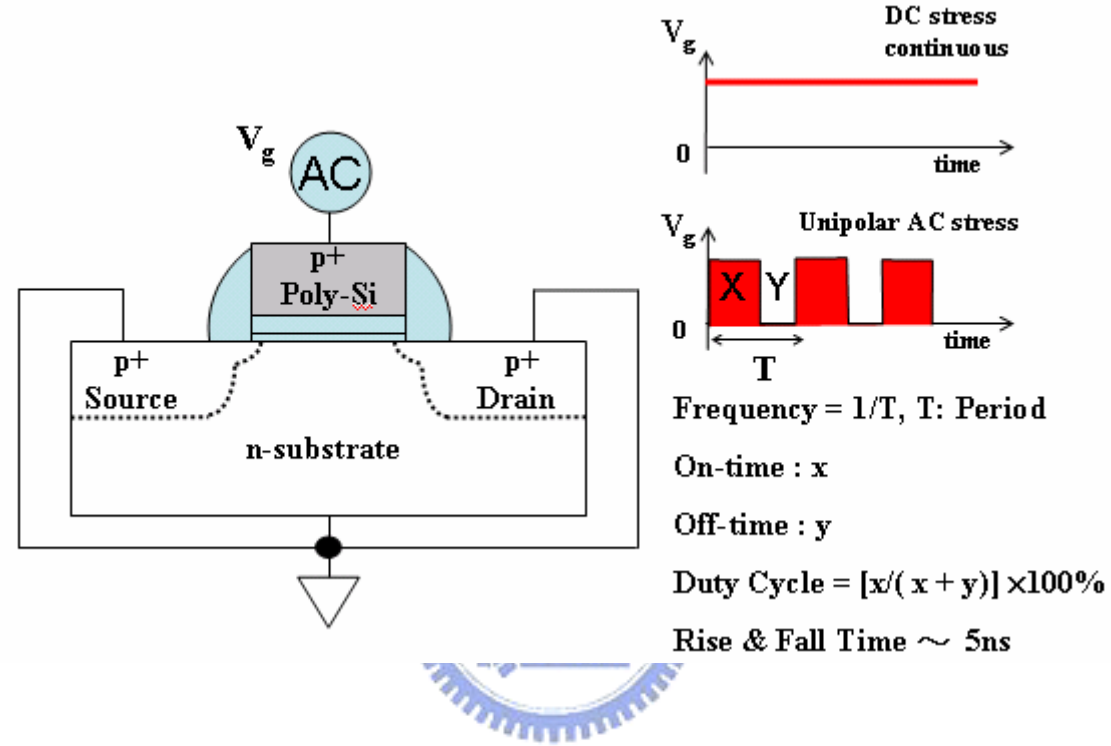


Fig. 5.10 Setup structure of AC stress with the definition of frequency, on-time, off-time, and duty cycle.

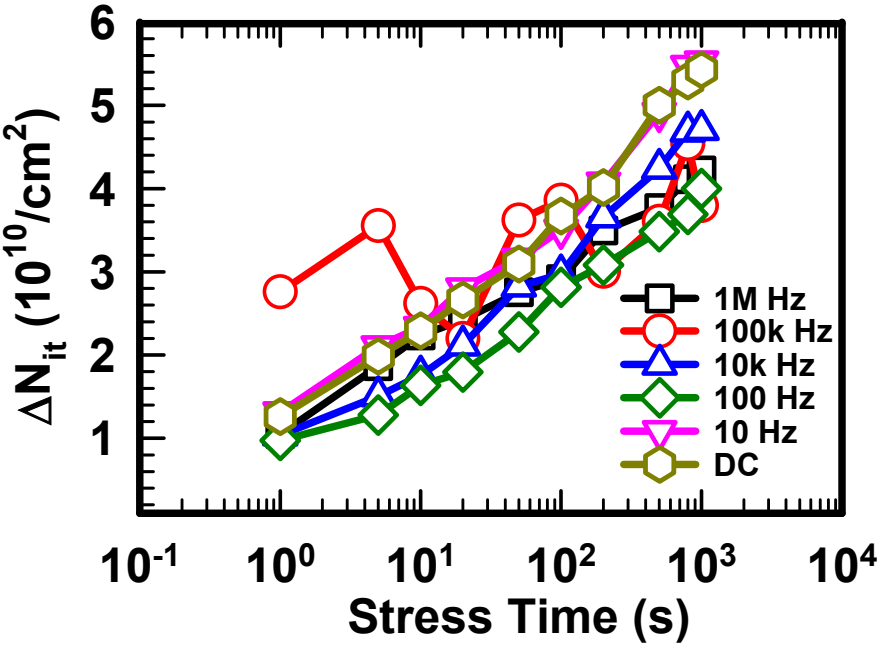


Fig. 5.11 Generated interface state densities as a function of stress time for various stress voltage frequencies. (V_{go}= −2.2V, duty cycle of 50%, w/o post N_2O plasma treatment).

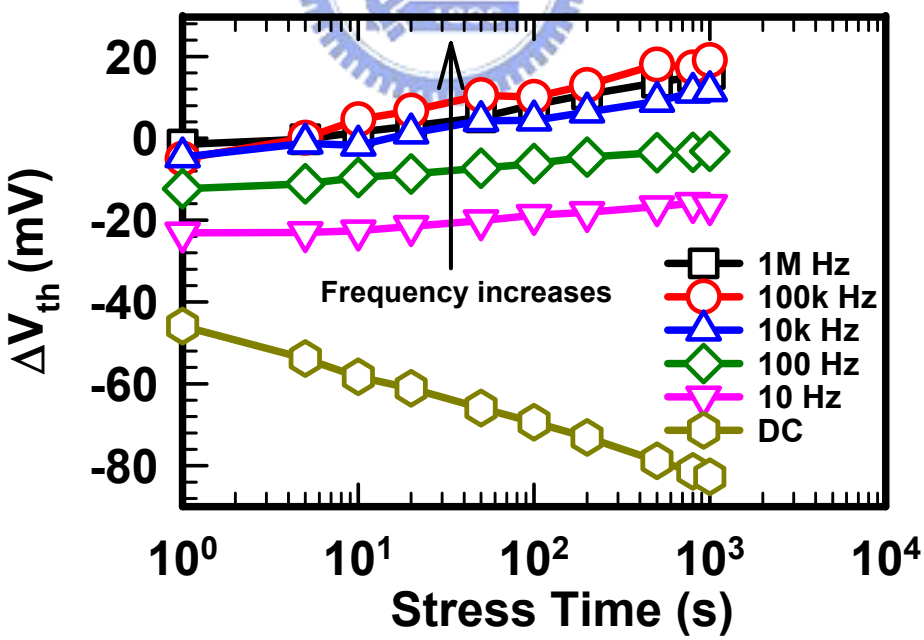


Fig. 5.12 Threshold voltage shift as a function of stress time for various stress voltage frequencies. (V_{go}= −2.2V, duty cycle of 50%, w/o post N_2O plasma treatment).

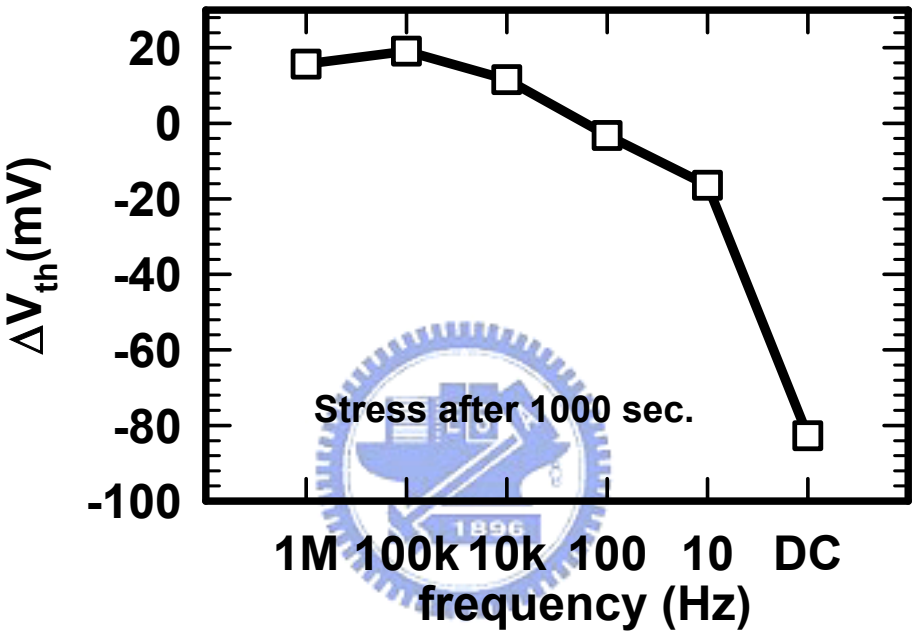


Fig. 5.13 Threshold voltage shift at stress time of 1000 seconds versus gate pulse frequency (w/o post N_2O plasma treatment).

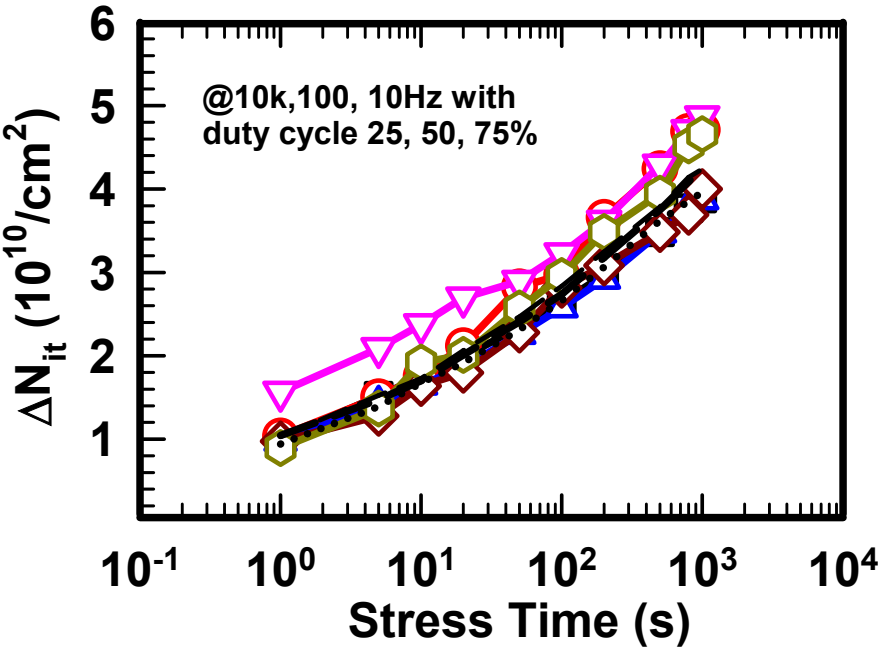


Fig. 5.14 Generated interface state densities as a function of stress time for various duty cycle of stress voltage. (V_{go}= –2.2V, w/o post- N_2O plasma treatment).

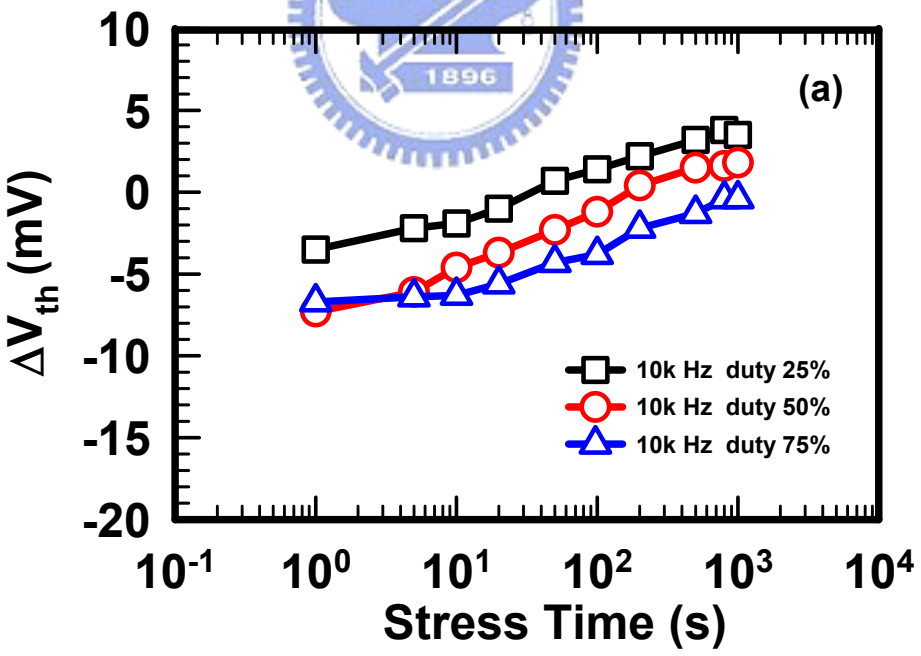


Fig. 5.15 Dependence of threshold voltage shift versus stress time for various stress voltage duty cycles. V_{go}= –2.2V at (a) 10k Hz (b) 100 Hz, and (c) 10 Hz. (w/o post-N_2O plasma treatment).

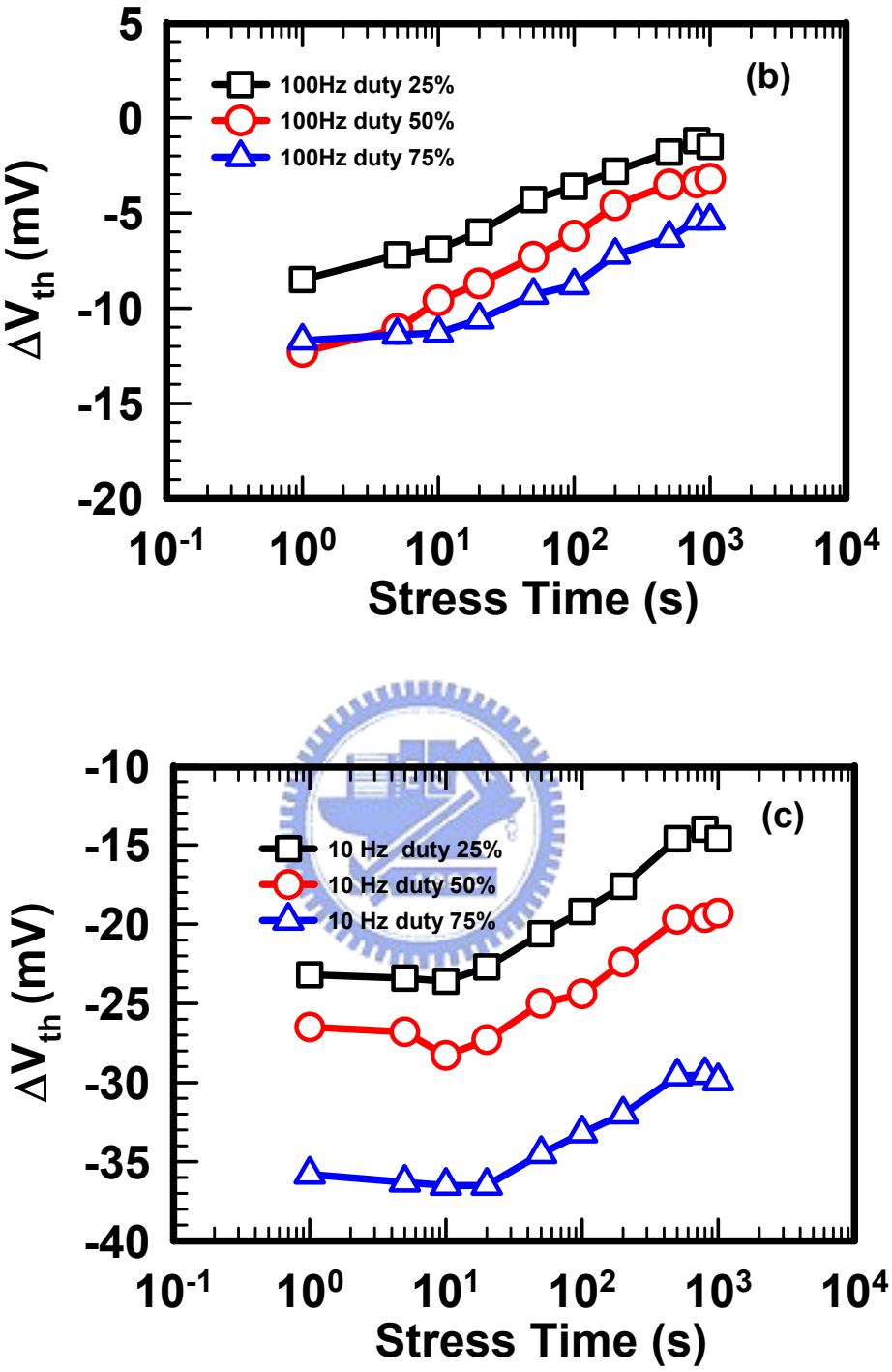


Fig. 5.15 Dependence of threshold voltage shift versus stress time for various stress voltage duty cycles. V_{go}= –2.2V at (a) 10k Hz (b) 100 Hz, and (c) 10 Hz. (w/o post-N_2O plasma treatment).

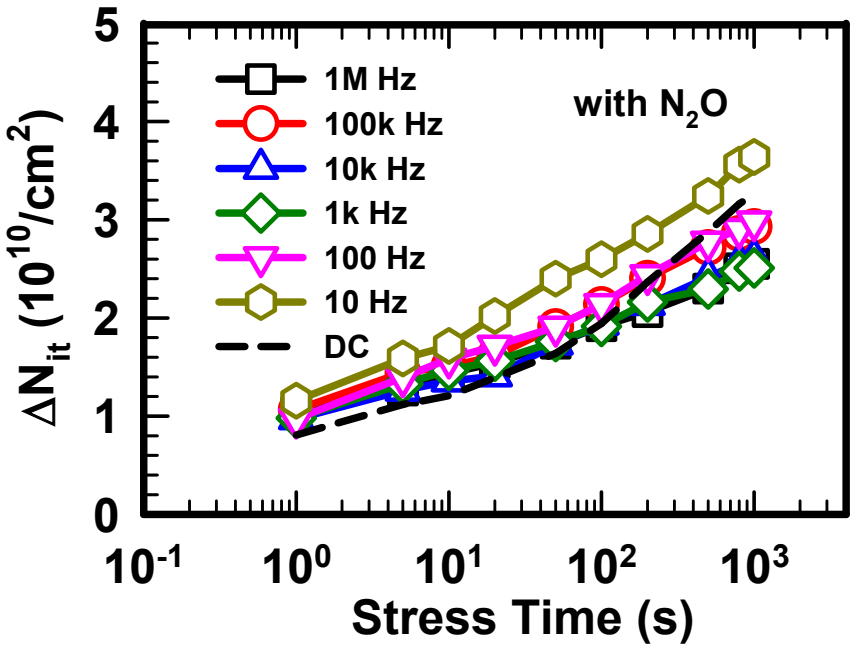


Fig. 5.16 Dependence of generated interface state densities versus stress time for various stress voltage frequencies. (V_{go}= –2.2V, duty cycle of 50%, with post N_2O plasma treatment).

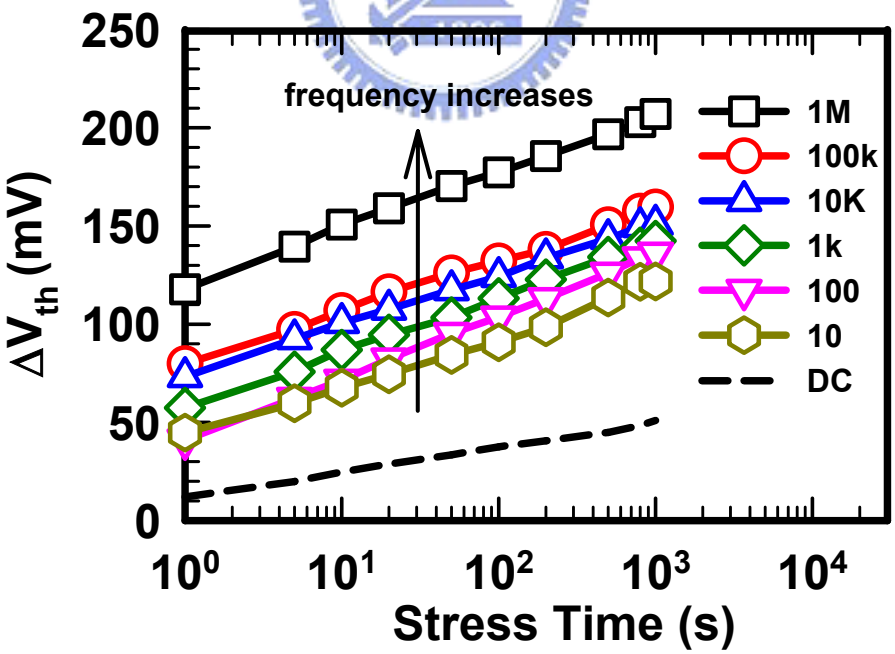


Fig. 5.17 Dependence of threshold voltage shift versus stress time for various stress voltage frequencies. (V_{go}= –2.2V, duty cycle of 50%, with post N_2O plasma treatment).

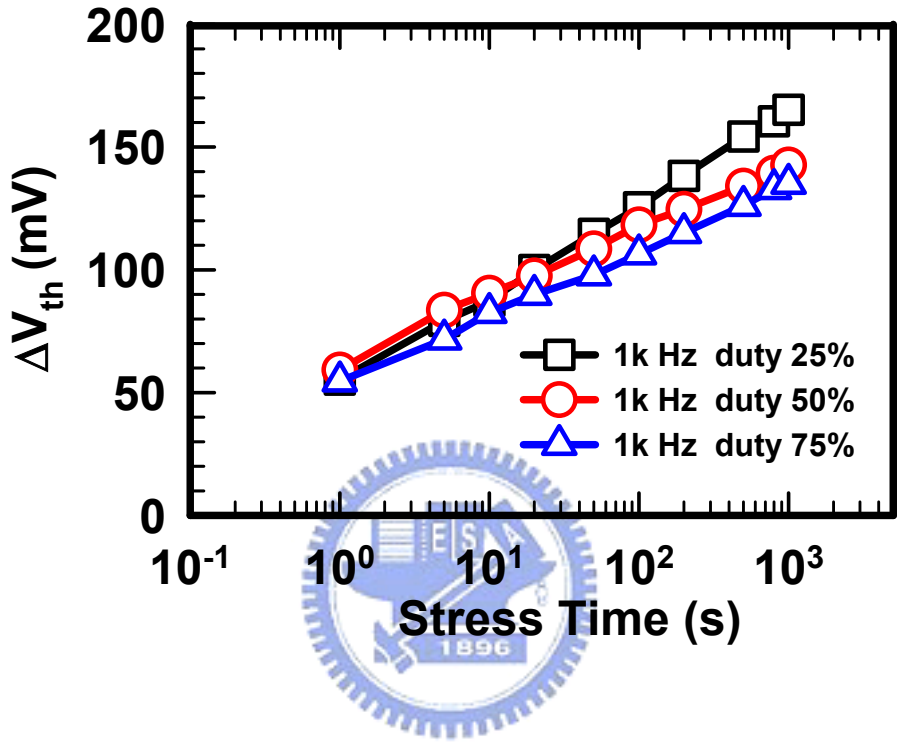


Fig. 5.18 Dependence of threshold voltage shift versus stress time for various stress voltage duty cycles. V_{go}=-2.2V at 1k Hz (w/ post-N_2O plasma treatment).

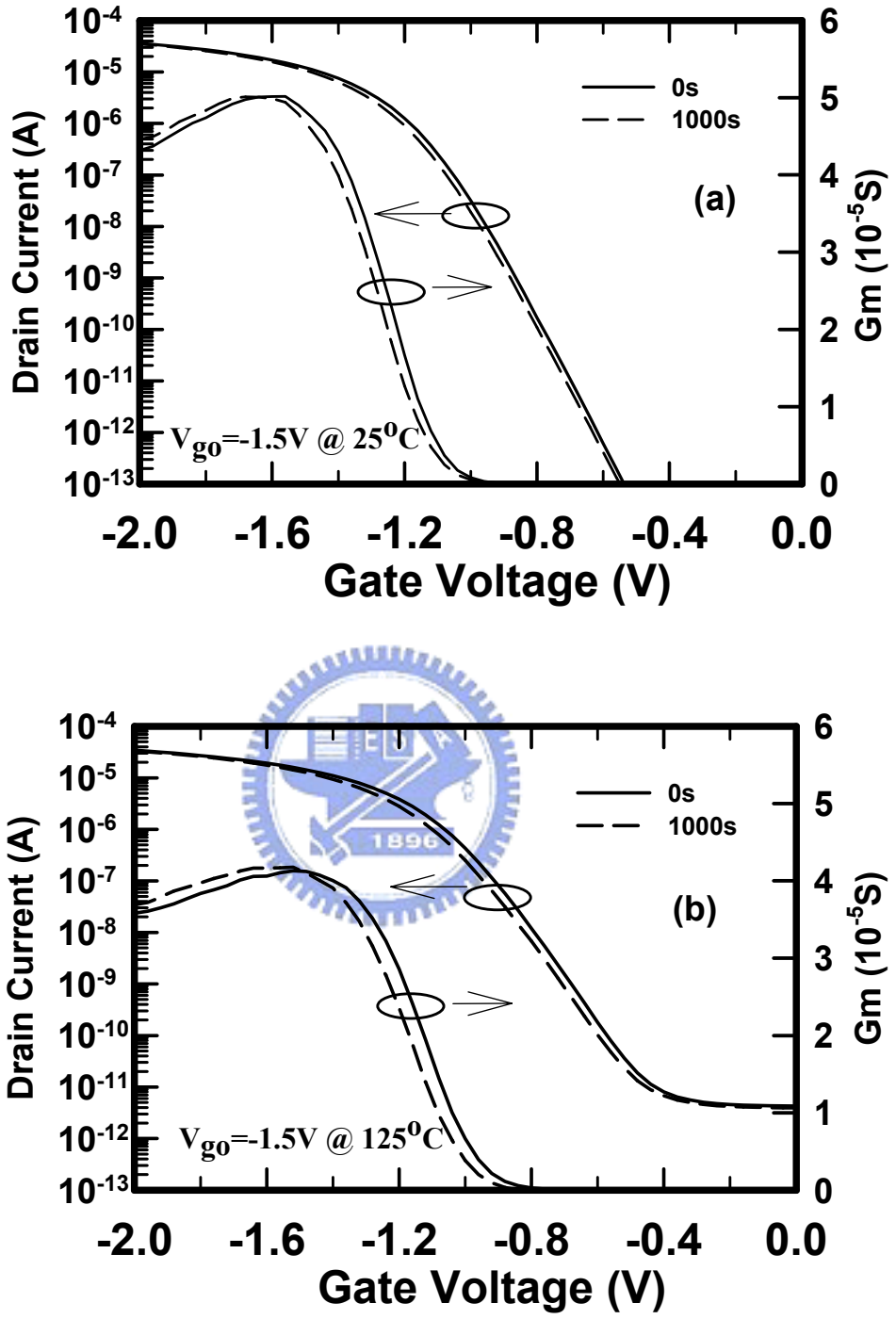


Fig. 5.19 I_d,G_m-V_g characteristics for p^+gated pMOSFETs before and after 1000 seconds stress for (a) room temperature, and (b) 125℃ (w/o post-N_2O plasma treatment).

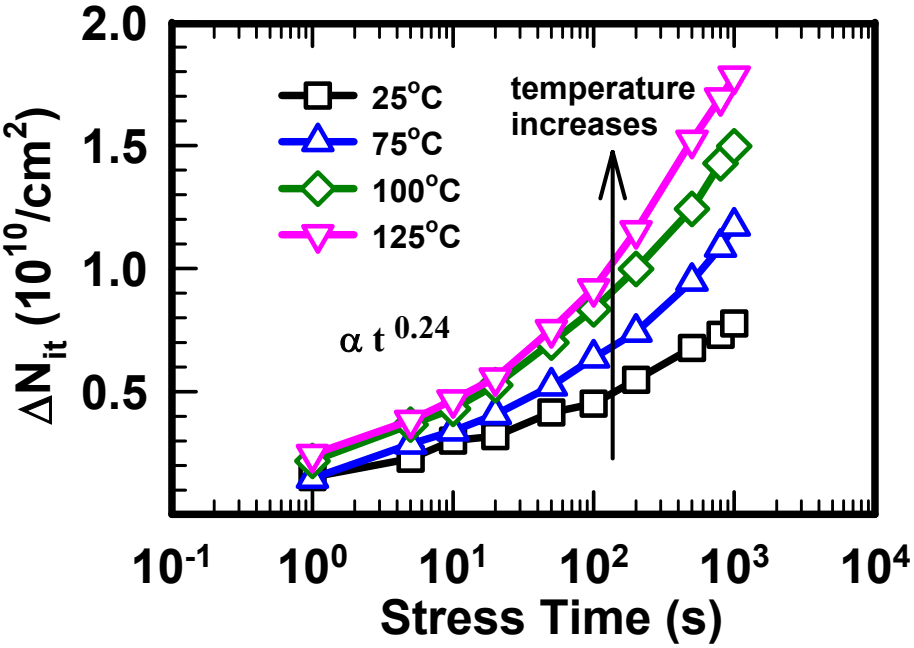


Fig. 5.20 Generated interface state densities as a function of stress time under BTS at various stress temperatures. V_{go}= –1.5V (w/o post-N_2O plasma treatment).

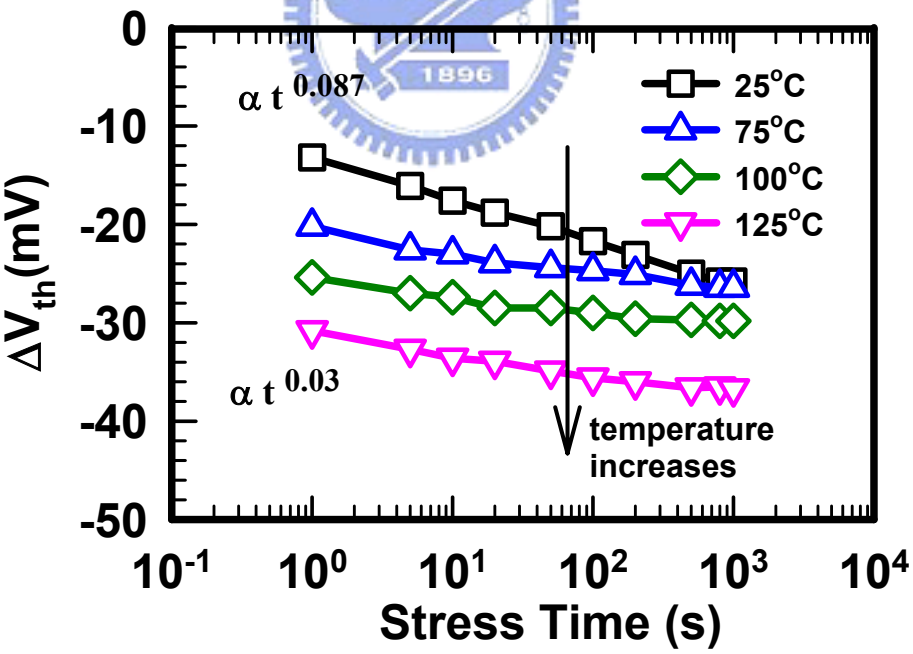


Fig. 5.21 Threshold voltage shift as a function of stress time under BTS at various stress temperatures. V_{go}= –1.5V (w/o post-N_2O plasma treatment).

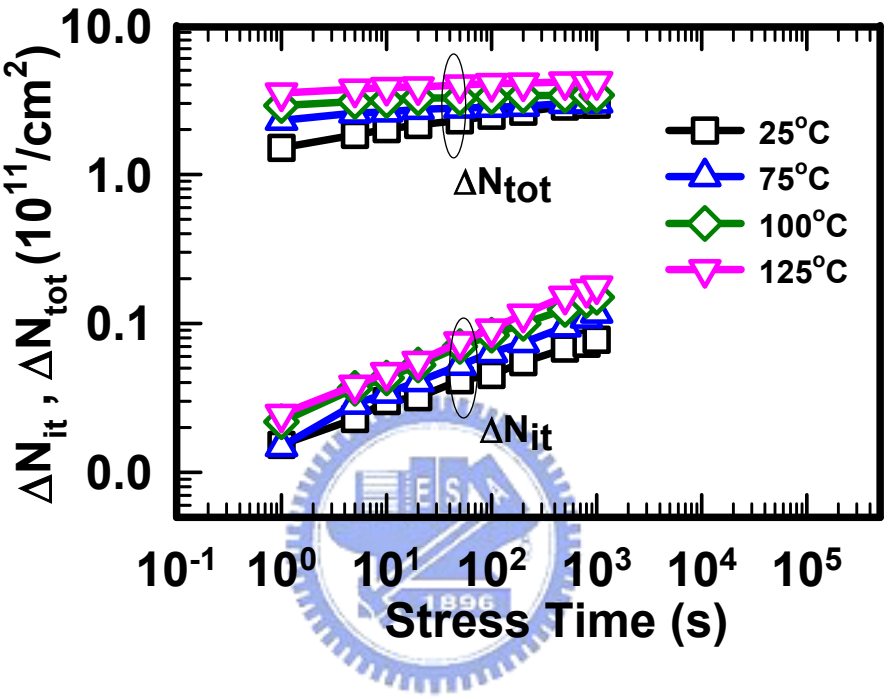


Fig. 5.22 Dependence of $\triangle N_{it}$ and $\triangle N_{tot}$ on stress time under V_{go}= –2V at various temperatures (w/o post-N_2O plasma treatment).

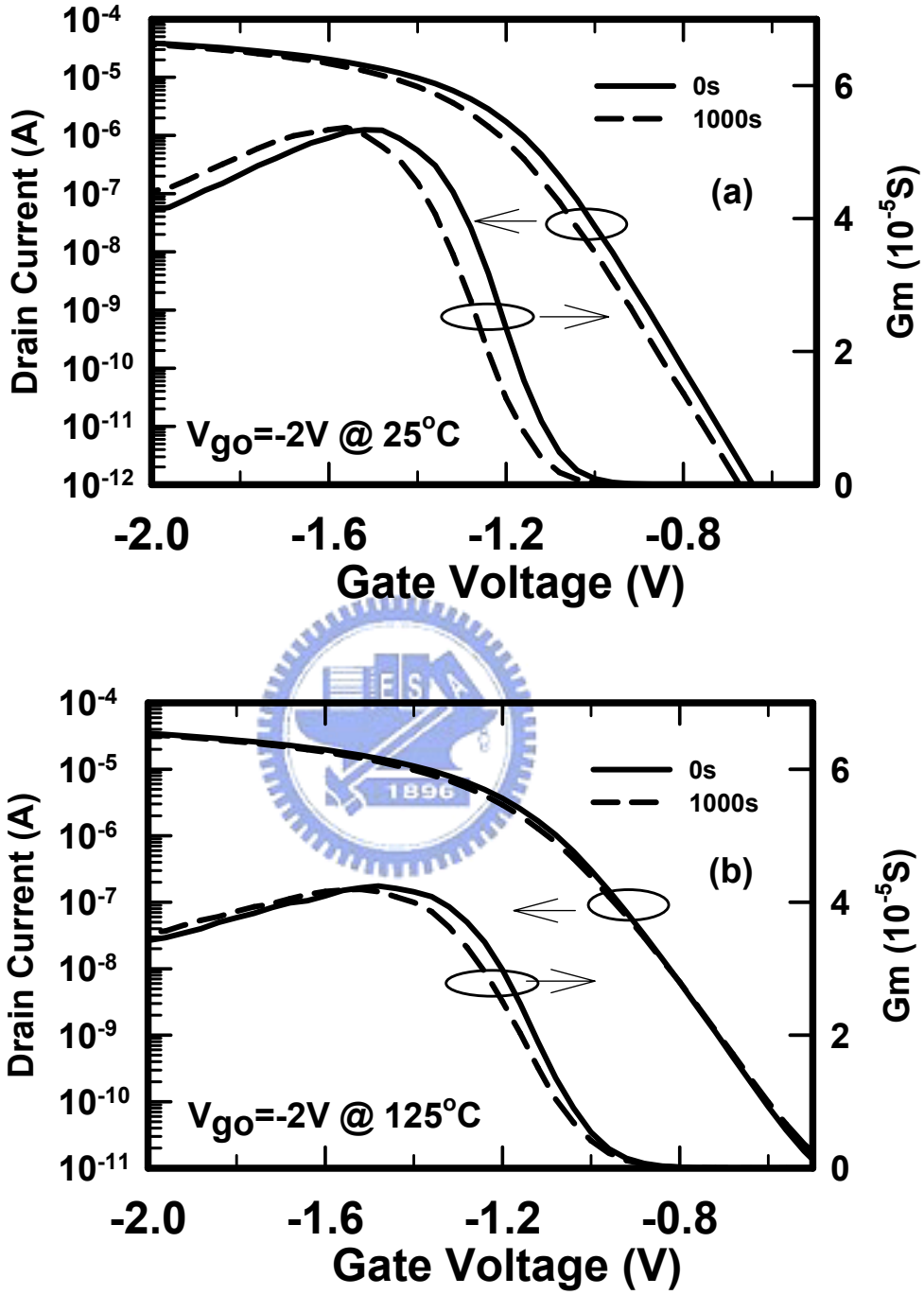


Fig. 5.23 I_d, G_m-V_g characteristics for p^+ gated pMOSFETs before and after 1000 seconds for (a) room temperature, and (b) 125℃ (w/o post-N_2O plasma treatment).

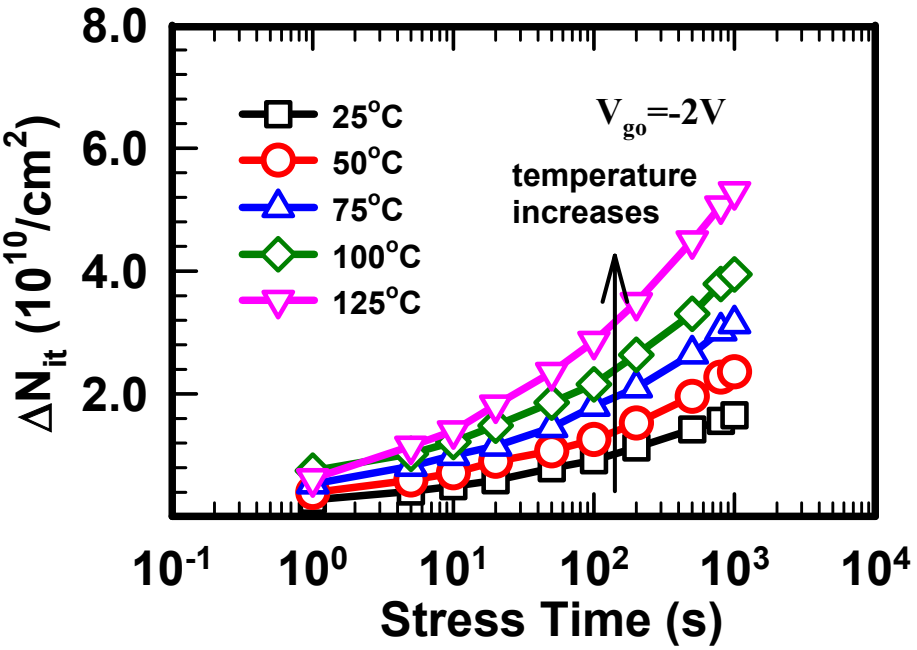


Fig. 5.24 Generated interface state densities as a function of stress time under BTS at various stress temperatures. V_{go}= –2V (w/o post-N_2O plasma treatment).

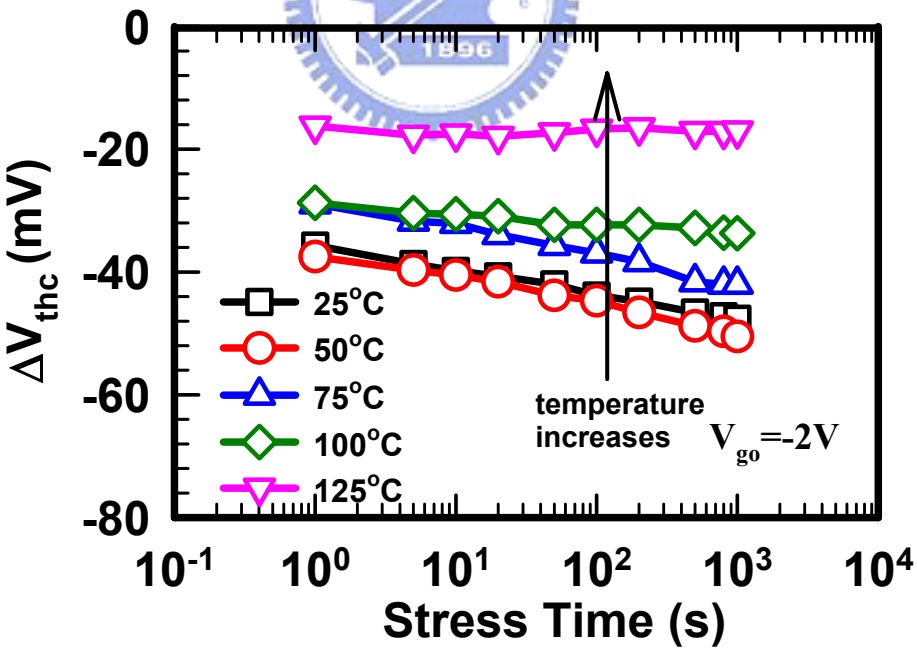


Fig. 5.25 Threshold voltage shift as a function of stress time under BTS at various stress temperatures. V_{go}= –2V (w/o post-N_2O plasma treatment).

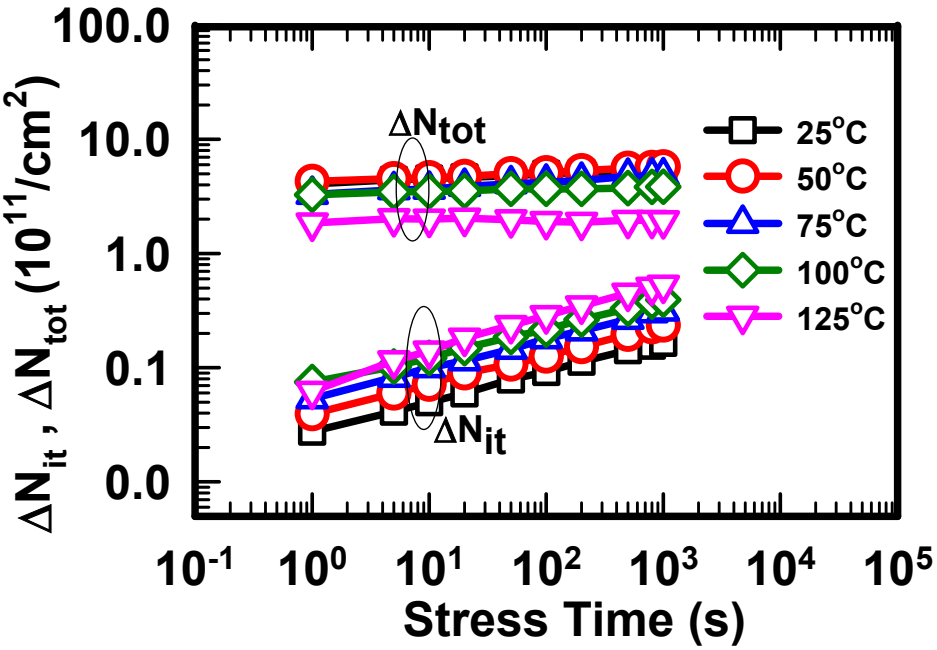


Fig. 5.26 Dependence of $\triangle N_{it}$ and $\triangle N_{tot}$ on stress time under V_{go}= –2V at various temperatures (w/o post-N_2O plasma treatment).

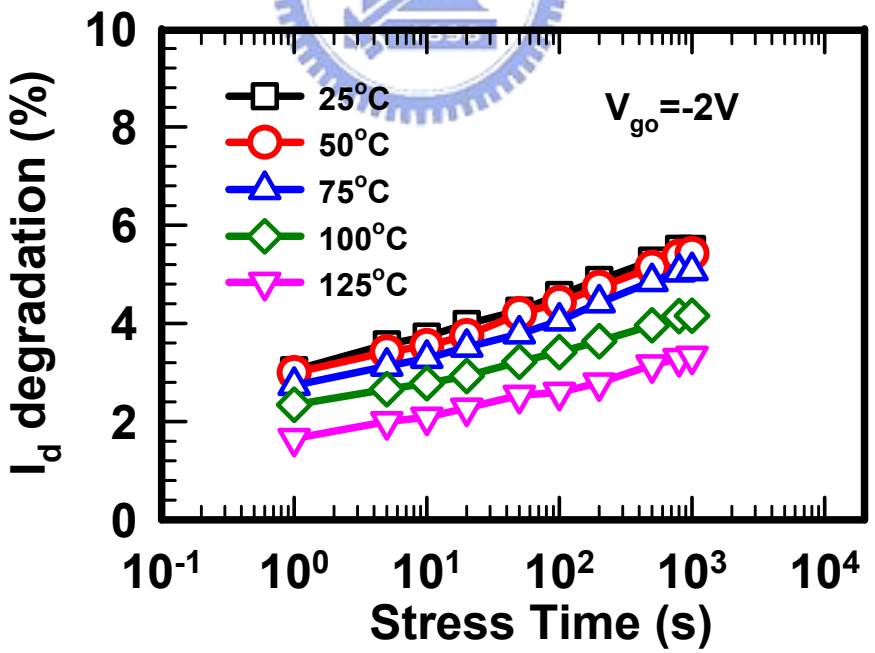


Fig. 5.27 Dependence of I_d degradation on stress time under V_{go}= –2V at various temperatures (w/o post-N_2O plasma treatment).

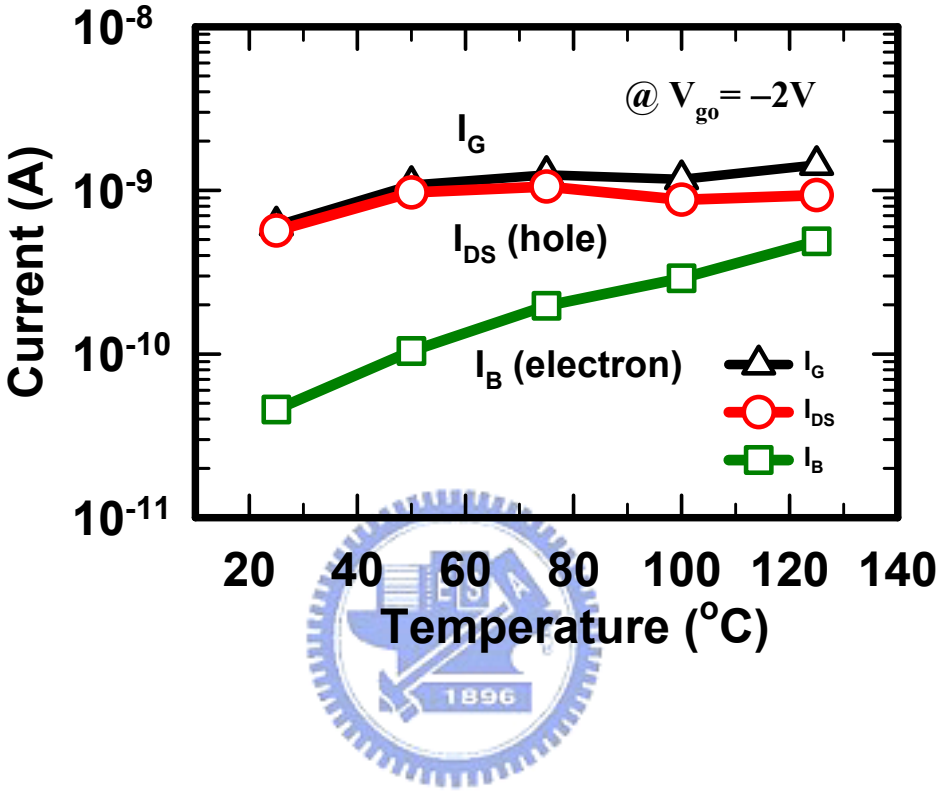


Fig. 5.28 Gate, source/drain, substrate currents for fresh pMOSFETs at various temperatures. V_{go}= –2V (w/o post-N_2O plasma treatment).

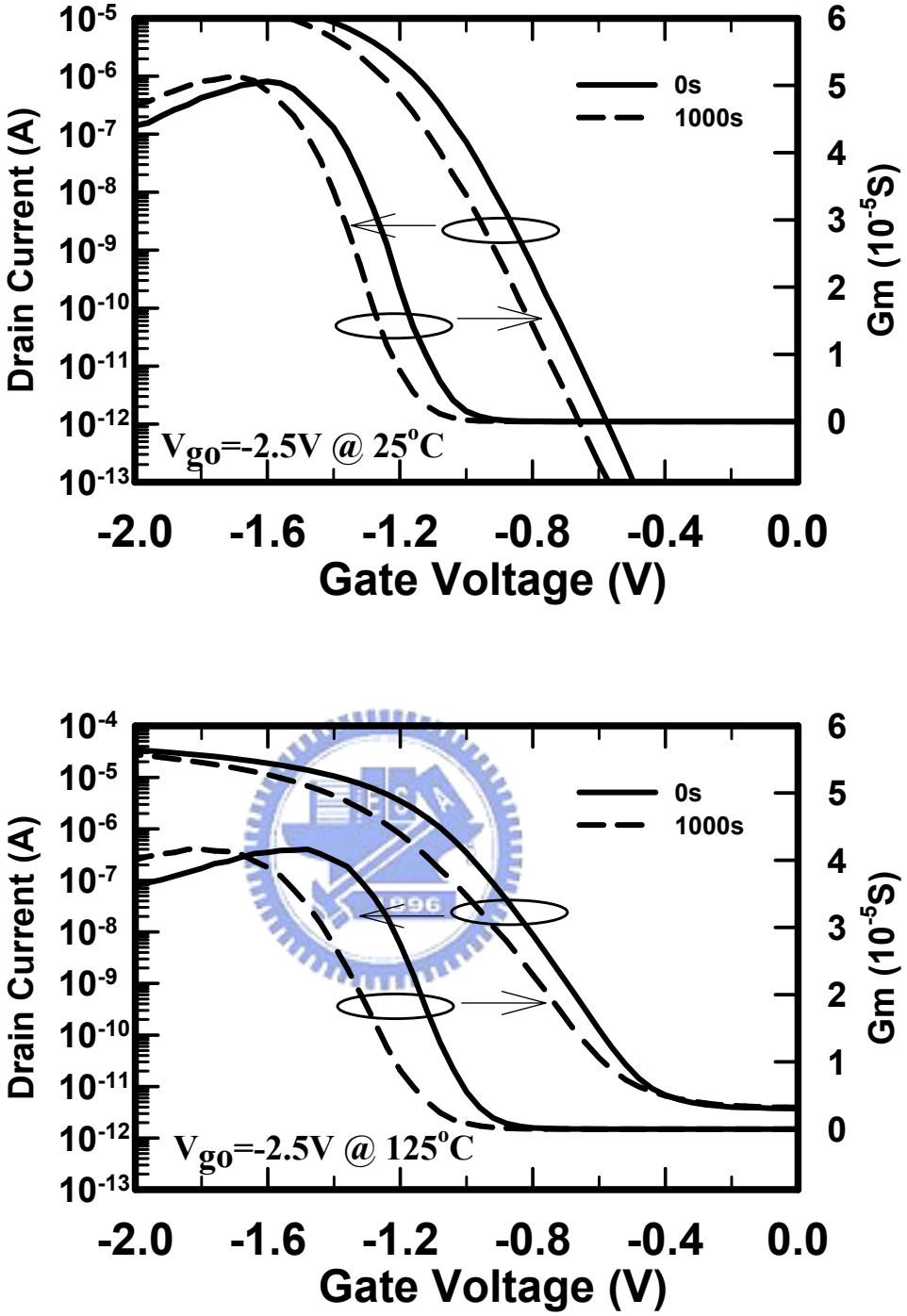


Fig. 5.29 I_d, G_m-V_g characteristics for p^+ gated pMOSFETs before and after 1000 seconds for (a) room temperature, and (b) 125℃. (w/o post-N_2O plasma treatment).

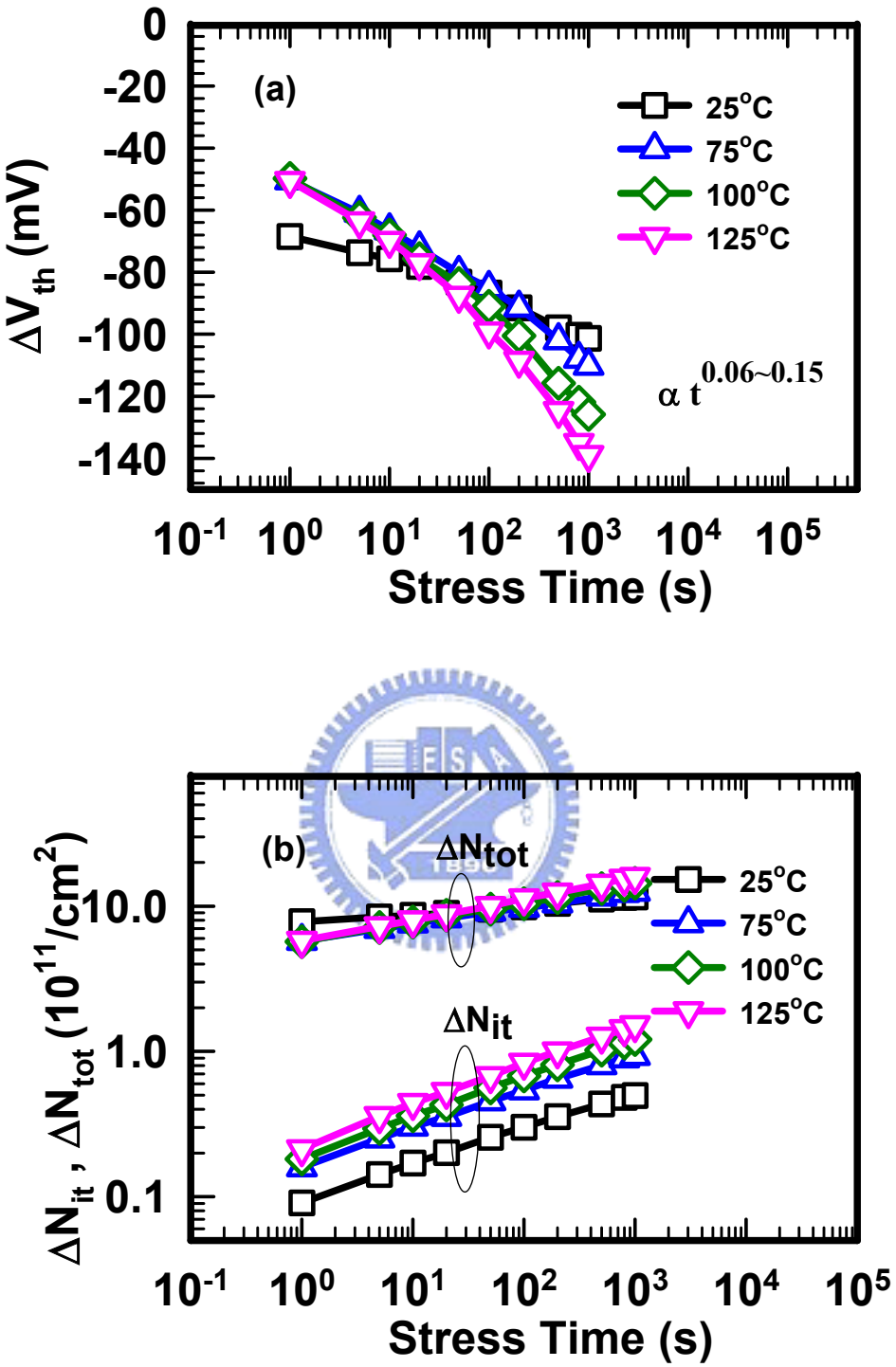


Fig. 5.30 (a)Threshold voltage shift (b)$\triangle N_{it}$ and $\triangle N_{tot}$ as a function of stress time under BTS (V_{go}= –2.5V) at various stress temperatures. (w/o post-N_2O plasma treatment).

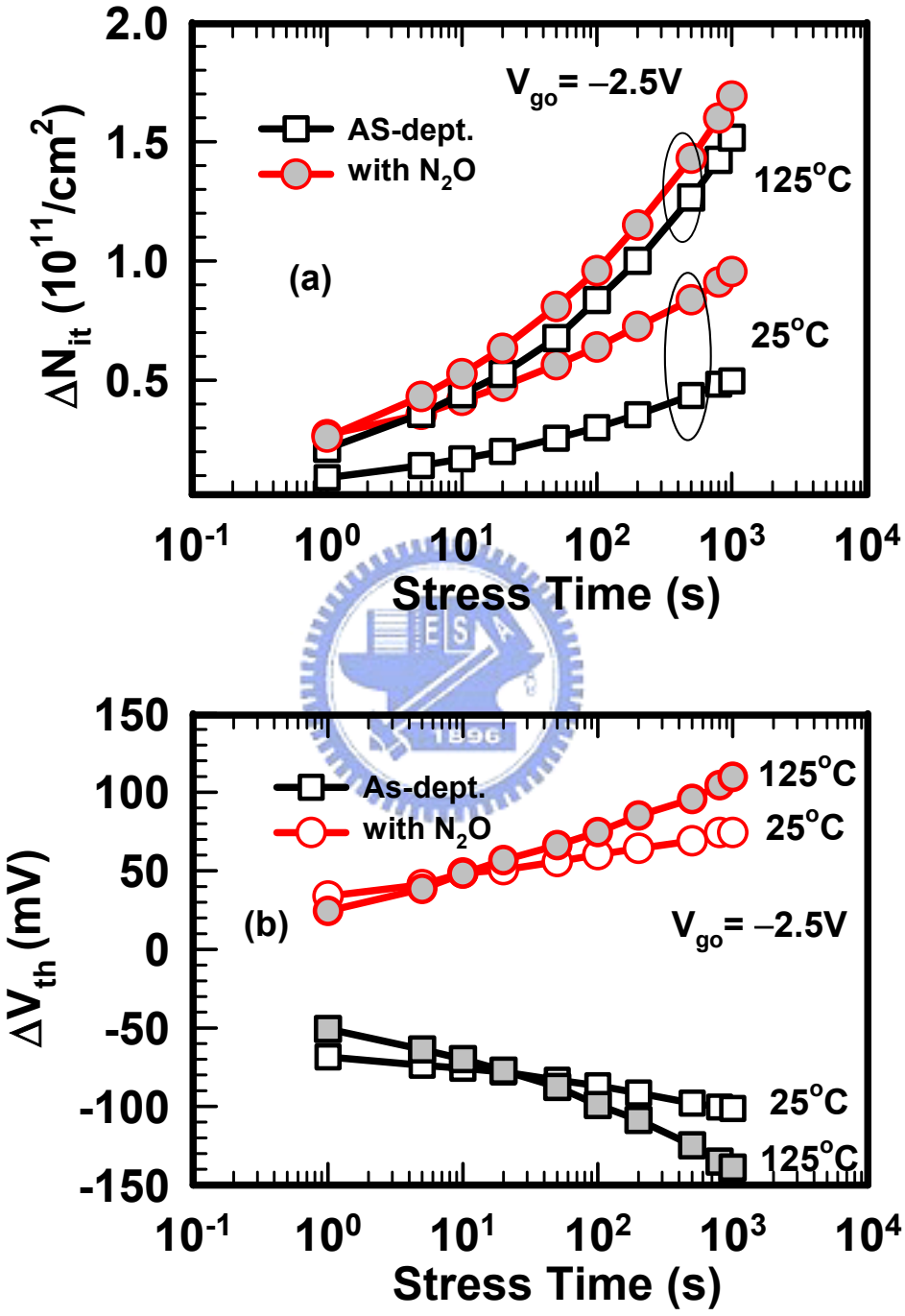


Fig. 5.31 (a)Interface trap shift and (b) Threshold voltage shift as a function of stress time under BTS at various stress temperatures. (V_{go}= –2.5V).

Chapter 6

Effects of Fluorine Incorporation on the Electrical Characteristics of pMOSFETs with HfO_2/SiON Gate Stack

6.1 Background and Motivation

HfO_2 has emerged as the leading high-k candidate due to its relatively high dielectric constants (~25), wide band gap, suitable tunneling barrier heights for both electrons and holes (>1 eV), and good thermal stability when placed in direct contact with silicon or polysilicon. Notwithstanding, there are still a number of pending issues, including channel mobility degradation, large number of fixed charges and charge traps, and threshold voltage instability [1-4]. There are numerous literature reports regarding methods to incorporate nitrogen [5-6] or Si [7-8] into Hf-based films or stacks to improve the film's quality. However, to the best of our knowledge, there are no related reports on the influence of F incorporation on HfO_2 gate dielectric. In this work, fluorine incorporated into HfO_2 gate stack by fluorine implantation into the source/drain regions was used to evaluate the impact of F on the constant voltage stress instability and negative bias stress instability (NBTI) of pMOSFETs. It was clearly seen that the degradation is improved in the F-incorporated samples. Moreover, since few studies [9] have been done on the area plasma charging effects of HfO_2 gate

stacks, we have performed a systematic study, and found that higher area antenna ratio will result in more severe degradation. More importantly, our data also show that the phenomenon can be significantly improved by the F incorporation into the HfO_2 gate stacks.

6.2. Experimental

PMOSFETs with HfO_2/SiON gate stacks were fabricated in this work. Briefly, after conventional LOCOS isolation, standard RCA cleaning with a final HF-dip was performed on all wafers, followed by the growth of a 0.6nm thin interfacial oxyntride layer (SiON) using rapid thermal processing in an N_2O ambient at 700°C. Subsequently, a 3nm HfO_2 layer was deposited by atomic vapor deposition (AVD) using an AIXTRON Tricent® system at a substrate temperature of 500°C. All samples were then annealed in an N_2 ambient at 700°C for 20s to improve the film quality. A 200nm polycrystalline silicon (poly-Si) layer was next deposited by low pressure chemical vapor deposition (LPCVD). Then the gate electrode patterning was implemented through lithographic and etching processes. Subsequently, some samples received a fluorine (F, 2×10^{15} cm^{-2}) ion implantation into source/drain region without removing the photoresist on the gate electrode. This was deliberately done in order to avoid the complication of enhanced boron penetration by F. After photoresist removal, source/drains were formed by implantation, with the dopants activated at 950°C by rapid thermal annealing (RTA) for 20s in an N_2 atmosphere. It should be noted that the activation thermal budget also served to diffuse the F species into the gate stacks. After passivation, contact holes formation, Al metallization and patterning, the forming gas annealing at 400°C was finally performed for 30minutes to complete the device fabrication.

Current-Voltage (*I-V*) and capacitance–voltage (*C–V*) characteristics were evaluated using an HP4156A precision semiconductor parameter analyzer and an HP4284 LCR meter, respectively. The equivalent oxide thickness (EOT) of the gate dielectrics was extracted from high-frequency (100 kHz) capacitance-voltage (*C-V*) curves at strong inversion (EOT = $\varepsilon_{SiO_2}/C_{inv}$) without considering the quantum effect. Charge pumping current was measured with fixed amplitude method at a frequency of 1Mhz [10].

The interface trap density (N_{it}) was analyzed using the charging pumping technique [10]. We used square waves (f = 1MHz) as gate voltage waveform, varying the base voltage from inversion to accumulation, and keeping pulse amplitude at 1.2 V. A MOSFET with gate area A_G gives the charge pumping current as:

$$I_{cp} = qA_G f N_{it,} \qquad (6\text{-}1)$$

Interface trap density could be evaluated by this equation.

The increase of total trap density, $\triangle N_{tot}$, which includes both the interface trap density increase and the bulk trap density increase, was calculated from $\triangle V_{th}$ by assuming that the charge was trapped at the interface between the dielectric and the substrate.

$$\triangle N_{tot} = C\triangle V_{th}/qA_G \qquad (6\text{-}2)$$

6. 3. Results and Discussions

6. 3. 1 Basic Electrical Properties of Devices

Fig. 6.1 shows *C-V* curves of pMOSFETs with HfO_2/SiON gate stack, both with and without F incorporation. It can be seen that the values of EOT measured from strong inversion region for samples with and without F incorporation are similar to each other. **Fig. 6.2** (a) shows typical I_d-V_g curves and transconductance

characteristics of pMOSFETs with HfO_2/SiON gate stack, both with and without F incorporation. The two samples show almost the same values of initial threshold voltage and transconductance. **Fig. 6.2** (b) illustrates the cumulative probability of the threshold voltage (V_{th}) for the fabricated devices. It can be found that the distribution of V_{th} is not influenced by the addition of F into HfO_2/SiON gate stack. Typical I_d-V_d characteristics of the p-MOSFETs with and without F incorporation as a function of gate overdrive are displayed in **Fig. 6.3**. **Fig. 6.4** illustrates the initial interface state density and subthreshold swing (S.S) of two samples. We can find that output characteristics and initial interface state density are almost identical between two samples with and without F incorporation. **Fig. 6.5** compares the gate leakage currents of the pMOSFETs with HfO_2/SiON gate stack under both inversion and accumulation modes. The fluorine incorporation into HfO_2/SiON gate stack does not degrade the gate leakage. From these results, we conclude that all fundamental electrical properties of as-fabricated devices, including the values of EOT, V_{th}, driving current, interface state density (N_{it}), swing, and gate leakage current are almost non-distinguishable between the two samples with and without F incorporation. This indicates that F incorporation into HfO_2/SiON gate stack exhibits little or no adverse impact on dielectric integrity.

The carrier conduction mechanisms of the gate leakage current through HfO_2/SiON dielectric layers have been investigated for unstressed pMOSFETs, using carrier separation method [11], in which the p+ polysilicon gate can be biased negatively or positively, while the source/drain and n-Si substrate were grounded. The current measured at the source/drain terminals was denoted as I_{SD}, while the other currents measured at the gate and substrate terminals were referred to as I_G and I_B, respectively. The carrier of the gate leakage current can be separated into hole and

electron by using this method. **Fig. 6.6** shows measured results in the inversion region and **Fig. 6.7** demonstrates the measured results in the accumulation region for the p^+-gated pMOSFETs with HfO_2/SiON gate stack, both with and without F-incorporation. It is found that the source/drain current I_{SD} is almost identical to the gate leakage current (I_G) under inversion region, while the substrate current I_B is almost identical to the gate leakage current (I_G) under accumulation region. This indicates that inversion carriers, holes, flowing from S/D tunneling through gate dielectric are the dominant component of conduction mechanism under inversion region, and electrons from gate electrode tunneling through gate dielectric are the dominant component of conduction mechanism under accumulation region.

Fig. 6.8 (a) and **Fig. 6.8** (b) exhibit the band-diagrams and current flows of carrier separation measurement under inversion mode, respectively. The substrate current I_B is mainly composed of the electron current from the gate electrode, meanwhile the source/drain current I_{SD} corresponds to the hole current from Si substrate when the device is biased at inversion mode. Electrons supplied from the gate conduction band in pMOSFETs are limited by the generation rate of minority electron in p^+ gate. On the other hand, the probability for carrier tunneling through gate dielectrics is strongly affected by tunneling distance and barrier height [12]. Due to the asymmetry of the HfO_2/SiON band structure, one observes that electrons tunnel more difficultly through the gate dielectrics as compared to holes. Consequently, electrons will contribute much less to the current through the gate stack than holes do. In pMOSFETs, hole current from the channel is the predominant injection current under stressing.

In contrast, **Fig. 6.9** (a) and **Fig. 6.9** (b) show the band-diagrams and current flows of carrier separation measurement under accumulation mode, respectively. The

electrons of conduction band in the substrate possesses higher tunneling probability than that for holes of valence band from the gate electrode, thus resulting in the substrate current's domination of the gate leakage current.

Fig. 6.10 shows the temperature dependence of gate current I_g as a function of gate voltage for the HfO_2/SiON layer with and without F incorporation, both under inversion and accumulation regions. Clearly, the gate current in each sample increases with increasing temperature, implying that the conduction mechanism of the gate current is trap-related, i.e. trap-assisted tunneling (TAT), Frenkel-Poole, etc.

Because the gate leakage current for the HfO_2/SiON stack-gated devices with and without F incorporation are composed of two kinds of carriers, i.e. hole current and electron current, we need to separately determine the mechanism of carrier conduction in the HfO_2/SiON dielectrics for each case. Therefore, we made Frenkel-Poole (F-P) plots for hole current and electron current respectively.

The current from Frenkel-Poole emission is of the form:

$$J = B \times a \times E_{eff} \times \exp\left(\frac{-q(\phi_B - \sqrt{aqE_{eff}/\pi\varepsilon_{HfO2}\varepsilon_0})}{kT}\right);\ B = q\mu N_T\ ,\ \text{a} = \frac{\varepsilon_{SiO2}}{\varepsilon_{HfO2}} = \text{constant}$$

$$\Rightarrow \quad \ln(J/E_{eff}) = \frac{q\sqrt{aq/\pi\varepsilon_{HfO2}\varepsilon_0}}{kT}\sqrt{E_{eff}} - \left[\frac{q\phi_B}{kT} + \ln(aB)\right]$$

$$\text{or} \quad \ln(J/E_{eff}) = E_{act} \times \left(\frac{q}{kT}\right) + \ln(aB)\ ;\quad E_{act} = -(\phi_B - \sqrt{aqE_{eff}/\pi\varepsilon_{HfO2}\varepsilon_0})$$

where B is a constant related to the trapping density and carrier mobility in the HfO_2 film, ϕ_B is barrier height, E_{eff} is the effective electric field in the SiO_2 film, ε_0 is the free space permittivity, ε_{HfO2} is the dielectric constant of HfO_2, k is Boltzmann constant (1.38×10^{23} J/K), E_{act} is a field dependent effective activation energy and T is the temperature measured in Kelvin. From arrhenius plot of E_{act} [i.e., $\ln(J/E_{eff})$ vs. (q/kT)], we can obtain E_{act} and aB. Then, barrier height ϕ_B and dielectric constant ε_{HfO2}

of HfO_2 can be calculated from the intercept of y axis and the slope of the fitting curves in the E_{act} vs. $\sqrt{E_{eff}}$ plot according to $E_{act} = q\sqrt{aq\pi\varepsilon_k\varepsilon_0}(\sqrt{E_{eff}}) - q\phi_B$.

As shown in **Fig. 6.13** and **Fig. 6.14**, under inversion mode, excellent linearity for each current characteristic has been observed for both samples. This tendency indicates that the Frenkel-Poole conduction mechanism is dominant for both electron and hole currents. Moreover, the conduction mechanism does not change as F is incorporated. Barrier height φ_B and the dielectric constant ε_{HfO2} of HfO_2/SiON for both cases can be calculated. The ε_{HfO2} value from F-P conduction mechanism is found to be $\sim$10.2 for both samples, respectively. This indicates that in this work, F incorporation into HfO_2/SiON does not significantly degrade the dielectric constant of the HfO_2 film.

The φ_B for the "hole" traps in the control sample and F-incorporated sample are about 0.74 eV and 0.71 eV, respectively. On the other hand, for the "electron" traps the φ_B of the control sample and F-incorporated sample are both about 0.97 eV. It is noted that the φ_B to be discussed in this chapter is "effective" values that represent the HfO_2/SiON gate stack [13]. We consider that the injected carriers flow across HfO_2/SiON by the hopping via the trap sites with energy barrier φ_B, which value depends on the fabrication process [14]. These experimental results confirm that the energy level of traps in the control sample is similar to that of the F-incorporated sample and the electron traps seem to be deeper than the hole traps by around 0.2 eV.

For material analysis, transmission electron microscopy (TEM) was used to determine the exact thickness and identify the interface situation between HfO_2 and the Si substrate and the interface between HfO_2 and the gate electrode. **Fig. 6.15** shows HRTEM images of the devices with HfO_2/SiON gate stack. We can univocally see that owing to RTA treatment, interfacial layer thickness becomes thicker by about

0.4 nm, which must be carefully controlled in order to maintain a sufficiently low EOT value. From the HRTEM, we can also find that the estimated value of the dielectric constant for HfO_2 is about 11.4.

6. 3. 2 Appropriate Measurements for Evaluating High-k Gate Dielectric

Fig. 6.14 and **Fig. 6.15** illustrate DC I_d-V_g characteristics for the control sample and the F-incorporated sample, respectively. First, we measure forward-1 (0 V ~ −2 V) for the "Forward 1" then measure reverse-1 (−2 V ~ 0 V) for the "Reverse 1" as the first cycle, and then repeat this sweeping cycle again. It can be seen that V_{th} shifts toward negative voltage after first cycle, which indicates that net positive charges are trapped in the gate dielectric layer when the devices are being measured. Besides, V_{th} recovers during the second cycle without applying a small stress. However, this recovery is only partial, i.e., V_{th} does not go back fully to its initial value, indicating that some positive charges still remain in the gate dielectrics. These observations suggest that both fast trapping and de-trapping charges occur in the HfO_2 during measurement.

There are two noticeable features for both samples with applying the additional small stress. First, the fact that forwad-2 I_d-V_g in Cycle 2 matches forwad-1 I_d-V_g in Cycle 1 reveals that the unstable fast charge is successfully eliminated by using the small stress, which allows us to accurately estimate the result of the measurement. Secondly, V_{th} of forward I_d-V_g for both cycles maintains the same value, and implies that using the small stress does not cause any extra damage to the gate stacks, nor does it affect device parameters. **Fig. 6.16** shows a schematic illustration for the possible case of fast charging effects (FCE).

Therefore, to alleviate the unstable fast charge trapping and detrapping effects [15]-[19], a small positive voltage (0.5 V) for several seconds was applied to detrap them before I_d-V_g and charge pumping measurements, without causing any extra damage to the gate stacks. The purpose of this step is to more accurately estimate the density of slow traps without being affected by the variation of interval between the stress and measurement. In order words, we will focus on the slow traps in the gate stacks at this stage.

6. 3. 3. NBTI of Control and Fluorine-Incorporated Devices

Negative bias temperature instability (NBTI) is an important reliability issue because it causes the threshold voltage shift and the generation of interface states, which in turn results in the degraded driving current with electrical stressing. To evaluate device degradations due to the bias temperature (BT) stress, the gate electrode of the devices was subjected to stress condition with negative bias (－3.5 V) varying from 25°C to 125°C, while the drain/source and substrate were all grounded, as shown in **Fig. 6.18**. The dependences of the threshold voltage shift, the generation of interface trap density, the bulk trap density, and the drain current on stress time were investigated for various temperatures.

For both control and fluorine incorporated devices, negligible change is observed in S.S under constant voltage stress at room temperature, as shown in **Figs. 6.19** (a) and (b). This indicates that interface state generation plays no significant role. Rather, charge trapping in the bulk dielectric is the primary mechanism leading to CVS issues in high-k dielectrics. V_{th} shift of the control sample is found to be slightly larger.

The threshold voltage shift ($\triangle V_{th}$) is measured from the I_d-V_g curves shown in **Fig. 6.20** (a) linear scale and (b) logarithm scale. The threshold voltage shifts toward

negative gate voltage ($\triangle V_{th} < 0$), thus implying that net positive charges are trapped in the gate dielectric layer as the device is stressed. It is clear that the F-incorporated sample always shows smaller $\triangle V_{th}$ than the control sample under different stress voltages. **Fig. 6.20** (b) shows that V_{th} degradation obeys the power law [20]-[21],

$$\triangle V_{th}(t) = At^b \qquad (6\text{-}3)$$

and the exponential values of both devices at $V_g = -4$V (~0.12) are much larger than those of the devices at $V_g = -3.5$ V (about 0.03~0.04). This denotes that the V_{th} degradation could be more serious under larger constant voltage stressing. The exponential value is voltage dependent relative to the bulk trap generation.

To further gain insights into the degradation mechanism during voltage stressing, the interface states generation, $\triangle N_{it}$, and the increase of "effective" total trap density, $\triangle N_{tot}$, which was calculated from ΔV_{th} assuming the charge was trapped at the interface between the dielectric and the substrate, are plotted as a function of the stress time in **Figs. 6.19** (a) and (b). Apparently, $\triangle N_{tot}$ is found to be significantly larger than $\triangle N_{it}$, suggesting that the degradation under CVS is dominated by the charge trapping in the bulk of HfO_2 film, rather than the generation of interface states, irrespective of whether F is added or not. The instability of HfO_2/SiON gate stack is mainly determined by the bulk charge traps, contrast to that in the SiON gate stacks. In addition, the improvement in charge trapping is larger than that in interface generation for the F-incorporated samples.

The degradation in the device drain current after CVS is shown and compared in **Fig. 6.20**. Due to a larger V_{th} shift and interface state generation ($\triangle N_{it}$) of the control sample, more severe drain current degradation is observed and the degradation increases with increasing stress voltage.

Fig. 6.23 shows that the F-implanted sample can improve the degradation of (a)

threshold voltage shift ($\triangle V_{th}$) and (b) interface trap density shift ($\triangle N_{it}$) as compared to the control sample. It is worthy to note that the improvements for $\triangle V_{th}$ and $\triangle N_{it}$ increase as the channel length decreases. Since the diffusion distance of F atoms is constant, the ratio of diffusion distance divided by channel length would be higher as the channel length decreases, and more F have the chance to be trapped. This asserts that the method of using fluorine implant into S/D is highly applicable to the future CMOS technology. The improvement may be due to fluorine atoms, similarly to nitrogen atoms, form complexes at the interface as well as in the dielectrics, which can effectively reduce the total number of dangling bonds at the interface and defects in the bulk, thus leading to reduced CVS degradation.

The I_d-V_g curve is observed to shift toward negative gate voltage with increasing stress time at 125°C for both the control and fluorine incorporated devices, as shown in **Figs. 6.22** (a) and (b). V_{th} shift of the control sample is slightly larger. There is visible change in S.S at high temperature as compared to that at room temperature, indicating that $\triangle N_{it}$ increases with increasing temperature. **Figs. 6.23** (a) and (b) depict the time evolution of interface states generation for both the control and fluorine incorporated devices at various temperatures. It can be also found that $\triangle N_{it}$ of fluorine incorporated device is always smaller than the control devices at all temperatures.

Fig. 6.24 (a) compares the NBT-stress-time dependence of threshold voltage shift for the HfO_2/SiON gate stack with and without F incorporation. The BT stress condition is V_g = −3.5V under 125°C. It can be seen that F incorporated films exhibit NBTI improvement similar to fluorine-induced NBTI improvement in SiOF case [11-12]. **Fig. 6.24** (b) shows that the exponential values of both samples at 125°C (about 0.13~0.14) are much larger than those of the devices at 25°C (about 0.03~0.04).

This indicates that the V_{th} degradation is more severe under BT stress at high temperatures [22]. The exponential value is temperature dependent relative to bulk trap generation.

Figs. 6.25 (a) and (b) show $\triangle N_{it}$ and $\triangle N_{tot}$ as a function of time during NBTI for the two devices at different temperatures. The major degradation of NBTI is caused by the positive charge trapping in the films rather than the interface generation, suggesting that the positive charge trapping is not completely caused by the H^+ capturing. Therefore, except for positive charge caused by H species, a large amount of extra trapping centers is also present in the HfO_2/SiON gate stack. F atoms seem to effectively decorate these trapping centers, leading to less degradation.

Fig. 6.26 shows the I_d degradation for the samples with and without F-incorporation. It can be seen that fluorine is effective for the improvement of the BT instability. In order to gain sight into the mechanism of NBTI for fluorine into HfO_2/SiON film, $\triangle V_{th}$ and $\triangle N_{it}$ after 1000sec NBT-stress as a function of temperature are used to estimate the activation energy of NBT degradation for the samples with and without F-incorporation, as shown in **Figs. 6.27** (a) and (b). The activation energies of NBT degradation for fluorine incorporated HfO_2/SiON gate stack are nearly identical to those without fluorine incorporation. The activation energies of $\triangle V_{th}$ are 0.08 eV and that of $\triangle N_{it}$ are 0.14 eV for two devices. Activation energies of $\triangle V_{th}$ are lower than those of $\triangle N_{it}$, indicating that V_{th} instability is not only contributed by interface trap generation but mainly comes from the more significant charge trapping in the bulk of high-k dielectric. Furthermore, it should be noted that both $\triangle V_{th}$ and $\triangle N_{it}$ are improved by fluorine incorporation, while maintaining almost the same activation energies. This implies that fluorine seems to electrically passivate a significant amount of hole traps and interface states.

6. 3. 4 Dynamic AC Stress

Most gate dielectrics reliability tests make use of DC stressing because of its simplicity. However, in actual CMOS circuit operation, AC gate bias with specific frequency and duty cycle is usually used. AC stress is therefore more realistic and can provide additional insights into the trapping dynamics. It has been reported that AC stressing of SiO_2 results in longer lifetime than DC stress [23]-[24]. **Fig. 6.28** illustrates the schematics of the measurement setup for the threshold voltage instability testing under dynamic stress. During the AC stress, AC square wave pulses from pulse generator are applied to the gate electrode; while the other three terminals are grounded. **Fig. 6.29** and **Fig. 6.30** display the stress time evolution of threshold voltage shift and interface generation for HfO_2/SiON gate stack with and without F incorporation as a function of frequency of AC stress, respectively. In order to have a fair comparison, the cumulative 'on-time' under the AC unipolar stress is defined as 'stress time' and the duty cycle is fixed at 50% for all samples. For different duty cycles, frequency is fixed at 10KHz for all the samples. Negligible variation in $\triangle N_{it}$ with increasing frequency and decreasing duty cycle under AC stress for both samples is observed, as shown in **Fig. 6. 31** and **Fig**. **6. 32**. Fig. **6. 33** and Fig. **6. 34** show the frequency dependence of $\triangle V_{th}$ for both samples under AC stress at V_g= –4V, 25°C. Clearly, $\triangle V_{th}$ of both samples shifts toward positive gate voltage as frequency of AC stress increases. On the other hand, $\triangle N_{it}$ of both samples seems to show no dependence on the "frequency" of AC stress. **Fig. 6.31** and **Fig. 6.32** show the stress time evolution of threshold voltage shift and interface generation for HfO_2/SiON gate stack with and without F incorporation as a function of the "duty cycle" of AC stress,

respectively. It is found that that $\triangle N_{it}$ of the F-incorporated sample is smaller than that of the control sample under AC stress for any given frequency and duty cycle. This is in agreement with the result of $\triangle N_{it}$ under DC stress. It is observed from **Figs. 6.36** (a) and (b) that the V_{th} degradation is strongly dependent on the frequency and duty cycle of the dynamic stress. V_{th} for both cases shift toward more positive gate voltage as frequency increases, and similar trend is observed as duty cycle decreases. $\triangle V_{th}$ for F-incorporated sample is lower irrespective of frequency and duty cycle. The film quality of fluorine incorporation is more robust under AC stress.

Since V_{th} degradation of pMOS is primarily caused by charge trapping in the HfO_2 film and shifts toward negative gate voltage under DC stress. The bulk traps of HfO_2 appears to be the dominant factor in the threshold voltage instability of pMOSFETs with HfO_2/SiON dielectric by trapping or detrapping charges during AC stress. This finding suggests that both hole trapping and electron trapping occur during DC stress. Further, hole trapping, from carrier separation technique, is the dominant trapping phenomenon, since hole current is much larger than electron current under inversion region. However, when stressed under high AC frequency, holes do not have enough time to tunnel into gate stack to be trapped; in strong contrast, electron flow can follow the varying AC signal, and get trapped during the on-period. Moreover, electrons are more likely to be trapped because they can directly tunnel into high-k dielectric, while holes need to first go through SiON film before getting trapped in HfO_2 film. Therefore, the amount of trapped electrons does not seem to be significantly affected as we change the stress condition from DC to AC. This can be confirmed by the observed significant positive V_{th} shift under AC stress. The above speculation can be explained by the following band diagram, shown in **Fig. 6.10** (a). As a result, the larger V_{th} shift toward positive gate voltage at higher

frequencies, lower duty cycles is thought to be caused by electrons not being able to follow the high frequency signal, so only few holes are trapped during on-period in HfO_2 gate dielectric.

6. 3. 5 Fast Transient Charge Trapping Technique (FTCT)

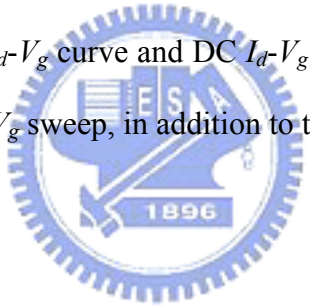
In order to evaluate charge-trapping phenomena at faster measurement times, the measurement configuration of the conventional fast transient pulsed Id-Vg measurement is set up, as shown in **Fig. 6.35**. An external resistance (load resistance) is linked to the drain between V_{DD} and the drain electrode and in general, V_{DD} is set up at a small voltage of 100 mV. A single pulse with fast rise and fall time as well as a longer period is biased at the gate electrode. By using a digital oscilloscope, the gate and drain voltages are simultaneously recorded, which emulates the nFET in an inverter circuit where I_d is expressed as

$$I_D = \frac{100mV}{V_D}\left[\frac{100mV - V_D}{R_L}\right] \quad (6\text{-}4)$$

where V_{DD} is 100 mV, V_D is the voltage recorded at the drain of the nFET, and R_L is the load resistance. Measurements were done as outlined in [3] with t_r, t_f, and the pulse width (PW) values being equally set. For the W/L = 10/1 μm transistor, the load resistance, R_L, is 330 Ω. **Fig. 6.36** (a) illustrates the representative single pulse I_d–V_g characteristics for a MOCVD-deposited Hf silicate (20% SiO_2). The shift in the I_d–V_g curves between the up and down swings of V_g reflects the effect of the charge trapping (i.e., ΔV_t). The V_t shift is extracted at 50% of the maximum I_d current. Another approach is to plot I_d versus time as demonstrated in **Fig. 6.36** (b). In a plot such as this, the degradation in drive current over time can be seen. Note that the vertical drop at V_g = 2.5 V of the I_d–V_g curve (**Fig. 6.36** (a)) is associated with the

'droop' at the top of the I_d–time current pulse (**Fig. 6.36** (b)).

Fig. 6.37 shows the new single pulsed I_d–V_g method to improve the noises and parasitic capacitance of conventional method (**Fig. 6.35**). **Fig. 6.38** shows the results of different rising and falling times of a single pulse. We can clearly find that the width of I_d-V_g curves reduces with the shorter rising and falling times of a single pulse. This is due to the longer rising and falling times of a single pulse would result in more significant charge trapping and detrapping, respectively. Therefore, shorter rising and falling times of a single pulse are preferred because most of charge trapping can now occur during the stable period of the pulse. From **Fig. 6.38** (a), we can see that fast transient trapping for both samples belongs to electron trapping; while the sample with fluorine incorporation does show less fast transient electron trapping. Moreover, comparing the pulsed falling I_d-V_g curve and DC I_d-V_g curves, it can be seen that hole trapping occurs during DC I_d-V_g sweep, in addition to transient electron trapping.



6.4 Summary

From previous results, we find that the exponential value of ΔN_{it} is about 0.23~0.25 for both samples, either under CVS or NBTI. This value of ΔN_{it} is similar to that of traditional SiO_2 dielectric under stressing, while the exponential value of ΔV_{th} is voltage dependent and temperature dependent. As a result, we conclude that charge trappings in the bulk of HfO_2/SiON gate stack are responsible for the observed instability. We can expect that the trap charges consist of a continuous distribution, rather than discrete value, of cross sections in HfO_2 high-k film [15]. So a better interface plays only a minor role in reducing the V_{th} instability. Bulk traps need to be reduced.

The experimental results show that hole trapping dominates in DC stress while electron trapping is dominant in AC stress. Bias frequency and duty cycle dependence under AC dynamic stress suggest that bulk trap in HfO_2 is the primary factor responsible for changing ΔV_{th} polarity in HfO_2/SiON pMOSFETs.

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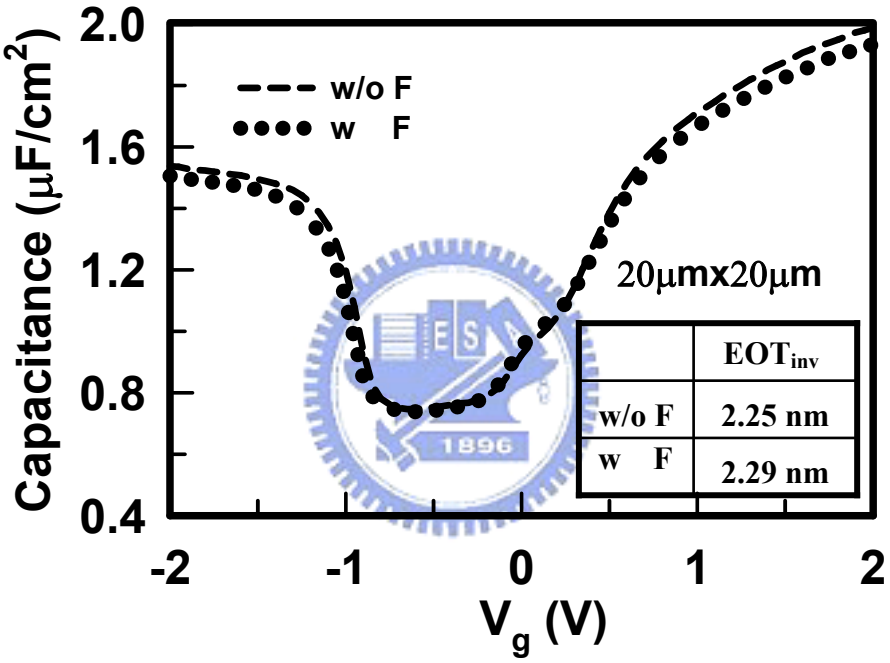


Fig. 6.1 *C-V* curves for p-channel MOSFETs with HfO_2/SiON gate stack, both with and without F incorporation.

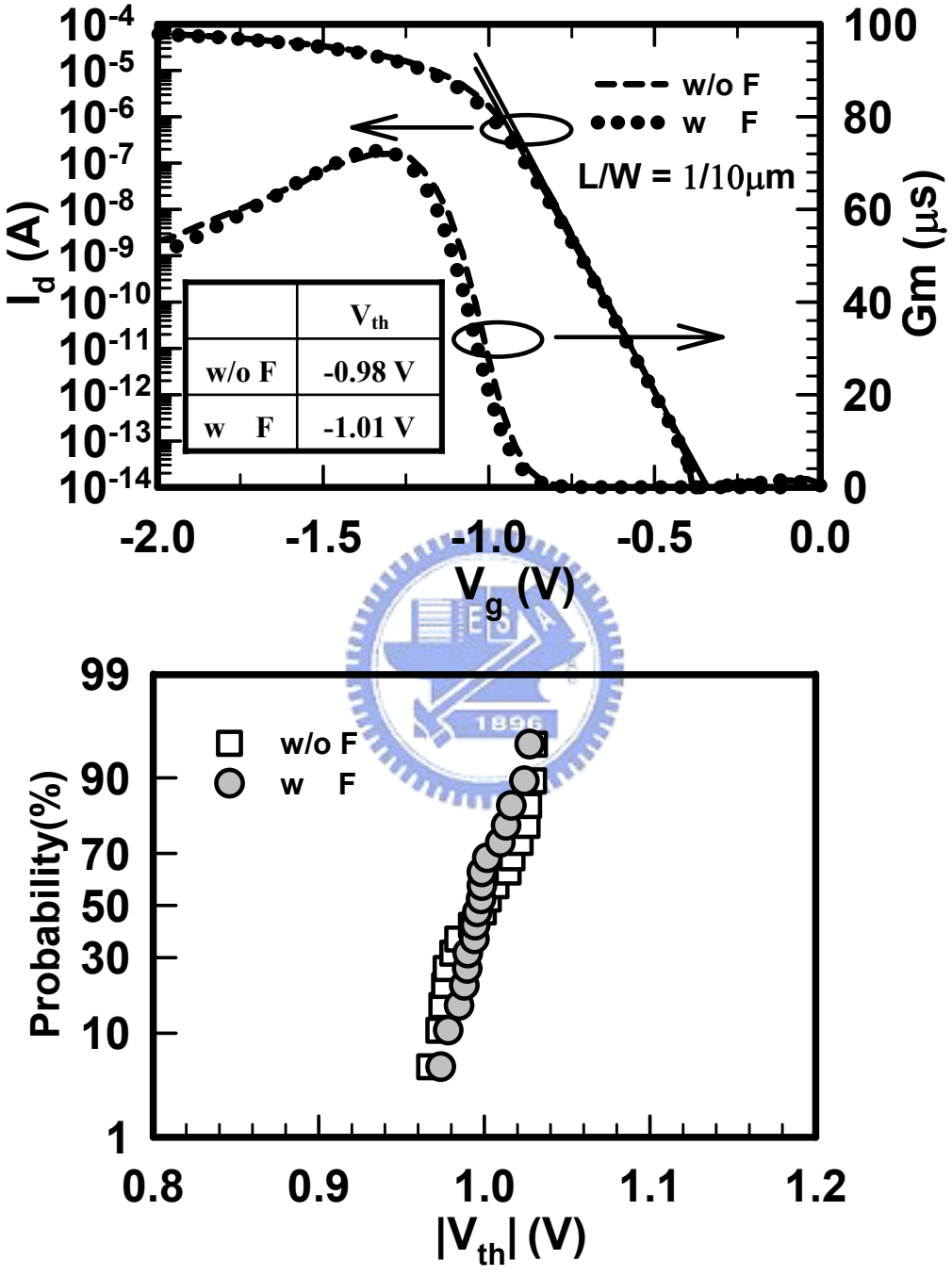


Fig. 6.2 (a) Initial I_d-V_g and G_m-V_g characteristics for fresh p-channel devices (b) Cumulative probability of initial threshold voltage (V_{th}) for HfO_2/SiON gate stack with and without F incorporation.

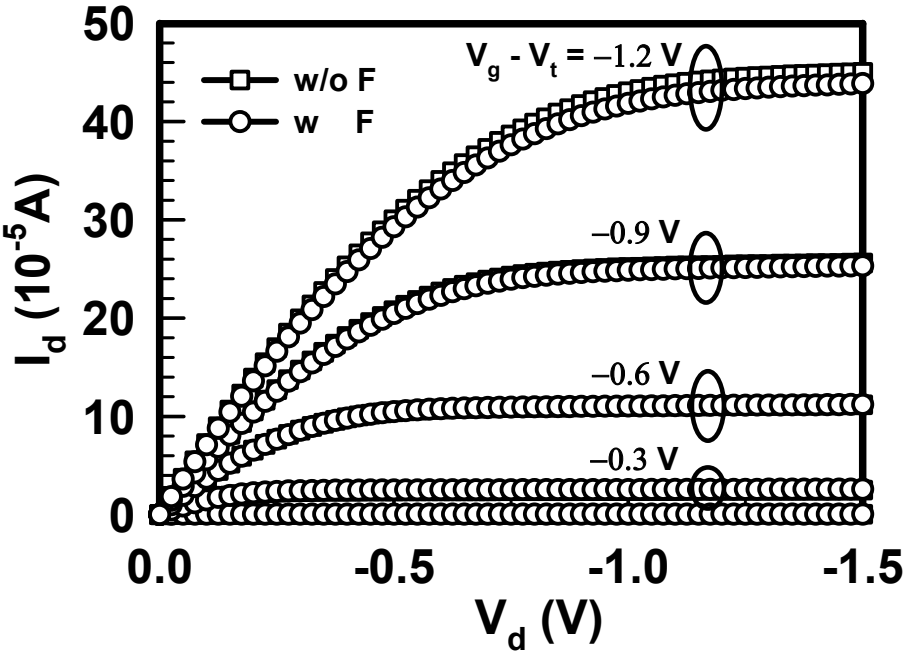


Fig. 6.3 Initial I_d-V_d characteristics for fresh p-channel devices with and without F incorporation.

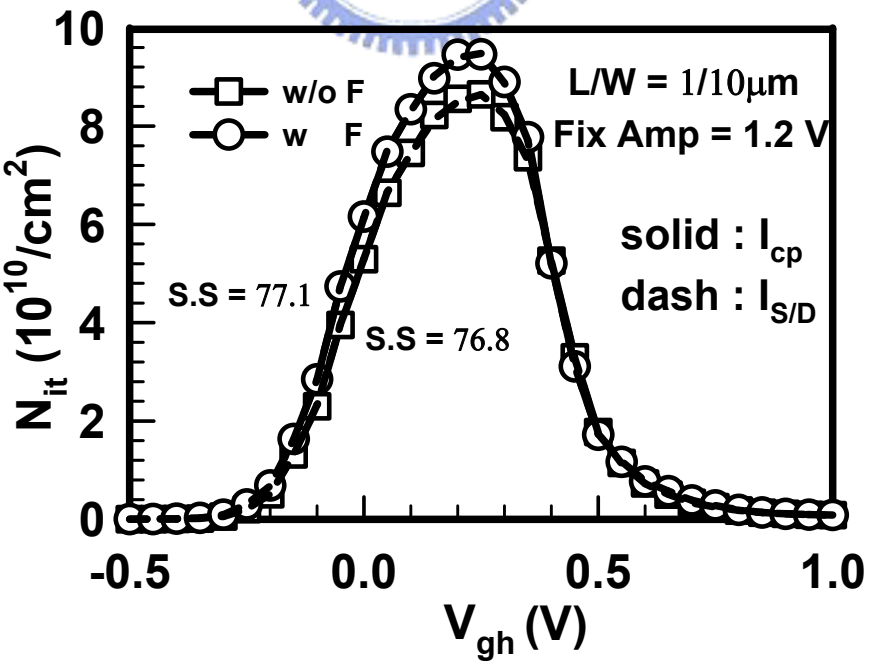


Fig. 6.4 Initial interface trap (N_{it}) characteristics for fresh p-channel devices with and without F incorporation.

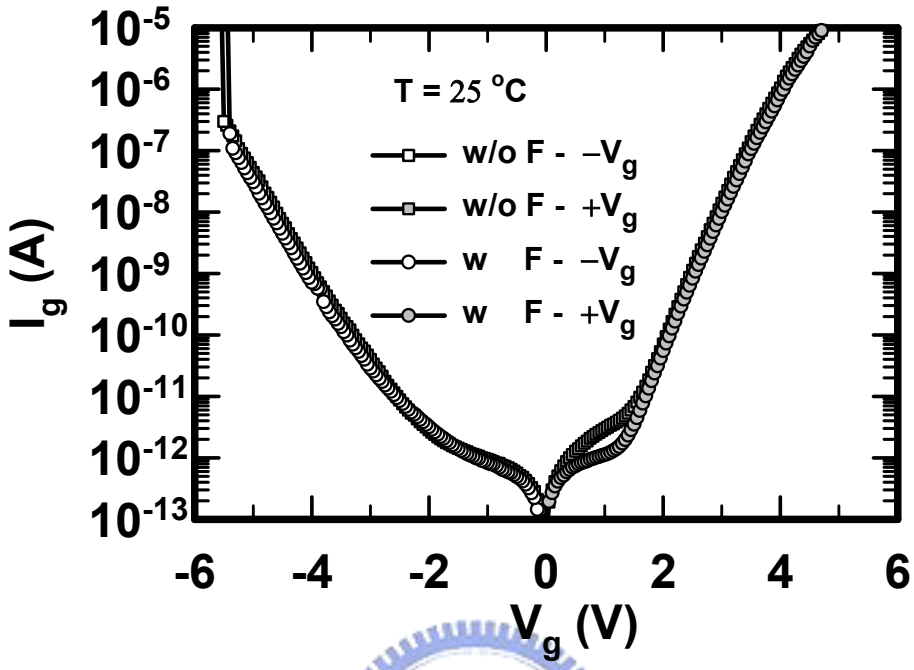
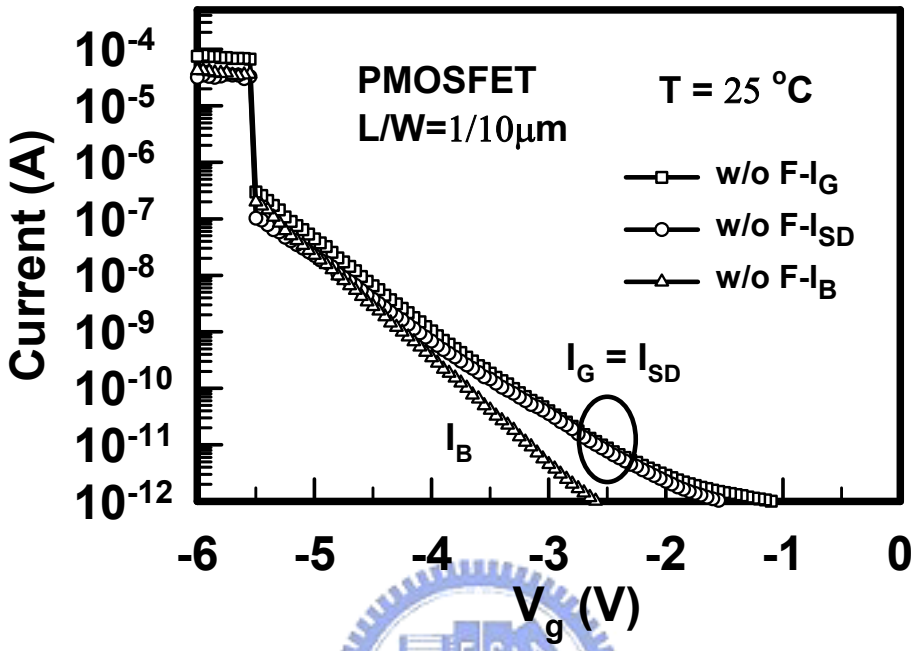


Fig. 6.5 Gate leakage current versus gate bias for fresh p-channel devices with and without F incorporation at room temperature.



(a)

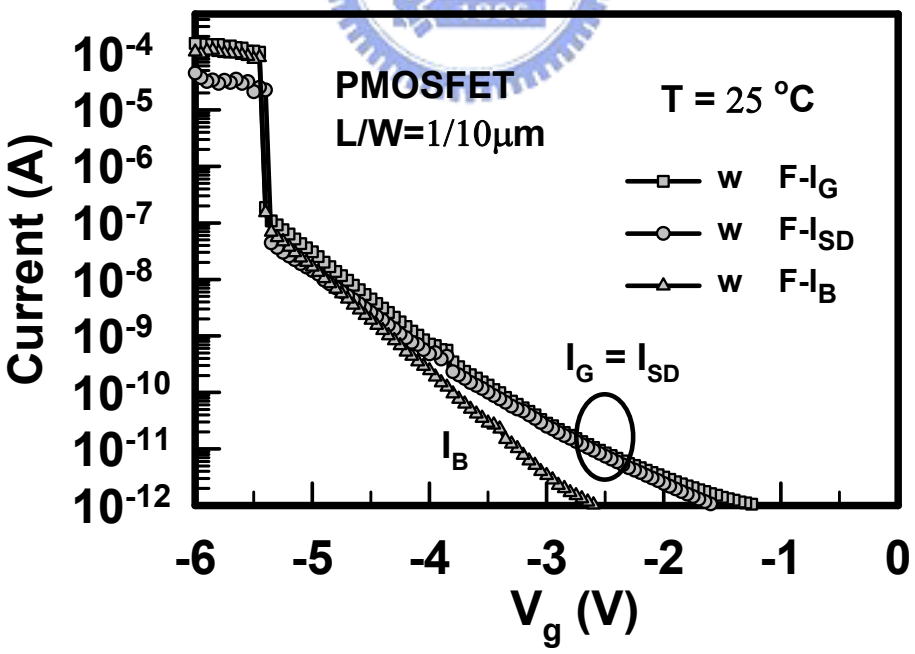
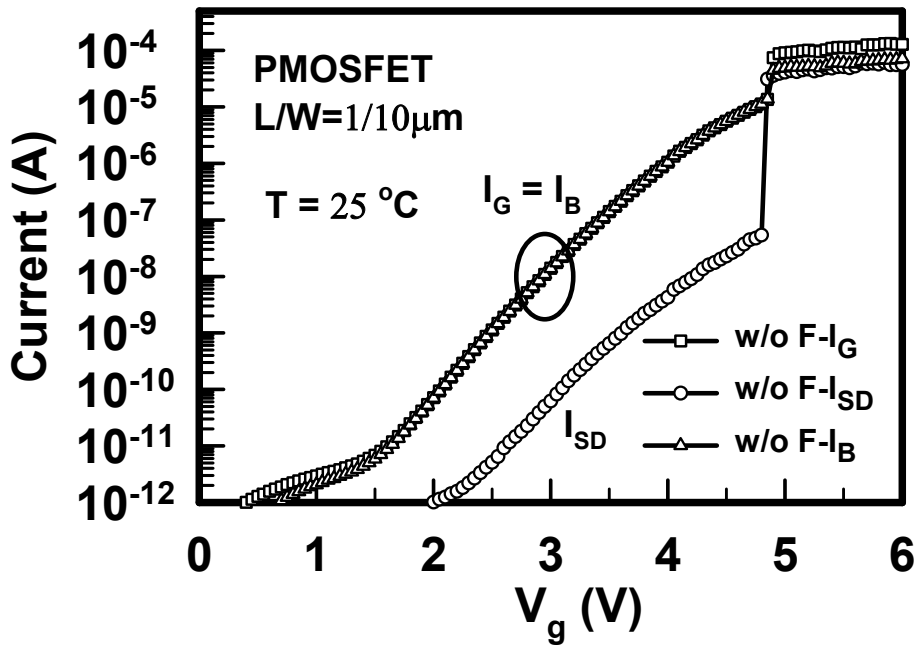
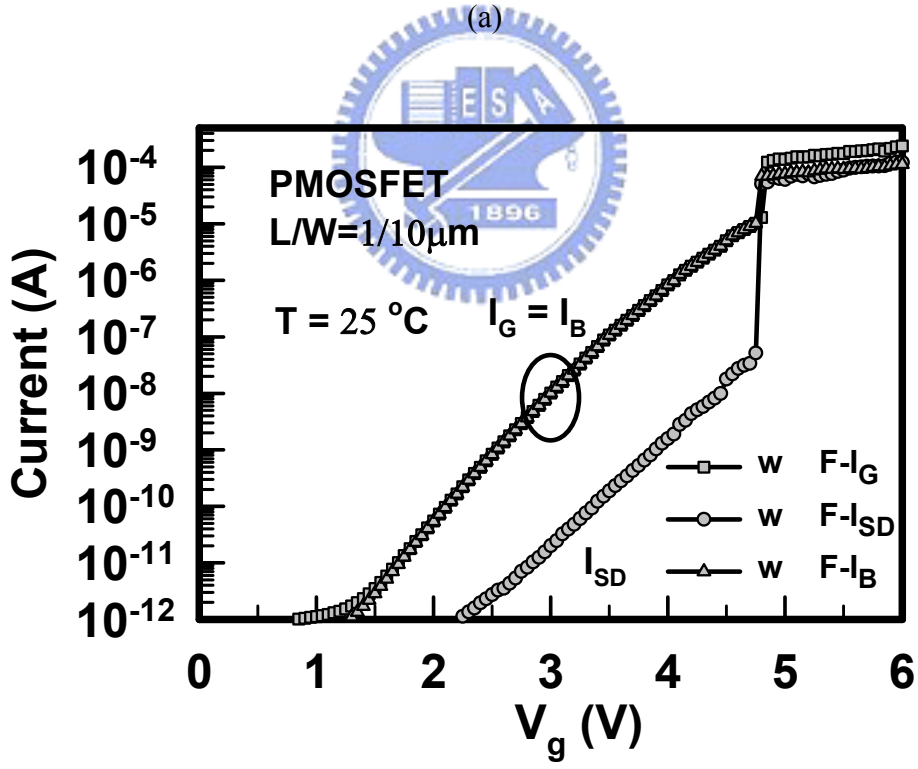


Fig. 6.6 Carrier separation under inversion region (a) w/o F sample (b) with F sample.



(a)



(b)

Fig. 6.7 Carrier separation under accumulation region (a) w/o F sample (b) with F sample.

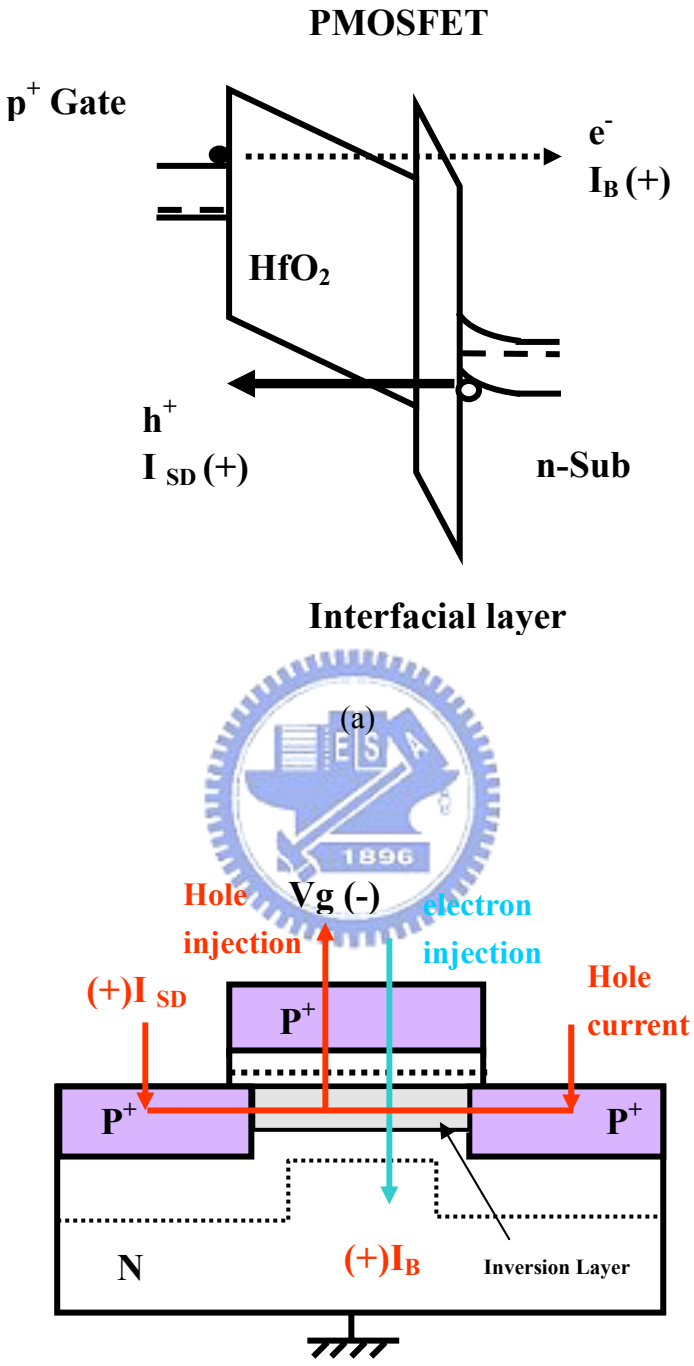
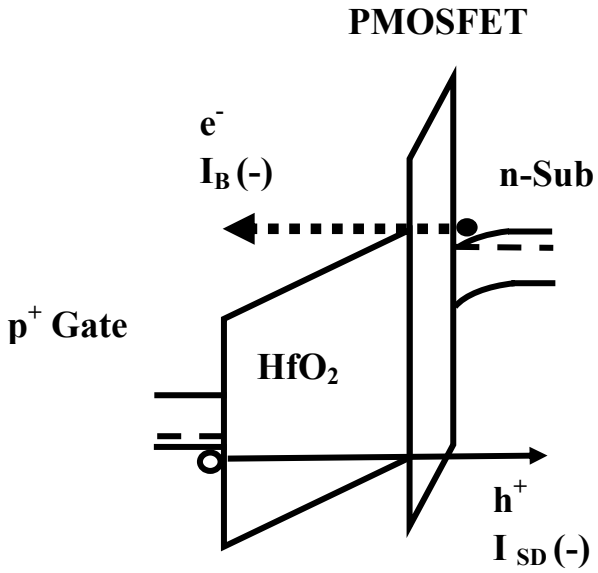
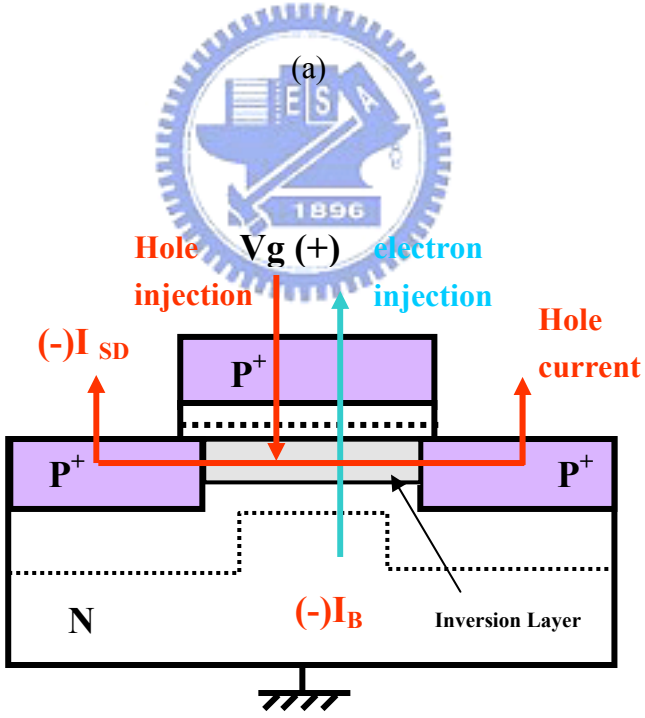


Fig. 6.8 p^+-gated pMOSFET with HfO_2/SiON gate stack under inversion region (a) Band diagrams (b) A schematic illustration of carrier separation experiment.



(a)



(b)

Fig. 6.9 p^+-gated pMOSFET with HfO_2/SiON gate stack under accumulation region (a) Band diagrams (b) A schematic illustration of carrier separation experiment.

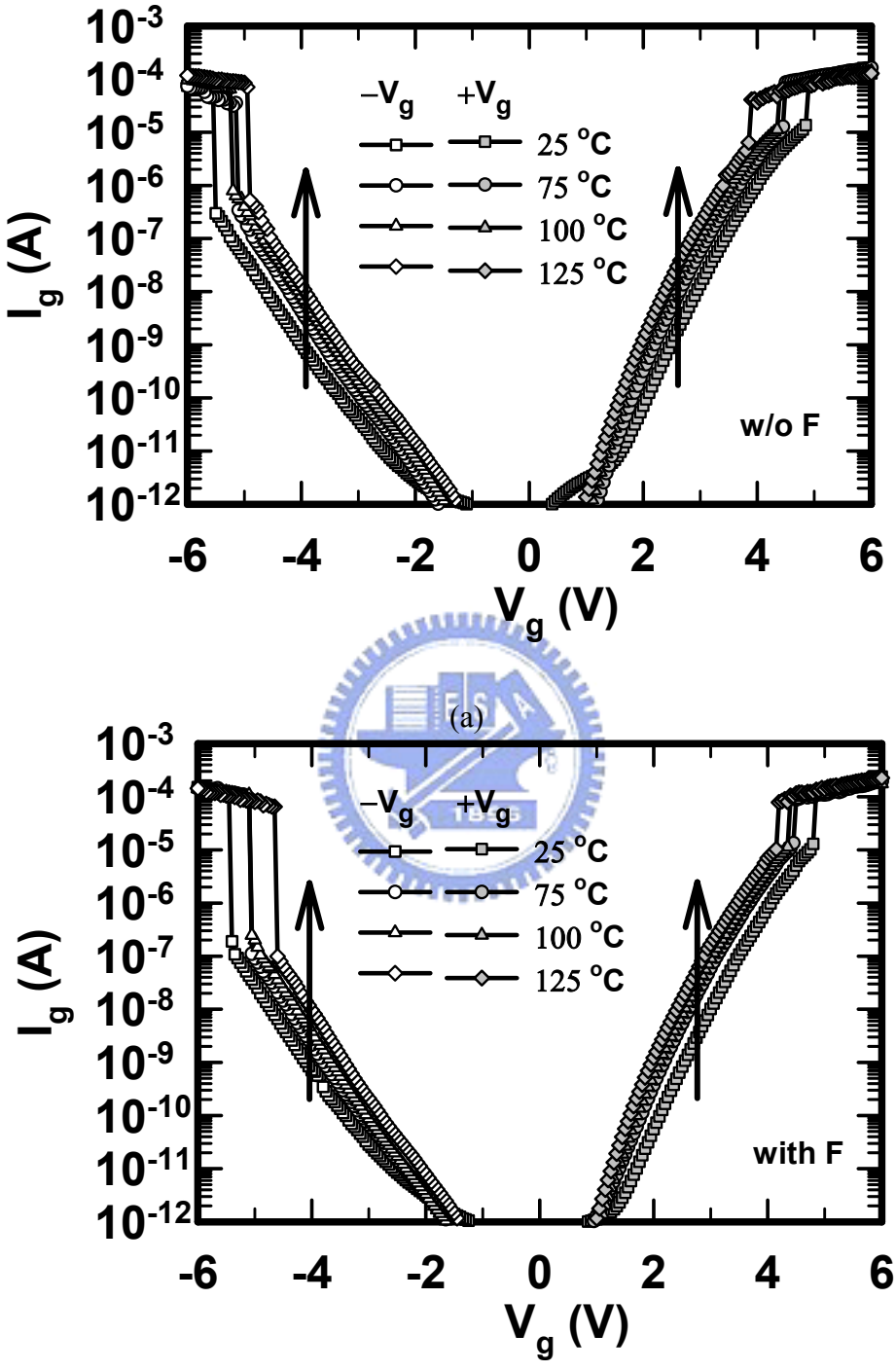
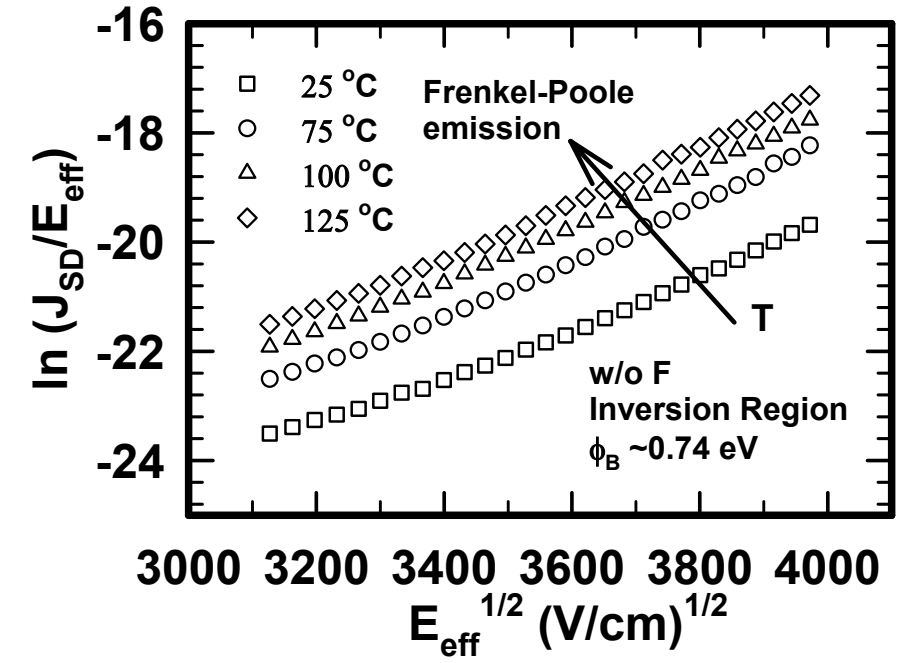
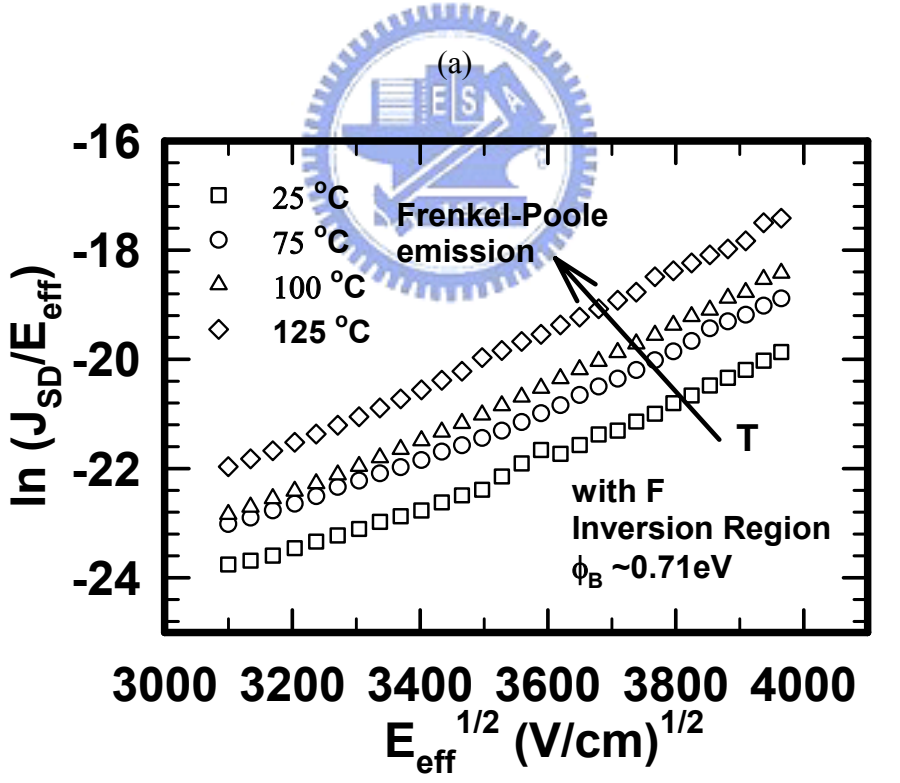


Fig. 6.10 Gate leakage current versus gate bias for fresh p-channel devices at various temperatures (a) w/o F sample (b) with F sample.

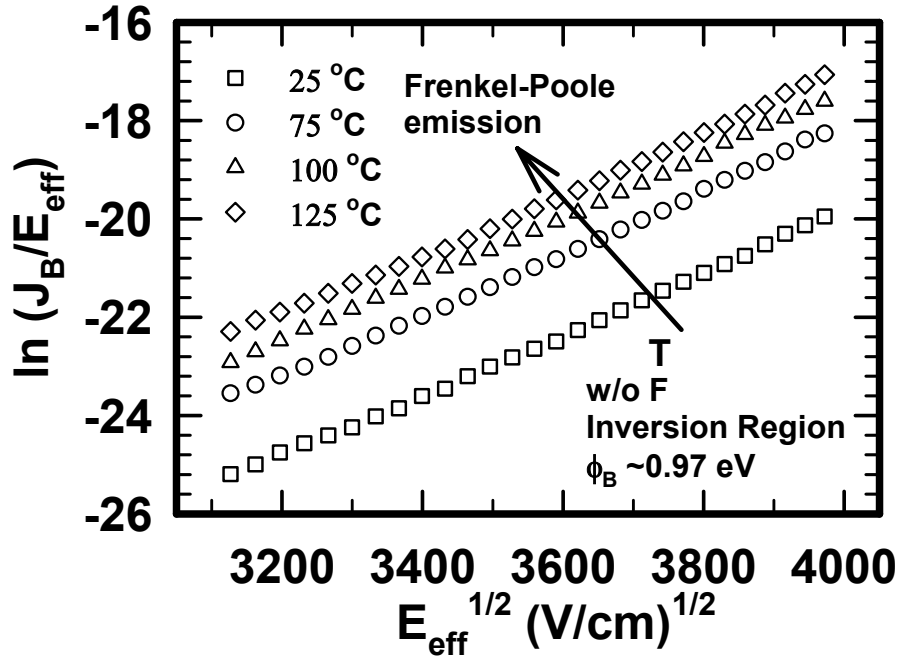


(a)

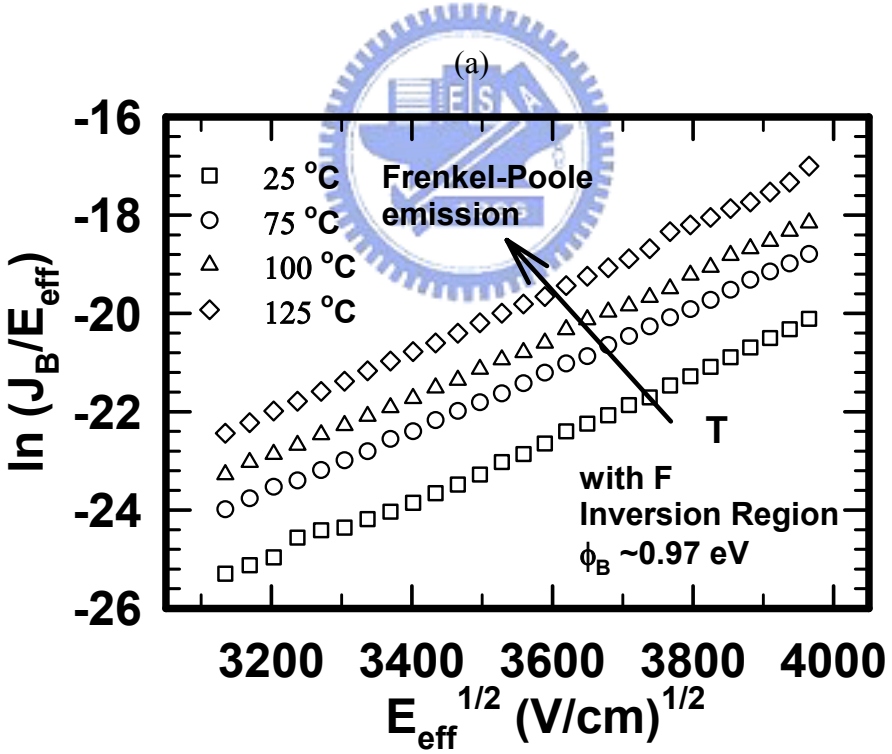


(b)

Fig. 6.11 The conduction mechanism for source/drain current fitting under inversion region (a) w/o F sample (b) with F sample.



(a)



(b)

Fig. 6.12 The conduction mechanism for substrate current fitting under inversion region (a) w/o F sample (b) with F sample.

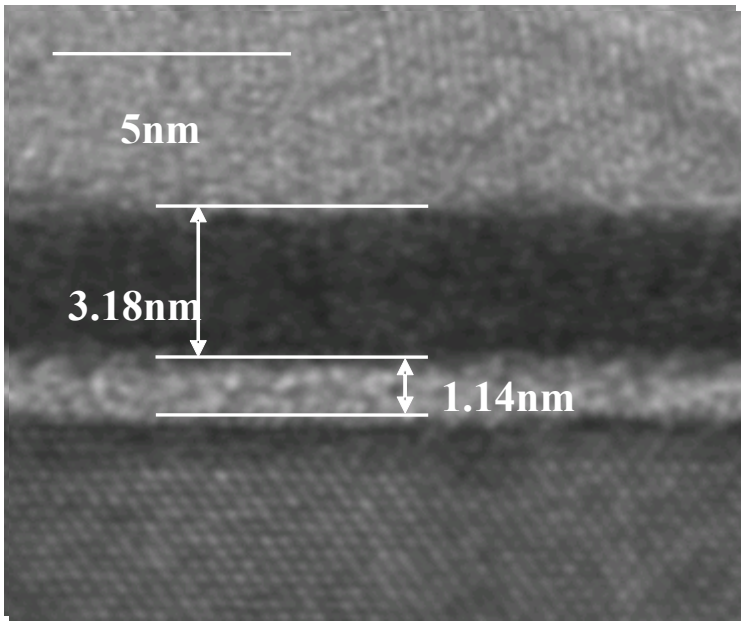
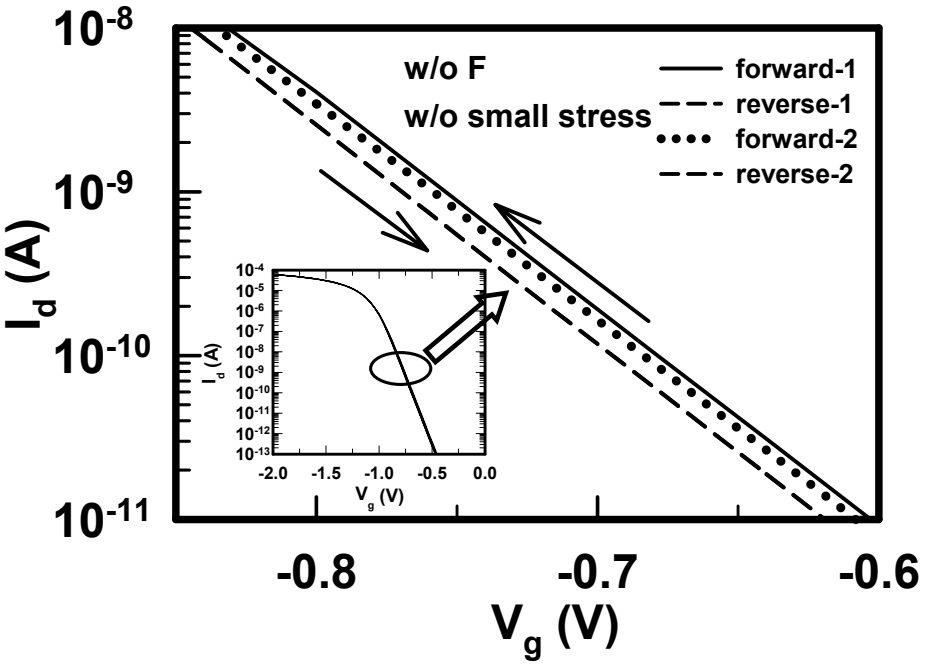
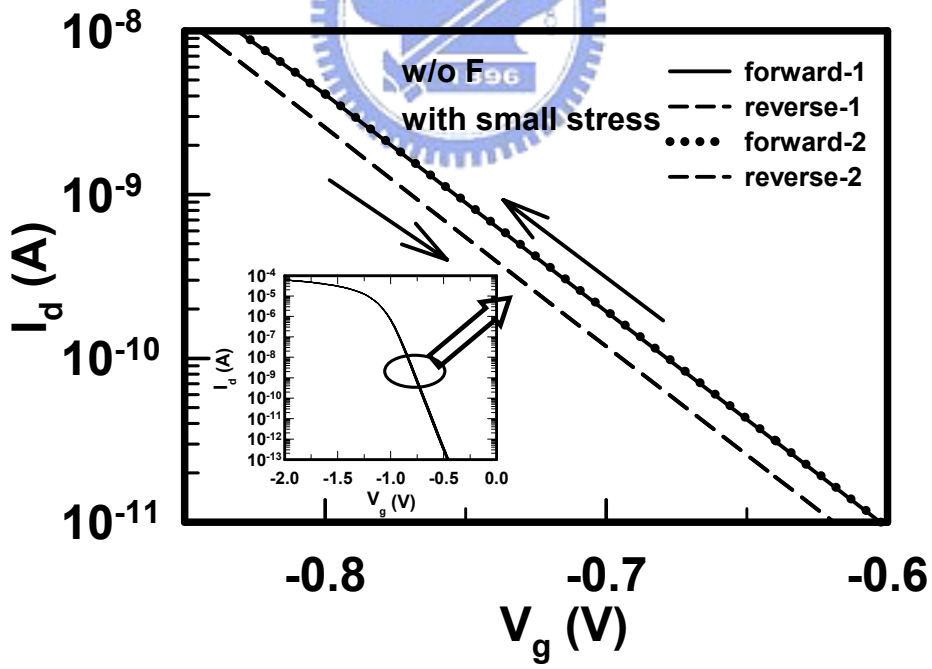


Fig. 6.13 The HRTEM image of the device with HfO_2/SiON gate stack.

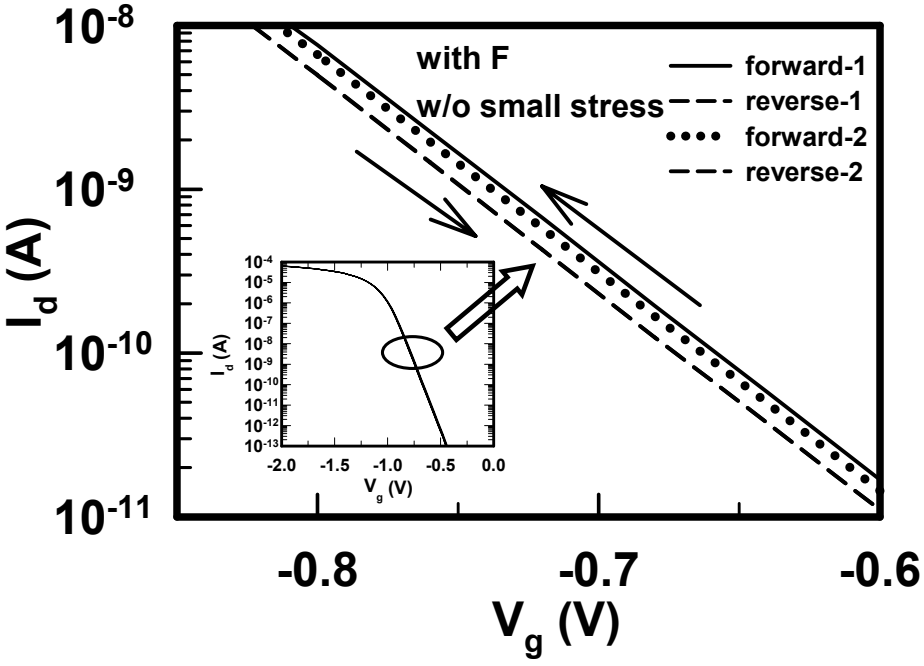


(a)

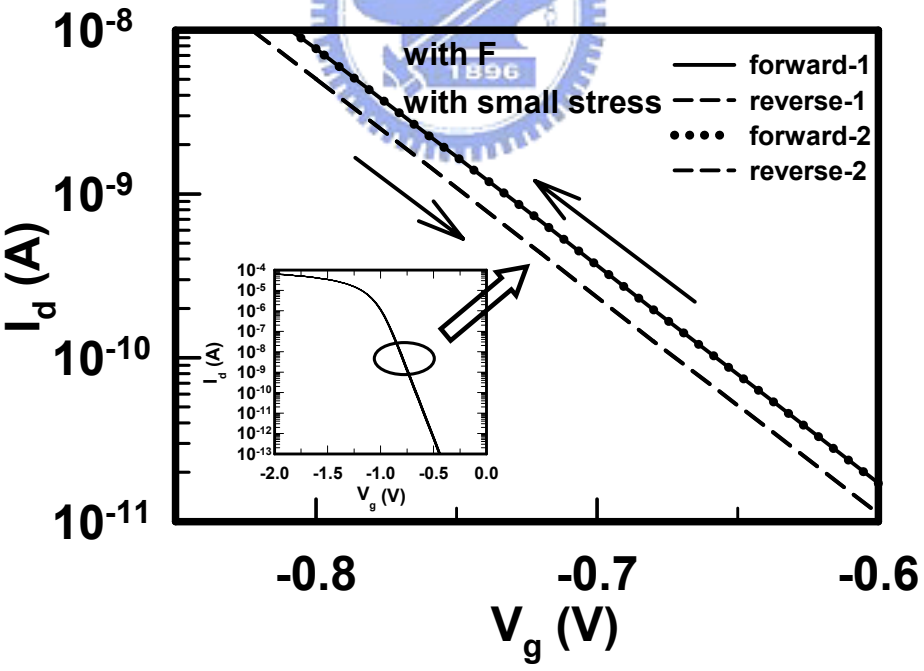


(b)

Fig. 6.14 I_d-V_g characteristics for p^+-gate pMOSFET without F incorporation (a) w/o small stress (b) with small stress.



(a)



(b)

Fig. 6.15 I_d-V_g characteristics for p^+-gate pMOSFET with F incorporation (a) w/o small stress (b) with small stress.

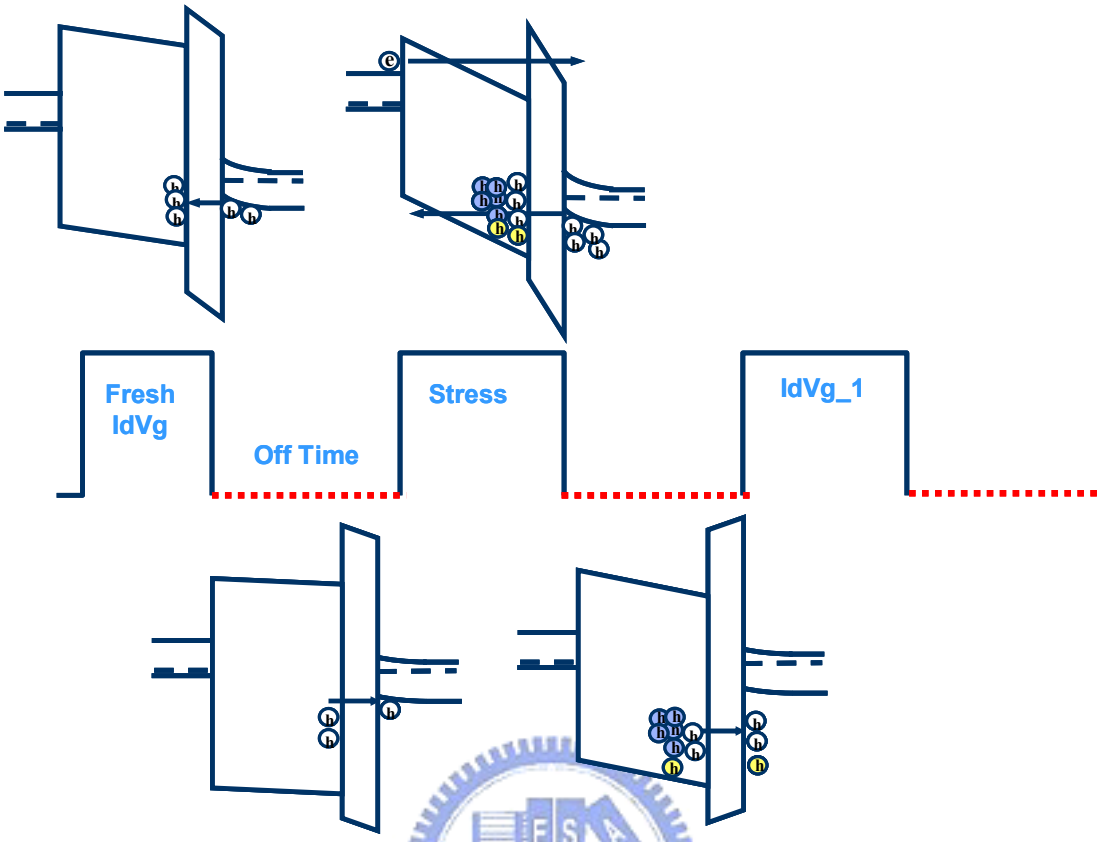
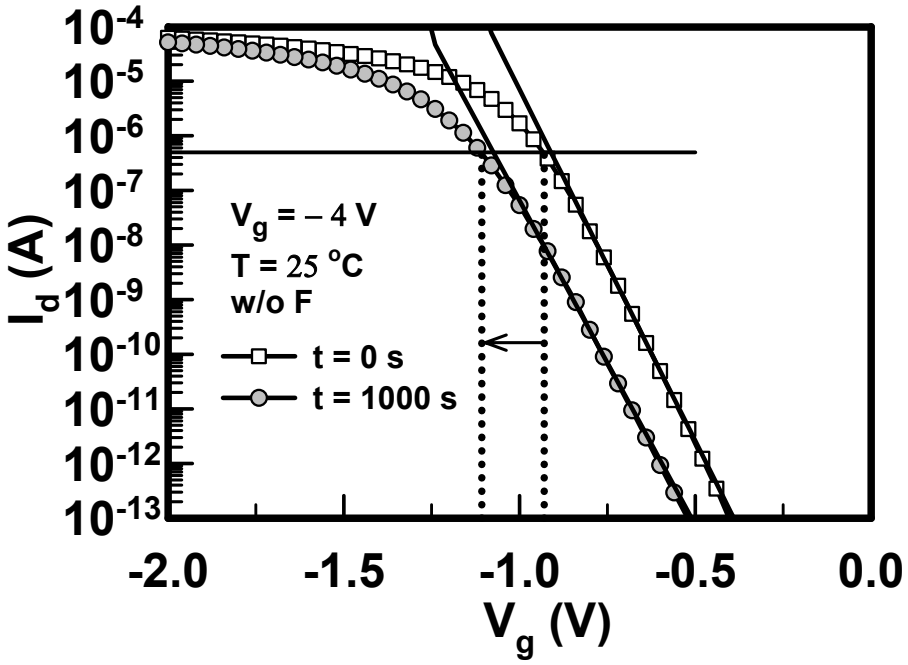
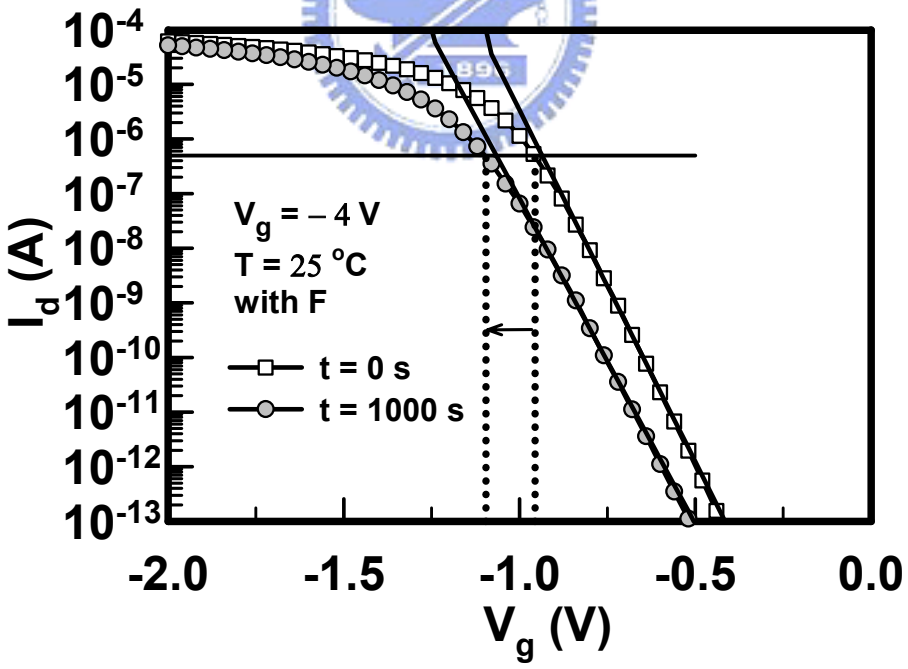


Fig. 6.16 A schematic illustrate for the possible case of Fast Charging Effects (FCE).

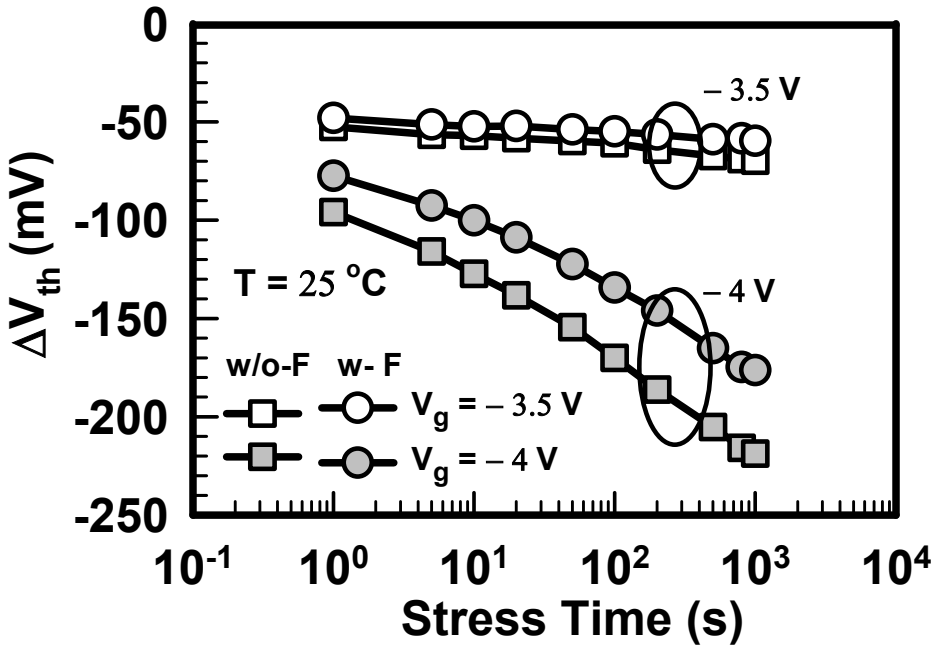


(a)

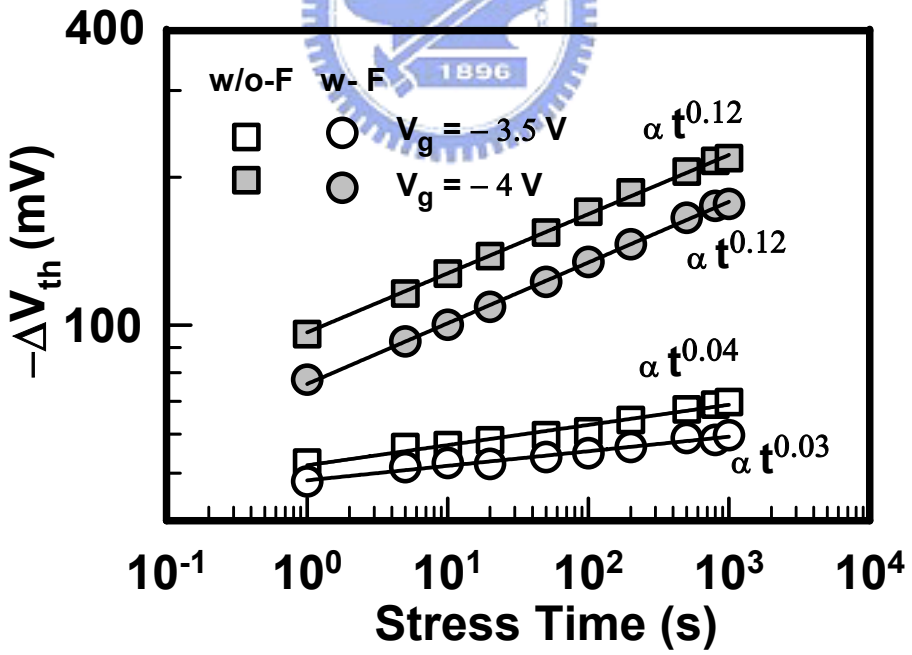


(b)

Fig. 6.17 I_d-V_g characteristics for p^+-gate pMOSFETs before stress and after stress 1000 s at 25 °C (a) w/o F sample (b) with F sample.

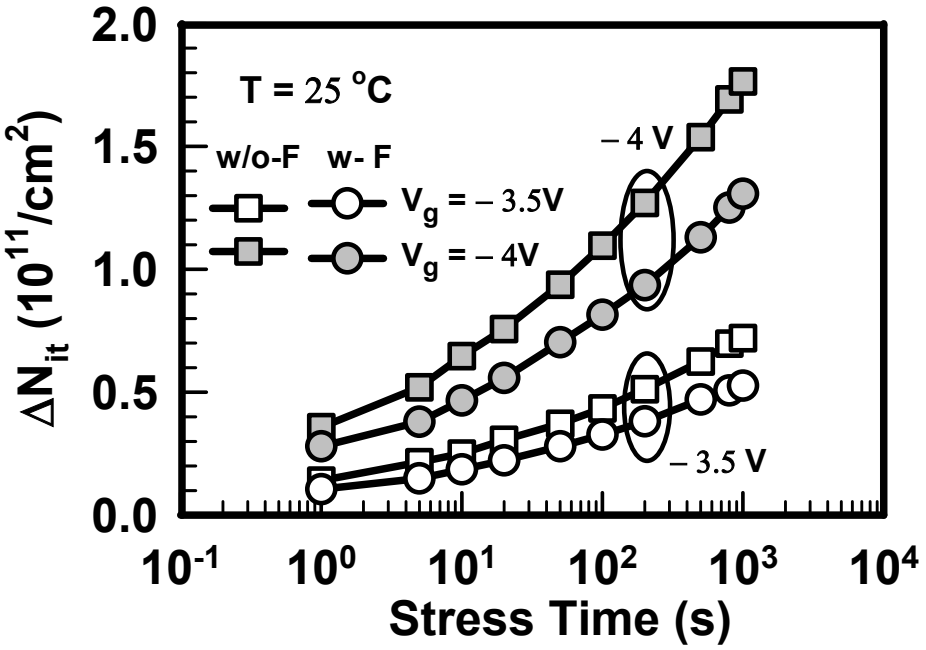


(a)

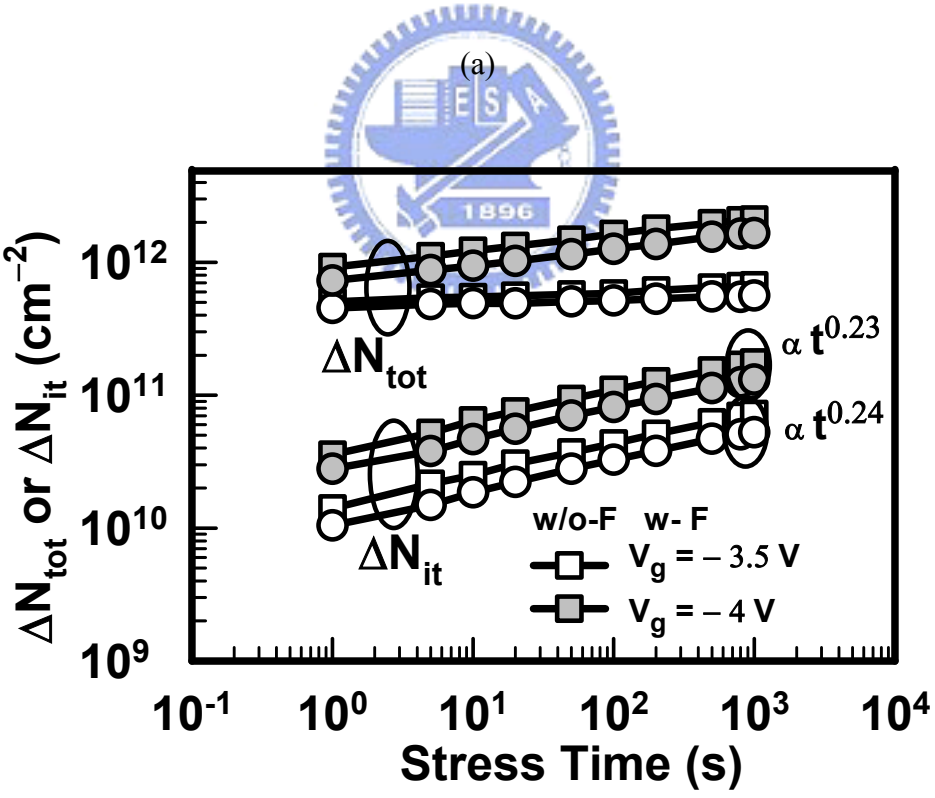


(b)

Fig. 6.18 Threshold voltage shift as a function of stress time, stressed at 25 °C, V_g = –3.5 V & –4 V (a) linear scale (b) logarithm scale.



(a)



(b)

Fig. 6.19 Interface trap shift and (b) total trap shift as a function of stress time, stressed at 25 °C, V_g = –3.5 V & –4 V.

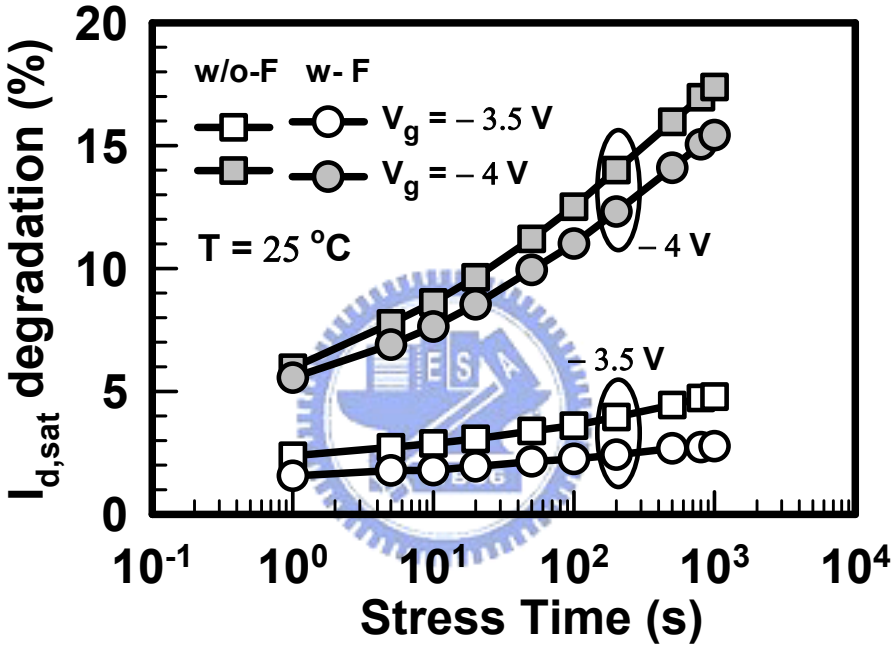
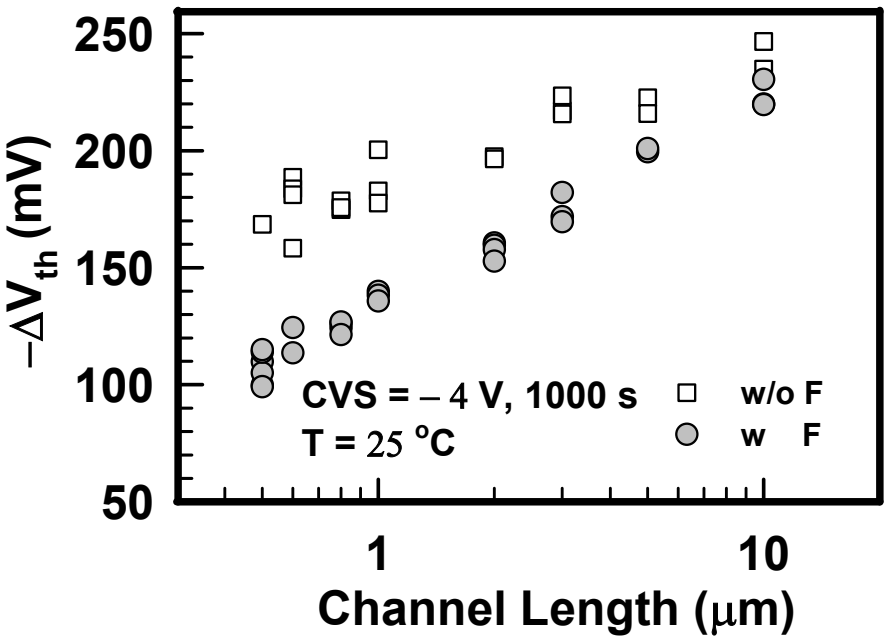
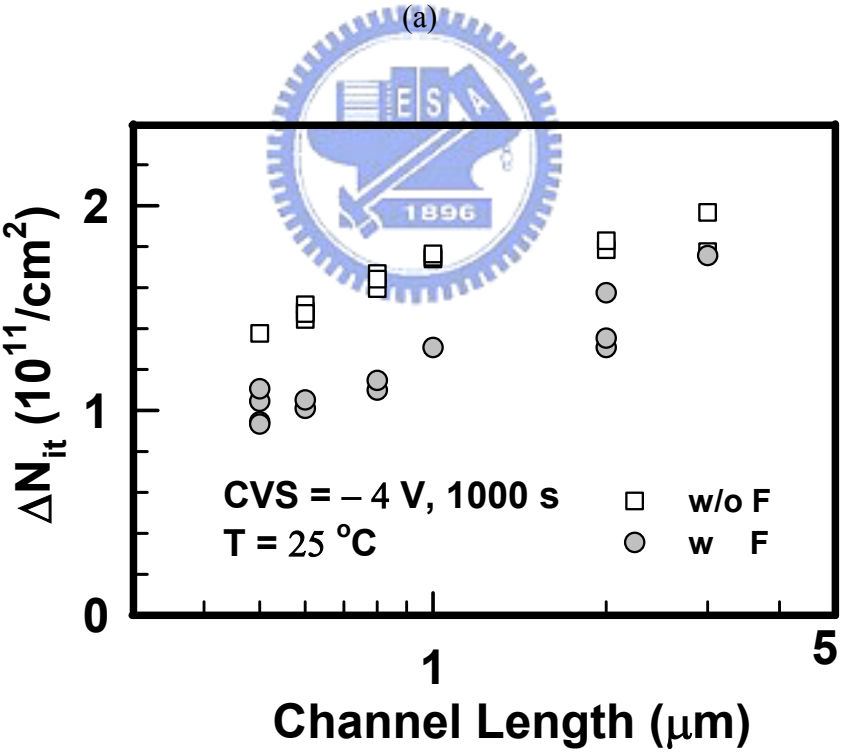


Fig. 6.20 Drain current degradation in a saturation regime of stress time, stressed at 25 °C, V_g = –3.5 V & –4 V.

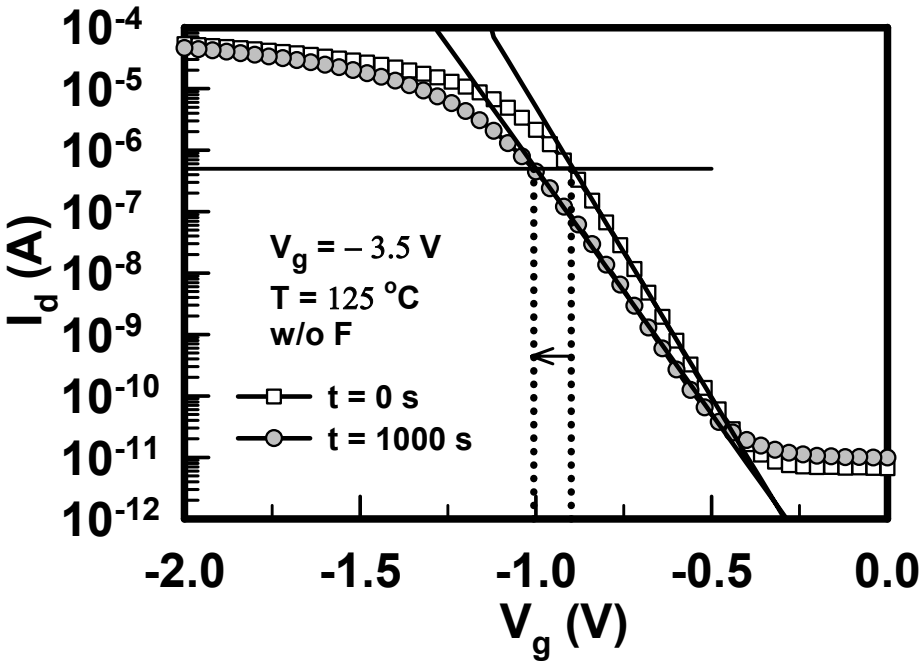


(a)

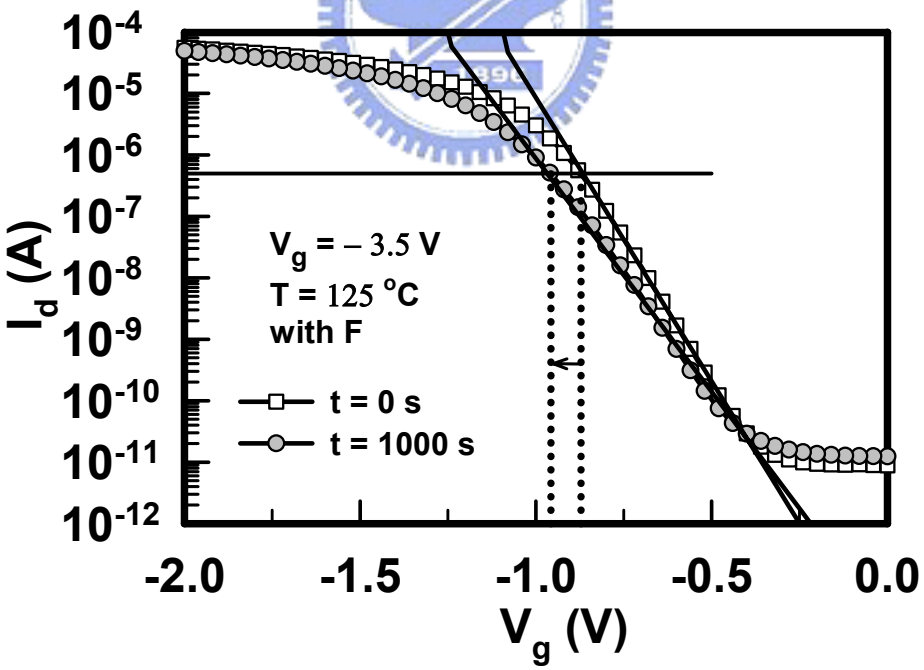


(b)

Fig. 6.21 Threshold voltage shift (b) Interface trap shift as a function of channel length, stressed at 25 °C, V_g =–4 V.

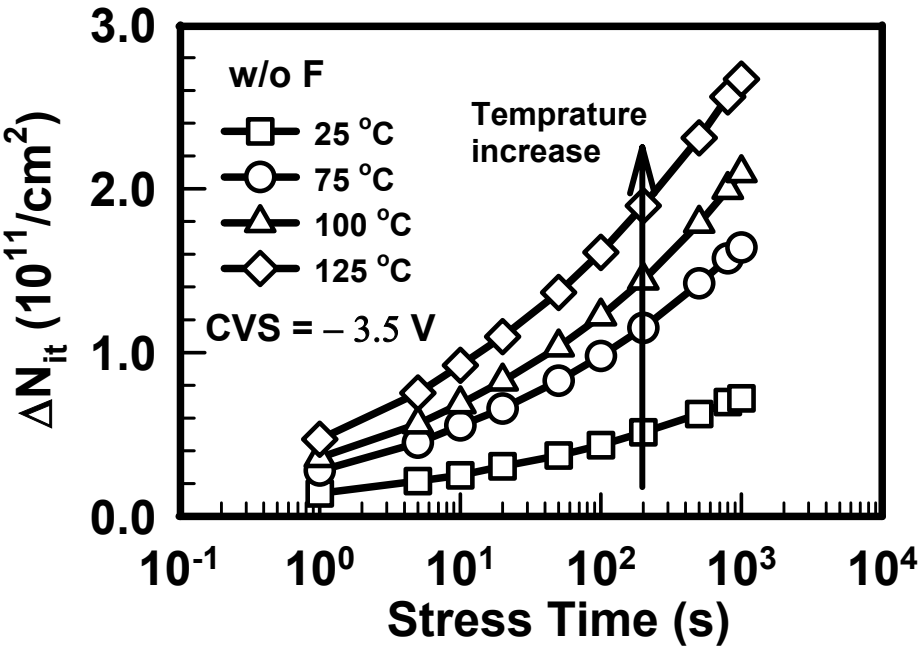


(a)

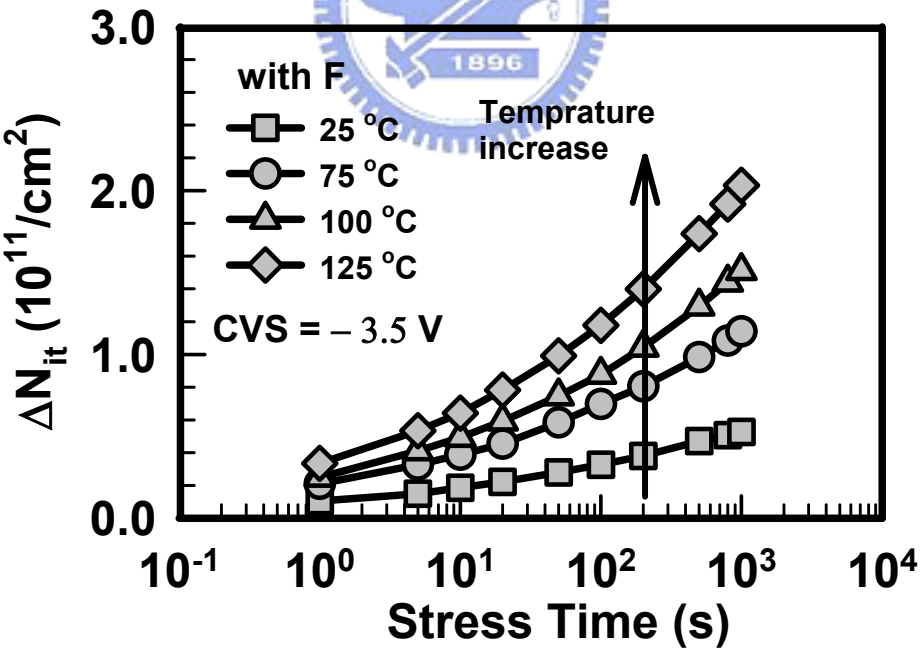


(b)

Fig. 6.22 I_d-V_g characteristics for p^+-gate pMOSFETs before stress and after stress 1000 s at 125 °C (a) w/o F sample (b) with F sample.

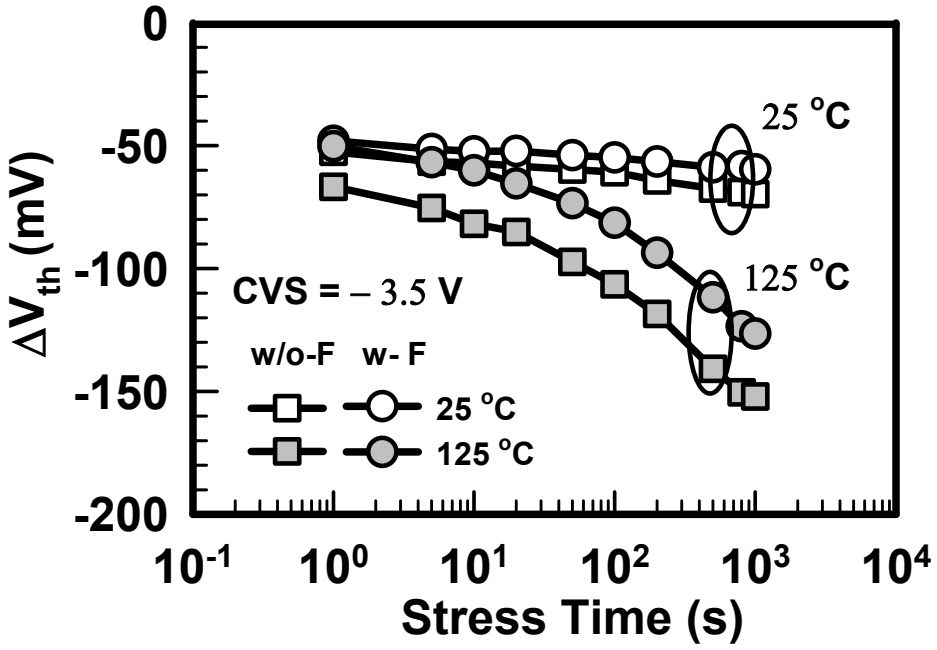


(a)

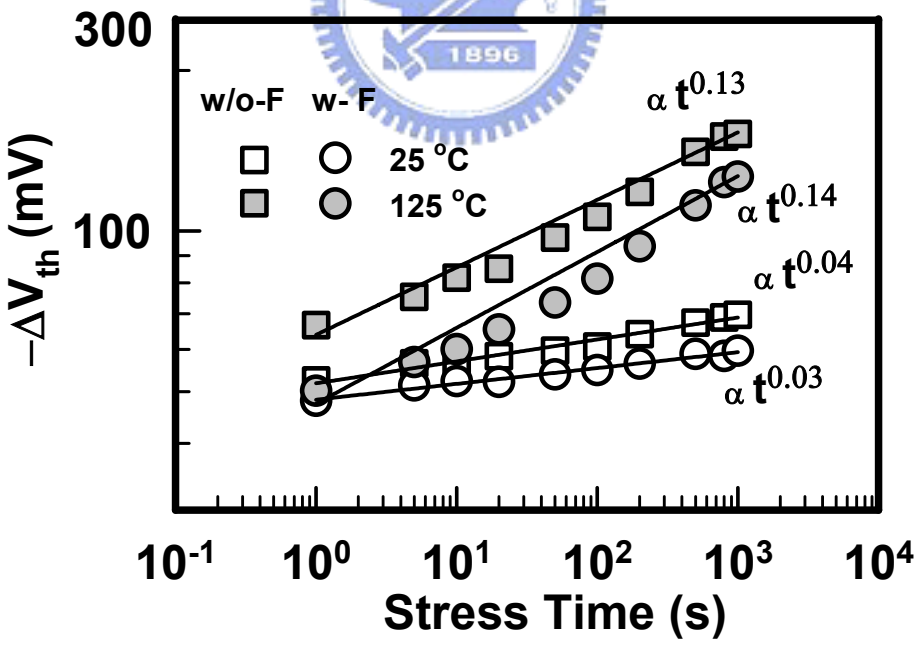


(b)

Fig. 6.23 Interface trap shift as a function of stress time under BTS at different stress temperature, V_g =–3.5 V (a) w/o F sample (b)with F sample.

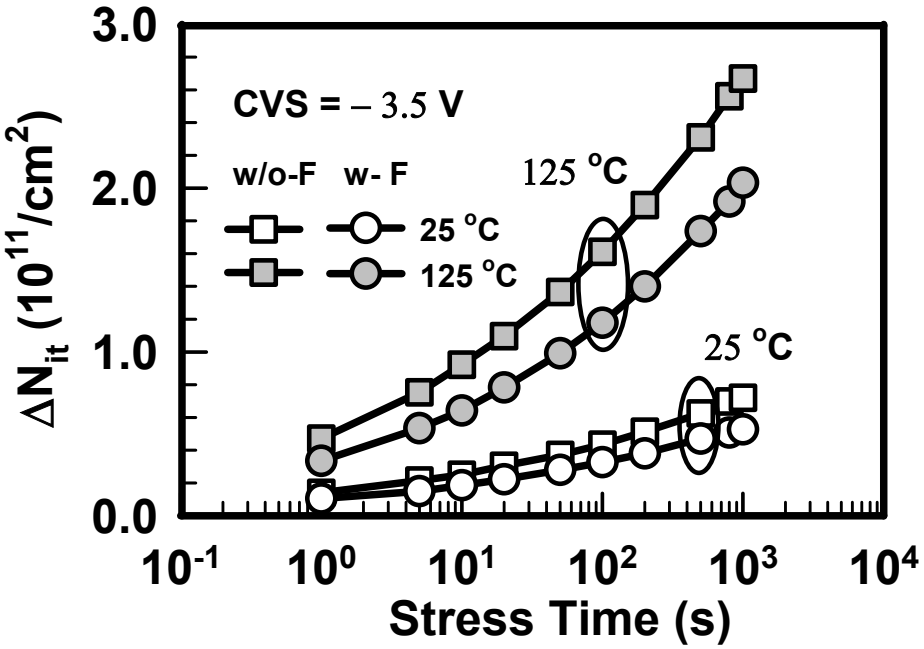


(a)

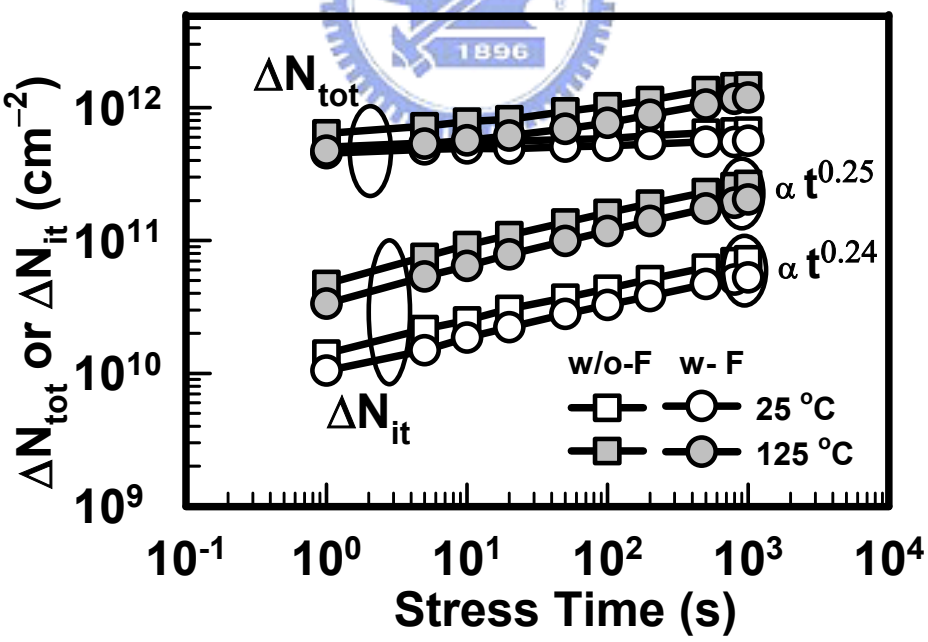


(b)

Fig. 6.24 Threshold voltage shift as a function of stress time under BTS at different stress temperature, V_g = –3.5 V (a) linear scale (b) logarithm scale.



(a)



(b)

Fig. 6.25 Interface trap shift and (b) total trap shift as a function of stress time under BTS at different stress temperature, V_g = –3.5 V.

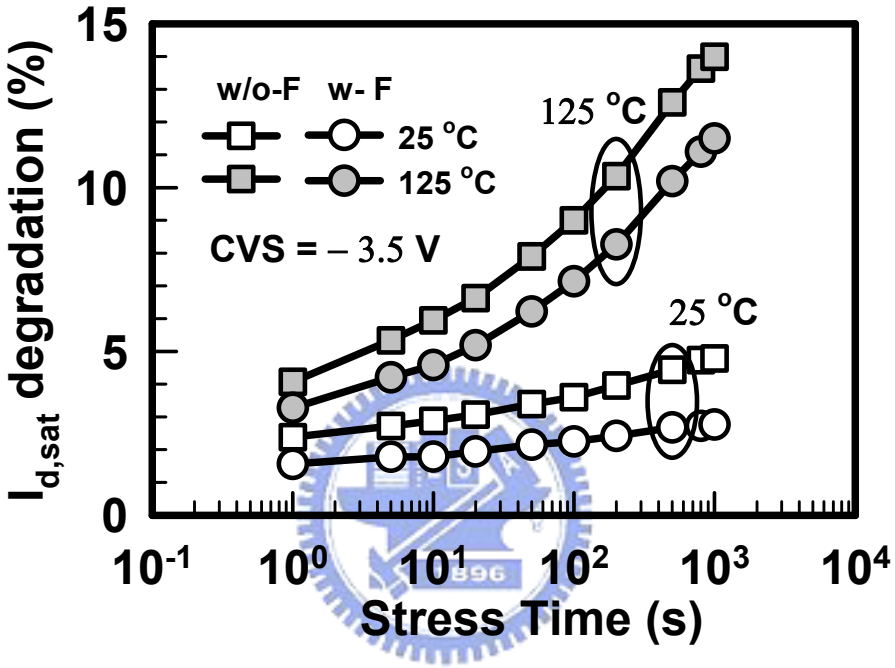
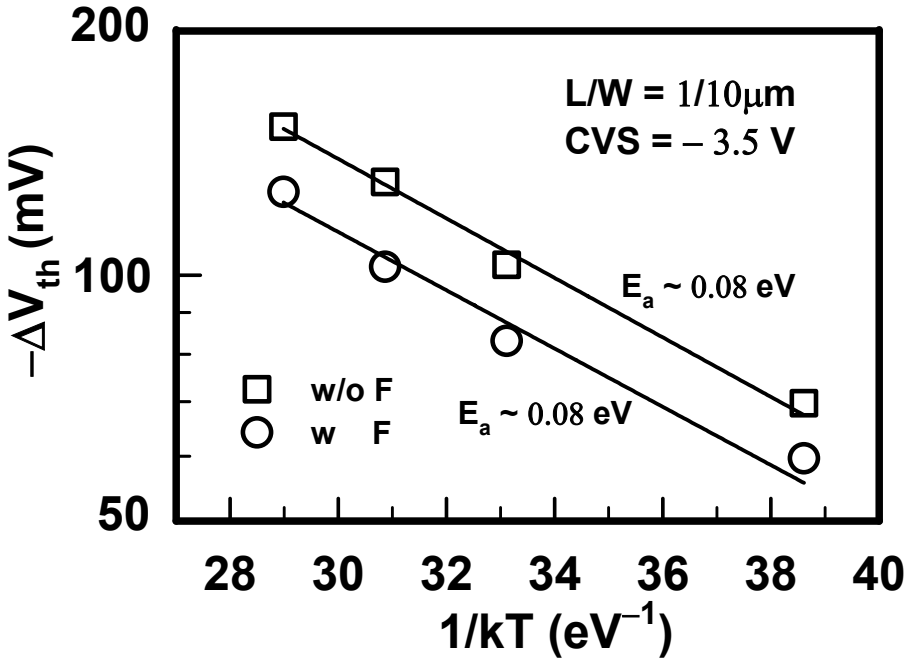
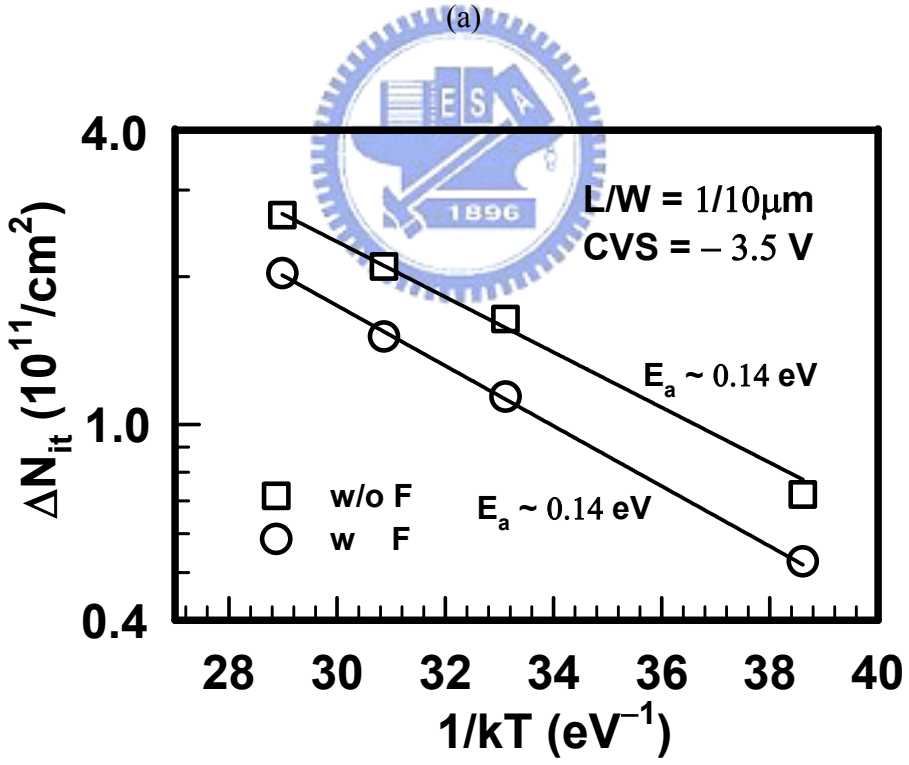


Fig. 6.26 Drain current degradation in a saturation regime of stress time, stressed at different stress temperature, V_g = –3.5 V.



(a)



(b)

Fig. 6.27 Temperature dependence of both (a) $\triangle V_{th}$ (b) $\triangle N_{it}$. NBT stress was applied under V_g = –3.5 V.

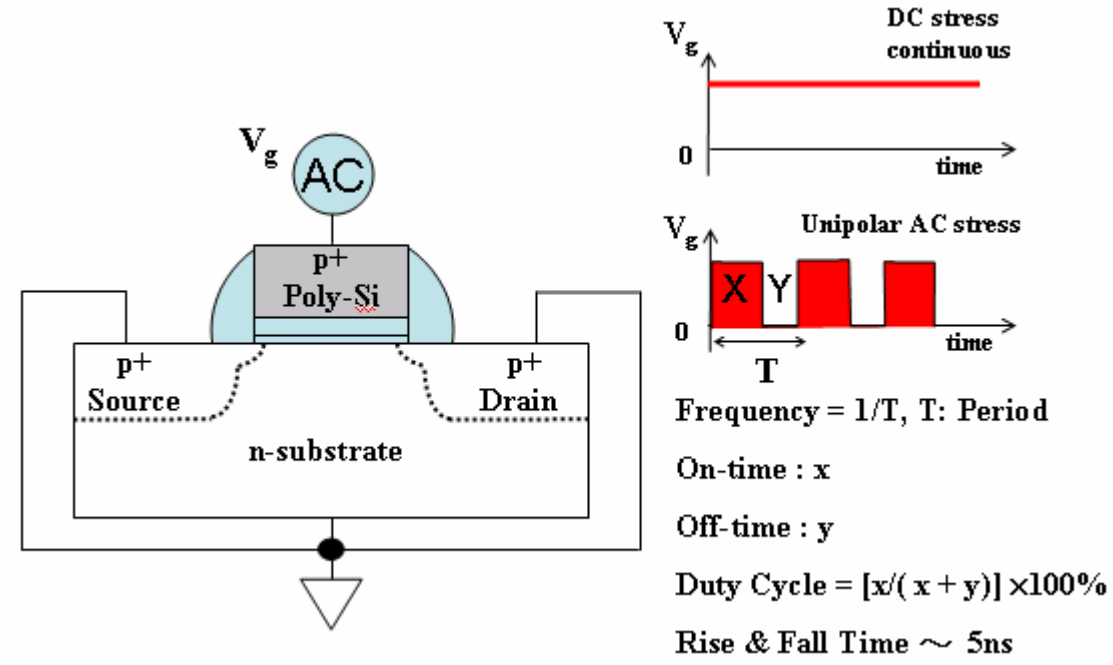
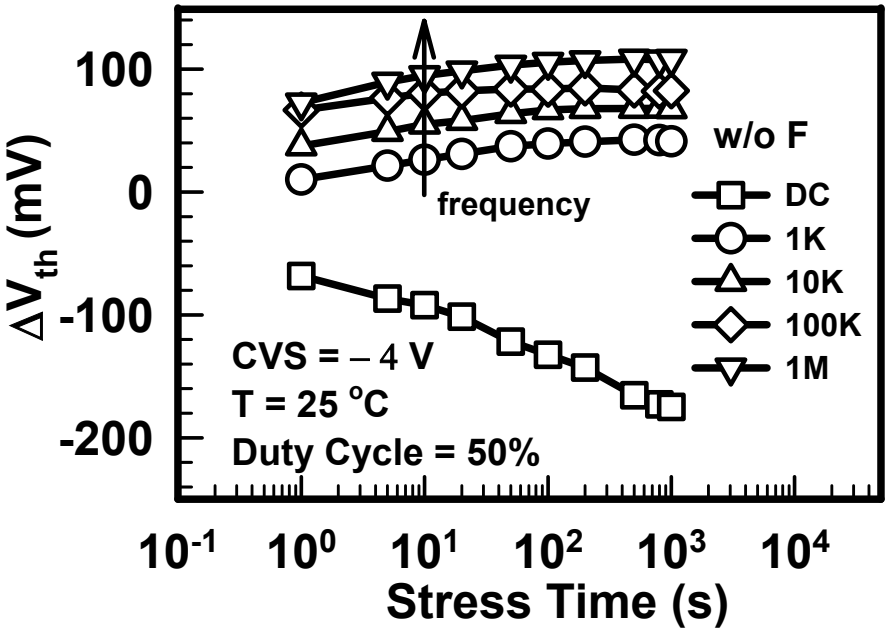
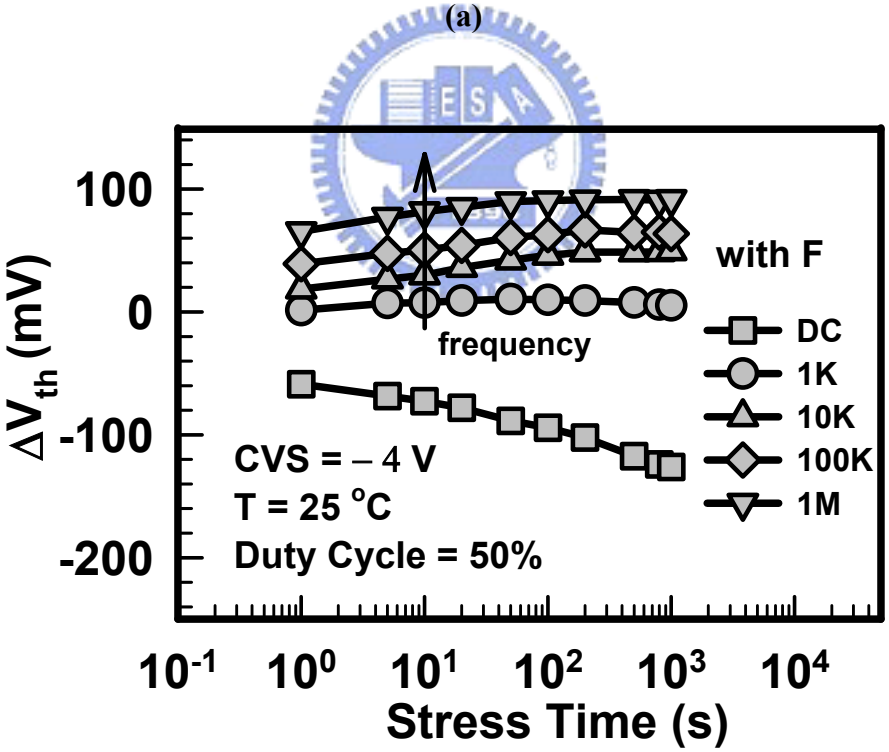


Fig. 6.28 Schematic setup and several parameters for measuring threshold voltage instability under AC dynamic stress.

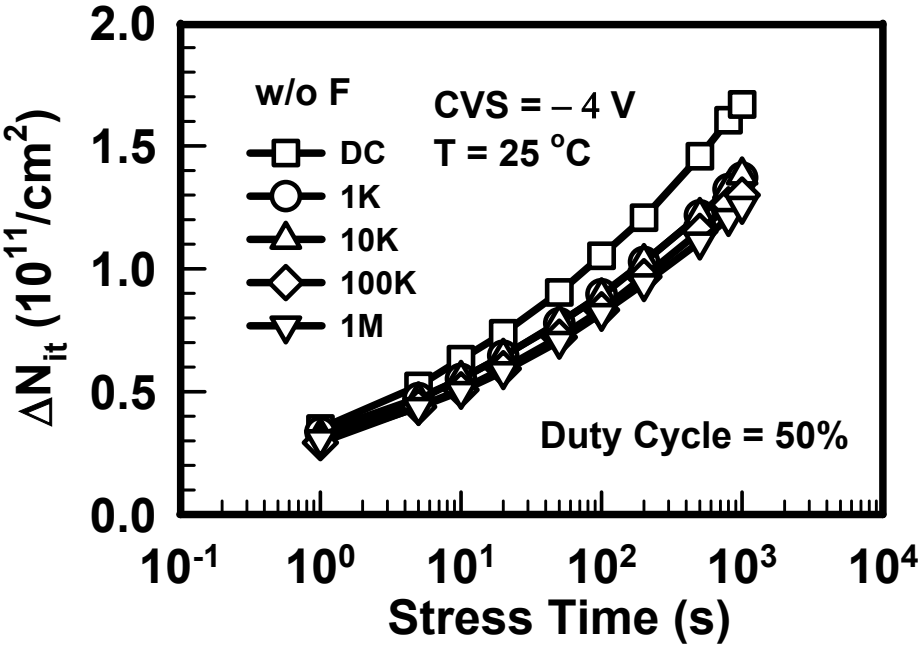


(a)

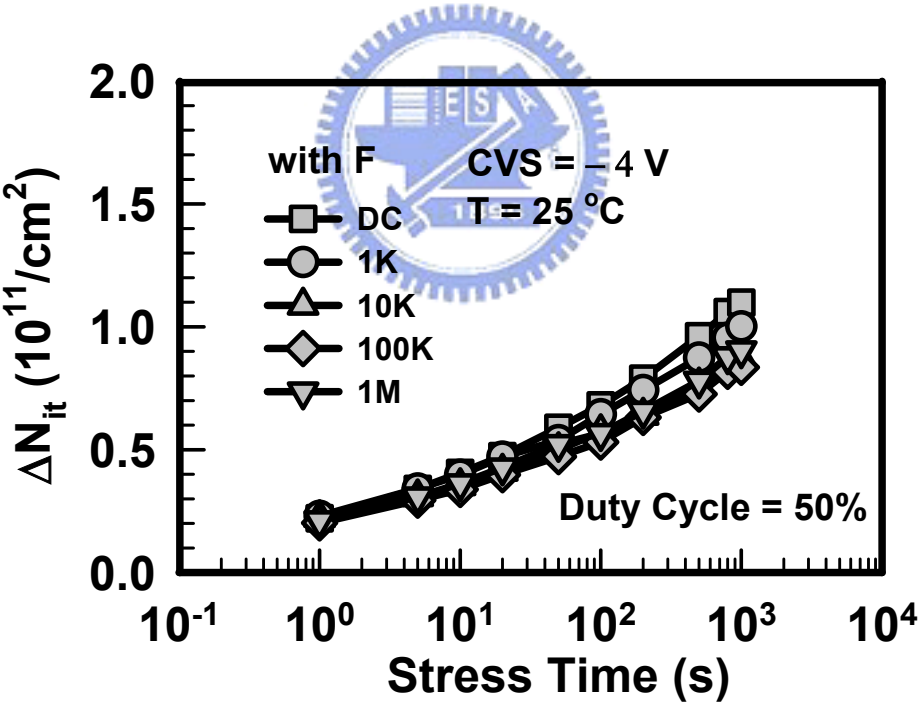


(b)

Fig. 6.29 V_{th} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different frequency (a) w/o F sample (b) with F sample.

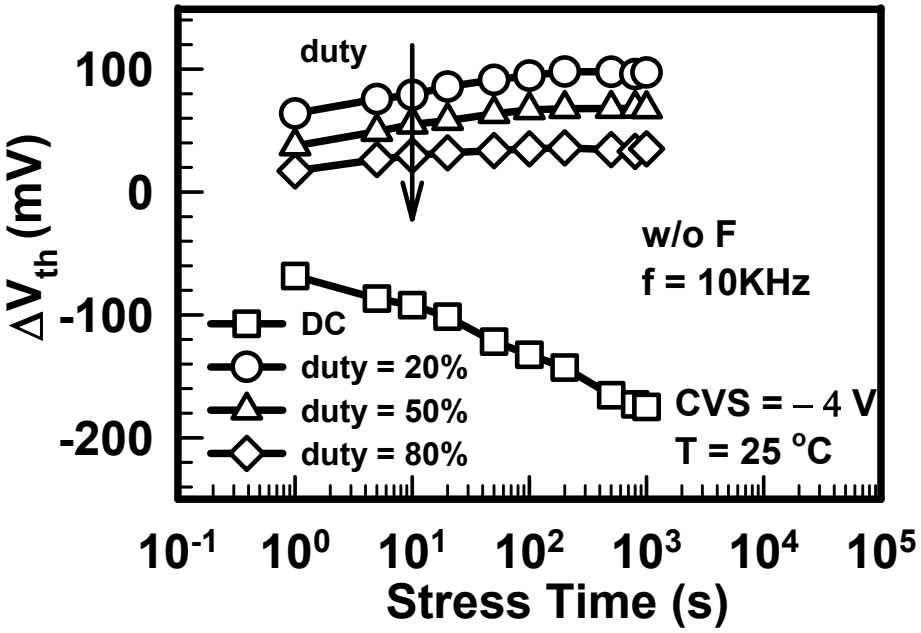


(a)

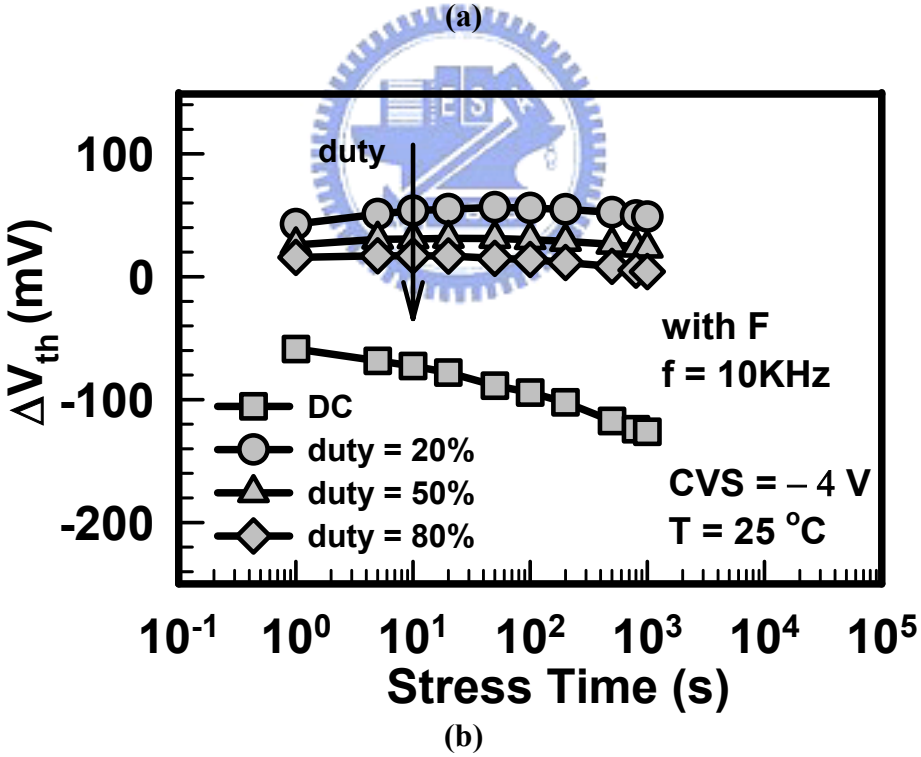


(b)

Fig. 6.30 N_{it} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different frequency (a) w/o F sample (b) with F sample.

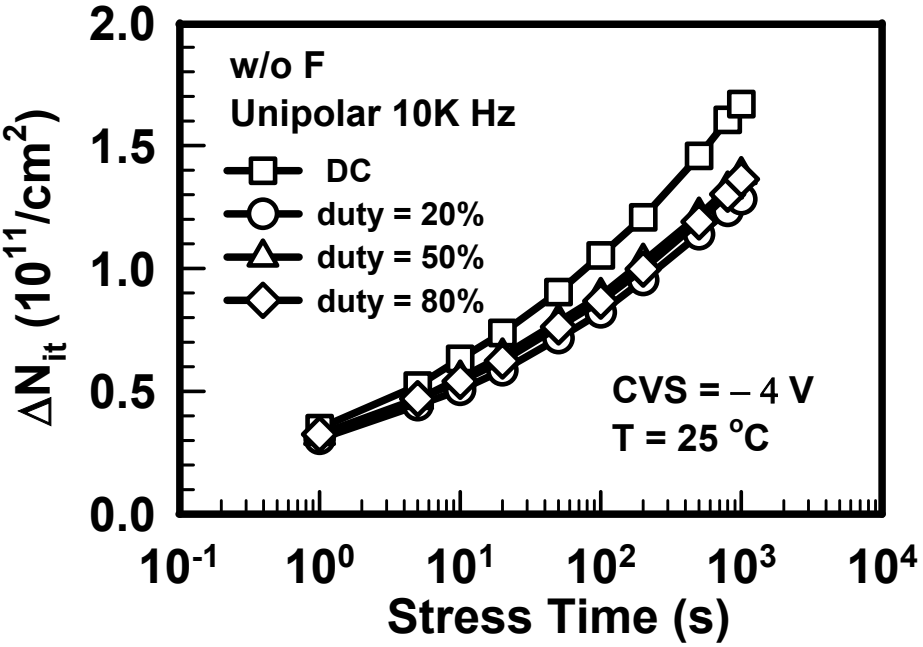


(a)

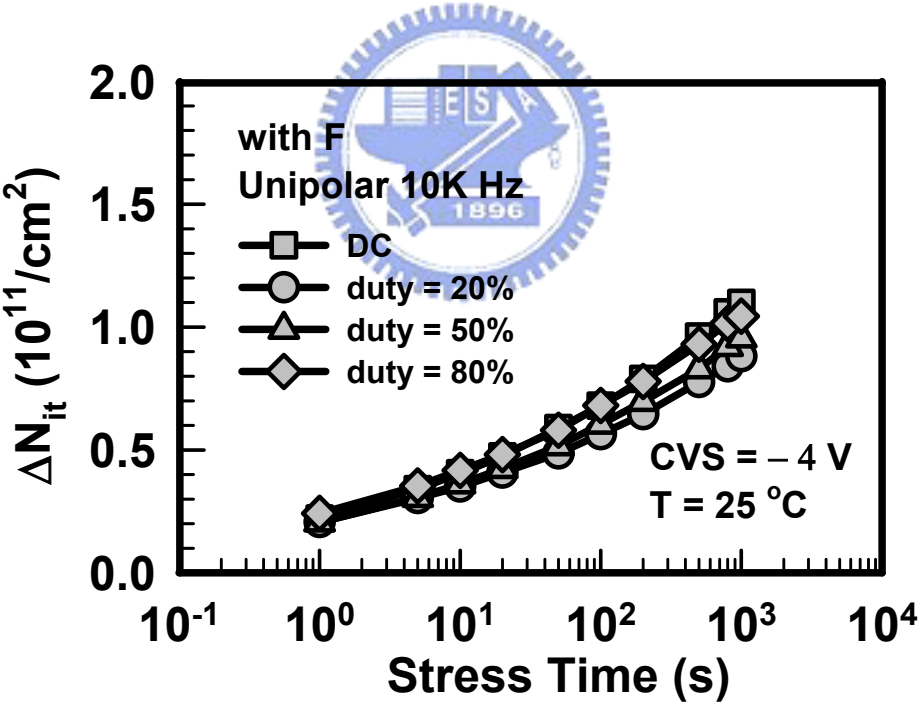


(b)

Fig. 6.31 V_{th} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different duty cycle (a) w/o F sample (b) with F sample.

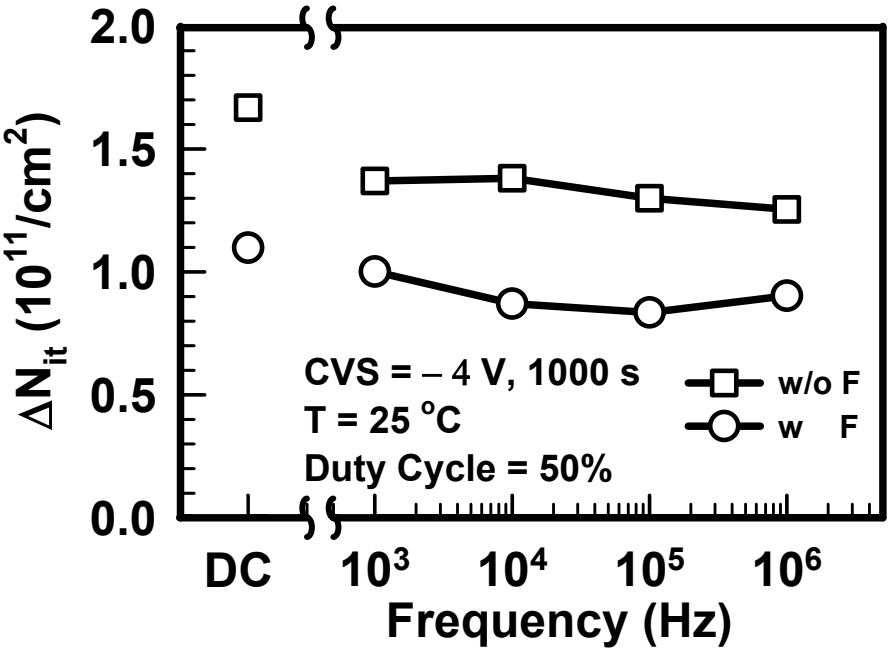


(a)

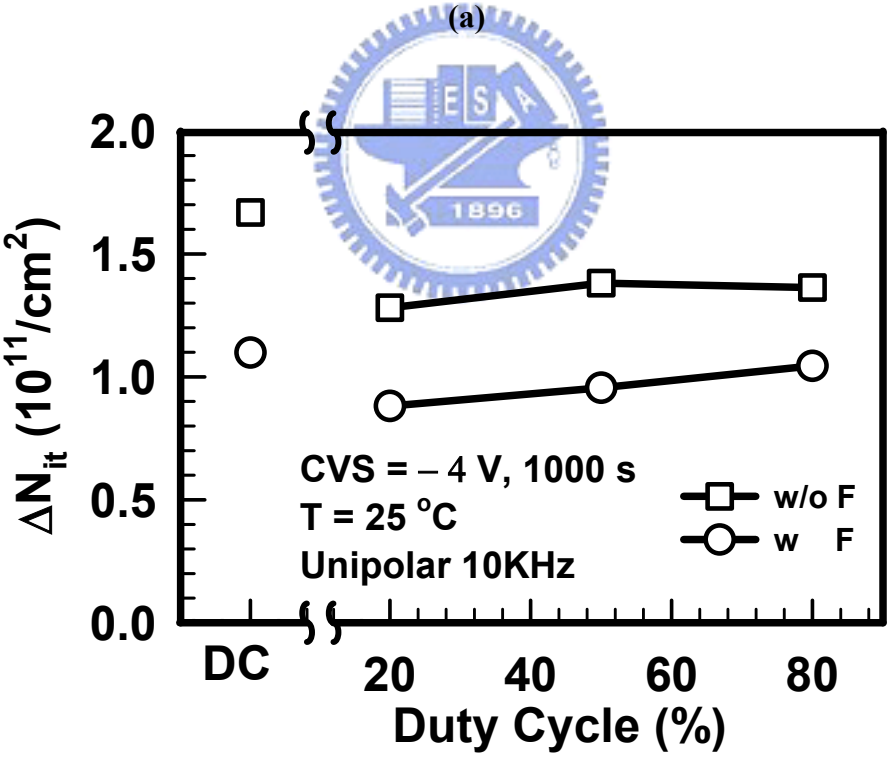


(b)

Fig. 6.32 N_{it} shift time evolution for pMOSFETs with HfO_2/SiON gate stack, under static and dynamic stresses of different duty cycle (a) w/o F sample (b) with F sample.

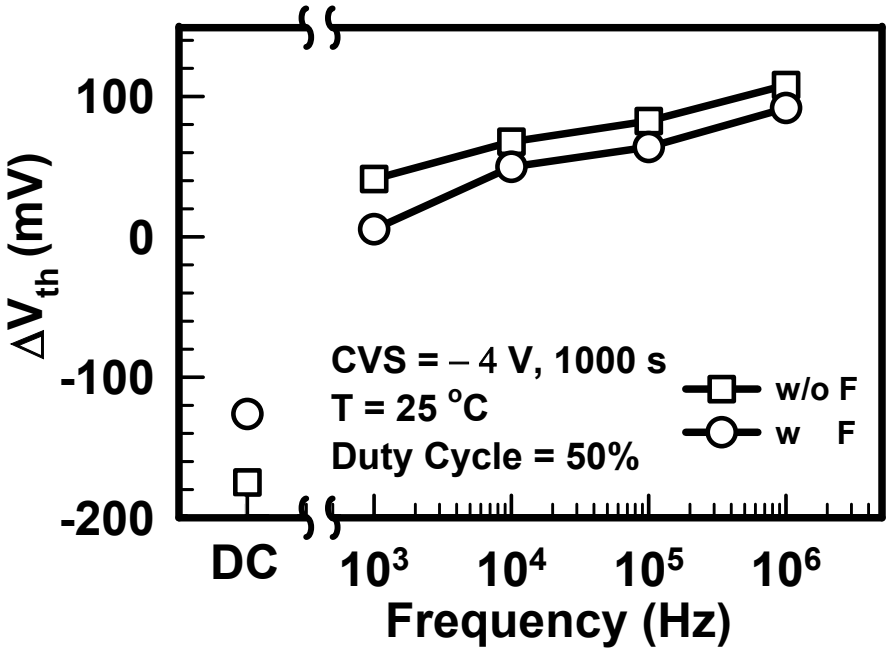


(a)

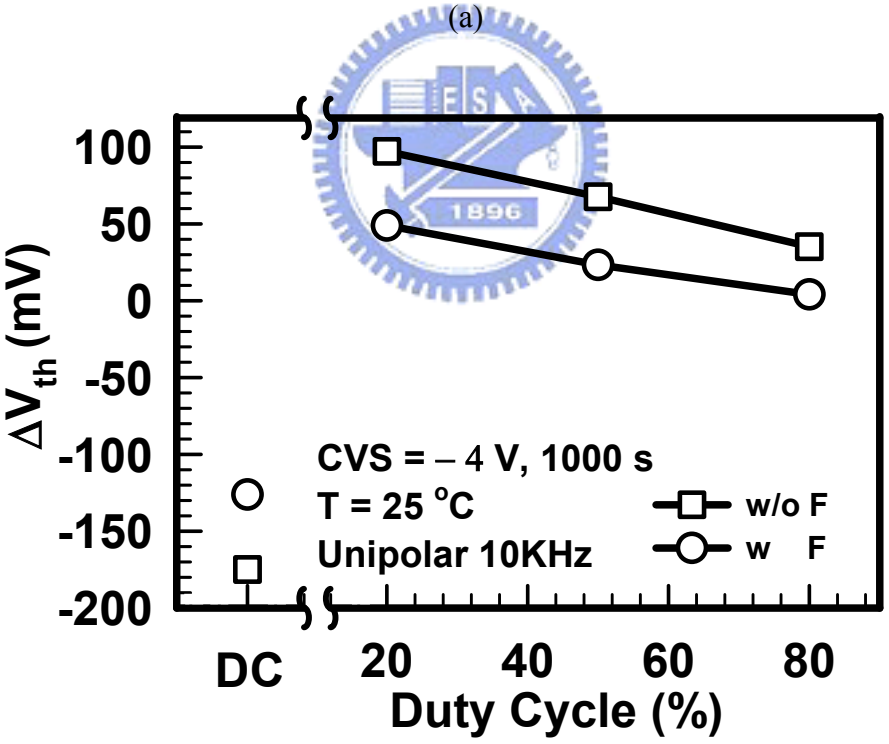


(b)

Fig. 6.33 (a) Frequency dependence of $\triangle N_{it}$, stressed at 25 °C, $V_g = -4$ V under duty cycle = 50% (b) Duty Cycle dependence of $\triangle N_{it}$, stressed at 25 °C, $V_g = -4$ V under unipolar 10KHz.



(a)



(b)

Fig. 6.34 Frequency dependence of $\triangle V_{th}$, stressed at 25 °C, V_g = –4 V under duty cycle = 50% (b) Duty Cycle dependence of $\triangle V_{th}$, stressed at 25 °C, V_g = –4 V under unipolar 10KHz.

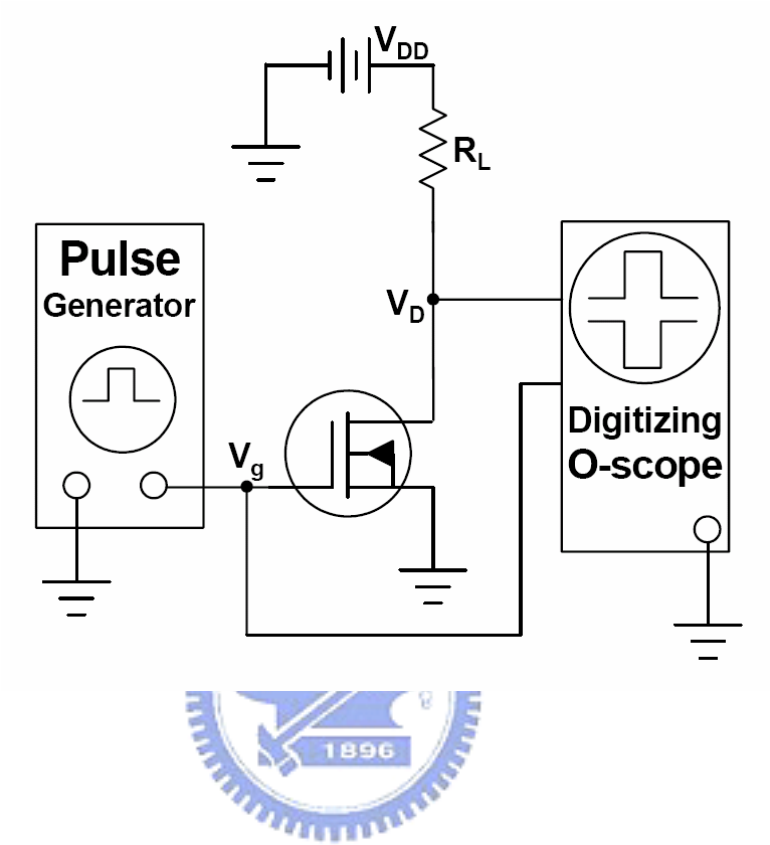


Fig. 6.35. The transistor is used in an inverter circuit with the gate receiving a single pulse from the pulse generator. The voltage is measured at the transistor drain and converted to drain current because the load resistance value is known.

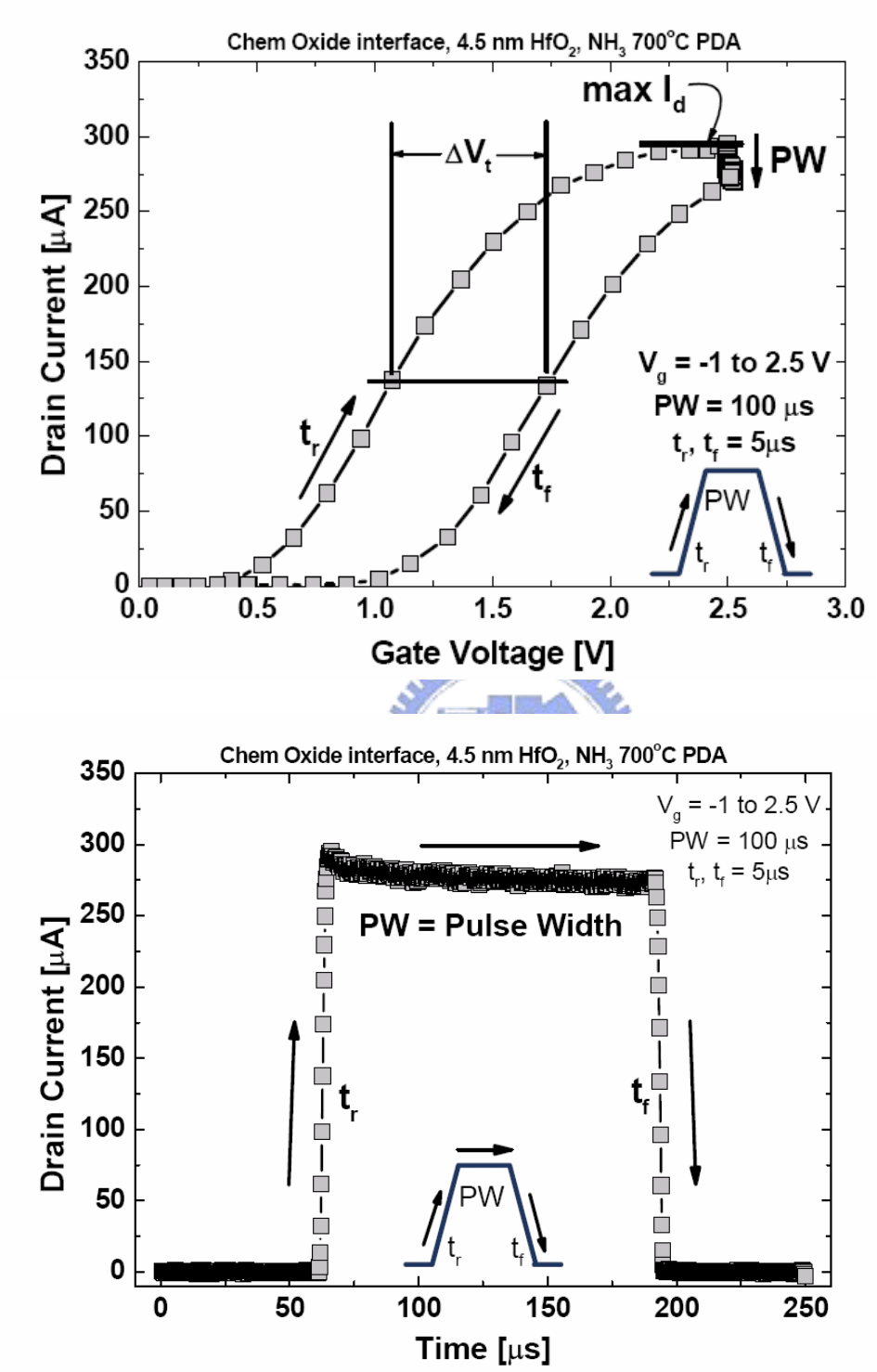


Fig. 6.36 (a) Example data of the pulsed I_d-V_g where ΔV_t is measured at 50% of the maximum I_d on a W/L = 10/1 μm transistor. (b) Example data of the pulsed I_d versus time on a W/L = 10/1 μm transistor where the 'droop' at the top is associated with the drop of pulsed I_d-V_g at V_g = 2.5 V.

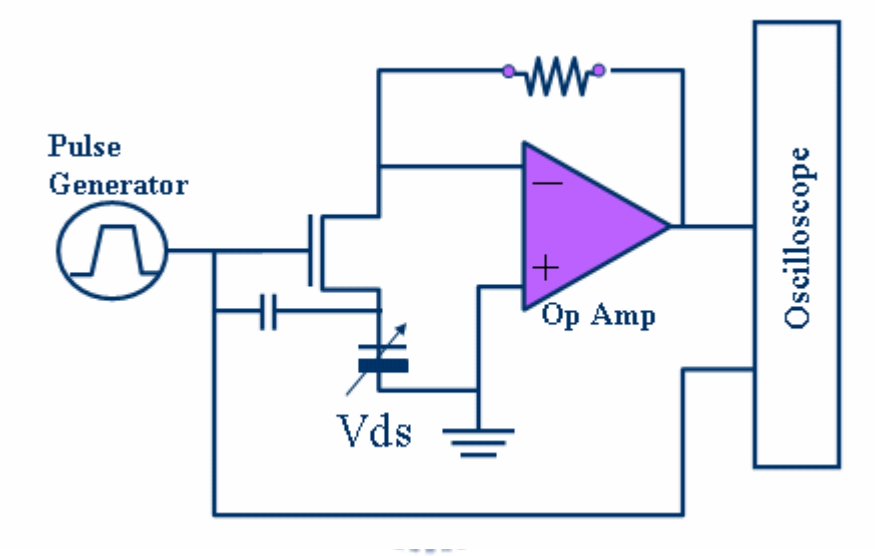


Fig. 6.37 A new single pulsed I_d-V_g method to improve the noises and parasitic capacitance of conventional method (Fig. 6.35).

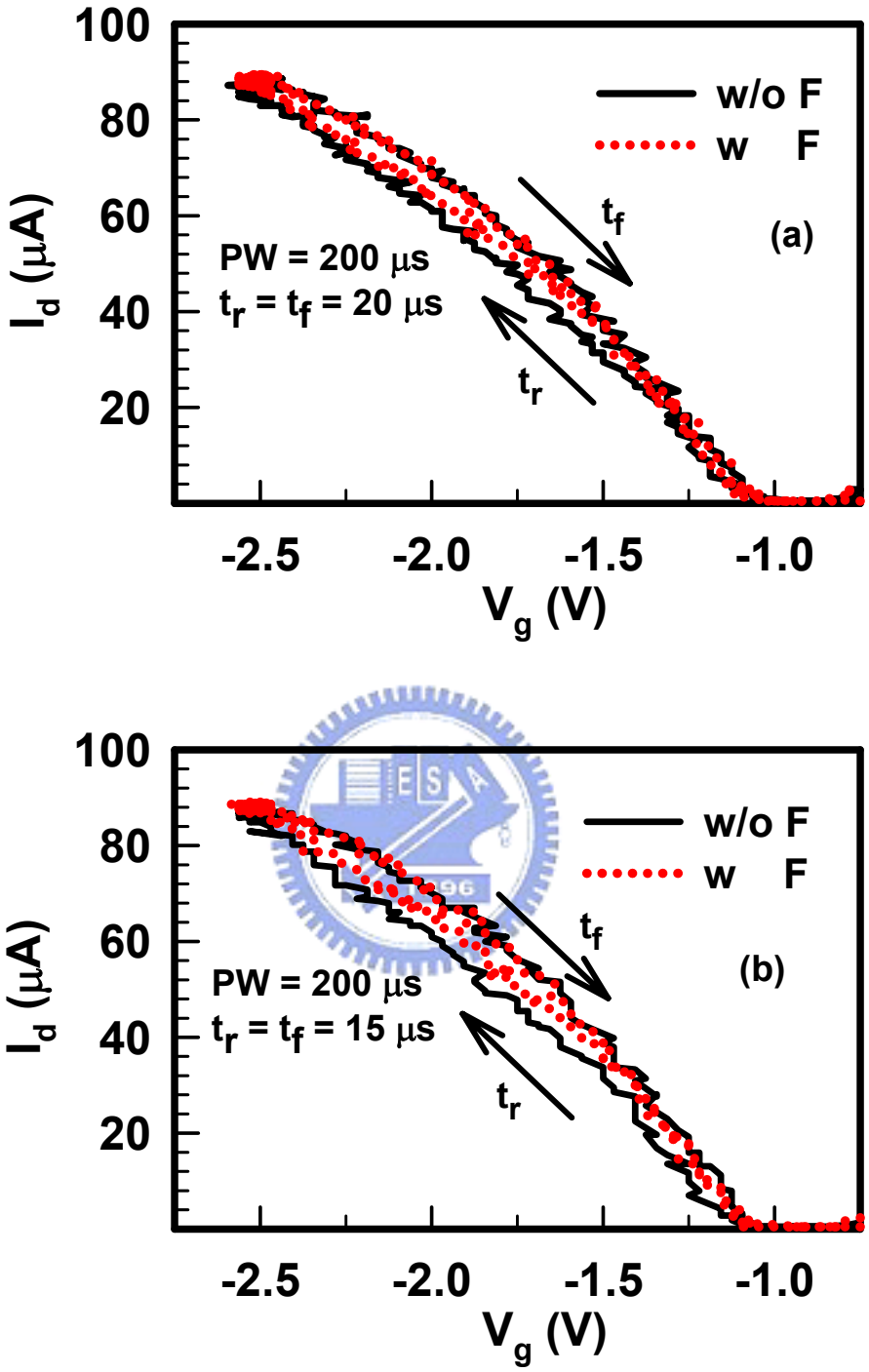


Fig. 6.38 "Single Pulse I_d-V_g characteristics for different rising and falling time of (a) 20 μs (b) 15 μs (c) 6 μs illustrating increased trapping (Vt shift) with increased rising and falling time for pMOS. The included pMOS DC ramp I_d-V_g result demonstrates the effect of hole charge trapping during the slower measurement, except electron trapping.

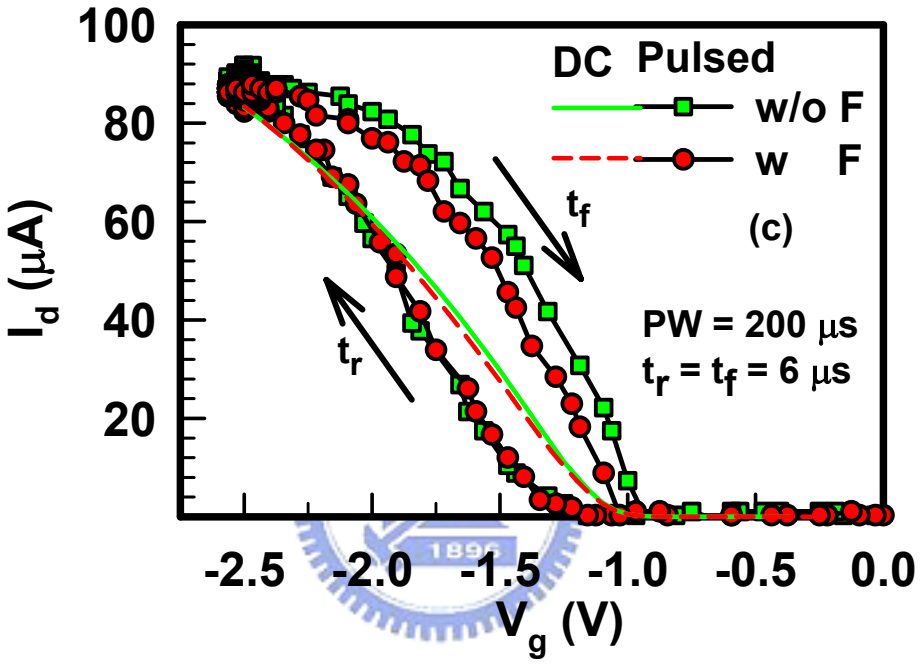


Fig.6.38 "Single Pulse" I_d-V_g characteristics for different rising and falling time of (a) 20 μs (b) 15 μs (c) 6 μs illustrating increased trapping (V_t shift) with increased rising and falling time for pMOS. The included pMOS DC ramp I_d-V_g result demonstrates the effect of hole charge trapping during the slower measurement, except electron trapping.