Chapter 7
Improved Immunity against Plasma Charging Damage of pMOSFETs with HfO_2/SiON Gate Stack by Fluorine Incorporation

7. 1 Introduction

Plasma processes have been known to cause gate oxide and MOSFET degradations. Many plasma processing steps, such as poly-silicon etching for transistor gate length definition [1]-[2], metal etching [3], and photo-resist ashing [4] are indispensable for wafer fabrication. With the scaling of the transistor gate length and gate oxide thickness, the gate edge damage and gate oxide damage could both become more serious by the poly-silicon etching. Meanwhile, it has been shown that metal etching and its subsequent resist ashing could induce serious plasma charging damages. With the fabrication of multi-level metal interconnect in ULSI circuits, repetitive exposures to plasma processes are unavoidable. Consequently, better understanding of plasma damage is essential to achieve highly reliable ULSI circuits.

To detect plasma process-induced damage (P^2ID), a typical test structure is a small area capacitor or transistor connected to a conductive antenna receiver. Metal antenna structures attached to the gate electrode with various antenna area ratios (AAR) are used to monitor the plasma charging damage. In conventional pMOSFETs with SiO_2 gate, severe charging damage could occur at the center, due to the

non-uniform plasma generation caused by the gas injection mode of the asher.

In this chapter, HfO_2/SiON pMOSFETs with antenna structures are employed as the test devices. We also study the effects of fluorine incorporation on plasma charging damage. The HfO_2/SiON gate stack degradation due to the charging damage can be evaluated using constant voltage stress (CVS) and bias-temperature stress (BTS). Furthermore, more detailed information, such as the effects of antenna size, charging polarity and the device location on the wafer, is carefully examined. We for the first time demonstrate that F incorporation into HfO_2/SiON gate stack could strengthen the immunity against plasma charging damage [5].

7.2 Results and Discussions

7. 2.1 Plasma Charging Damage in Control and Fluorine Incorporated Samples

PMOS transistors with p^+ poly-Si gate were fabricated on 6-inch wafers. Metal antennas with various antenna ratios (AAR) were attached to the gate. The AAR is defined as the area ratio between the metal pad and the active device region. Schematic of a transistor with area antenna is shown in **Fig. 7.1**.

In our processing, after metal patterning, the remaining photo-resist layer was stripped off with O_2 plasma in a down-stream plasma asher, whose configuration and plasma potential can be found in [6]. CHARM-2 wafer sensor was used to detect the potential distribution in the chamber. Highly negative and positive potential values were detected at the wafer center and edge, as shown in **Fig. 7.2** (a) and **Fig. 7.2** (b), respectively.

Fig. 7.3 (a) and **Fig. 7.3** (b) compare the interface state density of the devices

with and without F incorporation for various AAR ratios as a function of device location on the wafer before and after H_2 sintering. The interface-state density of the antenna devices was also analyzed using the charge pumping technique. The value of N_{it} for all samples after receiving H_2 sintering shows an order magnitude lower than that before receiving H_2 sintering. This indicates that H_2 sintering can effectively electrically passivate the interface states, generated during as-fabricated processing. The value of N_{it} for the control devices with AAR of 60K is found to be the largest even after H_2 sintering, and the F incorporation can significantly suppress the interface state generation during plasma processing.

Fig. 7.4 (a) and **Fig. 7.4** (b) show the threshold voltage of the devices with and without F incorporation for various AAR ratios as function of device location on the wafer before and after H_2 sintering. It is interesting to find that the $|V_{th}|$ values for the control devices with AAR of 60K are the largest, irrespective of H_2 sintering. This indicates that hole traps generation occurs during plasma processing. In addition, the most serious case occurs at wafer center, suggesting that more severe hole traps generation is taking place at the wafer center. This result is consistent with that in the experiment of negative CVS stress bias, i.e., the higher negative stress voltage, the more hole traps are created. Moreover, we can observe that fluorine also can passivate the hole generation in addition to interface state generation. It is worthy to note that both $|V_{th}|$ and N_{it} of the samples with and without F incorporation are reduced after H_2 sintering. This implies that H_2 forming gas anneal effectively improves MOSFET characteristics. These can be attributed to improved interface quality and reduced bulk trap in HfO_2 film by H atoms.

Fig. 7.5 (a) and **Fig. 7.5** (b) display the cumulative probability of the threshold voltage (V_{th}) and interface trap density (N_{it}) for the fabricated devices with and

without F incorporation for various AAR ratios around the wafer central region. Remarkably, the control devices with AAR of 60K depict larger $|V_{th}|$ and N_{it} values than their counterpart with F incorporation. Plasma charging damage would cause more positive charge trapping in HfO_2 film, and more interface state density would result in larger $|V_{th}|$.

Output characteristics for the fresh devices with AAR of 1K and 60K located at the wafer central region, both with and without F incorporation, are shown in **Fig. 7.6**. It is interesting to find that the drain current in the fresh devices is smaller for the control device with AAR of 60K. This is ascribed to a higher $|V_{th}|$ for the fresh devices with a larger antenna, implying that more hole trapping events occur after plasma processing. This result is different from the case of traditional PMOS transistor with SiO_2 gate oxide, in which the device with a larger antenna has a lower $|V_{th}|$, i.e., more electron trapping events occur during plasma processing. Moreover, all these results indicate that the plasma antenna charging effect creates more hole traps in the HfO_2/SiON gate stack, and F incorporation can significantly reduce the impact of plasma charging effect.

7. 2. 2 Effects of Plasma Charging Damage on NBTI

Figs. 7.7 (a) and (b) show the time evolution of the threshold voltage shift at 25°C for the devices with area antenna ratios (AAR) of either 1K or 60K, both with and without F incorporation, in linear scale and logarithm scale, respectively. All selected devices come from the same die location on the wafer center. It should be noted that in **Fig. 7.7** (a), V_{th} shift is larger for the control devices with AAR of 60K, indicating that negative (i.e., wafer center) plasma charging generates positive charges

in the bulk of HfO_2 film, consistent with the aforementioned results. **Fig. 7.7** (b) shows that V_{th} degradation obeys the power law, and the exponential values of all devices at V_g =−4 V (about 0.1~0.13) are similar. **Fig. 7.8** (a) and **Fig. 7.8** (b) compare $\triangle N_{tot}$ and $\triangle N_{it}$ as a function of time. It should be noted that $\triangle N_{tot}$ was calculated from $\triangle V_{th}$ assuming that the charge was trapped at the interface between the dielectric and the substrate. $\triangle N_{tot}$ is about 1.5～2 order larger than $\triangle N_{it}$ for all devices, indicating that charge trapping in the bulk trap dominates threshold voltage shift. Apparently, the F incorporation is shown to be effective in suppressing $\triangle N_{tot}$ and $\triangle N_{it}$ on the devices with large antenna. The reductions in drain current after CVS for the devices are shown and compared in **Fig. 7.9**. Due to a larger V_{th} shift caused by plasma charging effect, enhanced drain current degradation is observed for the control devices with AAR of 60K.

Fig. 7.10 shows threshold voltage shift as a function of stress time, stressed at 125 ^{o}C, V_g = –3.5 V. When the antenna size increases, NBTI worsens. The V_{th} shift is higher for the devices with large AAR (e.g., 60K). This indicates that the generation rates of interface states and the positive charge trapping during the NBTI stressing are degraded due to the plasma charging damages. It can be seen that F incorporated films exhibit NBTI improvement similar to fluorine-induced NBTI improvement in SiOF case [11-12]. The major degradation of NBTI is caused by the positive charge trapping in the films rather than the interface generation, suggesting that the positive charge trapping is not completely caused by the H^+ capturing. Therefore, except for positive charge caused by H species, a large amount of extra trapping centers is also present in the HfO_2/SiON gate stack. F atoms seem to effectively decorate these trapping centers, leading to less degradation. **Fig. 7.10** (b) shows that the exponential values (~0.18) of power law relationship between $\triangle V_{th}$ and stress time. Devices with

AAR of 60K at V_g = −3.5 V are much larger than the devices with AAR of 1K at V_g = −3.5 V (~0.1), both with and without F incorporation. This implies that the degradation could be more serious for the devices with higher AAR (i.e., 60K) during NBTI stressing. Such V_{th} shift observed in p-channel MOSFETs can be attributed to the enhanced positive charge build-up in the HfO_2 dielectric and an increase in interface state density, as shown in **Fig. 7.11** (a) and **Fig. 7.11** (b). In **Fig. 7.12**, pMOS high-k dielectrics also demonstrate higher sensitivity to the BTS when subjecting to the plasma charging damage with larger antenna.

Fig. 7.13 and **Fig. 7.14** show the temperature dependence of the N_{tot} and N_{it} generation for the devices with a large antenna (e.g., AAR = 60K) under CVS stress. A large degradation in all parameters is observed when stress temperature increases [7]-[10]. These results show that when temperature increases, the increase in the bulk trap generation is higher than that in interface state generation, resulting in more serious V_{th} shift degradation when plasma charging damage occurs. Bulk trap generation is the main degradation in HfO_2 high-k film, and is accelerated at high temperatures. More importantly, F-incorporated films do exhibit better NBTI improvement because hole traps can be electrically passivated.

The above results confirm that the NBTI of PMOS devices is severely degraded by plasma charging effect. The possible mechanism is that the enhanced hole trapping events caused by the plasma charging increase the generation of interface states and bulk traps. The hole trapping in the bulk, rather than the interface generation, is the dominant mechanism responsible for the degradation; while it can be significantly improved by the F incorporation.

7. 3 Summary

In this study, the effects of the plasma charging on pMOSFETs with HfO_2/SiON gate stack were comprehensively investigated. In addition, we have also investigated the influences of F incorporation on the reliability of high K films. Our results show that the integrity of high-k films would be degraded by the plasma charging damages, especially during NBTI stress at high temperature and with higher antenna area ratio. As a result, the devices with large antenna depict degraded V_{th}, N_{it} and I_d. The enhanced degradations are believed to occur during photo-resist stripping step. The build-up of positive trapped charges in the high-k dielectrics is the primary cause for aggravated NBTI, rather than interface states generation.

Finally, we have also proposed that the CVS and NBTI characterization could be cleverly employed as a sensitive method for characterizing the antenna effects in the devices with HfO_2/SiON gate stack. Both CVS and NBTI on pMOSFETs antenna-structures with HfO_2/SiON gate stack are also found to be primarily due to charge trap generation in the bulk of HfO_2 ($\triangle N_{ot}$), instead of at the interface ($\triangle N_{it}$). For the first time, we demonstrated that plasma charging effect induces hole trapping in the HfO_2/SiON gate stack; while it can be effectively suppressed with F incorporation. In other words, F incorporation can reduce hole traps in HfO_2 high-k film.

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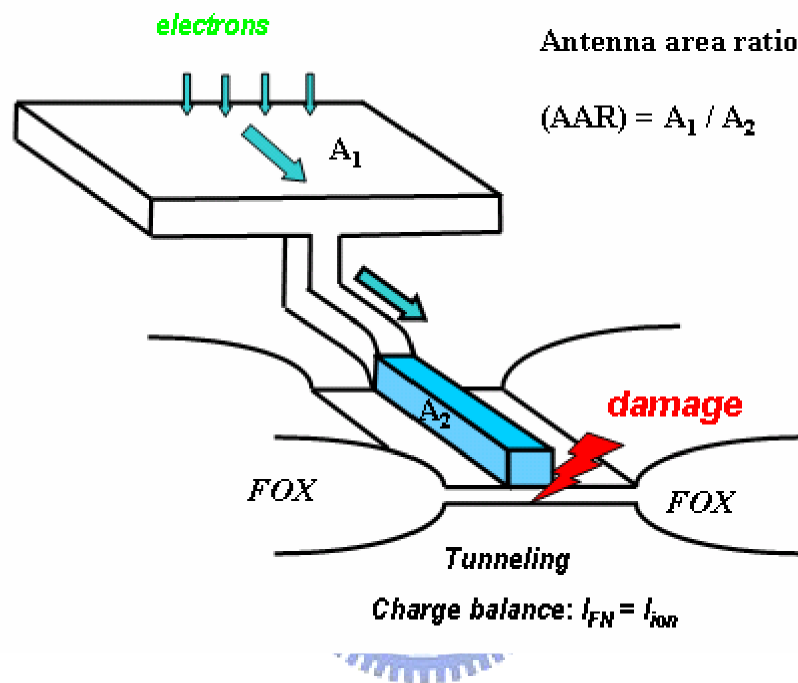
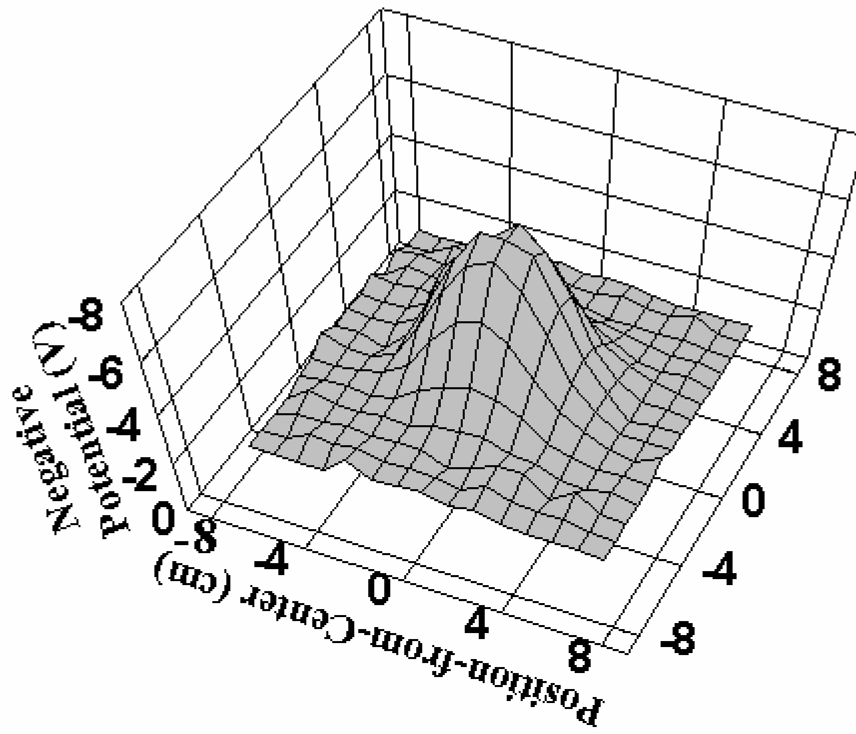


Fig. 7.1 The schematic of metal antenna transistor and definition of Antenna Area Ratio (AAR).



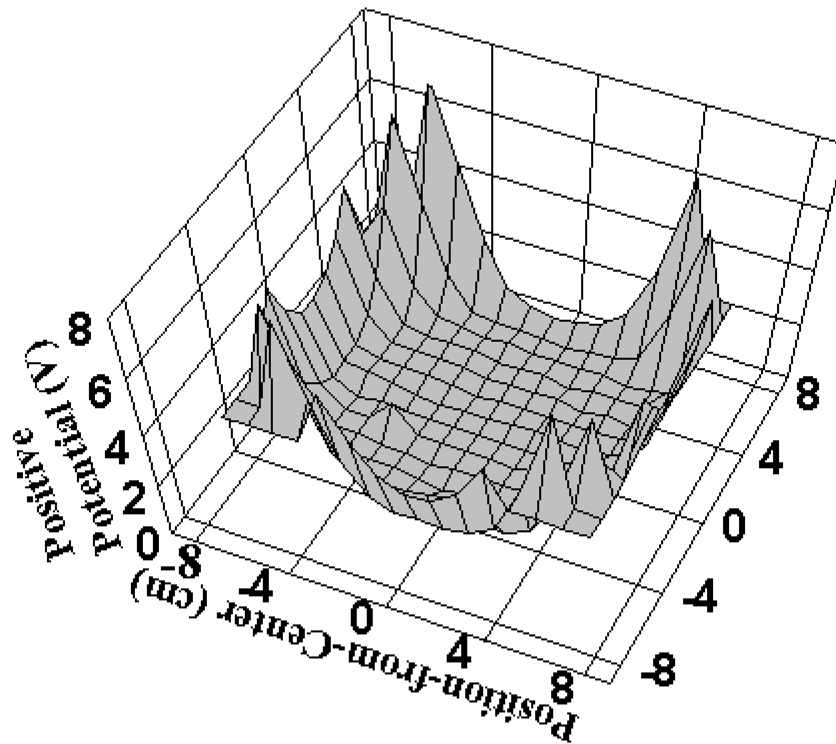


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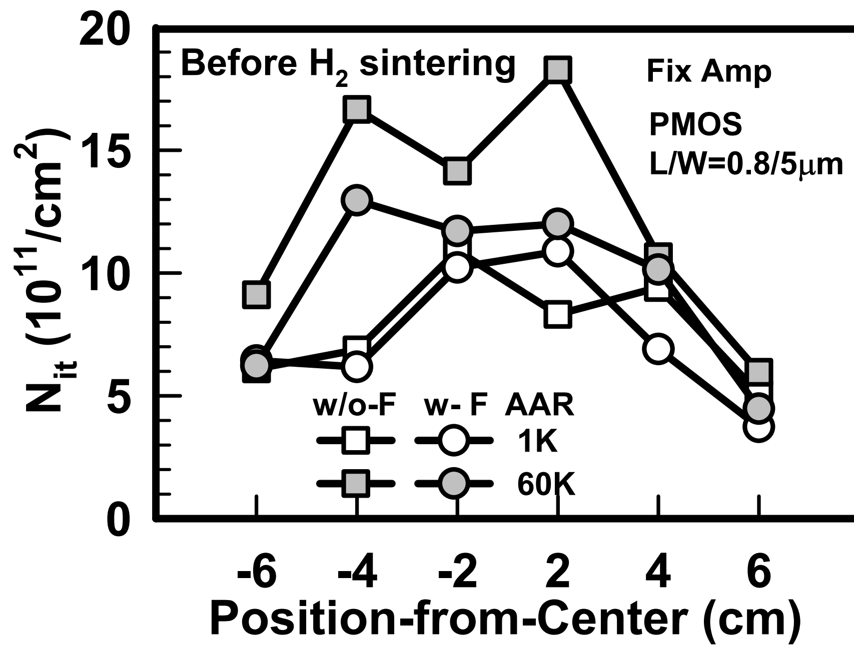
Fig. 7.2 Wafer maps of (a) negative and (b) positive potential values recorded by CHARM-2 sensors.



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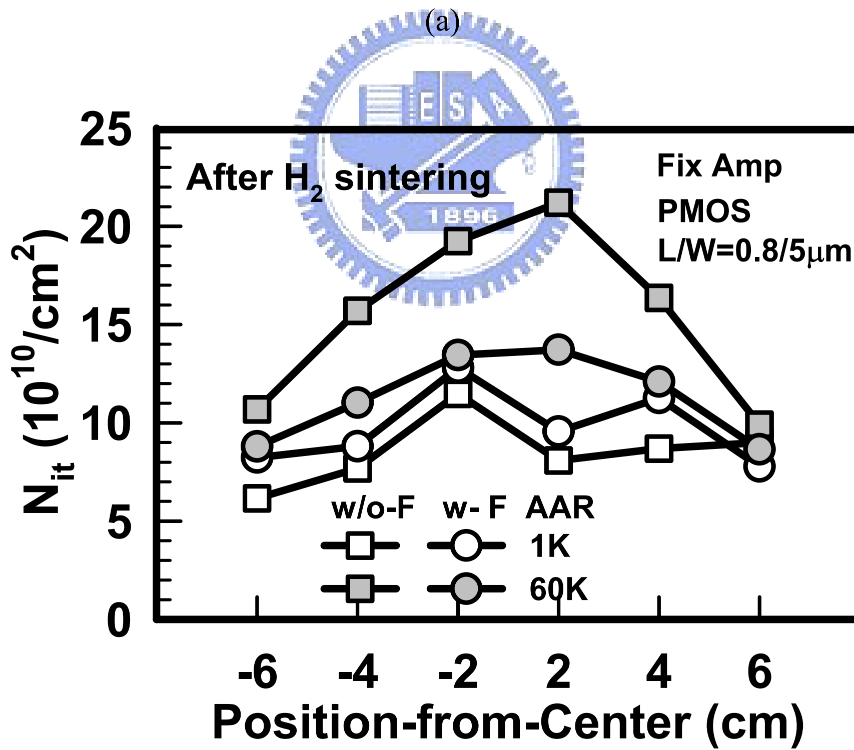

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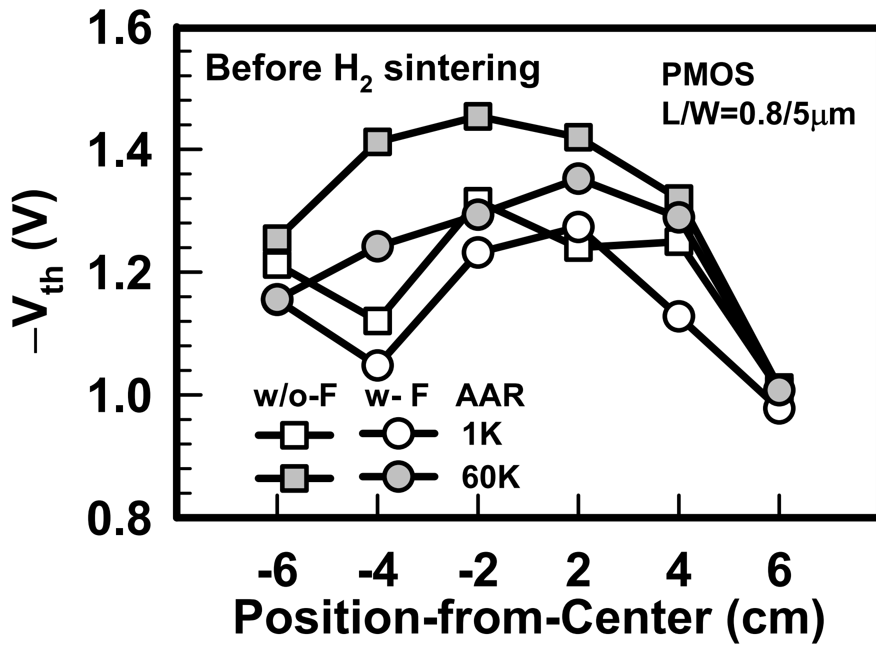
Fig. 7.3 N_{it} of PMOS devices with and without F incorporation (a) before sintering (b) after sintering as a function of device location.



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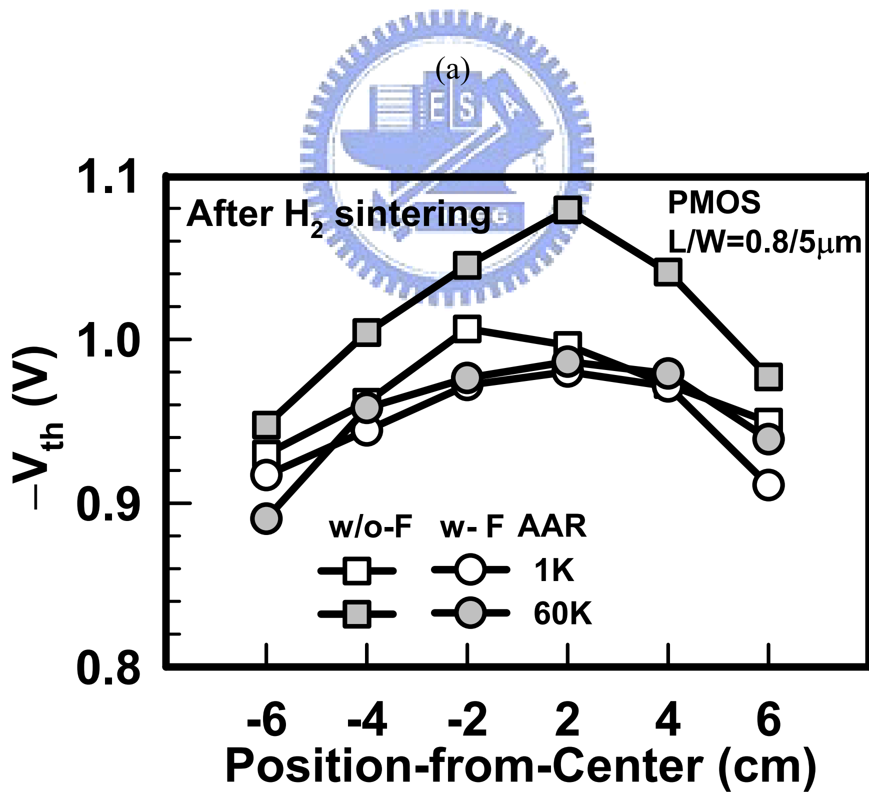

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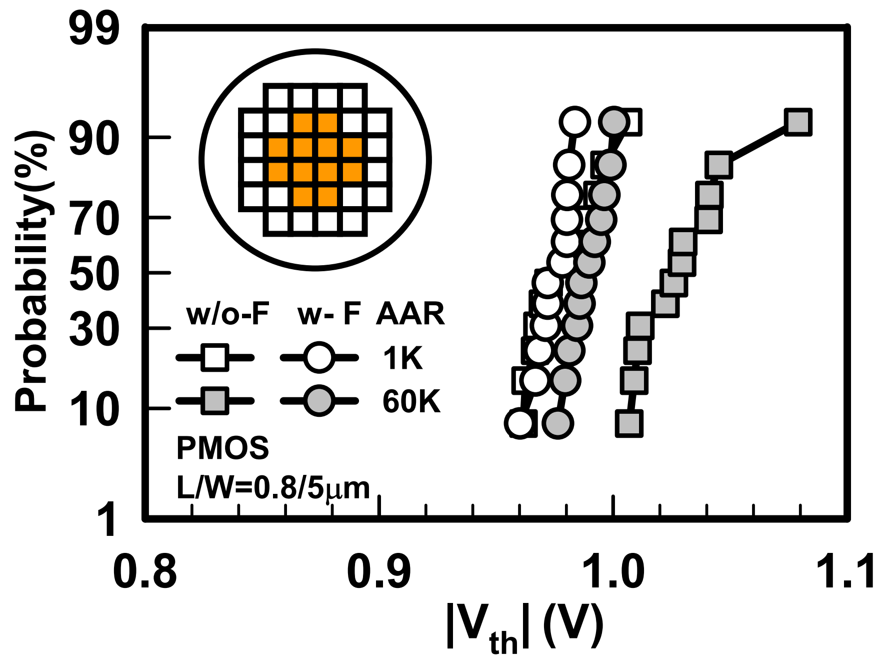
Fig. 7.4 V_{th} of PMOS devices with and without F incorporation (a) before sintering (b) after sintering as a function of device location.



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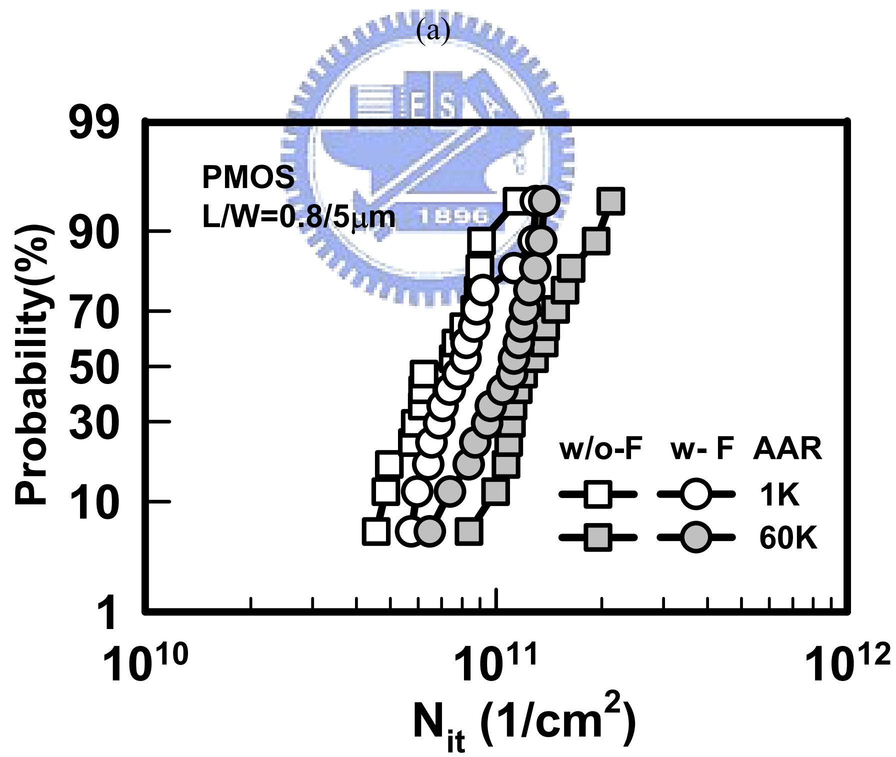


(b)

Fig. 7.5 Cumulative probability of the (a) threshold voltage (V_{th}) and (b) interface trap (N_{it}).

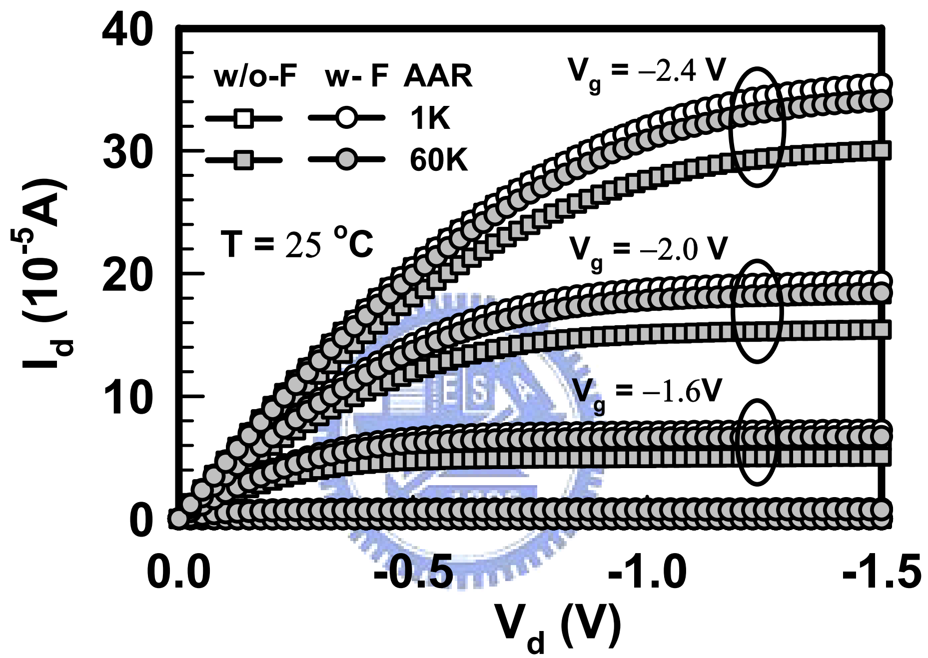
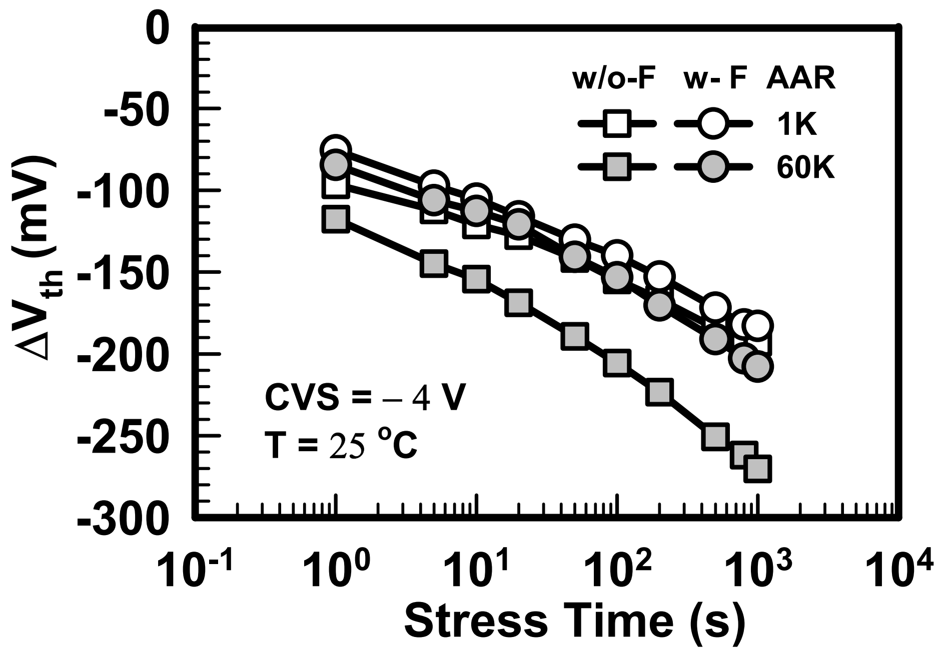


Fig. 7.6 Output characteristics for fresh devices with AAR of 1K and 60K.



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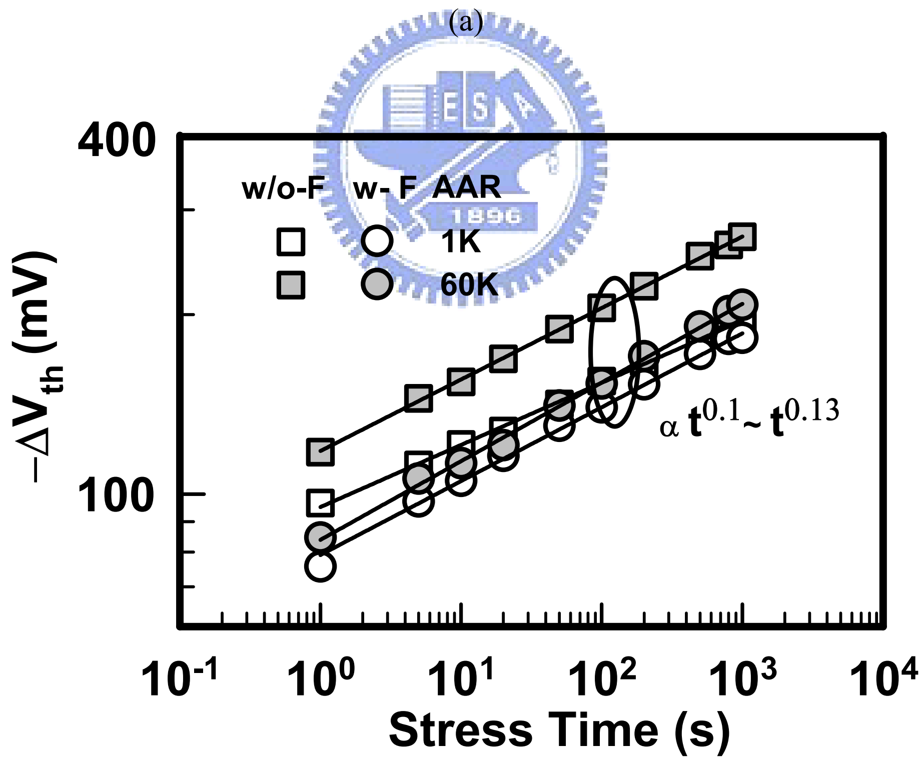

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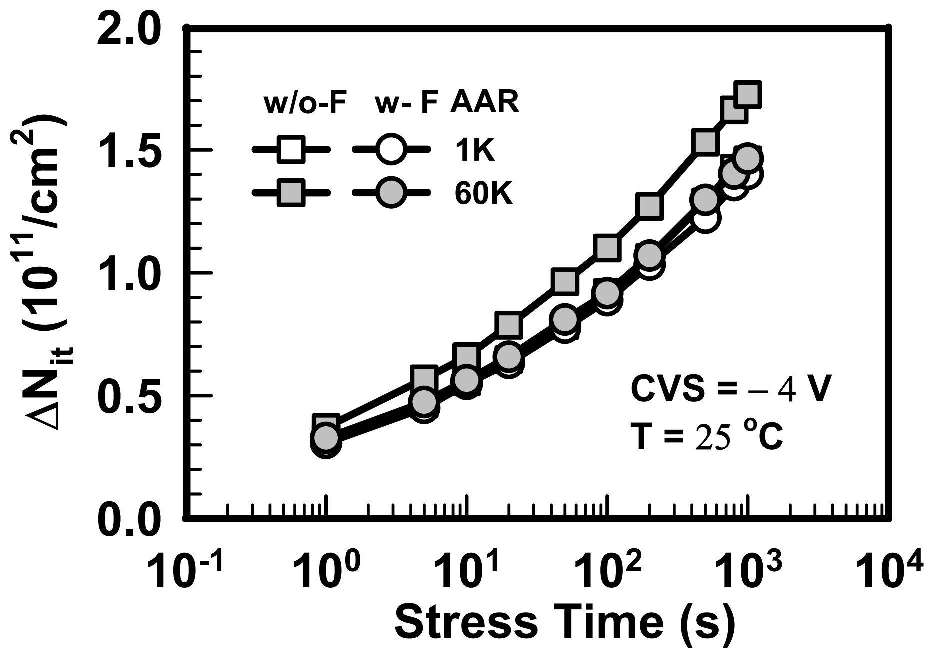
Fig. 7.7 Threshold voltage shift as a function of stress time, stressed at 25 ^{o}C, V_g = −4 V (a) linear scale (b) logarithm scale.



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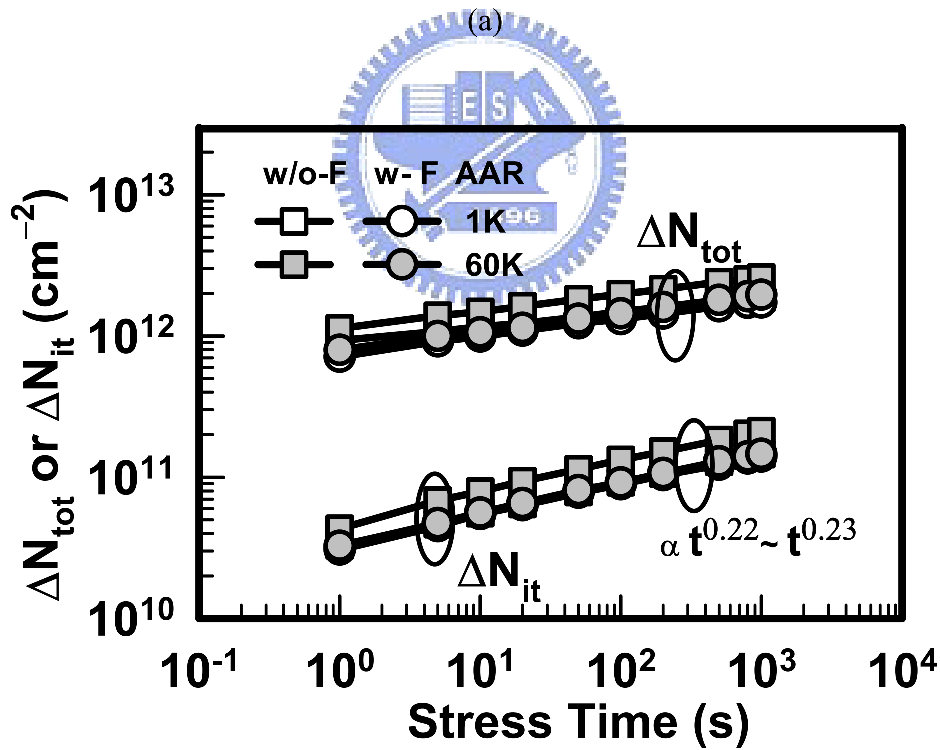

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Fig. 7.8 (a) Interface trap generation and (b) total trap density increase as a function of stress time, stressed at 25 °C, V_g = –4 V.

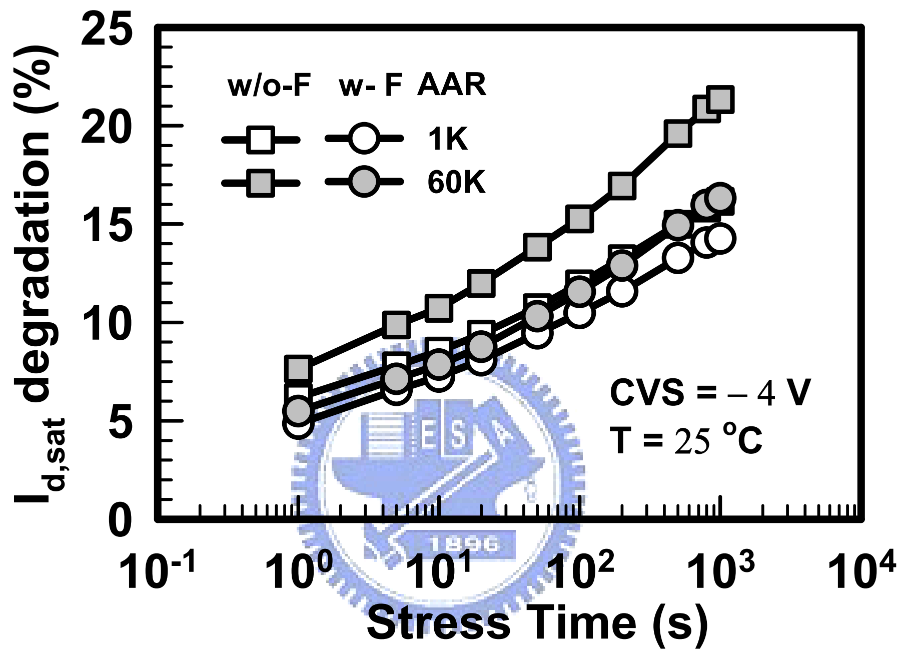
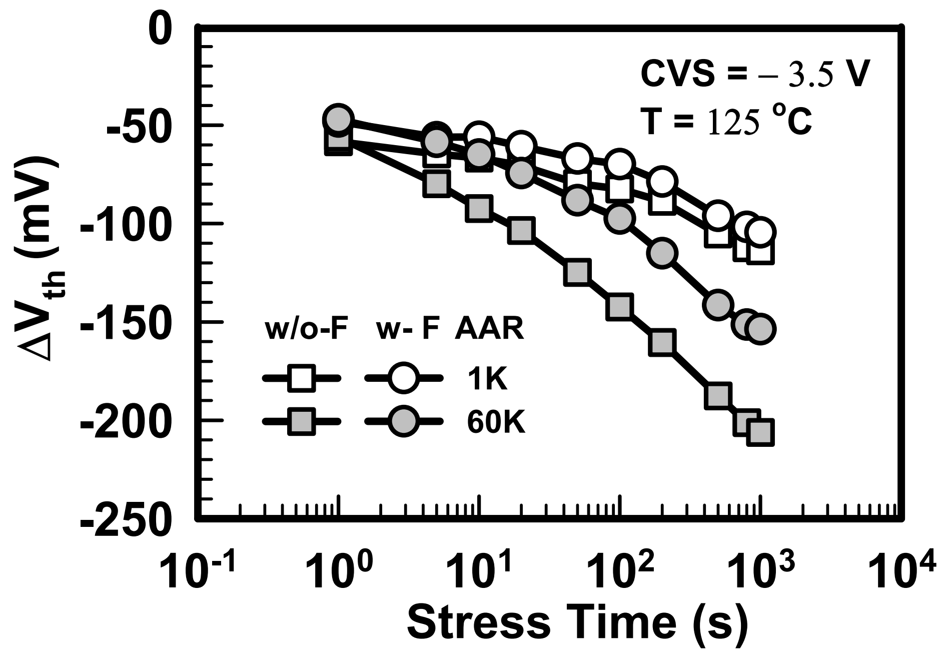


Fig. 7.9 Drain current degradation in a saturation regime of stress time, stressed at 25 °C, $V_g = -4$ V.



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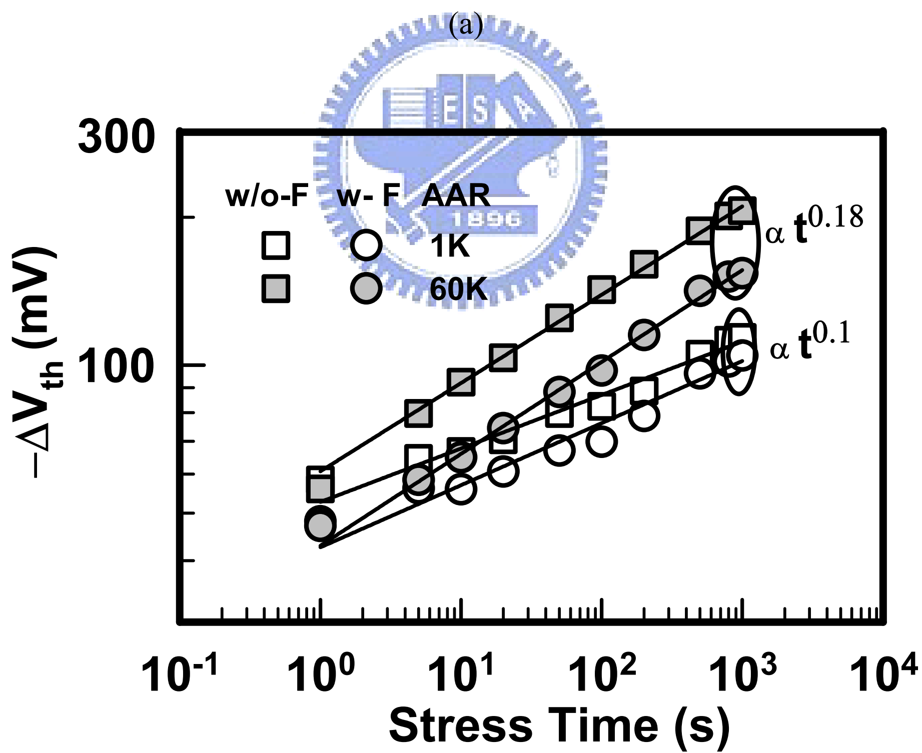

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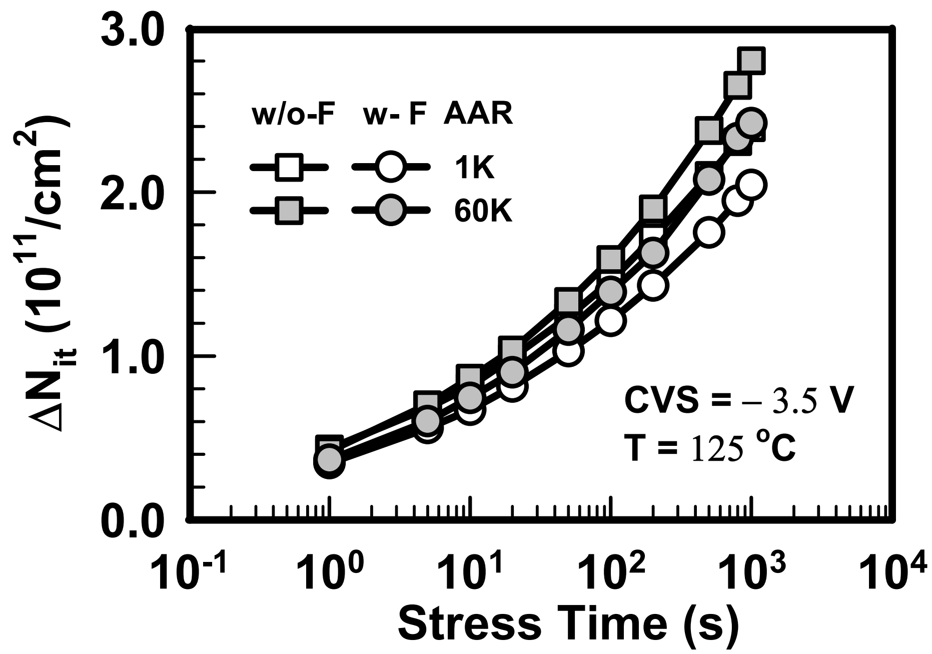
Fig. 7.10 Threshold voltage shift as a function of stress time, stressed at 125 °C, V_g = −3.5 V (a) linear scale (b) logarithm scale.



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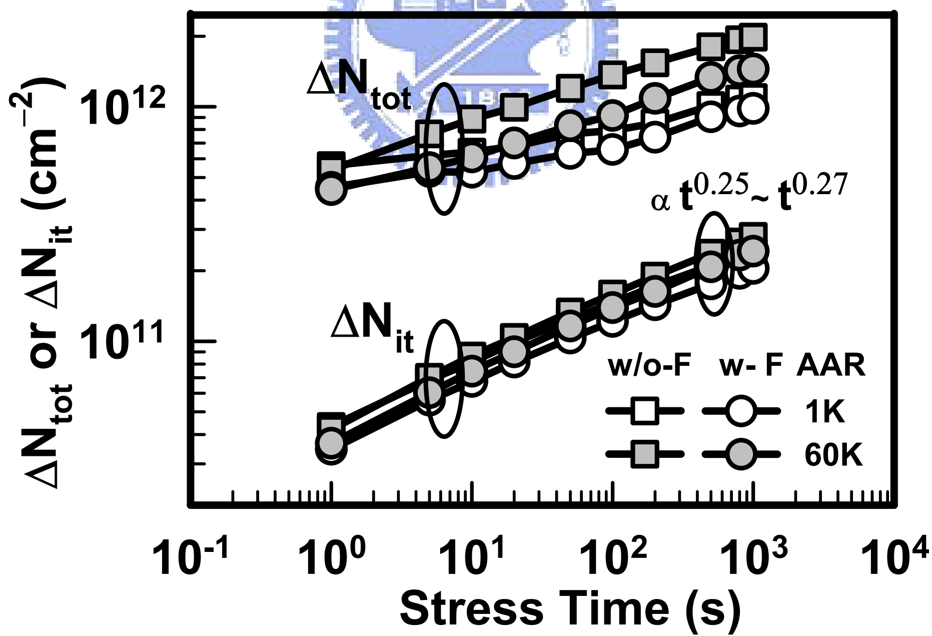

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Fig. 7.11 (a) Interface trap generation and (b) total trap density increase as a function of stress time, stressed at 125 °C, $V_g = -3.5$ V.

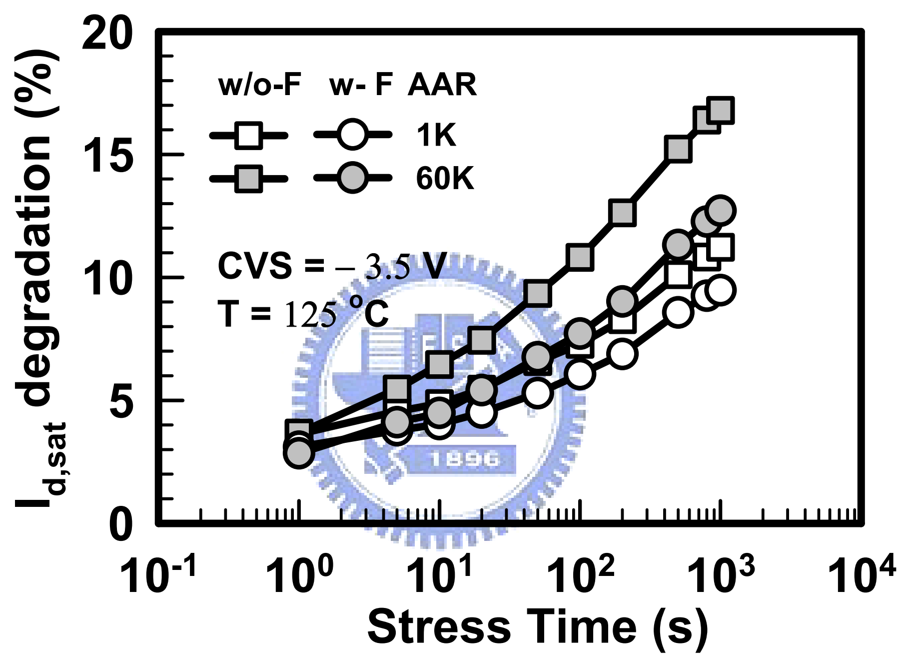
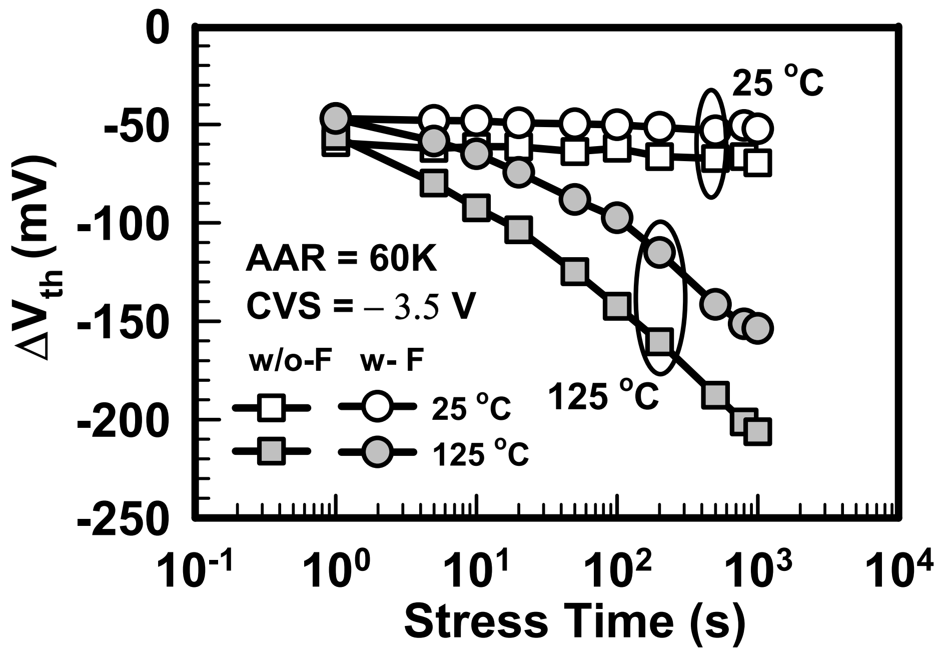


Fig. 7.12 Drain current degradation in a saturation regime of stress time, stressed at 125 °C, $V_g = -3.5$ V.



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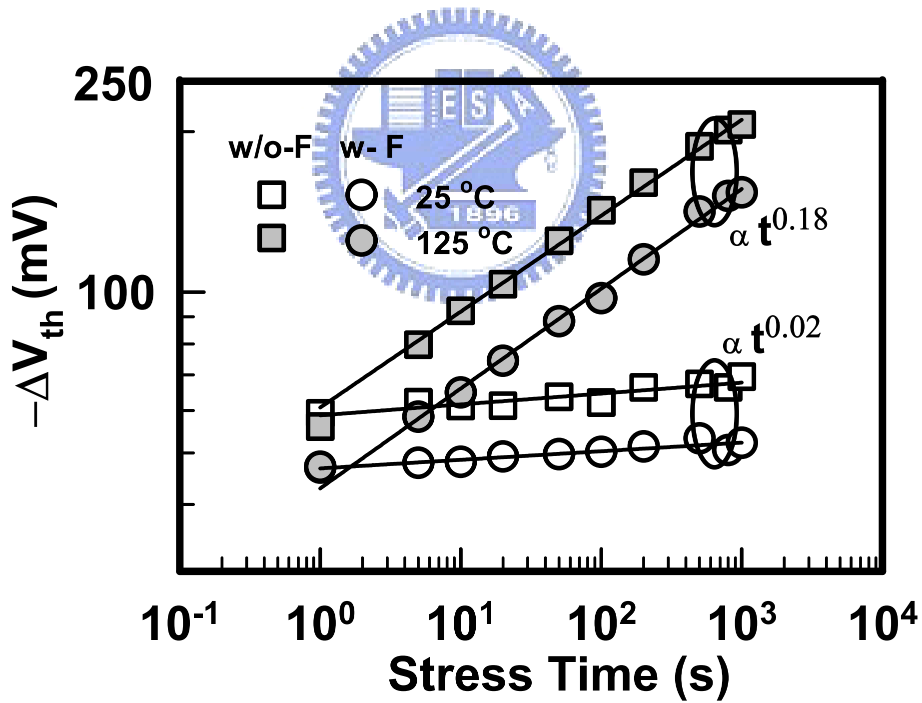

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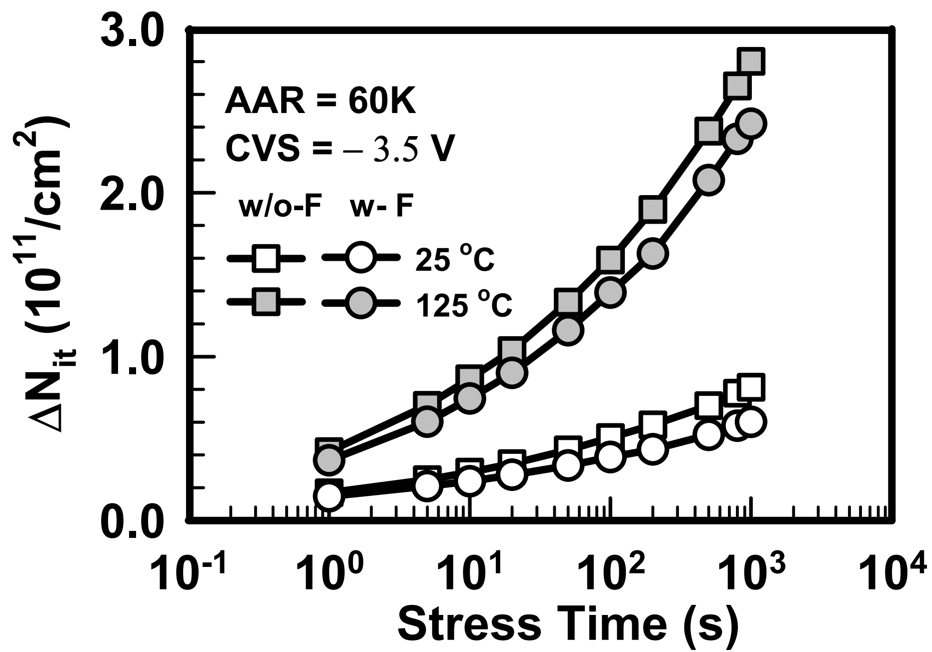
Fig. 7.13 Threshold voltage shift as a function of stress time under BTS at different stress temperature, V_g =−3.5 V. AAR is 60K (a) linear scale (b) logarithm scale.



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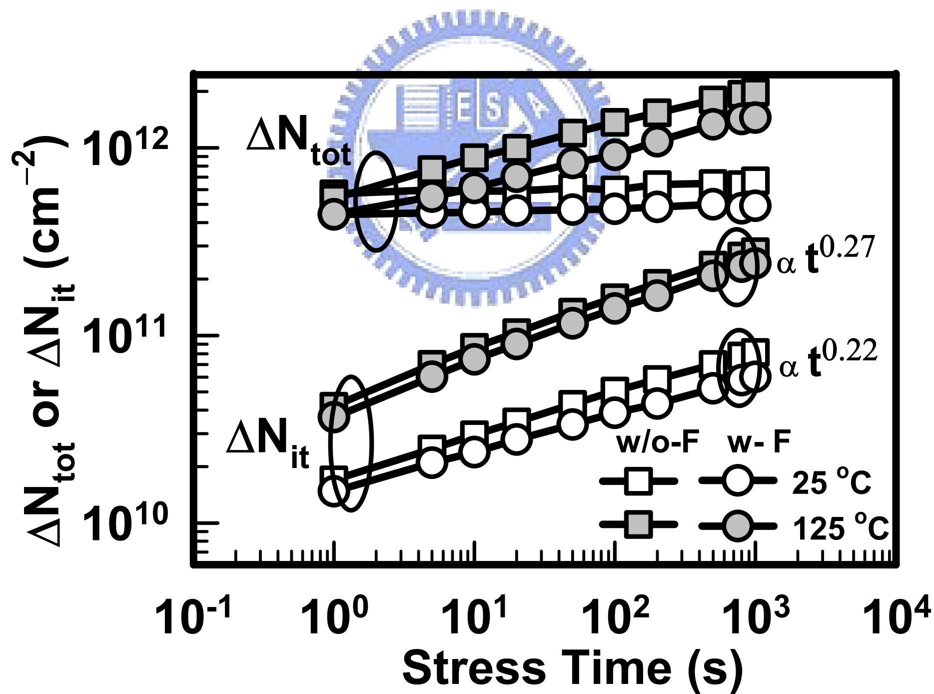

(b)

Fig. 7.14 (a) Interface trap shift and (b) total trap shift as a function of stress time under BTS at different stress temperature, $V_g = -3.5$ V. AAR =60K.

Chapter 8
Conclusions and Suggestions for Future Study

8.1 Conclusions

In this dissertation, the electrical characteristics of pMOSFETs with $HfO_2/SiON$ gate stack subjected to various nitridations, i.e., pre-deposition plasma treatments, post-deposition N_2O plasma Nitridation, low-temperature NH_3 Nitridation, and fluorine incorporation, were discussed. The related reliabilities, including CVS stress, NBTS, dynamic unipolar AC stress, and plasma charging damage, were comprehensively investigated. In addition, the characteristics of charge trapping in the HfO_2 high-k film also were studied. Several important results are summarized as follows:

1. In Chapter 2, we investigated the effects of various pre-deposition plasma treatments on HfO_2/SiO_2 gate stacks. In order to significantly reduce gate leakage current, a good quality interfacial layer is essential prior to the deposition of high-k film. The samples with conventional RTA show much lower leakage current, lower frequency dispersion, and smaller hysteresis than the counterparts because of the formation of a thicker interfacial layer.

We also studied hole trapping characteristics in HfO_2/SiO_x gate dielectrics stack. We proposed that hole trapping occurs through filling of pre-existing hole traps in HfO_2 film, and we employed continuous capture cross section model to fit our experimental data. The fitting results match well with experimental data, and the fitting parameter β possesses larger

distributed capture cross section than that of electron traps.

2. In Chapter 3, we proposed a post-deposition low-temperature (~ 400°C) NH_3-treatment on the HfO_2/SiO_2 gate stacks with TiN gate electrode. Our results indicate that samples subject to the LTN treatment exhibit superior *C-V* characteristics, less frequency dispersion, and lower gate leakage. In addition, the defect density in the bulk and the immunity against trap generations are significantly improved, especially for samples with subsequent 700°C PDA.

3. In Chapter 4, we investigated the effects of the post-deposition N_2O plasma treatment on the characteristics of pMOSFETs with HfO_2/SiON gate stack. We have found many improvements, including reduced leakage current, better subthreshold swing, enhanced normalized tranconductance, and higher driving current. These improvements were ascribed to the lower interface states and bulk traps, as confirmed by various types of charge pumping measurements. Although CP measurement was a powerful technique to evaluate the interface states and bulk traps presented in the high-k films, to precisely measure the bulk traps at a lower frequency, it should be better to measure charge pumping current (I_{cp}) and source/drain current (I_{ds}) simultaneously and confirm that I_{cp} and I_{ds} are identical. Noted that the effect of the leakage current on the CP measurement in PMOSFETs is rather different from that in NMOSFETs, where the leakage current will not contribute to the substrate current, but to the source/drain current only.

   In evaluation of the reliability, it was found that the degradation caused by the voltage stress was dominated by the charge trapping in the bulk of HfO_2 films, rather than interface states generation, no matter whether the N_2O plasma treatment was employed or not. In addition, it was observed that the N_2O plasma treatment did significantly improve the charge trapping characteristics, and the electron trapping was the main mechanism during stressing, which was opposite to the hole trapping observed in the case without the N_2O plasma treatment.

4. In Chapter 5, several kinds of reliability testing for HfO_2/SiON gate stack with and without the post-deposition N_2O plasma treatment have been performed, such as dynamic stress, investigation of bulk or IL breakdown, and NBTI. It was found that the post-N_2O plasma treatment may not be beneficial because of the resulting higher electrons trapping under AC stress, even though it exhibits several advantages as discussed in Chapter 4. Bias temperature instability shows that leakage current can affect the threshold voltage shift behavior, due to the electron and hole current components in the gate leakage, resulting from the asymmetric energy band diagram. Our data also confirm that two different mechanisms exist in HfO_2/SiON gate stacks, i.e., trapping and the NBTI. Moreover, the effect of trapping is the dominant degradation for HfO_2/SiON gate stacks with and without the post-deposition N_2O plasma treatment, rather than the reaction-diffusion effect. However, the interface state generation still obeys the reaction-diffusion model since the interfacial layer is SiON film.
5. In Chapter 6, the effects of fluorine incorporation into HfO_2/SiON gate stack were investigated. We found that F introduction only negligibly impacts the fundamental electrical properties of the fabricated transistors. All leakage currents can be categorized by fitting to be of Frenkel-Poole type. The barrier height of electrons and holes for the control sample are 1.02eV and 1.22eV, respectively. The results are also the same for the F-incorporated sample. We also studied the NBTI mechanism and AC dynamic stressing of the polysilicon gate HfO_2 MOSFETs, with and without F incorporation. $\triangle V_{th}$ is primarily caused by the charge traps in the HfO_2 dielectric, not by the interfacial degradation. F incorporation is effective in suppressing $\triangle N_{it}$ as well as $\triangle N_{ot}$, thus improving threshold voltage instability. For traditional SiO_2 gate dielectric, both $\triangle V_{th}$ and $\triangle N_{it}$ are improved by fluorine incorporation, while maintaining almost the same activation energies of about 0.2 eV. Similar trends are observed in our devices. The activation energy of $\triangle V_{th}$ is 0.08 eV and that of $\triangle N_{it}$ is 0.14 eV for both devices.

Fluorine is found to effectively electrically passivate traps without changing the NBTI mechanism.

The experimental results of dynamic AC stressing show that threshold voltage shifts toward more negative voltage in DC stress, but shifts toward more positive voltage under AC unipolar stress. This is believed to be due to less hole charge trapping during on-time. The interface trap generation depends weakly on both frequency and duty cycle. Instead of interface trap, the bulk trap of HfO_2 eventually plays a preponderant role during AC stress.

6. In Chapter 7, we have clearly shown that plasma charging damage introduces more hole traps in the HfO_2/SiON gate stack, thus aggravating the NBTI. F incorporation can significantly reduce the impact of plasma charging effect. Suppressing the traps in bulk is important for pMOSFETs with HfO_2/SiON gate stack. Fluorine incorporation is found to be an excellent technique to improve BTI immunity and strengthen the immunity against plasma charging damage, thus enhances high-k devices' stability and reliability.

8.2 Suggestions for Future Study

There are some works valuable for future researches:

It is generally conceived that the introduction of high-k gate dielectrics is inevitable for the technology nodes of 50 nm and beyond, in order to satisfy the stand-by power requirement without sacrificing metal oxide semiconductor field effect transistor (MOSFET) performance. HfO_2 is considered as one of the most promising high-k dielectrics. However, threshold voltage instability and inadequate mobility of HfO_2 MOSFETs are major issues that remain to be solved.

1. For the threshold voltage instability issue, we found that the exponential value of $\triangle V_{th}$ for pMOSFETs with HfO_2 gate dielectric is voltage and temperature

dependent due to the charge trapping in bulk HfO_2. More efforts on developing the model of time evolution of V_{th} instability, so that we could extrapolate ten years lifetime for devices by this model, are necessary.

2. To fabricate thinner interfacial layer and gain lower gate leakage current is very important for future high-k application.
3. To fabricate Hf-based films composed of three or four elements and investigate the electrical characteristics, mobility, and reliabilities.
4. How to more accurately and automatically estimate high-k films is very important for the application of high-k film to ULSI industry.
5. The relationship between the electron and hole trapping and the trapping position in the energy band is important for investigating the dielectric breakdown and reliabilities.
6. It is important to clarify the issue: Is the breakdown mechanism related to electrons or holes?
7. The bond structure of HfO_2 film with fluorine incorporation is important, and deserves more research efforts.
8. More research efforts are needed in understanding the Fermi-level pinning effect of high-k film and gate electrode, and impacts of various gate electrodes on electrical characteristics, charge trapping, mobility, and reliability of high k film.
9. Introduction of the strained silicon is known to enhance channel mobility. However, locally strained pMOSFETs with HfO_2 gate dielectric have not been reported. More research efforts are needed to understand channel mobility and reliability of this structure, as well as their impacts on future ULSI technology.

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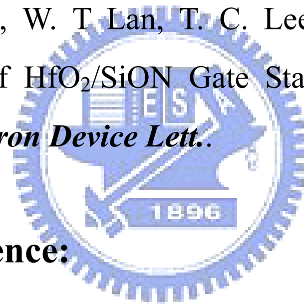
其電性特性與可靠性影響

Effects of Nitridation and Fluorine Incorporation on the Electrical Characteristics and Reliabilities of MOSFETs with HfO_2/SiON Gate Stack

Publication List

A. International Journal:

1. **W. T. Lu**, P. C. Lin, T. Y. Huang, C. H. Chien, M. J. Yang, I. J Huang and P. Lehnen, "The characteristics of hole trapping in HfO_2/SiO_2 gate dielectrics with TiN gate electrode," ***App. Phys. Lett***, Vol. 85, pp. 3525-3527, 2004.
2. **W. T. Lu**, C. H. Chien, I. J Huang, M. J. Yang, P. Lehnen and T. Y. Huang, "Effects of low-temperature NH_3-treatment on the characteristics of HfO_2/SiO_2 gate stack," ***Journal of Electrochemical Society*****,** Volume 152, Number 11.
3. **W. T. Lu**, C. H. Chien, W. T Lan, T. C. Lee, M. J. Yang, S. W. Shen, P. Lehnen and T. Y. Huang, "Improvements on the electrical characteristics of pMOSFETs with HfO_2 gate stacks by Post-Deposition N_2O plasma treatment," accepted to ***Jpn. J. Appl. Phys.***.
4. **W. T. Lu**, C. H. Chien, W. T Lan, T. C. Lee, P. Lehnen and T. Y. Huang, "Improved Reliability of HfO_2/SiON Gate Stack by Fluorine Incorporation," submitted to ***IEEE Electron Device Lett.***.



B. International Conference:

1. **W. T. Lu**, C. H. Chien, Y. C Lin, M. J. Yang and T. Y. Huang, "Effects of low temperature NH_3 treatment on HfO_2/SiO_2 stack gate dielectrics fabricated by MOCVD system," in the 2004 ***Joint International Meeting*** (including ***the 206th Meeting of The electrochemical Society***), held 2004 fall in Honolulu, October 3-October 8, 2004.
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C. Local Conference:

1. Da-Yuan Lee, Horng-Chih Lin, Wan-Ju Chiang, **Wen-Tai Lu**, Guo-Wei Huang, Tiao-Yuan Huang, and Tahui Wang, “Enhanced Negative-Bias-Temperature Instability of P-Channel MOSFET by Plasma Charging Damage,” in *Symposium on Nano Device Technology*, Hsin-Chu, Taiwan, 2001.
2. Da-Yuan Lee, Horng-Chih Lin, Wan-Ju Chiang, **Wen-Tai Lu**, Guo-Wei Huang, Tiao-Yuan Huang, and Tahui Wang, “Effects of Process Treatments on Negative-Bias-Temperature Instability of P-Channel MOSFETs,” in *Electron Devices and Materials Symposium*, pp. 515-518, Taipei, Taiwan, 2001.