國 立 交 通 大 學

電子工程學系電子研究所

博 士 論 文

準分子雷射低溫製備之鈦酸鍶鉛薄膜元件特性分析之研究

Study on the Characterization of Devices with Perovskite Lead-Strontium-Titanate Thin Films Fabricated by Excimer Laser Deposition at Low-Temperatures

研 究 生 ： 王 志 良

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中華民國 九十六 年 二 月

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事由：推薦電子研究所博士班研究生王志良提出論文並參加國立交通大學博士論文口試。

說明：本校電子研究所博士班研究生王志先生，業已修畢部訂所需學分，通過電子研究所博士資格考之學科考試，並完成博士論文初稿之撰寫，論文名稱為：『準分子雷射低溫製備之鈦酸鍶鉛薄膜元件特性分析之研究』，並已有數篇相關之期刊論文、會議論文及專利發表或送審，茲列舉如下：

1. "Polarization Degradation and Breakdown of Pulse-Laser-Deposited (Pb,Sr)TiO3 Films at Low Temperatures", ***Jpn. J. Appl. Phys.***, vol. **46**, pp. 267-271, 2007.
2. "Characteristics of Low-temperature Pulse-Laser-Deposited (Pb,Sr)TiO3 Films in Metal/Ferroelectric/Silicon Structure", ***J. Phys. D: Appl. Phys.***, vol. **40**, pp.254-259, 2006.
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5. "Ferroelectric Characteristics of Pulse-Laser-Deposited Pt/(Pb,Sr)TiO3/Pt Capacitors at Low Temperatures", submitted to ***J. Phys.: Condens. Matter***.
6. "Characteristics of (Pb, Sr)TiO3 Films Post Treated by Low Temperature Technologies", ***Electrochemical Society Proceedings***, vol. 22, Physics and Technology of High-k Gate Dielectrics II, pp. 469-478, 2003. (SCI)
7. "A Study of PTC Behavior of (Pb,Sr)TiO3 Thin Films Deposited by Novel Low Temperature Laser Technology", ***Proceedings of the 2004 International Electron Devices and Materials Symposia (IEDMS)***, Hsinchu ROC, pp. 197-200, December 20-23, 2004.
8. "Characterization of Pulsed-Laser Deposition (Pb,Sr)TiO3 Films with Low-Temperature Processing Parameters", ***10th European Meeting on Ferroelectricity 2003***, Cambridge UK, pp. 354, August 3-8, 2003.

9. "The Effect of Post Oxygen Treatment on Pt/(Ba,Sr)TiO_3/Pt Capacitors at Low Substrate Temperatures", ***IFFF 2002***, Nara Japan., pp. 161, May 28-June 1, 2002.
10. "鐵電元件之製造方法及鐵電材料之熱處理方法", 中華民國專利, No. I247045。
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此外，尚有數篇論文投稿中，準備發表於學術期刊。王志良先生已具備交通大學電子研究所應有之教育及訓練水準，因此推薦參加國立交通大學電子研究所博士論文畢業口試。

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準分子雷射低溫製備之鈦酸鍶鉛薄膜元件特性分析之研究

研究生 ： 王志良　　指導教授: 鄭晃忠 博士

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摘　要

本論文將研究以先進低溫製程技術製備之鈦酸鍶鉛((Pb,Sr)TiO3, PbSrT)薄膜之電容特性，採用的低溫製程技術包含先進低熱預算退火製程及低溫沉積製程等。本研究中，Pt/PSrT/Pt與Pt/PSrT/Si多層膜結構分別被應用於模擬capacitor over bit line (COB)結構及鐵電閘場效電晶體中的 金屬/鐵電/半導(metal/ferroelectric/semiconductor, MFS)結構。

以雷射剝鍍法(PLD)在低溫(200 ^{o}C)所沉積的鈦酸鍶鉛薄膜為非結晶態，具有極差的鐵電特性，因此需要後續處理以改善電氣特性。傳統的快速退火製程(RTA)可輕易增進鈦酸鍶鉛薄膜的結晶性，但同時亦因表面缺陷(如：微孔洞)及界面擴算導致急遽惡化的漏電流。準分子雷射退火(ELA)可在局部區域達到高溫而不損傷下層結構，因此可用於增進鈦酸鍶鉛薄膜的結晶性。鈦酸鍶鉛薄膜經由準分子雷射退火後，可減少薄膜表面氧缺乏，並在薄膜上層區域有較佳的結晶性。然而，準分子雷射退火之效用僅作用於薄膜表層形成"淺層加熱"，無法使整層薄膜都能結晶。而以準分子雷射退火使鈦酸鍶鉛薄膜進行預先產生晶核，然後搭配快速退火製程促使晶粒成長的二階段雷射輔助退火製程則能同時實現緻密的薄膜表面、良好的結晶性、可區別的電容–電場(C-E)電滯曲線、較大的介電常數(492)及壓抑的漏電流。因而，此二階段雷射輔助退火製程能成功製備具有優越的鐵電特性、較高的崩潰電壓、較長的元件壽命之Pt/PSrT/Pt電容器。

以雷射剝鍍在低基板溫度(300 – 450 ^{o}C)所製備的鈦酸鍶鉛薄膜具有緻密的薄膜表面、顯著的結晶性及明顯的鐵電特性。適當的沉積溫度有助於減少鈦酸鍶鉛薄膜的界面能態及陷阱能態，及較小的漏電流，其電流分析顯示Pt/PSrT/Pt電容在低電場時的導電機制主要為Schottky emission (*SE*)，在高電場則由Poole–Frenkel emission (*PFE*)主導，在本文中將以能帶圖分析探討此導電機制。實驗顯示，以雷射剝鍍製備的鈦酸鍶鉛薄膜，其從優取向結晶結構及陷阱能態隨著基板溫度而變化，進而影響薄膜電氣特性。因此，鈦酸鍶鉛薄膜的介電常數及鐵電特性亦深受從優取向影響，所以在350 – 400 ^{o}C沉積的鈦酸鍶鉛薄膜顯現強化的(100)從優取向結晶性與最佳化的鐵電特性。疲勞操作測試顯示當鈦酸鍶鉛薄膜的沉積溫度高於350 ^{o}C時，Pt/PSrT/Pt電容經10^{10}次切換操作後，僅損失低於17%的殘留極化值。本文中，400 ^{o}C製備的鈦酸鍶鉛薄膜顯示強化的結晶性及較少的缺陷，因此具有最低的漏電流、最佳的崩潰特性，即使經過10^{10}次切換操作後亦顯現近乎無疲勞的的電流密度–電場特性。

更進一步分析指出，雷射剝鍍低溫製備的鈦酸鍶鉛薄膜其電流密度隨著量測溫度及外加電場增加而增加。當量測溫度低於150 ^{o}C時，鈦酸鍶鉛薄膜可測得穩定的電流密度及薄膜電阻，換言之，鈦酸鍶鉛薄膜在積體電路元件操作溫度範圍內具有相當穩定性，可適用於記憶體應用。而當量測溫度為100 – 390 ^{o}C，鈦酸鍶鉛薄膜亦顯現出強烈的負溫度–電阻係數(negative temperature coefficient of resistance, NTCR)特性，此大範圍的薄膜阻值變動，暗示鈦酸鍶鉛薄膜可應用於熱敏電阻領域。

此外，鈦酸鍶鉛薄膜的從優取向結晶性、微結構以及電氣特性亦可經由調整雷射剝鍍時氧氣氛壓力參數(50 – 200 mTorr)而改變。當氧氣氛壓力高於100 mTorr時，鈦酸鍶鉛薄膜將從(100)從優取向結晶性轉換成(110)從優取向結晶性。因此，順電/鐵電轉變及薄膜介電常數亦與從優取向結晶性及氧含量相關而受到氧氣氛壓力調變之影響。較高的氧氣氛壓力有助於減少鈦酸鍶鉛薄膜中的氧空缺，使鈦酸鍶鉛薄膜具有較小的漏電流、較高的崩潰電場，進而增加Pt/PSrT/Pt

電容器的元件壽命。電流分析顯示Pt/PSrT/Pt電容在低電場時的導電機制主要為Schottky emission，在高電場則由Poole–Frenkel emission主導，但氧氣氛壓力為200 mTorr時，在低/高電場下都將僅由Schottky emission主導。藉由能帶圖分析疲勞特性，可得知在較低氧氣氛壓力製備的鈦酸鍶鉛薄膜其疲勞特性深受介面能態影響，相對的，在較高氧氣氛壓力製備的鈦酸鍶鉛薄膜其疲勞特性則由深的陷阱能態主導，這種差異導因於氧空缺集中在介面或薄膜內。

鈦酸鍶鉛薄膜亦可以雷射剝鍍法低溫(300 – 450 ^{o}C)沉積在p型矽晶片上應用於 金屬/鐵電/半導 結構。實驗結果顯示基板溫度可強烈增進鈦酸鍶鉛薄膜結晶性及影響其電氣特性，並且在此沉積溫度範圍內亦無發現交互擴散現象存在 鐵電/半導 (PSrT/Si)介面。300 ^{o}C沉積之鈦酸鍶鉛薄膜內將存在負的陷阱電荷，因此顯現出小的且為逆時針方向的介電場數–電場電滯曲線及正偏移的平帶電壓(flatband voltage)。隨基板溫度增加，鈦酸鍶鉛薄膜的結晶性顯著改善，因此具有較小的漏電流、較少的陷阱能態在電極界面、順時針方向的介電場數–電場(ε_r-E)電滯曲線及較大的記憶窗(memory window)。然而，過高的基板溫度(450 ^{o}C)可能導致較嚴重的的氧化鉛(Pb-O)揮發，產生較多的缺陷及漏電流特性惡化。分析固定電荷密度(fixed charge density)及平帶電壓偏移，顯示其陷阱能態特性亦與電氣特性相契合。本研究中，即使經過10^{10}次切換操作後僅導致記憶窗極小的變動(< 11%)，因此可實現良好的耐疲勞特性。總結，透過準分子雷射退火及沉積技術之整合，可在低溫製備具有良好結晶性、優越電氣特性之鈦酸鍶鉛(PSrT)薄膜電容元件，進一步與積體電路技術整合後，將成為深具潛力的非揮發性記憶元件。

Study on the Characterization of Devices with Perovskite Lead-Strontium-Titanate Thin Films Fabricated by Excimer Laser Deposition at Low-Temperatures

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Abstract

The characteristics of (Pb,Sr)TiO_3 (PSrT) films prepared by novel low-temperature techniques, including low-thermal budget annealings and a low temperature deposition, are systematically investigated in this dissertation. The multilayered structures of Pt/PSrT/Pt and Pt/PSrT/Si are proposed to simulate the practical capacitor over a bit-line (COB) and metal/ferroelectric/semiconductor (MFS) configuration of ferroelectric gate FET, respectively.

PSrT films pulsed-laser deposited at 200 ^oC exhibits amorphous crystallinity and worse ferroelectricities, which indeed require a post-treatment to reform electrical properties. Conventional rapid thermal annealing (RTA) can evidently improve the crystallinity of PSrT films but seriously degrade leakage current due to the unwilling surface defects (i.e. pin holes) and interfacial diffusion. An excimer laser annealing (ELA) technique can recognize local-high-temperature heating within short duration without the underlying damage, proposed to enhance the crystallinity of films. After ELA, the decrease of oxygen deficiency and superior crystallinity of the upper region of films can be obtained. However, the effect of ELA is very limited and can't

crystallize the whole thickness of film. Furthermore, the novel laser-assisted two-step process, the combination of initial crystal seed induced by ELA and the grain growth carried out by subsequent RTA, which can realize the dense surface, well crystallinity, distinct C-E hysteresis loops, large dielectric constant of 492, and inhibited leakage current density all at once. Thus, the superior ferroelectricity, higher breakdown field and longer lifetime of Pt/PSrT/Pt capacitors can be successfully achieved by this laser-assisted two-step process.

PLD PSrT films prepared at low substrate temperatures (T_s), ranging from 300 to 450 ^oC, behave dense surface, evident crystallinity, and apparent ferroelectric properties. Films grown at appropriate T_s yield fewer interface states and fewer trapping states, leading to a smaller leakage current. The conduction mechanism is identified as Schottky emission (*SE*) at low electric fields and as Poole–Frenkel emission (*PFE*) at high electric fields. The mechanism analysis shows the electrical characteristics strongly rely on the preferred-oriented textures and trapping states, adjusted by the low substrate temperature ($T_s \leq 450\ ^oC$) during PLD process. In addition, the dielectric constant and ferroelectricity are associated with the preferred orientation. The enhanced (100) preferred orientation of films deposited at T_s = 350 – 400 ^oC exhibits optimum ferroelectricity. The loss in remnant polarization and coercive field is found to be less than 17 % after 10^{10} switching cycles when T_s is higher than 350 ^oC. Consequently, the 400 ^oC-deposited PSrT film reveals the lowest leakage current, nearly fatigued-free J-E characteristics after 10^{10} switching cycles, and the best breakdown property, attributed to the enhanced crystallinity and fewer defects.

Moreover, the current density of these low-temperature PLD PSrT films increases as the measurement temperature and applied fields increase. Films show high stability of leakage current and film resistance below 150 ^oC, which is important

and well for memory application during the operation temperature of IC. Films exhibit strong negative temperature coefficient of resistance (NTCR) behavior at temperatures ranging of 100 – 390 °C. The larger resistance range of the PLD PSrT films infers a potential application of thermistor sensor.

Besides, the preferred orientation, microstructure, and electrical characteristics of PLD PSrT films could be apparently affected by ambient oxygen pressures (P_{O_2}), ranging from 50 to 200 mTorr. Films exhibit (100) preferred orientation at lower P_{O_2} and then transit to (110) preferred orientation above 100 mTorr. The paraelectricity/ferroelectricity transition and dielectric constant of films are associated with the preferred orientation and oxygen concentration at various P_{O_2}. Films deposited at higher P_{O_2} exhibit the longer lifetime, higher breakdown field and smaller leakage current density as a consequence of fewer oxygen vacancies (OVs). Except for the case of films deposited at 200 mTorr, the conduction mechanism is identified as *SE*/*PFE* at low/high electric fields. The fatigue properties are dominated by interfacial states at low P_{O_2} and by deep trapping states at high P_{O_2}, which could be ascribed to OVs located at the interfaces and inside PSrT films, respectively.

PLD PSrT films on p-type Si were studied at low T_s (300 – 450 °C) for MFS applications. The T_s strongly enhances film crystallinity without significant inter-diffusion at the PSrT/Si interface and affects the electrical properties. As T_s increases, films have smaller leakage currents, fewer trap states at the electrode interfaces, clockwise ε_r-E hysteresis loops, and larger memory windows correlated with superior crystallinity. Conversely, 300 °C-deposited films exhibit the small and counterclockwise loop with positive shift of the flatband voltage, attributed to more

negative trap charges within the films. However, the high T_s (450 °C) may produce serious Pb-O volatilization, incurring more defects and leakage degradation. The analyses of fixed charge density and flatband voltage shift reveal the trap status and agree well with the leakage characteristic. The excellent fatigue endurance with small variation of memory windows (< 11%) after 10^{10} switching is also demonstrated. Concisely, PSrT films can be the most promising candidate for future NVRAM capacitor, since the low-temperature process can be compatible to the IC's integration.

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Chapter 7

Chapter 1 Introduction

1-1 Overview on Ferroelectric Perovskite Materials

1-1-1 Background of Ferroelectric films

In last three decades, it has brought a marvelous increase in the research of ferroelectric materials in different forms, including single crystals, ceramics, composites, liquids, and thin films [1-8]. A very important group of ferroelectrics is the perovskites, named from the mineral perovskite calcium titanate ($CaTiO_3$). The perfect pervoskite structure (Fig. 1-1) is exteremely simple with the general formula ABO_3, where O is oxygen, A represents a cation (a divalent or monovalent metal) with a larger ionic radius, and B is a cation (a tetravalent or pentavalent metal) with a smaller ionic radius. It is cubic, with oxygen ions at the face centers, A ions at the cube corners, and B ions at the body centers. Ferroelectric materials exhibit spontaneous polarization that is reversible with applied electrical field due to the cation displacement of the body-center ion (B) in the structure of perovskite ABO_3 crystal as shown in Fig. 1-2(a). The displacement vector D is observed along c-axis and be expressed as

$$D = \varepsilon_0 E + P = \varepsilon_0 E + \chi_e \varepsilon_0 E = \varepsilon_0 \varepsilon_r E \,, \qquad (1\text{-}1)$$

$$\varepsilon_r = 1 + \chi_e \,,$$

where E is external electrical field, P is polarization, ε_0 is the vacuum permittivity, ε_r is the relative permittivity (dielectric constant), and χ_e is the electric susceptibility. Thus, the electrical polarization can be defined as

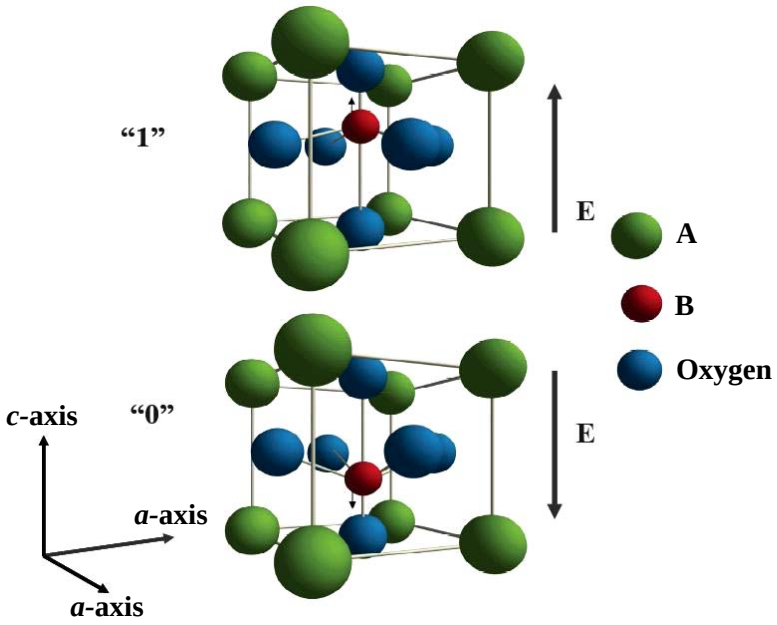


Figure 1-1 Typical crystal structure of perovskite ABO_3, where A is a divalent or or monovalent cation and B is a tetravalent or pentavalent cation, respectively. [3]

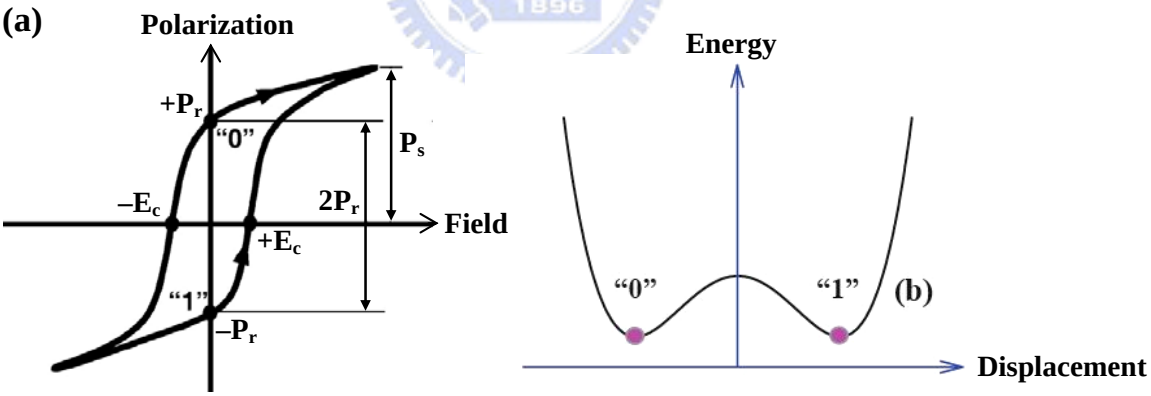


Figure 1-2 (a) Ferroelectric materials exhibit spontaneous polarization with applied electrical field due to the cation displacement of the body-center ion (B) in the perovskite structure (seen in Fig. 1-1). The saturation polarization, remnant polarization and coercive field are denoted as P_s, P_r and E_c, accordingly. (b) The plot of potential energy versus displacement for ferroelectric material. [1, 3]

$$P = \sum_{N} \varepsilon_0 (\varepsilon_r - 1) E \,, \qquad (1\text{-}2)$$

Figure 1-2(b) gives the plot of potential energy versus displacement for ferroelectric material, suggesting that the polarization-voltage curve has two stable states ("0" and "1") at zero voltage after the removal of the field. Ferroelectrics are prime candidates for nonvolatile digital memory devices, since their bi-stable polarization offers the potential for binary memory, which can remain stable after removal of electrical power. In principle, the phenomenon of spontaneous polarization can be analyzed by the energy equation [1].

$$W_{tot} = W_{dip} + W_{elas} = \left[\left(k / 2Nq^2 \right) - \left(N\alpha\gamma^2 / 9\varepsilon_0^{\,2} \right) \right] P^2 + \left[k' / 4N^3 q^4 \right] P^4 \,, \qquad (1\text{-}3)$$

where W_{tot}, W_{dip} and W_{elas} are the total energy of unit volume, energy of dipole moment and energy of elasticity, respectively. Here, γ is called Lorentz Factor, α is ionic polarizability, N is dipole density, k and k' are force constant. Spontaneous polarization can occur more easily in perovskite structure due to a high value of Lorenz factor (γ = 10^2). Besides, the polarizability of the perovskite ferroelectric material is usually sensitive to temperature, inducing the phase transition. According to the *Eq. (1-3)*, it supposes that the polarizability increases as temperature decreases, so a high α will result in ferroelectric phase, i.e. $\left(k / 2Nq^2 \right) - \left(N\alpha\gamma^2 / 9\varepsilon_0^{\,2} \right) < 0$. Oppositely, the temperature increasing will lead to paraelectric phase, i.e. $\left(k / 2Nq^2 \right) - \left(N\alpha\gamma^2 / 9\varepsilon_0^{\,2} \right) > 0$. Considering a first approximation of *Eq. (1-3)*, the well-know Currie-Weiss law is derived in paraelectric phase.

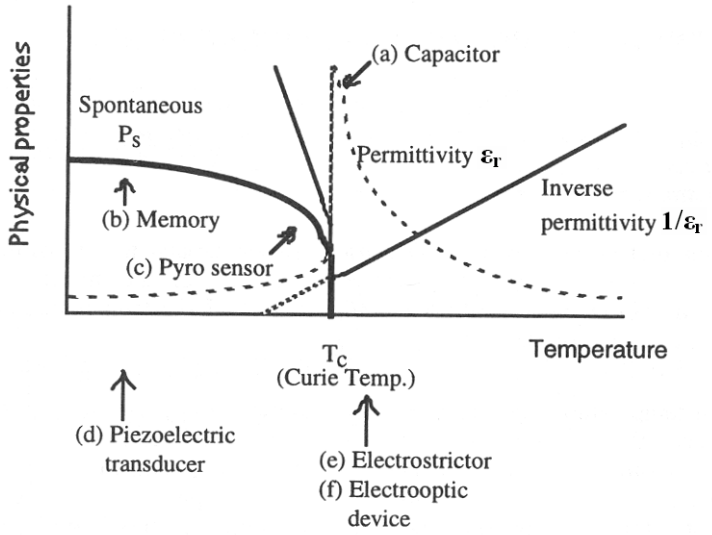
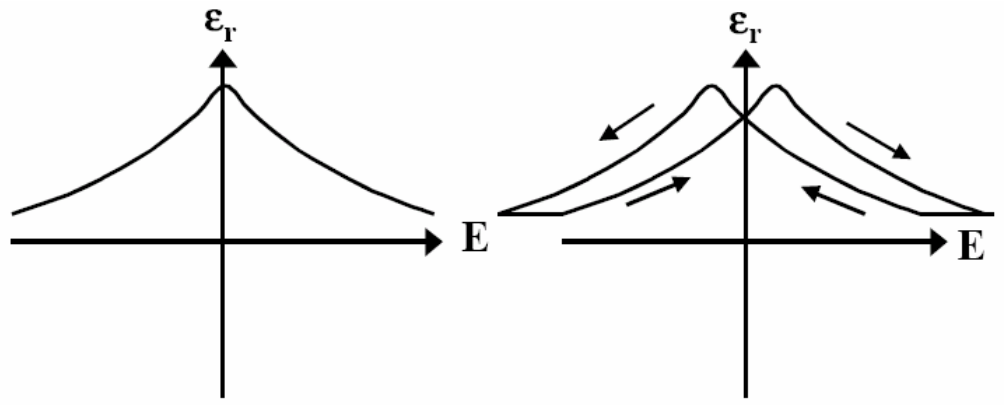


Figure 1-3 Temperature dependence of the spontaneous polarization and the permittivity in ferroelectric material. (a) – (f) indicate the temperature ranges for each application. [1]



(a) Paraelectric Phase **(b) Ferroelectric Phase**

Figure 1-4 The relation between permittivity ε_r and external field E for states of (a) paraelectric phase and (b) ferroelectric phase. [7]

$$\varepsilon = C(T - T_0), \qquad (1\text{-}4)$$

where C is the Currie-Weiss constant. T_0 is the Currie-Weiss temperature and slightly lower than the exact transition temperature T_c. While $T = T_c$, the phase transition occurs and the spontaneous polarization is continuously tending to zero. Figure 1-3 schematically shows the temperature dependence of the spontaneous polarization P_s and permittivity ε_r. P_s deceases as temperature increases and vanishes at Currie Temperature. The permittivity follows the Currie-Weiss law in paraelectric phase. The temperature ranges of each application of perovskite ferroelectric material are also denoted in the Fig. 1-3. The material in paraelectric phase, above T_c, is very promising for DRAM capacitor, and that in ferroelectric phase can be applied on nonvolatile memory. Figure 1-4 reveals the relation between permittivity ε_r and external field E for states of paraelectric phase and ferroelectric phase. Moreover, a large temperature dependence of the spontaneous polarization occurs below and near the Currie temperature, so the ferroelectric ceramic in this region is suitable for the pyroelectric sensors. These perovskite ferroelectric also possesses properties of piezoelectricity, pyroelectricity, electro-optical effect and acousto-optical effect [1-5].

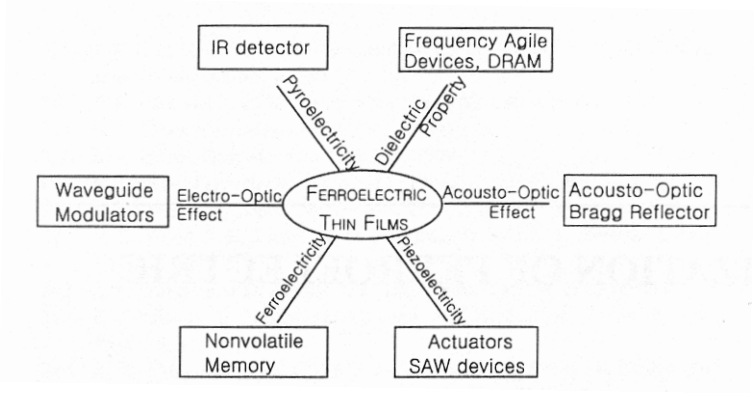


Figure 1-5 Applications of ferroelectric films. [3]

Hence, perovskite ferroelectric films can be widely applied on various electronic devices as shown in Fig. 1-5. In this dissertation, we will introduce the application of ferroelectric memory, as well as the nonvolatile random access memory (NVRAM) consisted of pervoskite (Pb,Sr)TiO3 (PSrT) films.

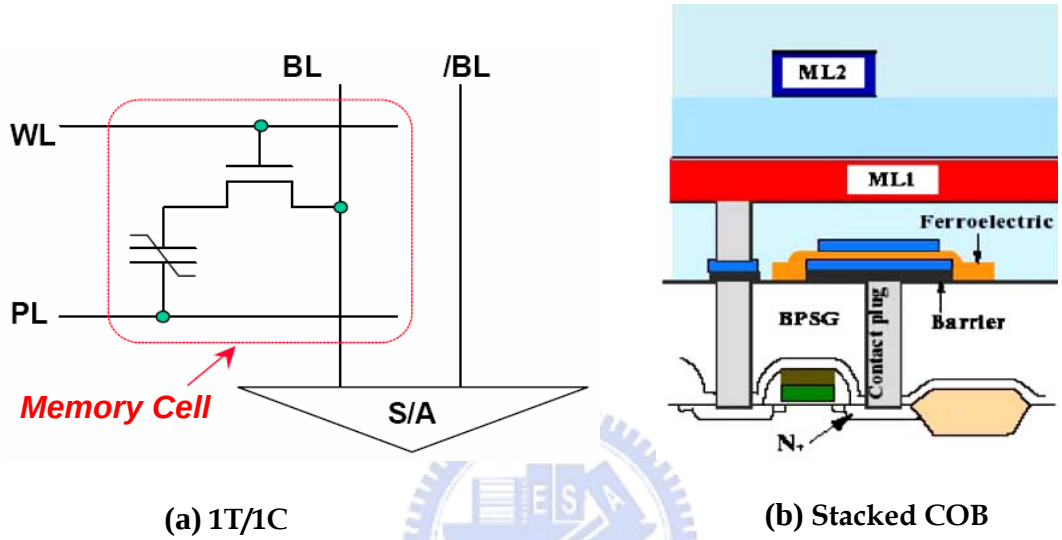


Figure 1-6 (a) Cell scheme of one-transistor/one-capacitor (1T1C) designed for FeRAM [12]. (b) Schematic stacked structure of typical ferroelectric capacitor over bit-line (COB) [13].

1-1-2 Ferroelectrics Capacitors Applied on Memory

A. Architectures of Ferroelectric Memory

Intensive research is taking place worldwide to develop a large-capacity, high-speed non-volatile memory to replace the dynamic random access memory (DRAM). A ferroelectric random access memory (FeRAM) using a ferroelectric is already mass-produced and available on the market, albeit on a small scale. As can be seen in Fig. 1-6(a), one bit of this FeRAM consists of a transistor and a capacitor

(1T1C) [11-13], which is the most commonly used. The word line (WL) and bit line (BL) are connected to the gate and drain of the transistor, accordingly. This cell is similar to a DRAM cell with the exception of the plate line (PL) which has a variable voltage level to enable the switching of the polarization of the ferroelectric capacitor, whereas its level is fixed in a DRAM. To write a "1" in the cell, the BL is set to VDD and the PL is grounded, then a pulse is applied at the WL to activate the cell transistor. Writing a "0" is accomplished in the same manner but this time the polarities of BL and PL are exchanged to reverse the polarization of the ferroelectric capacitor [11]. After the power supply is turned off, the ferroelectric capacitor can keep the digital state ("0" and "1") due to the storage of polarization (Fig. 1-2). The major difference between 1T1C FeRAM and DRAM is nonvolatile datum storage or not. Figure 1-6(b) shows the implementation of 1T1C FeRAM in a stacked structure of capacitor over bit line (COB) [8, 13], which can increase the polarization due to the capability of larger capacitor area [8].

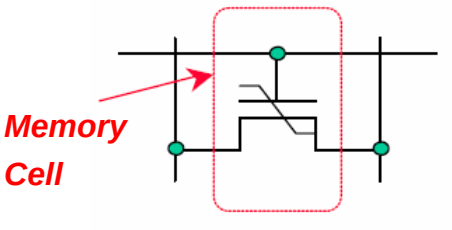
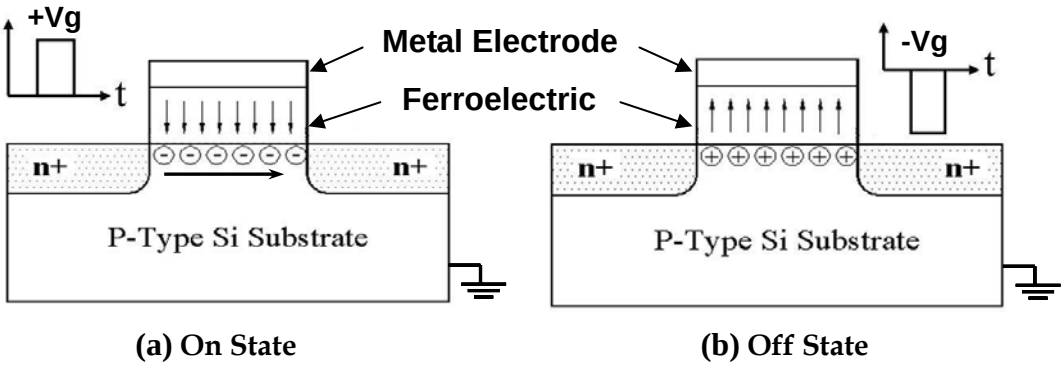


Figure 1-7 Cell scheme of one-transistor (1T) designed for FeRAM. [11]

Figure 1-7 presents another cell architecture consisted of a transistor, 1T FeRAM, which uses a ferroelectric film instead of the gate insulating film of the single field-effect transistor (FET) [10, 11]. Among several kinds of ferroelectric gate FET structures, a metal/ferroelectric/semiconductor (MFS) configuration is particularly promising due to the advantages of simple fabrication processes, low power consumption (without the voltage drop across the buffer insulator) and small memory cell size compared to its alternatives. The area required for a single cell is

merely the space occupied by the transistor. MFS-FET exploits the ferroelectric field effect, which is the modulation of conductivity by the electrostatic charges induced by ferroelectric polarization, and thus requires the direct deposition of ferroelectric thin films on silicon (Si) wafer. In this memory, the semiconductor surface conductor channel opens and closes after positive/negative voltage applied on the ferroelectric gate in response to the on/off status of FET, which dependents on the electric polarization stored by the ferroelectric film as shown in Fig. 1-8 [14]. The data memory status is read out as a function of the presence or almost absence of a flowing electric current when a voltage is applied between the drain and source electrodes on both ends of the conductor channel. An advantage of this cell type is that the reading operation does not reverse the ferroelectric polarization and the data is not destroyed (nondestructive read-out, NDRO). This structure is simple and its area is small. In this manner, the 1T FeRAM holds great promise as the ultimate semiconductor memory capable of further miniaturization (higher integration). However, there have still been the technical difficulties of achieving both a high-quality semiconductor surface and a high-quality ferroelectric, incurring the high leakage. The most important problem to be solved has been the short data retention time due to the leaky interface [10, 11].



(a) On State **(b) Off State**

Figure 1-8 Schematic device structure and operation of MFS-FET: (a) on state, and (b) off state. [14]

B. Electrical Characteristics of Ferroelectric Capacitor

Leakage current and power consumption are the critical concerns of the electrical properties applied on the memory capacitor. The conduction mechanisms of high dielectric constant or ferroelectric materials are complicated, which may be associated with dielectric itself, grain boundaries, interfacial layers, electrodes, etc. Besides, many high dielectric constant or ferroelectric materials are found to polarize in a manner that displays substantial time dependence. In addition to an essentially instantaneous or very high-frequency polarization, polarization charging current flow into such materials with a power-law time dependence of approximately t^{-n}, where $n \leq 1$ usually, as shown in Fig. 1-9 [15]. The charging current is the sum of the polarizing current, which dominates at short times because of its t^{-n} behavior, and the true leakage current is referred to the current flow from electrons or holes, which dominates at long time. Therefore it should be very careful to identify the real and steady leakage current from the polarizing current with including a proper delay time during the I-V measurements. The leakage behaviors of the ferroelectric material can be expressed by several conductive models due to many complicated mechanisms coexisted. Usually the Ohmic contact is not easily formed between the high dielectric constant or ferroelectric materials and electrodes, unless the carrier concentration of dielectrics is high enough in the interface and results in tunneling effect. Besides, the ultra-thin dielectric insulator (i.e. thinner than 30 nm) behaves tunneling current. Because there is strong temperature dependence of leakage current in the dielectrics, both Schottky emission (*SE*) (or thermionic emission) and Poole-Frenkel (*PFE*) transport are the possible conduction mechanisms [16-18]. The equations of these two conduction mechanisms are shown as the following

$$\textbf{SE}: J_{SE} = A^{*}T^{2}exp\left\{-q\left[\varphi_{B} - (qE/4\pi\varepsilon_{d}\varepsilon_{0})^{1/2}\right]/kT\right\}, \qquad (1\text{-}5)$$

$$\boldsymbol{PFE}: J_{PF} = BE\exp\left\{-q\left[\varphi_t - (qE/\pi\varepsilon_d\varepsilon_0)^{1/2}\right]/kT\right\}, \quad (1\text{-}6)$$

where A^* is the effective Richardson's constant, φ_B is the potential barrier height in the interface, B is a constant, φ_t is the trapped energy level, ε_d is the dynamic dielectric constant of the ferroelectric material in the infrared region, q is the unit charge, k is Boltzmann's constant, J is current density, T is absolute temperature, correspondingly .In addition, many researches reported lots of other theories about the leakage current, such as space charge limited current (SCLC) [19-20] and the effect of grain boundaries [21]. Consequently, the conduction mechanisms should be determined by the practical conditions, which is associated with the form of energy band diagram constructed from dielectrics, electrodes, grain boundaries, etc. [21-24].

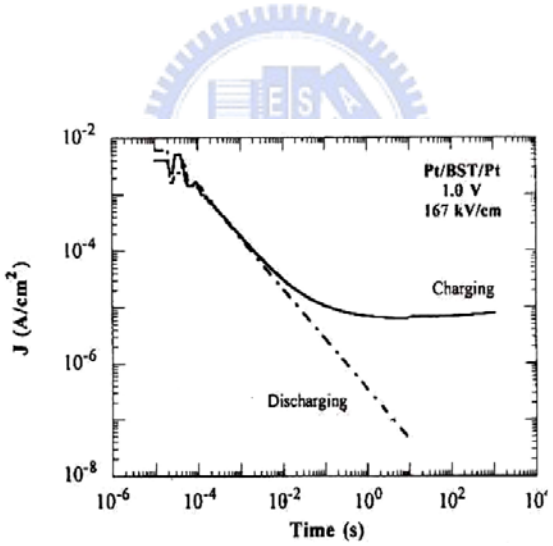
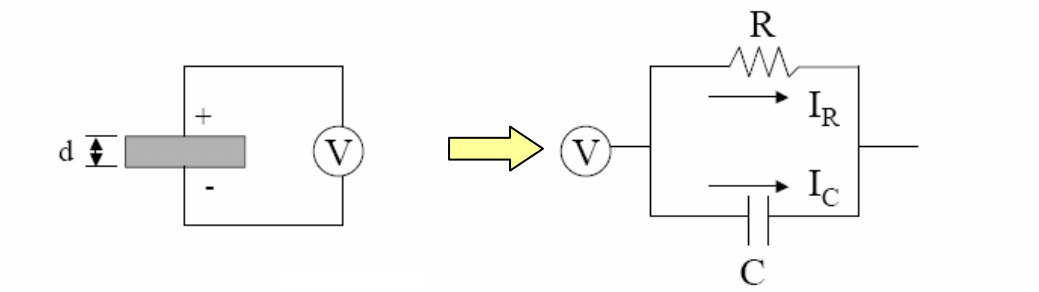


Figure 1-9 Short-time charging and discharging current in Pt/(Ba,Sr)TiO_3/Pt, exhibiting power-law behavior for the relaxation current. [15]

The tangent loss is due to the leakage current through the loss by a parallel resistance shown in Fig. 1-10 [7]. It is defined as the ratio of the leakage current through the resistance (I_R) to the leakage current through the ideal dielectric (I_C). Therefore the value of tangent loss can be extracted from the following equations:



$$Q = CV, V = V_0 e^{j\omega t}, \qquad Z = R + jX$$
$$I = \partial Q/\partial t = j\omega CV \qquad = 1/j\omega C$$
$$= j\omega C_0(\varepsilon' - j\varepsilon'')V \qquad = 1/j\omega C_0(\varepsilon' - j\varepsilon'')$$
$$= j\omega C_0\varepsilon' V + \omega C_0\varepsilon'' V \qquad = 1/\omega C_0(\varepsilon'' + j\varepsilon')$$
$$= I_C + I_R, \qquad = (\varepsilon' - j\varepsilon'')/\omega C_0(\varepsilon'' + j\varepsilon'),$$
$$\tan\delta = |I_R/I_C| = \varepsilon''/\varepsilon', \qquad \tan\delta = |\varepsilon''/\varepsilon'| = R/X,$$

Figure 1-10 The circuit model of tangent loss due to the leakage current through the loss by a parallel resistance. [7]

$$\begin{aligned} &Q = CV, \\ &V = V_0 e^{j\omega t}, \\ &I = \partial Q/\partial t = j\omega CV = j\omega C_0(\varepsilon' - j\varepsilon'')V = j\omega C_0\varepsilon' V + \omega C_0\varepsilon'' V = I_C + I_R, \\ &\tan\delta = |I_R/I_C| = \varepsilon''/\varepsilon', \end{aligned} \tag{1-7}$$

where $\varepsilon = \varepsilon' - j\varepsilon''$,

$$Z = R + jX = 1/j\omega C_0(\varepsilon' - j\varepsilon'') = (\varepsilon'' - j\varepsilon')/\omega C_0(\varepsilon''^2 + \varepsilon'^2),$$

$$\therefore \tan\delta = \varepsilon''/\varepsilon' = |R/X|, \tag{1-8}$$

where C is the capacitance, C_0 is the geometric capacitance in free space, Z is impedance, ε' and ε'' are the relative real and imaginary dielectric constants, R and X are series relative real and imaginary impedance (resistance). Usually the tangent loss comes from two mechanisms: resistive loss and relaxation loss. In the resistive loss mechanism, the energy is consumed by mobile charges in the film. In the case of

the relaxation loss mechanism, it is the relaxation of the dipole that expends the energy. Both two mechanisms of tangent loss are associated with the leakage current in the ferroelectric films, also investigated in this dissertation.

For the paraelectric or ferroelectric dielectrics, there are many electrical properties that will change with time, including the dielectric constant, remnant and saturation polarization, coercive field, tangent loss, leakage current, breakdown field, etc. Three time-dependent mechanisms will affect these electrical properties, which are aging, fatigue and resistive degradation.

Aging is generally defined as a spontaneous change in electrical properties with time, either under electrical stress or not. Fatigue is related to the ability decrease to switch the memory cell into the opposite state, after being kept programmed in one state for long periods of time. This effect is related to the polarization decrease in the hysteresis loop and it is proportional with the increasing number of switching cycles. Both mechanisms are found in ferroelectric states and believed due to the pinning of domain walls from charge trapping, oxygen vacancies and associated defect dipoles [2, 25-27].

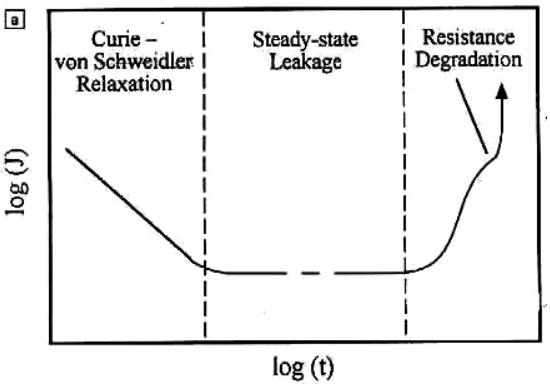


Figure 1-11 Scheme of different current regimes in metal-insulator-metal systems containing ferroelectric films. [28]

The third mechanism is time-dependent dielectric breakdown (TDDB), which is also referred as resistance degradation, for both paraelectric and ferroelectric dielectrics. It is defined as an increase of the leakage current under a constant applied electric field after prolonged times, also shown in Fig. 1-11 [28]. In this dissertation, the mechanisms of leakage, fatigue and TDDB for (Pb,Sr)TiO_3 (PSrT) films were methodically addressed.

1-1-3 Fabrication Methods of Ferroelectric Thin Films

Experientially, fabrication methods of perovskite thin films can be categorized into three types, such as chemical solution deposition (CSD), chemical vapor deposition (CVD) and physical vapor deposition (PVD).

1. *Chemical solution deposition (CSD)*

   The dielectric and ferroelectric films can be deposited by spin coating in CSD technique such as sol-gel [3, 22-24] and metal-organic deposition (MOD) [3]. Easy process, low cost, high throughput and simple facility requirement are the advantages of CSD technique. Although there are many advantages for CSD technologies, numerous problems still exist in this technology, such as the contamination control in the solvent and the porosity after baking. Besides, poor control of the perovskite phase stoichiometry can stem from varieties of the chemical source conditions. Poor step coverage and film crack after annealing are another problems.

2. *Chemical vapor deposition (CVD)*

   The CVD technology, such as metal-organic chemical vapor deposition (MOCVD) [29, 30], liquid source misted chemical vapor deposition (LSMCVD) [3, 4], etc., can fabricate ferroelectric film for high-density devices due to excellent step coverage and uniformity. However, more complicated

mechanisms of CVD process results in difficult process control, and the high temperature post-treatments are needed for removing the carbon species from precursor. Besides, the process temperature of CVD is still very high for CMOS technology because of the chemical reaction requirement. Also utilizing metal-organic precursors, with which the technique is so called MOCVD, reduces the process temperature. However, more complicated mechanisms of the process are resulted and the remove of carbon species from precursors is needed with post-treatments (curing and annealing). Besides, LSMCD is one of CVD methods to deposit dielectrics. Only single precursor is misted by atomizer, carried to a chamber by Ar carrier gas and deposited on a substrate. The drying (baking and curing) and high-temperature crystallization (annealing) processes are also needed. However, the uniformity for run to run is not stable.

3. *Physical vapor deposition (PVD)*

The PVD technique includes sputtering [3, 6-8], pulsed-laser deposition (PLD) [3, 31] … etc. Sputtering is a term used to describe the technology in which atoms are removed from the target surface by collision with high energy particles. Sputtering can afford to perform a uniform thickness using large area target. Besides, sputtering is a low cost, mature and easy-controlled technique. However, poor step coverage and different sputtering yield for different elements are disadvantages of sputtering. PLD can easily achieve a wide variety of stoichiometry of ferroelectric film, which is simple, versatile, and capable of epitaxy growth and excellent crystallinity without subsequent high-temperature annealing. In this dissertation, the excmier pulsed-laser deposition technique was applied on the fabrication of PSrT film.

Mostly, ferroelectric thin films require low-temperature processes for IC and MEMS applications to prevent the formerly-fabricated structure from thermal damage. The high-temperature process will result in the volatilization of Pb-O in lead-titanate-based films, the loss of Bi content in bismuth-tatanate-based films, the diffusion of constituent elements and/or the chemical reactions between ferroelectric film and underlying layer, which in turn affects the film composition and degrades the electric properties of ferroelectric device [3, 4, 8]. Thus, a low-thermal budget process, a relatively low-temperature process with short thermal-duration, is certainly required for the preparation of PSrT thin films.

1-2 Challenges of Advanced (Pb,Sr)TiO_3 (PSrT) Capacitors

1-2-1 Basic Properties and Literatures of PSrT Materials

$PbTiO_3$ (PTO) film has been considered for applications in nonvolatile random access memory (NVRAM), but many drawbacks of this film must be improved, such as high coercive field, high crystallization temperature, and poor microstructure. Normura and Sawada investigated polycrystalline samples of (Pb,Sr)TiO_3 (PSrT) ceramic system and established a complete series of solid solution from $PbTiO_3$ (PTO) to $SrTiO_3$ (STO) since 1955 [41, 42]. STO films have a cubic structure at room temperature and characterized by lower crystallization temperature and lower dielectric constant than those of PTO films [43, 44]. PTO and STO films, at room temperature, behave a tetragonal structure (ferroelectric phase) and a cubic structure (paraelectric phase), respectively, because PTO has the Curie temperature (T_c) at 490 ^oC and STO has the T_c at -220 ^oC. The T_c can be linearly adjusted from -220 ^oC to 490 ^oC by varying the lead (Pb) content in the PSrT ceramics as indicated in Fig. 1-12 [42]. It is reported that PTO forms continuous range of solid solution with STO, the lattice

volume and the tetragonality (c/a, the ratio of c-axis/a-axis lattice constant) of PTO decrease with the increment of Sr/Pb composition ratio [44-47], presented in Fig. 1-13. The effects of lead substituted by strontium (Sr) in the PTO film decrease the crystallization temperature and offer a good control of the dielectric properties at room temperature [47, 48].

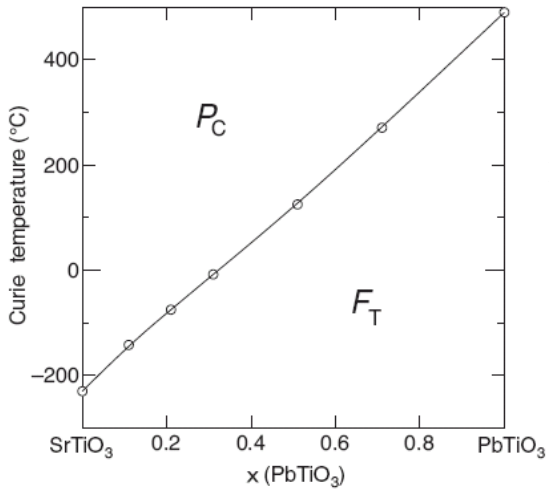


Figure 1-12 Phase diagram of $PbTiO_3$–$SrTiO_3$ system. [42]

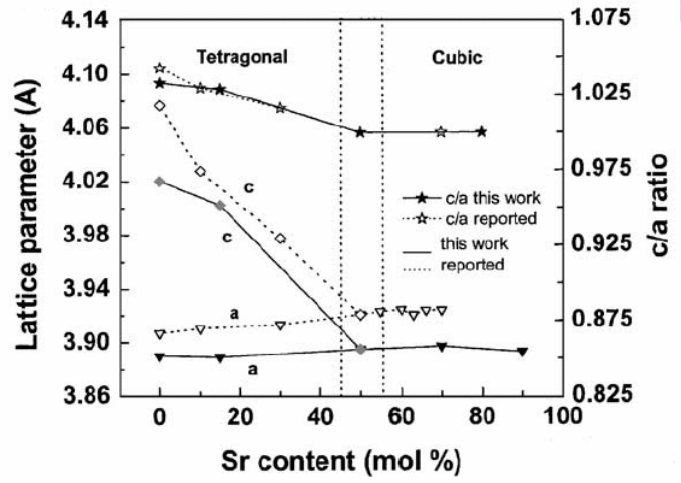


Figure 1-13 Lattice parameters at room temperature as a function of Sr/Pb composition. [45]

Moreover, PSrT have aroused considerable interest in the composite effect of negative and positive TCR (NTCR and PTCR), firstly found in 1988 [49]. In the past studies [50-55], PSrT ceramics are found to exhibit a NTCR behavior below T_c and the PTCR effect above T_c. Figure 1-14 indicates that the resistivity-temperature

properties of PSrT ceramics are functions of the composition Sr/Pb ratio and also affected by the fabrication process, such as the different sintering techniques. Therefore, PSrT is suitable for memory, sensor, frequency tuning devices and microwave applications due to its large electric-field-dependent dielectric constant and composition-dependent Curie temperature [42-60].

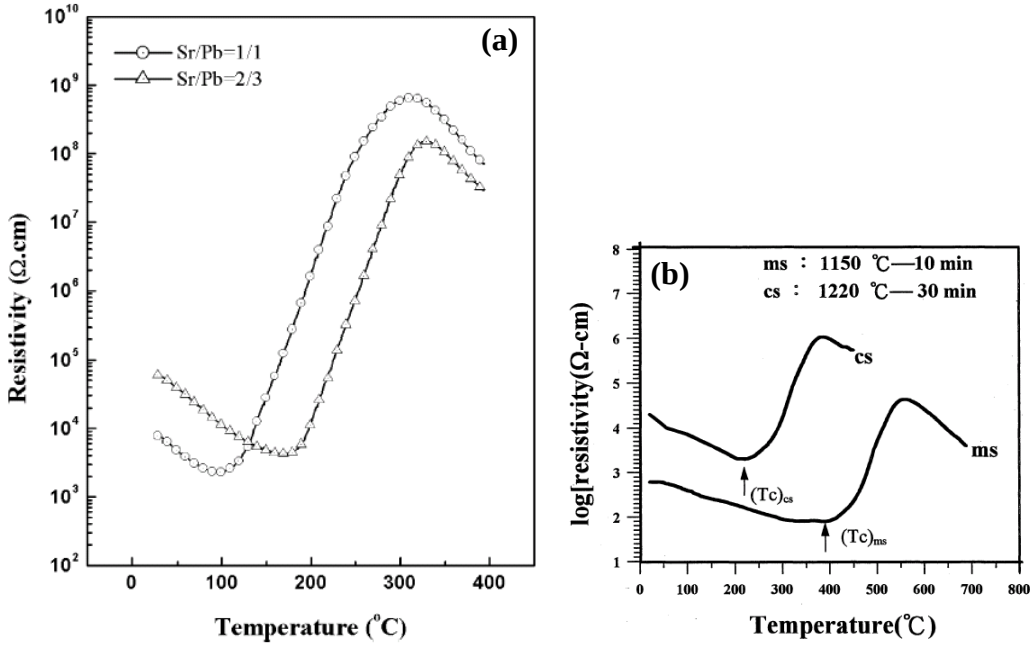


Figure 1-14 Resistivity-temperature proprieties of PSrT ceramics affected by (a) the composition Sr/Pb ratio [51] and (b) the sintering techniques, such as microwave sintering (ms) and conventional furnace sintering (cs) [50].

1-2-2 Challenges of PSrT Capacitors Integrated with CMOS IC Process

PSrT is the superior candidate material of future NVRAM, but there are still some challenges for the integrations of CMOS process.

1. *CMOS devices deformed by high temperature process*

In general, high deposition temperature (> 550 °C) of PSrT films is frequently

applied to obtain good crystallinity of a perovskite structure [42, 47, 56-60], but the high temperature process may deform the junction profile and alter the gate length of the metal-oxide-semiconductor (MOS) FET, especially on the deep submicron scale. In stacked-capacitor structure, the dopant of MOS-FET is always implemented prior to the capacitor fabricated, which needs to be fabricated at low temperature to avoid the damage of the MOS-FET.

2. *Suitable bottom electrode formation of PSrT capacitor*

Usually, there is serious reaction or inter-diffusion between ferroelectric and bottom electrode during the deposition processing at high temperature. A thermally and electrically stable bottom electrode is indeed required for ferroelectric capacitor prepared at relatively low-temperature. Here, Table 1-1 lists down the most significant requirements of bottom electrode for stacked PSrT capacitor.

3. *Dramatic variations of the electrical properties for the device operating in various temperatures*

As mentioned, PSrT exhibits strong TCR properties, especially when temperature approaches T_c. It means that the electrical properties of PSrT, i.e. leakage current, can dramatically change with temperature. Thus, the T_c of PSrT is necessary to be much higher than the temperature of memory operation. In general, the operation junction-temperatures for consumer IC applications and is designed lower than 125 °C and qualification spec ranges from –0 °C to +120 °C (ambient temperature ranging of –40 – +120 °C). In this dissertation, the TCR properties of PSrT are performed to sure if the normal device operation can be obtained at ≥ 120 °C.

4. *Unwilling interface properties between PSrT and silicon due to high temperature process*

The high-temperature process will cause the diffusion of constituent elements and/or the chemical reactions between ferroelectric film and underlying silicon, which produce undesirably high density of interfacial trap states. Thus, a leaky interface and high leakage current will appear and destroy device characteristics of MFS-FET. A low-temperature technique is the key for the using of PSrT in 1T FeRAM.

Therefore, the thin film technologies of the PSrT capacitors must overcome the above tough blockade, or it should be impossible to achieve the practical NVRAM applications.

Table 1-1 Summarized requirements of bottom electrode for stacked PSrT capacitor.

No.	List of the bottom electrode requirements
1	Must remain conductive after PSrT deposition
2	Must not react with PSrT
3	Must maintain low contact resistance to underlying plug
4	Must adhere to silicon, silicon dioxide & plug material
5	Must be depositable using production tools
6	Must be etchable down to deep submicron features

1-3 Method of Attack

It is clear that the low-temperature preparing techniques are necessary for PSrT films applied on memory. Furthermore, the noble metal platinum (Pt), with low resistivity, is considered as the electrode material because of its low power consumption and RC delay, and good stability to lead-based perovskite materials [4, 57]. In dissertation, we perform two approaches for this goal expressed as following

1. *PSrT films post-treated by novel laser-assisted annealing*

A low-thermal budget treatment, laser-assisted annealing, is proposed to improve the poor crystallinity of PSrT films deposited at extremely low temperature. The multi-layer structure of Pt/PSrT/Pt/Ti/SiO_2/p-type Si was used in this work. The specific parameters of PSrT film preparation and post-annealings were carefully controlled. The thinner (~ 120 nm) PSrT film was adapted due to the limited depth of laser absorption in ferroelectrics. The novel laser-assisted two-step process, the combination of initial crystal seed induced by ELA and the grain growth carried out by subsequent RTA, which may be a potential technique to improve the crystallinity and electrical properties of PSrT films and systematically investigated in this dissertation.

2. *PSrT films prepared by pulsed-laser deposition*

A relatively low-temperature (≤ 450 ^{o}C) pulsed-laser deposition is conducted to prepare PSrT film for two architectures, MFM and MFS, which are used to simulate the devices of COB and MFS-FET, accordingly. The process parameters were seriously controlled, and the material characterizations and electrical properties were scientifically conducted to obtain the optimal process conditions. The corresponding mechanisms were also thoroughly studied in this dissertation.

1-4 Motivation

This dissertation dedicated in obtaining excellent characteristics of PSrT capacitor fabricated by novel low-temperature technologies. The motivation and the major concepts of this study are listed below.

1. *Enhancing the crystallinity of PSrT films using the novel technique of laser-assisted annealing*

Low temperature prepared PSrT films usually exhibit poor crystallinity, so the films have to be post treated by the annealing process to enhance the crystallinity and ferroelectricities. A novel low-temperature technique, using excimer laser annealing (ELA) and subsequent rapid thermal annealing (RTA), was introduced in this work due to its very low thermal budget and high crystallization efficiency. ELA is an extremely powerful technology to achieve a successful integration process of IC at low temperature due to the shallow depth of energy absorption without the damage of under layer devices. Although ELA technology is widely used for preparing poly-Si thin film in thin film transistor (TFT) industry, but up to now, very few investigations report the ELA influence for ferroelectric films. Even though the process temperatures are high, the using of RTA process has been proposed for reducing the total thermal budget for depositing ferroelectric films. Thus, the novel laser-assisted two-step process, the combination of initial crystal seed induced by ELA and the grain growth carried out by subsequent RTA, which may be a potential technique to improve the crystallinity and electrical properties of PSrT films and systematically investigated in this dissertation.

2. *Optimizing the process controls for PLD PSrT thin film fabricated at relatively low temperature*

In general, the technique of the pulsed-laser deposition (PLD) is simple, versatile, and capable for growing a wide variety of stoichiometric oxide films without subsequent high-temperature annealing. Although a low-temperature technique is required for the deposition of PSrT in the semiconductor process,

controlling the crystallinity and ferroelectricities is normally more difficult with a low-temperature technique than with a high-temperature technique. The structural and the electrical characteristics of PLD ferroelectric films are strongly affected by the process parameters, such as substrate temperature and oxygen ambience. These process parameters and the electrical mechanisms were systematically studied to obtain the optimal process conditions.

3. *Investigating the temperature dependent properties of PSrT film*

PSrT have aroused considerable interest in the composite effect of negative and positive temperature coefficient of resistance (NTCR and PTCR). The TCR effect of PSrT bulk prepared by conventional ceramic solid state sintering processes has been reported. However, the TCR properties of PSrT thin films lack for systematically studies, which can be used as thermistor sensor embedded into micro-electro-mechanical systems (MEMS). Besides, the stable ferroelectricity of PSrT films is indeed necessary for memory application during the operation temperature of IC. PSrT films exhibit high stability of leakage current and film resistance below 150 ^{o}C, which is important and suitable for memory application. The strong negative temperature coefficient of resistance (NTCR) behavior at the ranging of 100 – 390 ^{o}C can be also obtained in film-type PSrT.

4. *Investigating the feasibility of Low-temperature pulse-laser-deposited PSrT films applied in metal/ferroelectric/silicon (MFS) gate structure of 1T-FeRAM*

PLD PSrT films can demonstrate well crystallinity and good ferroelectricities at low temperatures, which is a superior candidate for the MFS-FET devices. To date, much less is known about the properties of PLD PSrT films deposited on Si substrate. In our dissertation, the low-temperature PLD PSrT films can show

the enhanced crystallinity, few interfacial trap states and excellent fatigue endurance. Thus, a high-quality MFS structure without the buffer layer between PSrT films and Si substrate has been developed.

1-5 Thesis Organization

This dissertation reports how the novel low temperature techniques applied on the fabrication of PSrT capacitor. The multilayer structure of Pt/PSrT/Pt and the configuration of Pt/PSrT/Si were proposed to simulate the practical capacitor over a bit-line (COB) and metal/ferroelectric/semiconductor (MFS) configuration of 1T FeRAM, respectively. Material characterizations and electrical measurements are scientifically conducted in this dissertation.

Chapter 2 presents the details of the experimental concepts and the equipments of this dissertation. The experimental procedures, PSrT thin film fabrication processes, the treatments of post-annealings, and the techniques of material characterization and electrical measurement will be introduced in this chapter.

Chapter 3 reports the effects of various post-annealing techniques applied on the PSrT films. The detail analyses of physical properties and electrical characteristics are methodically discussed for PSrT films treated by RTA, ELA, and the novel laser-assisted two-step process.

Chapter 4 reveals the characteristics of the low-temperature PLD PSrT films. The well crystallinity and excellent ferroelectricities of PSrT can be achieved at low-temperatures by PLD technique. The corresponding analysis of the material, electrical properties and mechanisms are systematically performed in this chapter.

Chapter 5 investigated the influences of ambient oxygen pressure on the

low-temperature PLD PSrT films. Process parameters were carefully controlled and then the experimental results show ambient oxygen pressure plays a most important role in PLD process. The physical properties, electrical characteristics and related mechanisms will be thoroughly studied.

Chapter 6 indicates the temperature-dependent properties of Pt/PSrT/Pt capacitor. PSrT thin films have received much attention lately for their potential applications in the nonvolatile random access memory (NVRAM) and sensors. This chapter will focus on the temperature-dependent current density as well as the temperature coefficient of resistance (TCR) of film-type PSrT.

Chapter 7 demonstrates a structure of Pt/PSrT/Si capacitor to simulate the MFS configuration of ferroelectric gate FET. The interfacial properties and corresponding electrical characteristics will be methodically discussed. The excellent fatigue endurance with small variation of memory windows after 10^{10} fatigued switching can be realized in this investigation.

Chapter 8 makes summary and conclusions for this dissertation.

Chapter 9 addresses future prospects and innovative topics for further research.

Chapter 2 Experimental Overview

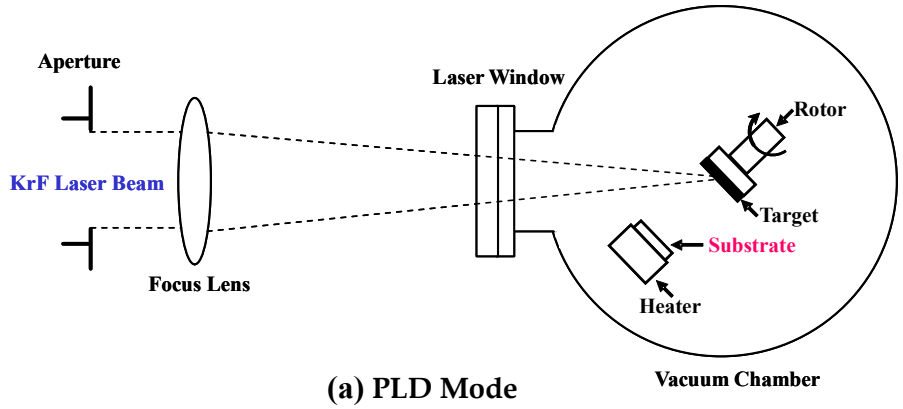
2-1 Background of Excimer Laser

2-1-1 General Feature of Excimer Laser

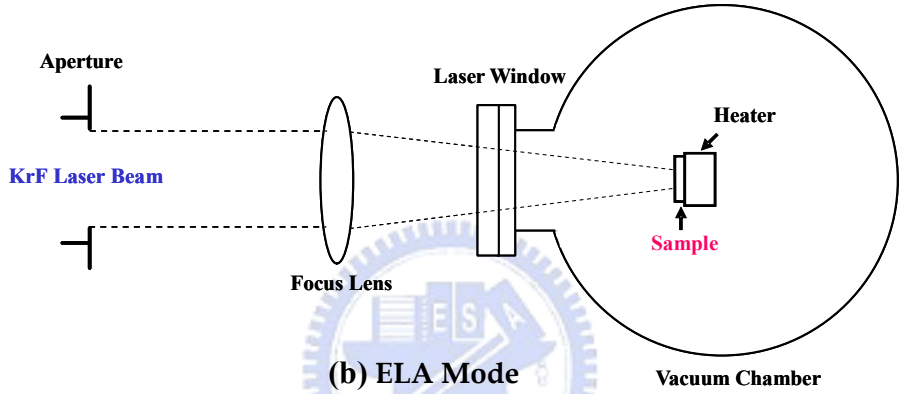
Excimer laser is the most powerful UV light source, and that has been widely applied on the semiconductor industry, such as lithography, thin film fabrication and post annealing [31-33]. The term excimer is short for 'excited dimer'. Under the appropriate conditions of electrical stimulation, a pseudo-molecule called a dimer is created, which can only exist in an energized state and can give rise to laser light in the ultraviolet range. An excimer laser typically uses a combination of an inert gas (Argon, krypton or xenon) and a reactive gas (fluorine or chlorine). Table 2-1 shows that the various wavelengths (λ), between 157 ~ 351 nm, can be obtained using different laser gas, and all excimer lasers are pulsed laser modes. In this dissertation, an equipment of KrF excimer laser (Lambda Physik Excimer Laser LPX 210i, λ=248 nm) was used as the light source of pulsed-laser deposition (PLD) and excimer laser annealing (ELA), which were proposed for PSrT film fabrication and post-annealing, accordingly. The mode of PLD or ELA can be adjusted by the modulation of optical lens of this laser equipment as shown in Fig. 2-1. The detail concepts of PLD and ELA are addressed as following.

Table 2-1 Wavelength (λ) of an excimer laser depends on the gas molecules used.

Excimer Laser Gas	F_2	ArF	KrF	XeBr	XeCl	XeF	CaF_2	KrCl	Cl_2
Wavelength (λ)	157 nm	193 nm	248 nm	282 nm	308 nm	351 nm	193 nm	222 nm	259 nm



(a) PLD Mode



(b) ELA Mode

Figure 2-1 Schematic drawings of the practical laser system for (a) PLD mode and (b) ELA mode conducted in this dissertation.

2-1-2 Concepts of Pulsed-Laser Deposition (PLD)

Rather than burning or cutting material, the excimer laser adds enough energy to disrupt the molecular bonds of the surface tissue, which effectively disintegrates into the air in a tightly controlled manner through ablation rather than burning. Moreover, excimer lasers have the useful property that they can remove exceptionally fine layers of surface material with less heating or change to the remainder of the material which is left intact. Hence, pulsed-laser deposition (laser ablation) is a superior technique for expressing the intrinsic properties of materials to

permit the formation of a high-quality laminate film.

Experimentally, PLD is extremely simple among all thin film growth techniques. Fig. 2-1(a) shows a schematic diagram of an experimental setup of PLD. It contains a target tray and a sample holder with heater in this vacuum chamber. A high-power KrF laser is used as an external energy source and is focused to the target surface by optical lens. As for basic mechanisms for pulsed laser sputtering [31], five different sputtering mechanisms are described as

1. *Collision sputtering*

   Collision sputtering in the sense of momentum transfer in direct beam-surface interactions cannot occur with laser pulsed. But indirect collision effects do, however, exist with photons.

2. *Thermal sputtering*

   Thermal sputtering, in the sense of vaporization from a transiently heated target, may require temperatures well above the melting of boiling points.

3. *Electronic sputtering*

   Electronic sputtering is not a unique process, but rather a group of processes having the common feature of involving some form of excitation or ionization.

4. *Exfoliational sputtering*

   Exfoliational sputtering, as when flakes detach from a target owing to reaped thermal shocks, would show an obvious and characteristic topography which is dominated in our work.

5. *Hydrodynamic sputtering*

   We use the term hydrodynamic to refer to processes in which droplets of material are form and expelled from a target as a consequence of the transient

melting, processes that have no analog in ion-surface interactions.

The secondary mechanism include various types of pulsed flow processes (outflow with reflection, effusion with reflection, and effusion with re-condensation) that differ both depending on whether the release is from the surface or from a reservoir , and also depending on whether particles that are backscattered toward the surface are reflected or absorbed (i.e. re-condensed).

Pulsed laser deposition is often described as a three-step process consisting of vaporization of a target material, transport of vapor plume, and film growth on a substrate. These steps are repeated thousands of time in a typical deposition run. Therefore, the structural and the electrical characteristics of PLD ferroelectric films are strongly affected by the process parameters. In this dissertation, the most two important process parameters of PLD, ambient oxygen pressure and substrate temperature, were fully investigated.

2-1-3 Concepts of Excimer Laser Annealing (ELA)

The low-temperature (≤ 200 °C) PLD PSrT films usually have poor crystallinity and unwilling ferroelectricities, so those films must be post annealed to improve the electrical properties. Figure 2-1(b) displays the schematic diagram for practical ELA setup. ELA can be carried out with low mechanical stress under low substrate temperature, but its process window is very hard to be controlled. The ELA technique can achieve local-high-temperature heating within very short duration time, which has been applied in the formation of ultra-shallow junction [34] and the production of low-temperature poly-silicon (LTPS) thin film transistor (TFT) [36-38]. However, the reports of ferroelectric films treated by ELA are very limited [39, 40]. Table 2-2 lists the comparisons of various post treatment technologies on

ferroelectrics. The advantage of ELA is obvious, except the concern of throughput. This chapter describes how a novel excimer laser annealing (ELA) technique can achieve local-high-temperature heating and crystallize the amorphous PSrT films. Physical and electrical properties are examined to study the detailed effects of excimer laser annealing on PSrT films. Furthermore, the novel laser-assisted two-step process, the combination of initial crystal seed induced by ELA and the grain growth carried out by subsequent RTA, which may be a potential technique to improve the crystallinity and electrical properties of whole PSrT films. The detail comparisons of various post-annealings are also presented.

Table 2-2 Summarized comparisons of various post-treatment technologies.

	Thermal Budget	Uniformity	Mechanical Stress Releaseing	Mass Production Throughput
Furnace Annealing	High	Δ	O	O
Microwave Annealing	High	O	Δ	Δ
Rapid Thermal Annealing (RTA)	Low	Δ	X	Δ
ELA with Optical Scanning System	Low	Δ	O	X *

*** The Throughput of ELA technique can be improved by equipment modifications.**

O: Good Δ: Normal X: Worse

2-2 *Experimental Details*

2-2-1 PSrT Films Post-Treated by Novel Laser-Assisted Annealing

A low-thermal budget treatment, laser-assisted annealing, is proposed to improve the poor crystallinity of PSrT films deposited at extremely low temperature (200 °C). Figure 2-2 shows the multi-layer structure of Pt/PSrT/Pt/Ti/SiO_2/p-type

Si used in this work. The Pt/Ti films of 100/4 nm were subsequently sputtered onto the SiO_2/Si as the bottom electrode/adhesion layer. The thinner PSrT film is adapted due to the limited depth of laser absorption in ferroelectrics. Table 2-3 describes the specific parameters of PSrT film preparation and post-annealings. The as-deposited PLD PSrT thin films were post treated by a rapid thermal annealing (post-RTA) technique (JetFirst Processor, Jipelec) with the conditions as following: the ambient oxygen gas flowing rate was 100 sccm, the process temperatures were 450 or 600 ^{o}C, the heating rate was programmed as 30 ^{o}C/sec or 50 ^{o}C/sec, respectively. Furthermore, the as-deposited films were also annealed by a novel laser-assisted two-step process: post-excimer laser annealing (post-ELA) and subsequent RTA (post-ELA + RTA). After the modulation of optical lens of the KrF excimer laser system, the post-ELA was processed with the conditions: the substrate temperature, the ambient oxygen pressures (P_{O_2}), the laser pulsed rate, the average laser energy fluence (LEF) and the number of laser pulses were 300 ^{o}C, 80 mTorr, 1 Hz, 47.6 – 105.6 mJ/cm^2 per pulse, 40 - 180 pulses, respectively. The LEF of laser pulse was calibrated inside the vacuum chamber by a photodiode meter. The subsequent RTA was executed at 450 or 600 ^{o}C in oxygen ambience with 60 sec duration time. The detail analyses of physical properties and electrical characteristics are methodically discussed for PSrT films treated by RTA, ELA, and the novel laser-assisted two-step process. After the physical examinations, the Pt top electrodes, with a diameter of 165 μm, were deposited by sputtering and patterned by shadow mask process. Next, the voltage was biased on the top electrode, and the bottom electrode was grounded for electrical measurements. The design of experiment is listed as step by step in Fig. 2-3.

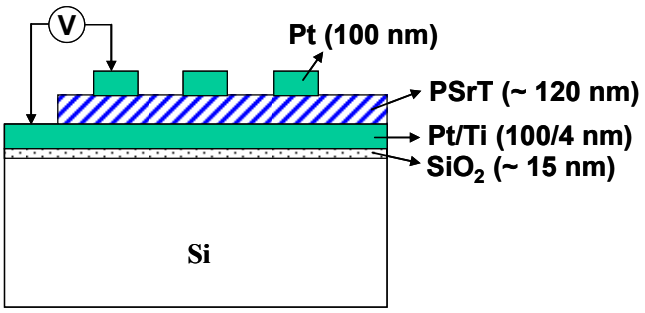


Figure 2-2 Schematic view of the multilayer structure conducted for PSrT films post-annealed in this dissertation.

Table 2-3 The process conditions of PSrT film treated with post-annealings: (a) PLD parameters for as-deposited PSrT film, and (b) post-annealing parameters of ELA and RTA.

(a) PLD Parameters for As-deposited PSrT Film	
Laser	KrF Excimer Laser (λ = 248 nm)
Target	$(Pb_{0.6}Sr_{0.4})TiO_3$ Ceramic Bulk
Distance between Target and Substrate	4 cm
Substrate	$Pt/Ti/SiO_2/Si$
Substrate Temperature (T_s)	200 °C
Ambient Oxygen Pressure (PO_2)	80 mTorr
Laser Energy Fluence (LEF)	1.55 J/cm^2 per pulse
Laser Pulsed Rate	5 Hz
PSrT Film Thickness	~ 120 nm

	(b) Post-Annealing Condition of PSrT Film	
ELA Parameters	Laser	KrF excimer laser (λ = 248 nm)
	Substrate Temperature (T_s)	300 °C
	Ambient Oxygen Pressure (PO_2)	80 mTorr
	Laser Pulses	40 – 180
	Laser Energy Fluence (LEF)	47.6 – 105.6 mJ/cm^2 per pulse
	Laser Pulsed Rate	1 Hz
RTA Parameters	Ambient Oxygen Flowing Rate	100 sccm
	Annealing Temperature	450 – 600 °C
	Heating Rate	30 – 50 °C/sec
	Annealing Duration	60 sec

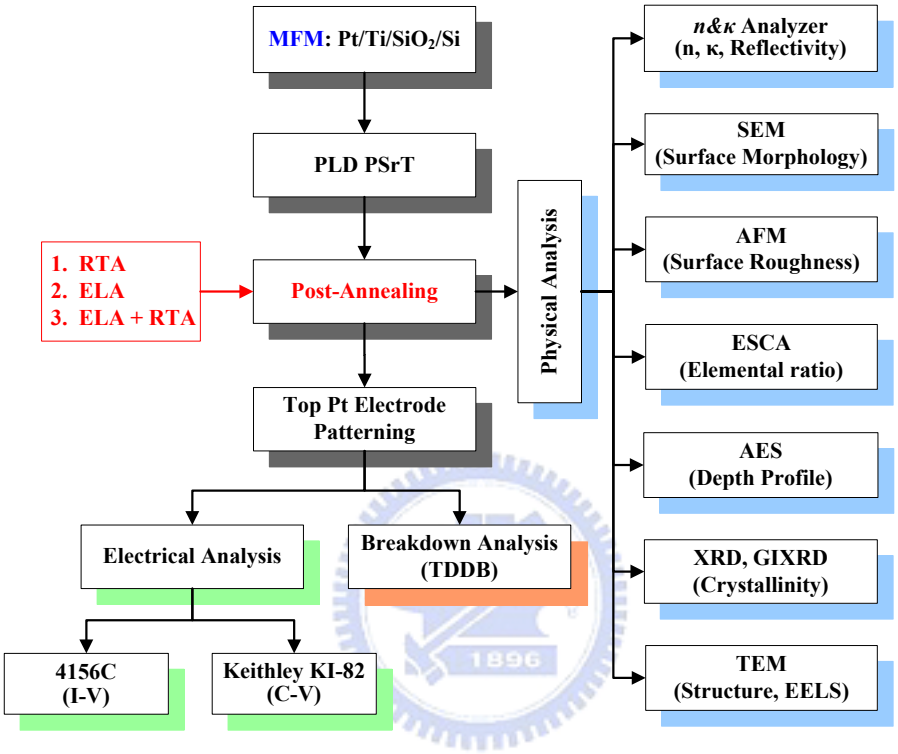


Figure 2-3 The experimental flow of PSrT films treated by post-annealing.

2-2-2 PSrT Films Prepared by Pulsed-Laser Deposition

A relatively low-temperature (≤ 450 °C) pulsed-laser deposition is conducted to prepare PSrT film for two architectures, metal/ferroelectric/metal (MFM) and metal/ferroelectric/semiconductor (MFS) (Fig. 2-4), which are used to simulate the devices of COB and MFS-FET, accordingly. PLD PSrT films (200 nm thick) were deposited on the $Pt/SiO_2/Si$ substrate or p-type Si (100) wafer. The deposition temperature (substrate temperature, T_s) varied from 300 °C to 450 °C, calibrated at the wafer upper surface. It means that a thermal couple, connected to a temperature controller, was used to touch the surface of samples and sense the temperature of $Pt/SiO_2/Si$ substrate, denoted as T_s. During the PLD process, the oxygen partial pressure, target to substrate distance, laser pulsed rate, and average laser power density (laser energy fluence) were 80 - 200 mTorr, 4 cm, 5 Hz, and 1.55 J/cm^2 per pulse, respectively, as denoted in Table 2-4. The physical properties of PSrT films were analyzed before Pt top electrode deposition. Then, the Pt top electrodes, with a thickness of 100 nm and a diameter 75 μm, were deposited by sputtering and patterned by shadow mask process to form a MFM capacitor structure or a MFS configuration.

The relationships among process parameters, physical properties, and electrical characteristics were systematically studied to obtain the optimal process conditions. The related mechanisms of conduction and fatigue will be thoroughly studied in this dissertation. Figure 2-5 reveals the detail experimental flow.

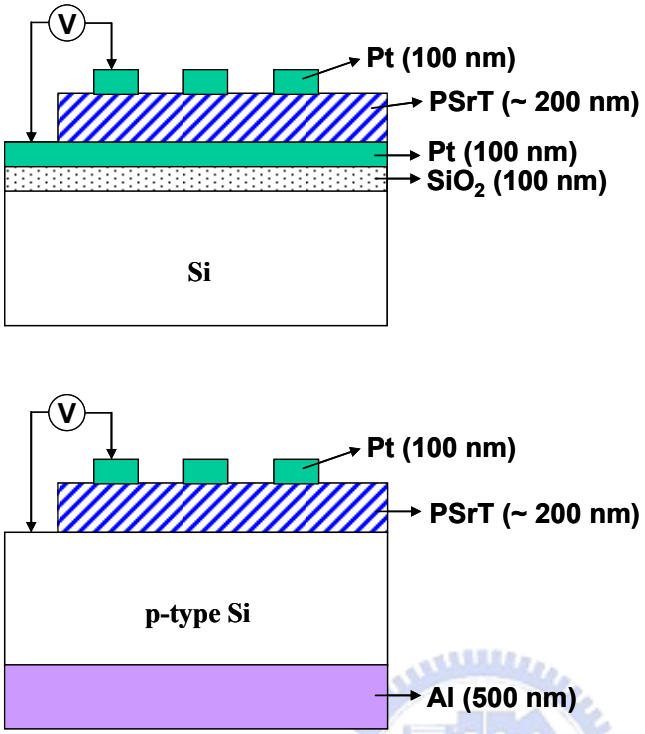


Figure 2-4 Schematic view of PSrT films applied in (a) MFM and (b) MFS structures in this dissertation.

Table 2-4 The PLD process conditions of PSrT film.

PLD PSrT Film Condition	
Laser	KrF Excimer Laser (λ = 248 nm)
Target	$(Pb_{0.6}Sr_{0.4})TiO_3$ Ceramic Bulk
Distance between Target and Substrate	4 cm
Substrate	$Pt/SiO_2/Si$ or p- type Si
Substrate Temperature (T_s)	300 ~ 450 °C
Ambient Oxygen Pressure (PO_2)	50 ~ 80 mTorr
Laser Energy Fluence (LEF)	1.55 J/cm^2 per pulse
Laser Pulsed Rate	5 Hz
PSrT Film Thickness	~ 200 nm

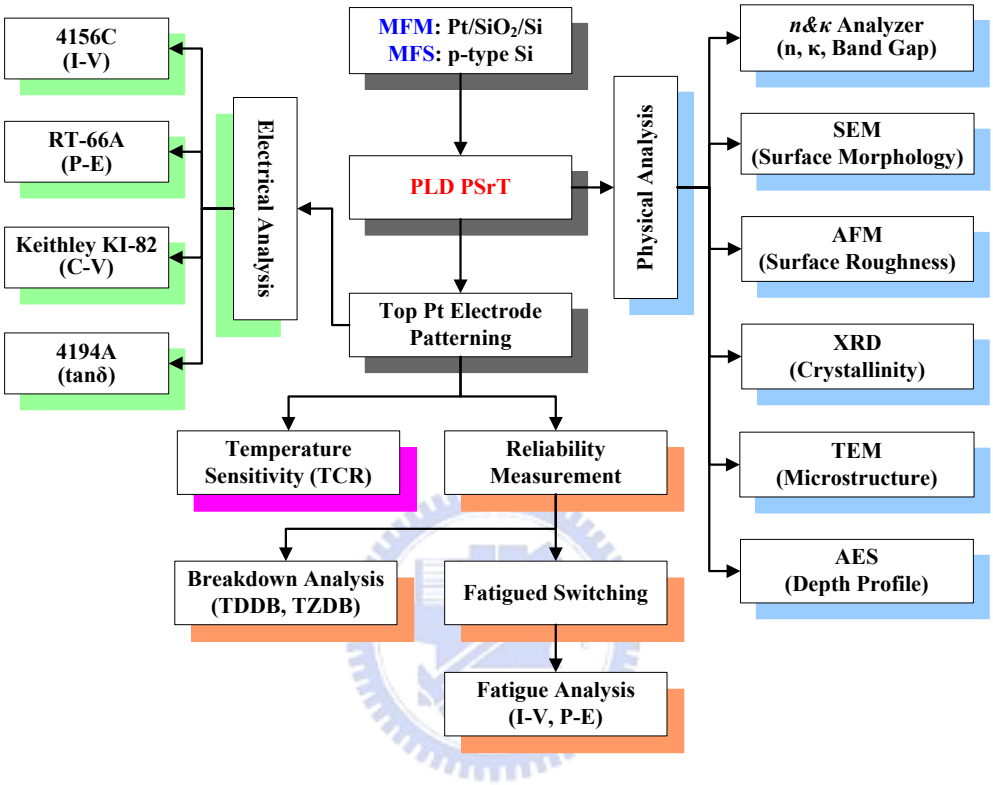


Figure 2-5 The experimental flow of PSrT films fabricated by PLD technique.

2-3 Material characterization Techniques

1. *n&κ Analyzer*

The reflectivity, refraction index (*n*), and extinction coefficient (*κ*) of PSrT film were measured by *n&κ* analyzer (1280, *n&κ* Technology). The *n* and *κ* are influenced by the electronic structure and/or crystallinity of the film. The band gap of PSrT films, E_{fg}, was also estimated by the optical investigation of *n* and *κ*.

2. *Scanning Electron Microscope (SEM)*

The thin film surface morphology, cross sectional profile, and film thickness were examined by field emission scanning electron microscopy (FESEM) (S4000, Hitachi).

3. *Atomic Force Microscope (AFM)*

The surface roughness and surface morphology were examined by AFM (DI Nano-Scope III, Digital Instruments). The root mean square value of the film roughness was calculated.

4. *Electron Spectroscope for Chemical Analysis (ESCA)*

An ESCA (ESCA 210, Fison (VG)) was performed to analyze the element ratios on the surface of PSrT films.

5. *Auger Electron Spectrum (AES)*

AES machines (Auger 670 PHI Xi, Physical Electronics, and Microlab 310D & 310F, Fison (VG)) were used to analyze the surface element ratios and element depth profile of PSrT films. The depth profiling was accomplished with incorporated ion guns that enable the specimen surface to be continuously

sputtered away while Auger electrons were being detected. Then the inter-diffusion of the elements was investigated.

6. *X-Ray Diffraction (XRD) Analysis*

Two X-Ray diffraction methods were generally used. For the theta-2 theta powder method, the detected X-ray beams are diffracted from the lattice-planes that are all parallel to the substrate. The powder method is suitable for comparison with standard X-ray powder diffraction data to find the preferred orientation in the films. Thus, the microstructures of the thin films can be characterized by a Siemens D5000 Diffractometer with Cu Kα (λ ~ 0.154 nm) radiation. However, for glancing angle method, the normals of diffracted lattice planes are not parallel to each other and incline at various angles to the substrate. The glancing method is good for phase identification and provides some "information" about orientation distribution. The crystallinity of the films with post-ELA was also analyzed by the glancing incident X-ray diffraction (GIXRD) machine (D/MAX2500, Rigaku, using Cu Kα, λ ~ 0.154 nm) with a fixed incident angle of 2 degrees.

7. *Transmission Electron Microscope (TEM)*

The crystallinity and nano-scale structure were examined by the TEM equipment (JEM-2000FX, JEOL, using the electron acceleration voltage of 200 kV). TEM samples were fabricated by standard sample preparation techniques with tripod polishing and ion milling using the Gatan PIPS system operated at 3 kV. The maximum resolution of this instrument is about 0.31nm. The diffraction pattern and bright/dark field image were performed in this investigation. The TEM was equipped with a Gatan image filter (GIF, Model 2000, Gatan) which provides the fingerprint of chemical bonding states with

high lateral/energy resolution in terms of electron energy loss spectroscopy (EELS) spectra, recorded with an energy resolution of 1.2 eV (full width at half maximum, FWHM, of zero-loss peak) and an energy dispersion of 0.3 eV per channel.

2-4 *Electrical Measurement Techniques*

After the material characterizations, the Pt top electrodes were then deposited by sputtering and patterned by shadow mask process to form the MFM capacitor or MFS gate structure. Next, the testing voltage or input signal applied on the top electrode, and the bottom electrode was grounded.

1. *Current-Voltage (I-V) Measurement*

   An automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station was used to measure the leakage current (I-V) characteristics and breakdown properties. The testing voltage biased on the top electrode, and the bottom electrode was grounded. The capacitors were stressed under various voltage to estimate the time depend dielectric breakdown (TDDB). Conduction mechanisms due to electrode-limited Schottky emission (*SE*) and bulk-limited Poole-Frenkel emission (*PFE*) in the PSrT film were investigated by analyzing current density versus electric field (J-E) curves.

2. *Capacitance-Voltage (C-V) Measurement*

   Computer-controlled Keithley package 82 system was used to obtain high frequency C-V and quasi static C-V simultaneous curves. The package 82 system includes a model 590 CV analyzer for high frequency C-V measurement, a model 595 quasi static C-V meter along with the 595 remote coupler, lower

noise BNC cables and IEEE 488 bus. A model 230-1 voltage source and a model 5905 calibration source are included too. In this work, the high frequency C-V data at 100 kHz were taken on the capacitor to determine the capacitance value in the accumulation mode. The dielectric constant was calculated from C-V using the following relation:

$$C = \varepsilon_r \times \varepsilon_0 \times A/d \,, \qquad (2\text{-}1)$$

where A is the capacitor area, d is the thickness of ferroelectric film, ε_0 is the vacuum permittivity, ε_r is the dielectric constant, and C is the ferroelectric capacitance.

3. *Tangent Loss Measurement*

Capacitance and tangent loss are functions of frequency, so the impedance/gain-phase analyzer (4194A, Hewlett Packard) was applied to extract the capacitance-frequency (C-f) and loss tangent-frequency (tanδ-f) data. The frequency of 4194A ranges from 100 Hz to 15 MHz. Tangent loss is an indicator of resistive leakage. The leakage path is parallel to the capacitance in the equivalent circuit. If the loss tangent increases, the impedance will decrease, then the leakage current will increase. The admittance and impedance spectra were measured as a function of frequency with 4194A impedance gain phase analyzer. The AC electrical data, in the form of parallel capacitance and conductance, were recorded in the frequency range of 100 Hz to 10 MHz at the AC signal amplitude of 0.1 V.

4. *Polarization Measurement*

The ferroelectric polarization-electric field (P-E) characteristics of the PSrT films were determined directly from virtual ground circuits (RT-66A, Radiant

Technologies). The pulse with a triangle-shaped wave at 10 kHz trains was conducted to measure the polarization. The P-E curve was obtained analytically by calculating the polarization P from the relative permittivity ε_r (dielectric constant) versus electric field E using the following equation.

$$P = \varepsilon_0 \times \int (\varepsilon_r - 1) dE \,, \qquad (2\text{-}2)$$

5. *Fatigue analysis Measurement*

A pulse generator (8110A, Hewlett Packard) and a pulse/function generator (8116A, Hewlett Packard) were connected together with low noise BNC cables to generate +3 V/-3 V bipolar wave pulsed at 1 MHz, confirmed by an oscilloscope (54645A, Hewlett Packard), as an input signal for the measurement of polarization switching degradation (fatigue). Figure 2-6 gives the schematic equipment setup and bipolar switching waveform. The measurement of fatigue analysis consists of four steps, described as (i) J-E & P-E measurements before fatigue switching, (ii) capacitors are fatigued with 1 MHz +3 V/-3 V bipolar waveform, (iii) J-E & P-E measurements after fatigue switching, and (iv) the fatigue mechanism can be analyzed by J-E curve fitting.

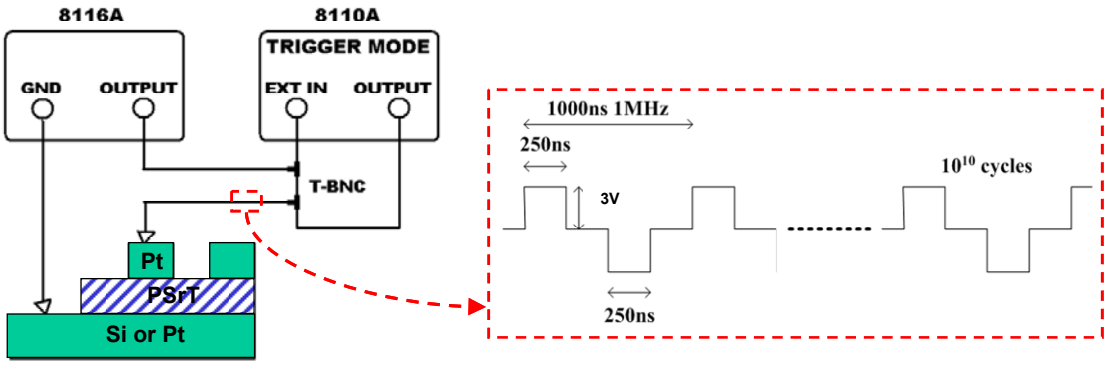


Figure 2-6 The schematic equipment setup and switching waveform for the operation of polarization bipolar switching degradation (fatigue).

Chapter 3 Studies on (Pb,Sr)TiO_3 Films Enhanced by Post-Excimer Laser Annealing (ELA) and Subsequent Rapid Thermal Annealing (RTA)

3-1 Concepts of Post-Annealing on Ferroelectrics

(Pb,Sr)TiO_3 (PSrT) films, with perovskite structure, have received much attention lately for their potential applications in memory, sensor, frequency tuning devices and microwave applications due to its large electric-field-dependent dielectric constant and composition-dependent Curie temperature [42, 47, 48, 56-58]. The PSrT film is constituted by a solid solution of $PbTiO_3$ (PTO) and $SrTiO_3$ (STO). PTO and STO films, at room temperature, behave a tetragonal structure (ferroelectric phase) and a cubic structure (paraelectric phase), respectively, because PTO has the Curie temperature (T_c) at 490 °C and STO has the T_c at -220 °C. The effects of lead (Pb) substituted by strontium (Sr) in the PTO film decrease crystallization temperature and offer a good control of the dielectric properties at room temperature [47, 48].

Ferroelectric films typically require low-temperature processes for IC and MEMS applications to prevent the formerly-fabricated structure from thermal damage. Nevertheless, depositions of ferroelectric lead-titanate films, such as PTO and Pb(Zr,Ti)O_3 (PZT), are typically conducted at high-temperatures (> 600 °C) to obtain the good crystallinity of a perovskite structure [61]. The high-temperature (> 450 °C) process will result in the volatilization of lead oxide (Pb-O compounds) in lead-titanate-based thin films [4, 62], which in turn affects the film composition and degrades the electric properties of ferroelectric device. Thus, a low-thermal budget process, a relatively low-temperature process with short thermal-duration, is

certainly required for the preparation of PSrT thin films.

In this chapter, PSrT films were prepared at 200 °C using the pulsed-laser deposition (PLD) technique and then the crystallinity of films was improved by rapid thermal annealing (RTA) technique or novel laser-assisted two-step process. Although the process temperatures are high, the using of RTA process has been proposed for reducing the total thermal budget for depositing ferroelectric films [35, 63]. The excimer laser annealing (ELA) technique is very attractive in terms of selective annealing area and local-high-temperature heating within very short duration time, which is applied in the production of low-temperature poly-silicon (LTPS) thin film transistor (TFT) [36, 37]. However, the influence of ELA is very limited on the top of ferroelectric films [35, 38-40]. Thus, the novel laser-assisted two-step process, the combination of initial crystal seed induced by ELA and the grain growth carried out by subsequent RTA, which may be a potential technique to improve the crystallinity and electrical properties of PSrT films and systematically investigated in this chapter.

3-2 Experiments

Multilayer of Pt/PSrT/Pt/Ti/SiO_2/p-type Si was used to simulate the practical capacitor over a bit line (COB). The Pt/Ti films of 100/4 nm were subsequently sputtered onto the SiO_2/Si as the bottom electrode/adhesion layer. PSrT films with 120 nm in thickness were deposited by a KrF (λ = 248 nm, pulse width = 25 nsec) pulsed-laser deposition (PLD) system (LPX 210i, Lambda Physik). A set of optical lens was used to focus the excimer laser beam onto the $(Pb_{0.6},Sr_{0.4})TiO_3$ target, prepared with conventional ceramic fabrication process [31]. During the PLD process, the target to substrate distance, the deposition temperature, the ambient oxygen

pressure (P_{O_2}), the laser pulsed rate and the average laser energy fluence (LEF) were 4 cm, 200 °C, 80 mTorr, 5 Hz and 1.55 J/cm² per pulse, respectively.

The as-deposited PLD PSrT thin films were post treated by a rapid thermal annealing (post-RTA) technique (JetFirst Processor, Jipelec) with the conditions as following: the ambient oxygen gas flowing rate was 100 sccm, the process temperatures were 450 or 600 °C, the heating rate was programmed as 30 °C/sec or 50 °C/sec, respectively. The duration time was as short as 60 sec to reduce the possible Pb-O volatilization and interfacial diffusion at high temperature [4, 35, 62, 63]. Furthermore, the as-deposited films were also annealed by a novel laser-assisted two-step process: post-excimer laser annealing (post-ELA) and subsequent RTA (post-ELA + RTA). After the modulation of optical lens of the KrF excimer laser system, the post-ELA was processed with the conditions: the substrate temperature, the P_{O_2}, the laser pulsed rate, the average LEF and the number of laser pulses were 300 °C, 80 mTorr, 1 Hz, 47.6 – 105.6 mJ/cm² per pulse, 40 - 180 pulses, respectively. The subsequent RTA was executed at 450 or 600 °C in oxygen ambience with 60 sec duration time.

The reflectivity and extinction coefficient (κ) were measured by an n&κ analyzer (1280, n&κ Technology). The surface roughness of films was inspected by atomic force microscope (AFM) (DI Nano-Scope III, Digital Instruments). The surface morphology of PSrT films were examined by field emission scanning electron microscopy (FESEM) (S-4000, Hitachi). An electron spectroscope for chemical analysis (ESCA) (ESCA 210, Fison (VG)) was performed to analyze the element ratios on the surface of PSrT films. The crystallinity of the film was analyzed by X-ray diffractometer (XRD) (D5000, Siemens, using Cu Kα, λ ~ 0.154 nm) and glancing incident X-ray diffraction (GIXRD) machine (D/MAX2500, Rigaku, using Cu Kα, λ ~

0.154 nm) with a fixed incident angle of 2 degrees. An Auger electron spectroscope (AES) (Microlab 310D, Fison (VG)) was used to analyze the element depth profile of PSrT films. Cross-sectional transmission electron microscopy (TEM) (JEM-2000FX, JEOL, using the electron acceleration voltage of 200 kV) samples were fabricated by standard sample preparation techniques with tripod polishing and ion milling using the Gatan PIPS system operated at 3 kV. The TEM was equipped with a Gatan image filter (GIF, Model 2000, Gatan) which provides the fingerprint of chemical bonding states with high lateral/energy resolution in terms of electron energy loss spectroscopy (EELS) spectra, recorded with an energy resolution of 1.2 eV (full width at half maximum, FWHM, of zero-loss peak) and an energy dispersion of 0.3 eV per channel. Next, the testing voltage biased on the top electrode, and the bottom electrode was grounded. The combination of a semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station was used to measure the leakage current (I-V) characteristics. A capacitance-voltage (C-V) analyzer (Package 82 system C-V 590, Keithley) was also used to measure C-V curves at 100 kHz.

3-3 Effects of Rapid Thermal Annealing (RTA) on PSrT Films

Figure 3-1 shows the SEM surface morphologies of PLD PSrT films un-annealed and post-rapid thermal annealed (post-RTA) at 450 and 600 °C. The un-annealed films reveal smooth and dense surface. The grain clusters of films post-RTA at 450 °C are not large enough and distinctive enough. On the contrary, films post-RTA at 600 °C show a surface image of distinctive grain clusters with obvious pin holes, which can act as defects. It suggests that the annealing time (60 sec) is too short to complete prompt grain growth. However, the longer annealing time could worsen the Pb-O volatilization and interfacial diffusion at high temperature [4, 35, 62, 63].

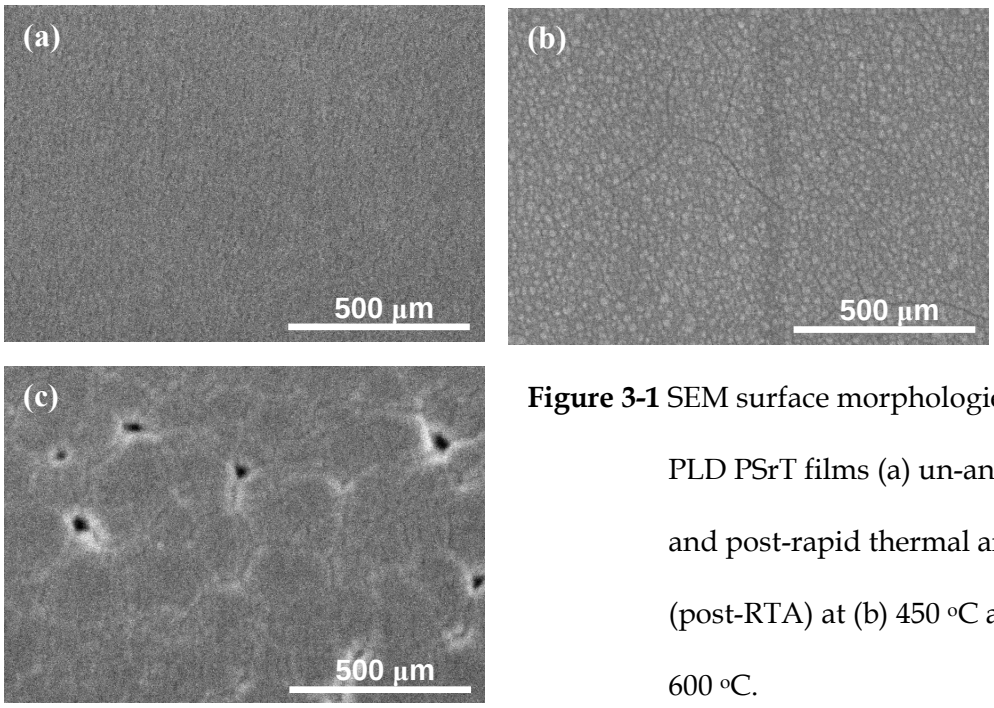


Figure 3-1 SEM surface morphologies of PLD PSrT films (a) un-annealed and post-rapid thermal annealed (post-RTA) at (b) 450 °C and (c) 600 °C.

Figure 3-2 presents the XRD pattern of films un-annealed and post-RTA. The un-annealed films are amorphous due to no apparent diffraction peaks. In contrast, the post-RTA ones exhibit the obvious diffraction peaks of $(Pb_{1-x}Sr_x)TiO_3$ perovskite structure [42, 47, 48, 58]. The diffraction peaks are indexed as (100), (110) and (211) orientations and their intensities increase as the annealing temperature increases. The crystalline PSrT films are observed at such low annealing temperature (450 °C) probably because of the addition of strontium, which induces a lower crystallization temperature of PSrT than that of PZT [35, 47, 63].

Figure 3-3 gives the capacitance versus electric field (C-E) characteristics of the PSrT films un-annealed and post-RTA. The figure presents the typical C-E hysteresis characteristics of ferroelectric materials. The capacitance shows a maximum value at negative bias, according to the coercive field (E_c) of the hysteresis loop, when the applied field sweeps from +200 kV/cm to -200 kV/cm. However, the maximum

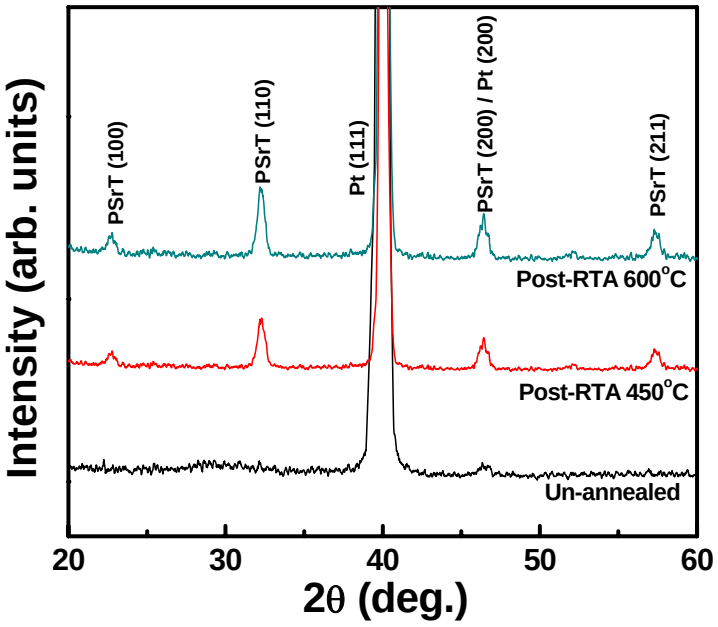


Figure 3-2 X-ray diffraction pattern of PSrT films un-annealed and post-RTA at 450 and 600 °C.

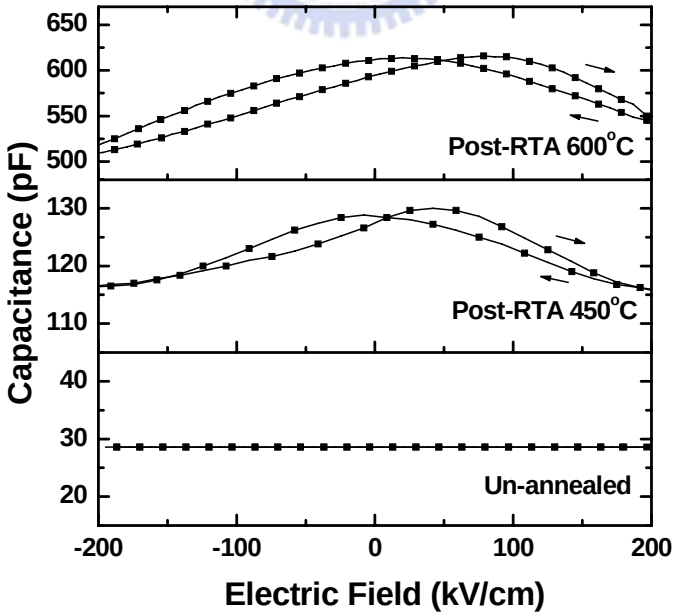


Figure 3-3 Capacitance-electric field (C-E) hysteresis loops of PSrT films un-annealed and post-RTA at 450 and 600 °C.

capacitance appears at positive E_c when the applied field sweeps in the reverse direction. It is argued that the asymmetric C-E loops can be possibly due to the different configuration of electrodes (i.e. the area of the bottom electrode is larger than that of the top electrode, as defined by shadow mask). Films un-annealed demonstrate an indistinct C-E hysteresis loop, which presents the paraelectric-like characteristic. On the contrary, it indicates that the distinct C-E hysteresis loops and larger capacitance can be obtained for films post-RTA at higher temperatures (450 - 600 °C). This result suggests that the ferroelectricity of PSrT films is evidently improved by post-RTA, which is consistent with the observation of XRD (Fig. 3-2).

Figure 3-4 displays the current density versus electric field (J-E) characteristics of Pt/PSrT/Pt capacitors under a positive bias. It is found that the leakage current is seriously increased when annealing temperature of post-RTA increases. These unwilling J-E characteristics could be linked to the defects (Fig. 3-1) and interfacial diffusion (addressed later) induced by post-RTA. As mentioned above, it is clear that the crystallinity and ferroelectricity of PSrT films can be visibly improved by post-RTA. However, the seriously deteriorative J-E characteristics of post-RTA films will restrict the application of memory.

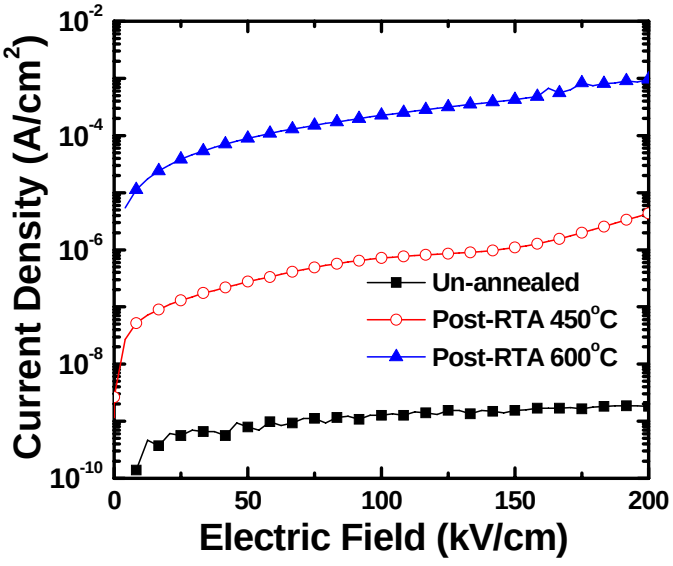


Figure 3-4 Current density versus electric field (J-E) characteristics of PSrT films un-annealed and post-RTA at 450 and 600 °C.

3-4 *Effects of Excimer Laser Annealing (ELA) on PSrT Films*

3-4-1 Physical analysis

Figure 3-5 shows the reflectivity and the extinction coefficient (κ) of amorphous PLD PSrT thin film for light wavelength from 190 nm to 900 nm. The reflectivity of 248-nm laser light for nearly amorphous PSrT film is 0.236. Thus, the incident energy transmitting into PSrT is as much as 76.4%. The law of absorption for the light intensity $I(x)$ of a parallel beam propagating in x-direction is described as follows [40]

$$I(x) = I(x=0)e^{-\alpha(\omega)x}, \quad (3\text{-}1)$$

$$\alpha(\omega) = 2\omega\kappa(\omega)/c = 4\pi\kappa(\omega)/\lambda, \quad (3\text{-}2)$$

where α(ω) is the absorption coefficient, ω is the angular frequency and $\kappa(\omega)$ is the extinction coefficient. The distance d for the intensity of propagating light decay to $1/e$ (1/2.718) as

$$\alpha d = 1,$$

$$d = 1/\alpha = \lambda/(4\pi\kappa(\omega)),$$

The $\kappa(\omega)$ of PSrT for 248-nm light is as high as 0.996 and d = 19.8 nm. Most of the propagating energy of the laser beam is absorbed to heat on the top 19.8 nm of PSrT film. The absorbed heat transfers from the PSrT surface to the interior region of the PSrT film and the underlayer films.

To precision probe into the effects of ELA on PSrT films, the following as-deposited specimens were also treated by mock-ELA with zero laser pulse (un-annealed) to deduct the influence of substrate heating during ELA process from later discussion. Figures 3-6 give the optical microscope surface images of PSrT films

un-annealed and post-excimer laser annealed (post-ELA) at laser energy fluence (LEF) of 47.6 mJ/cm² per pulse with 180 pulses. It is seen that a plume of surface color/brightness dispersion obtained in post-ELA films, reflecting the changes on optical property and/or microstructure of films.

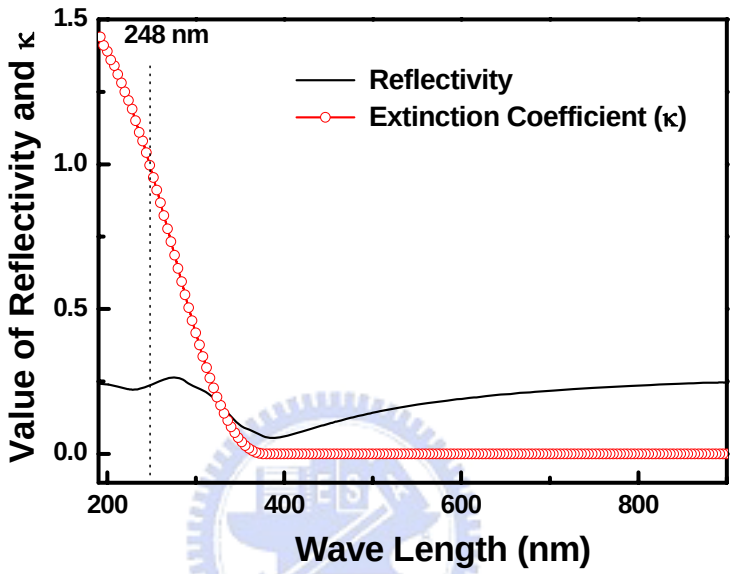


Figure 3-5 The reflectivity and the extinction coefficient (κ) of amorphous PLD PSrT thin film for light wavelength from 190 nm to 900 nm.

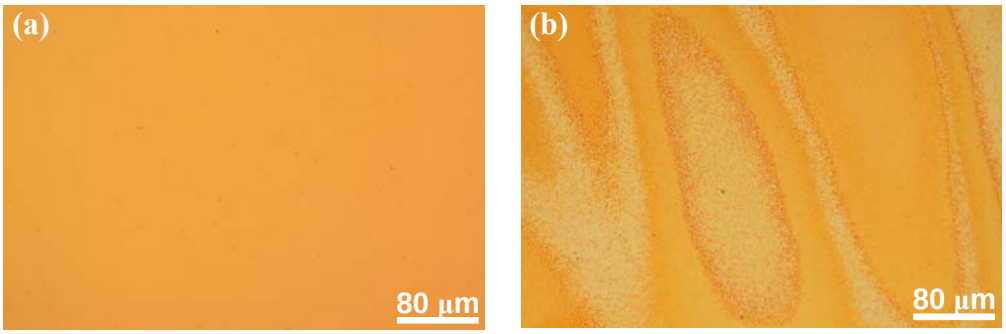


Figure 3-6 Optical microscope surface images of PSrT films (a) un-annealed and (b) post-excimer laser annealed (post-ELA) at laser energy fluence (LEF) of 47.6 mJ/cm² per pulse with 180 pulses.

Figure 3-7(a) displays the AFM images of PSrT films and indicates the surface morphology varies with the laser pulses associated with the heat reaction induced by laser irradiation. For numerical analysis, Fig. 3-7(b) gives the normalized root-mean-square roughness (R_{RMS}), revealing that the minimum R_{RMS} and maximum R_{RMS} are 0.5 nm and 8.5 nm for films un-annealed and post-ELA with 180 pulses, respectively, and then R_{RMS} decrease slightly with more laser pulses.

Figure 3-8 demonstrates the element ratios, evaluated from the integrated area of peaks with their according sensitivity factors, were analyzed on the film surface by ESCA technique. It reveals that the O/(Pb+Sr) varies from 2.83 to 3.07 as laser pulse increases, which can be connected to that the ELA experiment was executed in oxygen ambience. The element ratios of Pb/(Pb+Sr), Sr/(Pb+Sr) and Ti/(Pb+Sr) seem independent with the increasing of laser pulse. It suggests that the oxygen deficiency on the surface of films can be strongly compensated with more laser pulses.

Figure 3-9 displays the GIXRD pattern of PSrT films un-annealed and post-ELA with various numbers of laser pulses. The diffraction peaks are indexed as (100), (110), (200) and (211) orientated-planes of $(Pb_{1-x}Sr_x)TiO_3$ perovskite structure [42, 47, 48, 58]. The intensity of (200) orientation can be consisted of $(200)_{PSrT}$ and $(200)_{Pt}$, which is not evidently vary with the laser pulses, as opposed to those of (100), (110) and (211) orientations. However, the inset XRD pattern reveals that no obvious change between un-annealed film and post-ELA one with 120 pulses. In the basis of results of GIXRD and XRD, it suggests that the crystallinity of the upper region of films is evidently enhanced with the increasing of laser pulse, which is conformable to the calculated result of *Eq. (3-1)* and *Eq. (3-2)*: most of the propagating energy of the laser beam is absorbed within the upper region (~ 19.8 nm) of PSrT film. Nevertheless, too many laser pulses (180 pulses) incurs the intensity decreases of

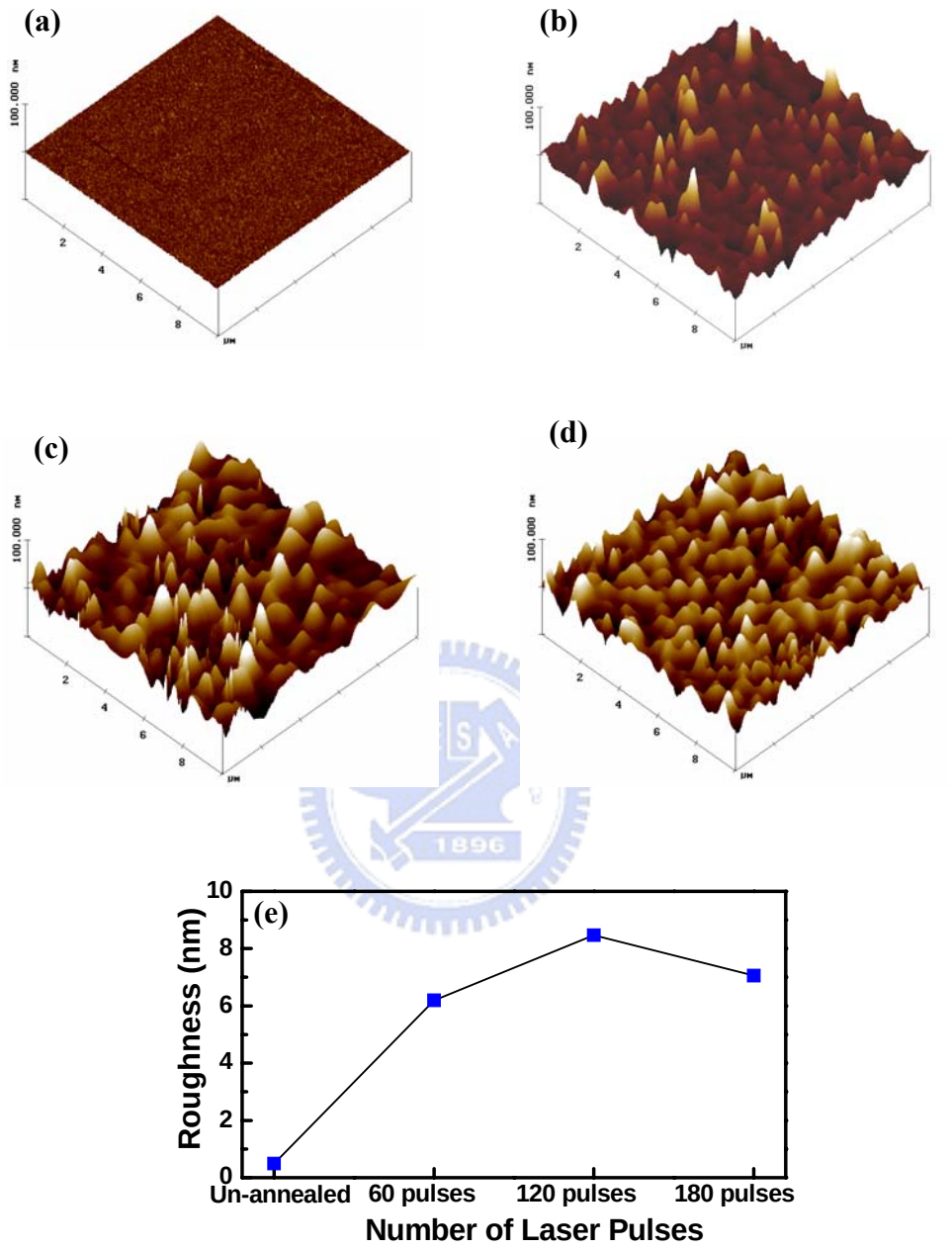


Figure 3-7 (a)-(d) AFM images and (e) surface roughness of PLD PSrT films un-irradiated and post-excimer laser annealed (post-ELA) with various numbers of laser pulses: (a) un-annealed, (b) 60 pulses, (c) 120 pulses and (d) 180 pulses.

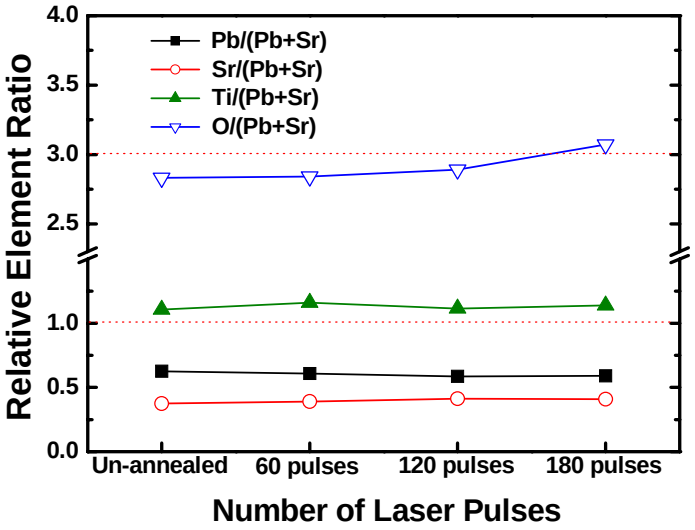


Figure 3-8 Relative element ratios (analyzed by ESCA technique) of PSrT films un-annealed and post-ELA with various numbers of laser pulses.

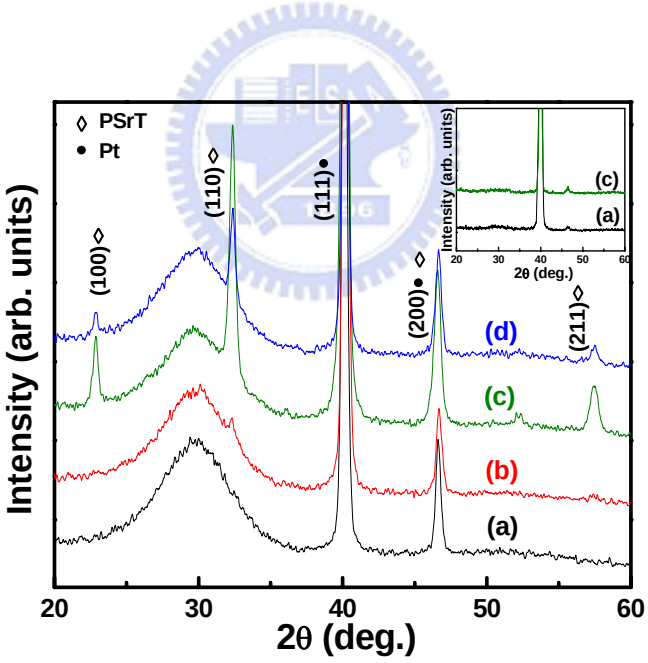


Figure 3-9 Glancing incident X-ray diffraction (GIXRD) pattern and the inset conventional XRD pattern for PSrT films un-annealed and post-ELA with various numbers of laser pulses: (a) un-annealed, (b) 60 pulses, (c) 120 pulses and (d) 180 pulses.

(100), (110) and (211) orientations, which may associate with the preferred orientation transited with the accumulated laser pulses [67, 68]. This observation is important that the heat, induced by ELA, can be evidently accumulated with laser pulses even the ELA experiments were configured as using the high thermal-conductivity (71.6 $Wm^{-1}K^{-1}$) of bottom electrode (Pt), a low laser pulse rate (1 Hz) and a low LEF (47.6 mJ/cm^2 per pulse) within the very short pulse width (25 nsec).

Figures 3-10 show the cross-sectional TEM images and selected-area diffraction patterns (SADPs) to investigate the microstructure of films, influenced by the accumulated laser pulses. The image of un-annealed PSrT film (Fig. 3-10(a)) can not be observed obvious contrast grains and its corresponding SADP also confirms the amorphousness with a diffused ring pattern. In contrast, post-ELA one reveals an image of a large reversed-pyramid single-grain (Fig. 3-10(b)), confirmed with the inset SADP, indicating that the crystallinity of films is greatly enhanced after ELA treatment. Furthermore, it reveals an image of large reversed-pyramid single-grain with inhomogeneous nano-size grains and a poly-crystallinity, confirmed with the minified bright-field/dark-field (BF/DF) images as seen in Figs. 3-10(c)-(d). The enlarged BF image of region *A* in Fig. 3-10(c) was shown in Fig. 3-10(e). It clearly shows that the size of nano-size grains reduced from film top to film bottom, which presents that the most of the propagating energy of the laser beam is absorbed within the upper region of PSrT film. The corresponding SADP (Fig. 3-10(f)) shows an intensive ring pattern and indicates the crystallinity of films is greatly enhanced after ELA treatment, consistent with the results of GIXRD and XRD analyses. However, the grain growth induced by ELA is not uniform and the influence of laser irradiation only works on the upper region of PSrT films since the radiation of KrF laser is heavily absorbed in a thin surface layer [39, 40]. It means that only few

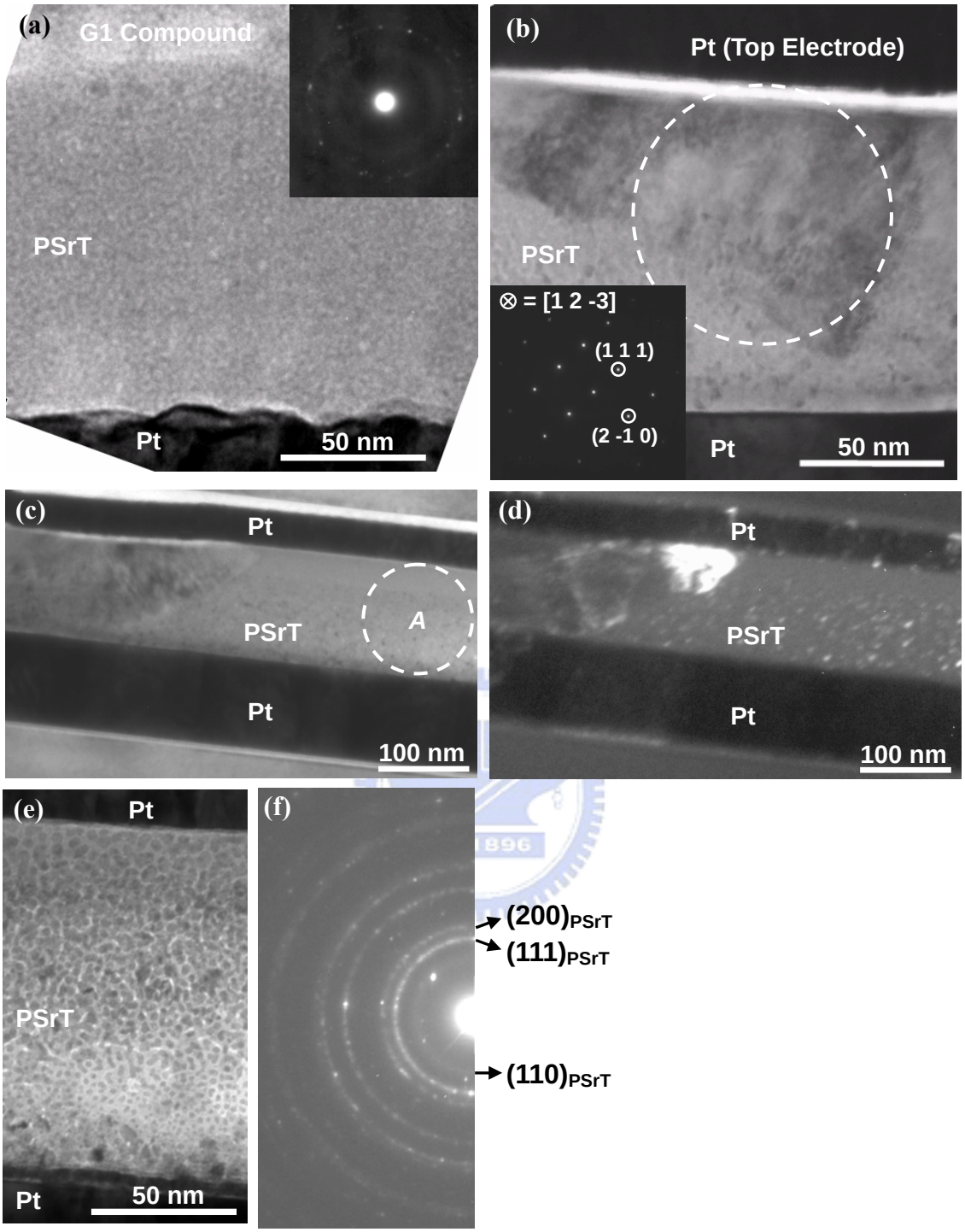


Figure 3-10 Cross-sectional TEM images and selected–area diffraction patterns (SADPs) of PSrT films un-irradiated and post-ELA at LEF of 47.6 mJ/cm^2 per pulse with 180 pulses: (a) bright-field (BF) image and SADP of un-annealed, (b) BF image and SADP of post-ELA, (c) minified BF image, (d) minified dark-field of post-ELA (DF) image of post-ELA, (e) enlarged BF image of region *A* and (f) SADP of region *A*.

nano-size grains can grow into large grains and most of nano-size grains would repeat the procedures of coarsening, dissolving and nucleation during the accumulated laser pulses, observed in excimer laser annealed poly-silicon [67, 68]. The detection of non-uniform and inhomogeneous grain growth can be linked to the plume of surface color/brightness dispersion obtained in post-ELA films (Fig. 3-6(b)).

Figure 3-11 provides the EELS spectra of zero-loss peak and shows a distinguishable difference in peak positions between the films un-annealed and post-ELA with 120 pulses, implying the change of microstructures [69, 70]. Nevertheless, the detailed evolution of microstructure and crystallinity during the duration between laser pulses is not clear at present. Since it is difficult to transform the whole PSrT film into provskite structure by post-ELA, a further treatment is necessary to do after ELA, such as a subsequent RTA.

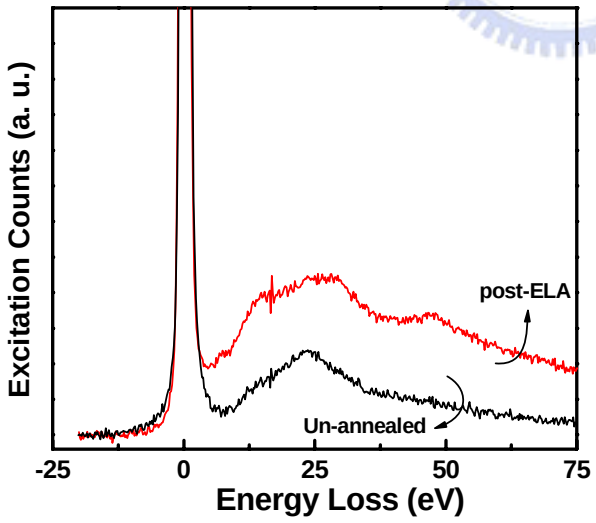


Figure 3-11 Electron energy loss spectroscopy (EELS) spectra of zero-loss peak.

3-4-2 Electrical Analysis

Figure 3-12 gives the capacitance versus electric field (C-E) characteristics of the PSrT films post-ELA with various numbers of laser pulses. It is argued that the

asymmetric C-E loops can be possibly due to the influence of ELA on the upper region of films. The dielectric constants, evaluated from the zero-field capacitance, are 18.1, 20.7, 61.7 and 46.8 for films un-annealed and post-ELA with 60, 120 and 180 pulses, respectively, which are consistent with the change of diffraction intensities. It indicates that the distinct C-E hysteresis loops and larger dielectric constants can be obtained with more laser pulses (≥ 120), suggesting that the ferroelectricity of post-ELA PSrT films is improved.

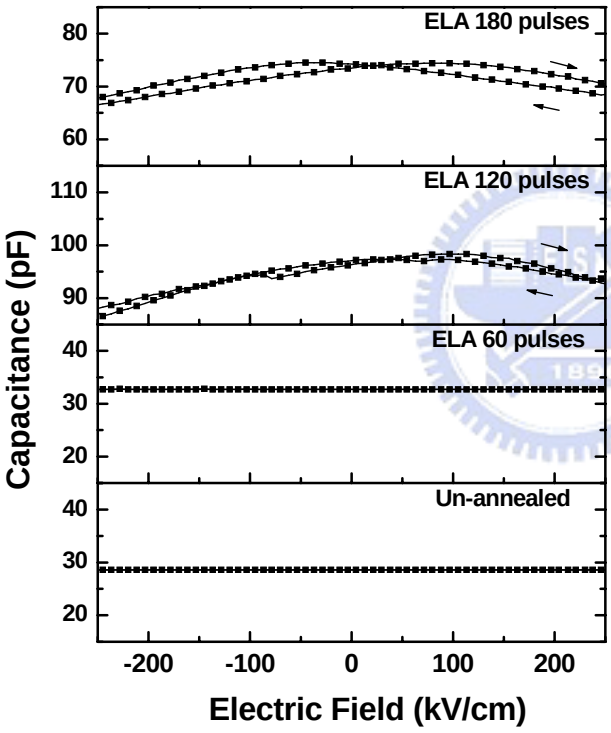


Figure 3-12 Capacitance-electric field (C-E) hysteresis loops of PSrT films un-annealed and post-ELA with various numbers of laser pulses.

Figure 3-13(a) displays the current density versus electric field (J-E) characteristics of Pt/PSrT/Pt capacitors under positive/negative biases. The leakage current is usually associated with the oxygen stoichiometry and interfacial properties of ferroelectric films [40, 66]. Thus, the leakage current of films deteriorates with the laser pulses principally due to the rougher surface. In addition, the inhibited leakage current is found when the number of laser pulse exceeds 120, attributed to the

compensated oxygen deficiency and reduced roughness on the surface of films, as well as a superior surface. The asymmetry of J-E curves is more observable as the increasing of laser pulse. Since both of the top and bottom electrodes are made from Pt materials, the larger leakage current under a negative bias can be linked to the interface defects in the upper electrode [71, 72].

Later in the text, the leakage current data under a negative bias are interpreted as Schottky emission (*SE*) at lower electric fields and Poole-Frenkel emission (*PFE*) at higher electric fields to analyze the trap state correlated to interface-limited and bulk-limited characteristics, accordingly [16, 40, 66]. Figure 3-13(b) presents the *SE* plot of Pt/PSrT/Pt capacitors post-ELA at various laser pulse counts. If the conduction current follows *SE* behavior, then a log (J/T^2) against $E^{1/2}$ plot should be linear, where T is absolute temperature. Similarly, a log (J/E) against $E^{1/2}$ plot can be made for *PFE*. As the number of laser pulse is 0 – 120, the increases of leakage current of films biased at lower electric fields are dominated by the more surface states and more surface defects, induced by ELA process. However, when the number of laser pulse exceeds 120, the inhibited leakage current of films biased at lower fields is correlated with the less surface states and fewer surface defects due to the superior surface (i.e. the compensated oxygen deficiency and reduced roughness on the surface of films). Moreover, it indicates that the conduction characteristics of PSrT films mainly are governed by *SE*, except the films post-ELA with more laser pulses (≥ 120) biased at higher fields. Figure 3-13(c) shows the *PFE* plot using the same experimental current-voltage (I-V) data. As laser pulses ≥ 120, it reveals that the *PFE* behavior is obtained at high applied fields, inferring that the deep trapping states are generated as laser pulses, which can be connected to the grain boundary defects of the large single-grains and the coarsening nano-crystallinity induced by ELA process (Fig. 3-10).

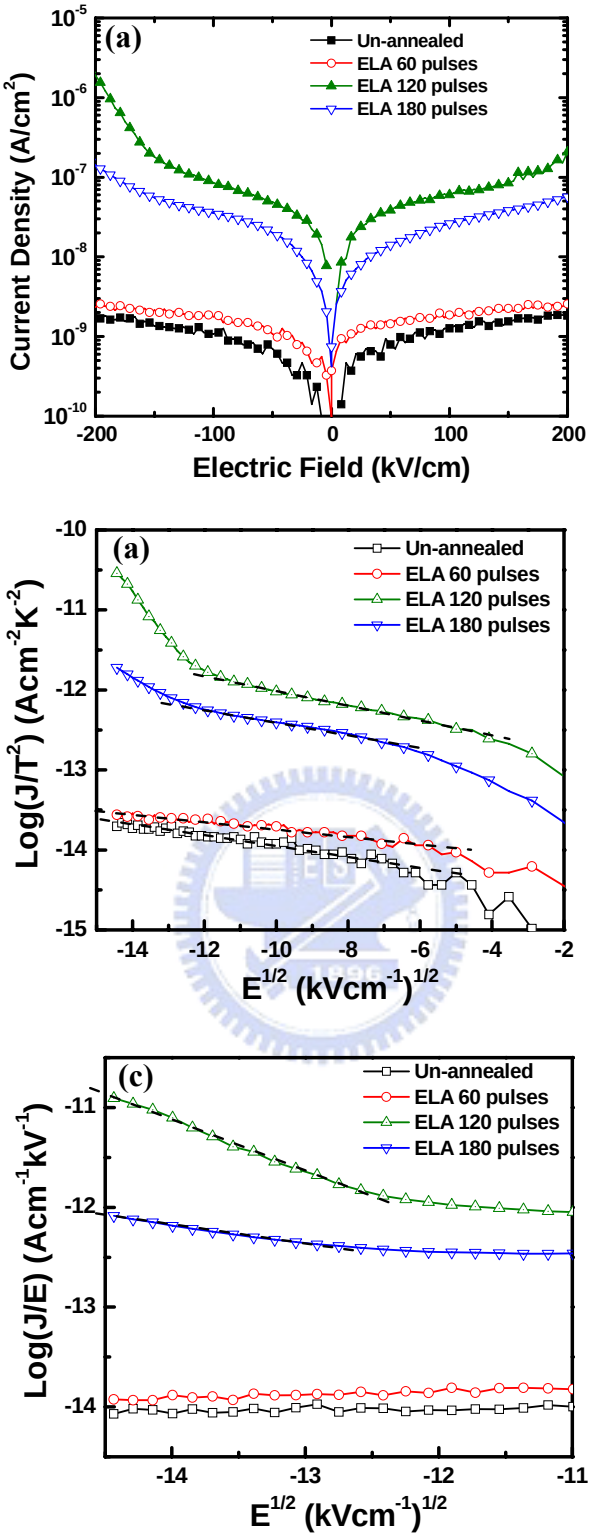


Figure 3-13 (a) Current density versus electric field (J-E) characteristics, (b) Schottky emission plot fitting of log (J/T^2) versus $E^{1/2}$, and (c) Poole-Frenkle emission plot fitting of log (J/E) versus $E^{1/2}$ for PSrT films un-annealed and post-ELA with various numbers of laser pulses.

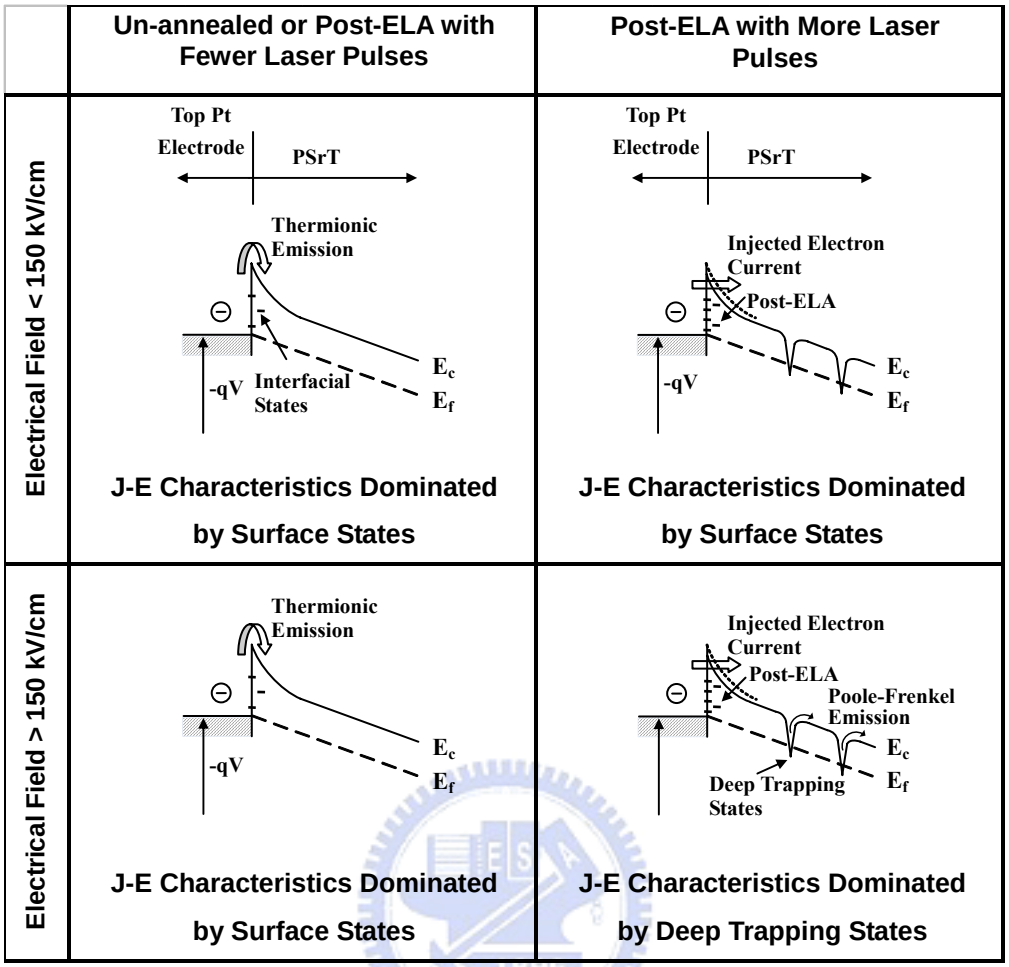


Figure 3-14 Schematic drawings of the electron energy band for PSrT films un-annealed and post-ELA with various numbers of laser pulses.

Figure 3-14 illustrates the electron energy band of PSrT films and shows the interface of substrate electrodes act as n-type semiconductors due to the generation of oxygen vacancies in ABO_3 perovskites [2, 40]. It reveals that PSrT films un-annealed and post-ELA with fewer laser pulses (< 120) have smoother surface and less surface defects, yielding the lower leakage current dominated by surface states and the conduction governed by *SE* behavior at the applied field range. Conversely, PSrT films post-ELA with more laser pulses (≥ 120) exhibit more rough surface, more surface defects and noticeable deep trapping states inside films, yielding the larger leakage current. For films post-ELA with laser pulses ≥ 120, the

low-field (< 150 kV/cm) leakage current is connected to the surface states and the high-field (> 150 kV/cm) leakage current is mainly associated with deep trapping states, which suggests that conduction biased at high-field is transited to *PFE* behavior.

3-5 Effects of Laser-assisted Two-Step Annealing on PSrT films

3-5-1 Physical analysis

As mentioned above, there are some advantages and drawbacks for films post-RTA and post-ELA, accordingly. Therefore, the novel laser-assisted two-step process (post-ELA + RTA), the combination of post-ELA and subsequent RTA, which is proposed to improve the crystallinity and electrical properties of PSrT films. Figures 3-15 show the SEM surface morphologies of films post-ELA, and subsequent RTA (post-ELA + RTA) at 450 and 600 °C. The post-ELA films reveal a dense surface as similar to the un-annealed ones do. The uniform and small grain clusters can be obtained in films post-ELA + RTA at 450 °C. Films post-ELA + RTA at 600 °C reveal a smooth surface with some light imprints. The change of surface morphologies implies that the crystallinity and microstructure of films could be affected by different annealing conditions.

Figure 3-16 presents XRD pattern of films un-annealed, post-ELA, and post-ELA + RTA at 450 and 600 °C. No observable change in XRD pattern is found between the films un-annealed and post-ELA. Conversely, the noticeable diffraction peaks of films post-ELA + RTA indicate that the crystallinity of post-ELA films is strongly improved after subsequent RTA process. The intensities of (100), (110) and (211) orientations increase while the annealing temperature of subsequent RTA increases.

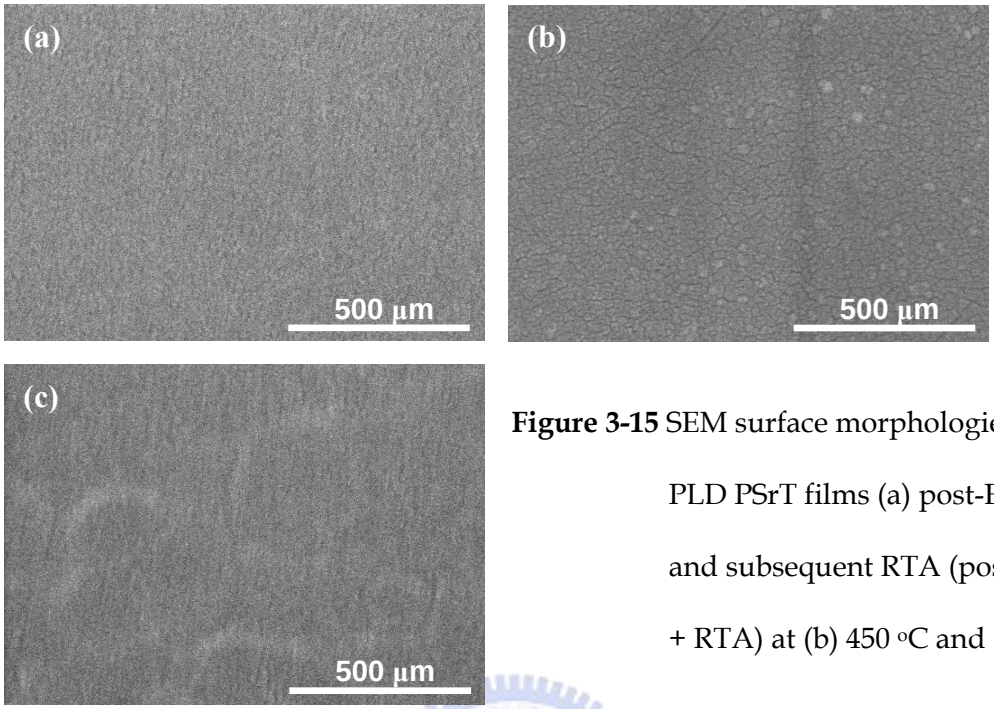


Figure 3-15 SEM surface morphologies of PLD PSrT films (a) post-ELA, and subsequent RTA (post-ELA + RTA) at (b) 450 °C and (c) 600

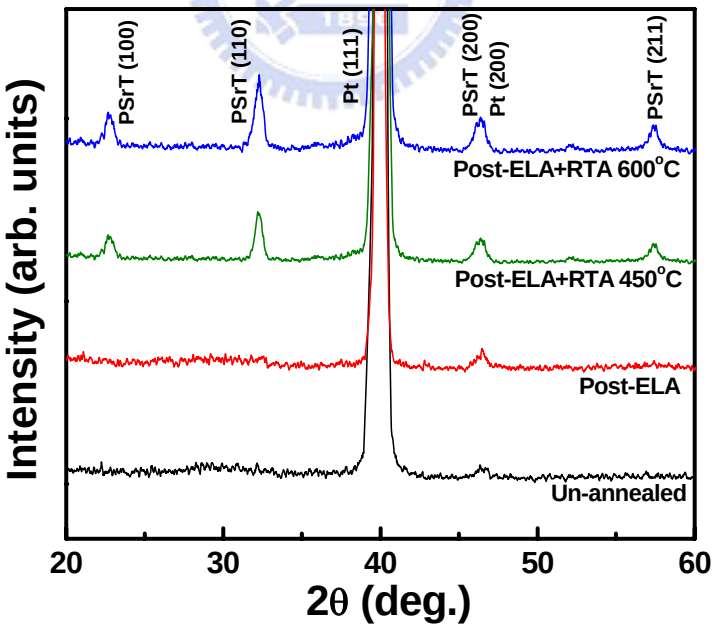


Figure 3-16 X-ray diffraction pattern of PSrT films un-annealed, post-ELA, and post-ELA + RTA at 450 °C and 600 °C.

Figure 3-17(a) shows the cross-sectional TEM image of post-ELA + RTA. It can be clearly investigated that microstructure of PSrT film is divided into two regions. The upper region can be connected to the initial crystal seed induced by ELA (Fig. 3-10) and the grain growth carried out by subsequent RTA (Fig. 3-16). Two PSrT grains with dark contrast were observed in this region. The inset selected–area diffraction patterns (SADPs) of those two PSrT grains along $[001]_{PSrT}$ direction disclose the well crystalline phase. The coarsening of top single-grain during subsequent RTA could be limited by the existed grain boundaries induced by post-ELA. This may be the reason for the film microstructure divided into two regions. The central dark-filed (CDF) images (Fig. 3-17(b)) of $(200)_{PSrT}$ and $(110)_{PSrT}$ diffraction spots also confirm above mention. It is seen that the bigger single-grain is exhibited in the lower region, which is associated with the nucleation from remained amorphous underneath and grain coarsening during subsequent RTA. In contrast, the smaller single-grain located in the upper region could be due to the coarsening limited by the existed grain boundaries. Furthermore, the preferred-orientations of grains located in the upper or lower regions are also strongly influenced by post-ELA + RTA. Nevertheless, the specific evolution of microstructure and crystallinity of films post-ELA + RTA is not clear at present.

Figures 3-18 reveal AES depth profiles of PSrT fIilms, deposited on $Pt/Ti/SiO_2/Si$ substrate, post-ELA and post-ELA + RTA at 600 ^oC. Without standard samples to calibrate the sensitivity factor, the count intensity of elements presented here can only be semi-quantitative, but not absolute. Film post-ELA shows a sharp interface between PSrT films and Pt electrode (Fig. 3-18(a)). Otherwise, it observes a slight diffusion of Ti, Sr and Pb elements from films to Pt electrode after the process of post-ELA + RTA (Fig. 3-18(b)).

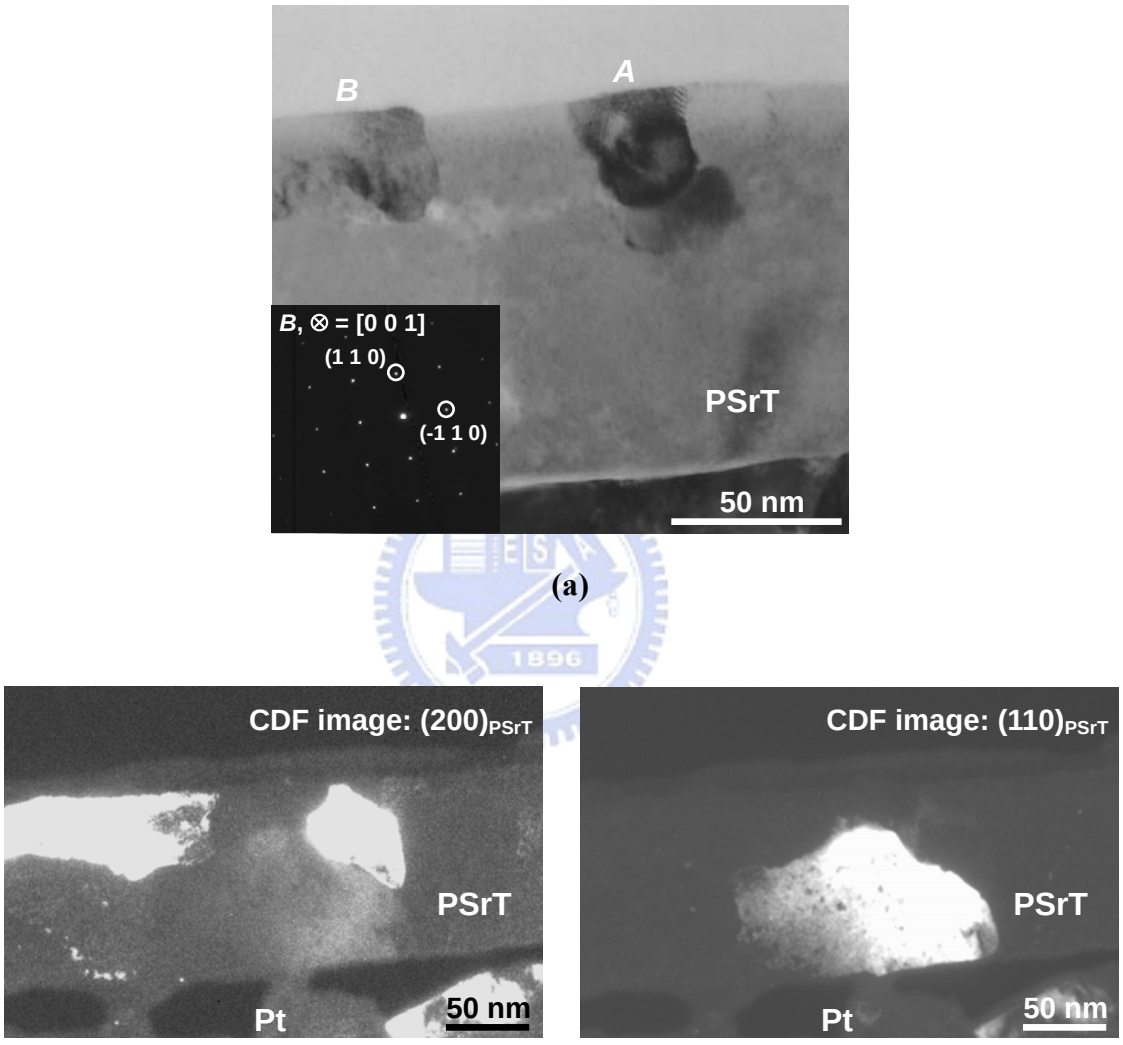


Figure 3-17 (a) Cross-sectional TEM image with inset selected-area diffraction patterns (SADPs), and (b) central dark-field (CDF) images of $(200)_{PSrT}$ and $(110)_{PSrT}$ diffraction spots for PSrT films post-ELA + RTA at 600 ^{o}C.

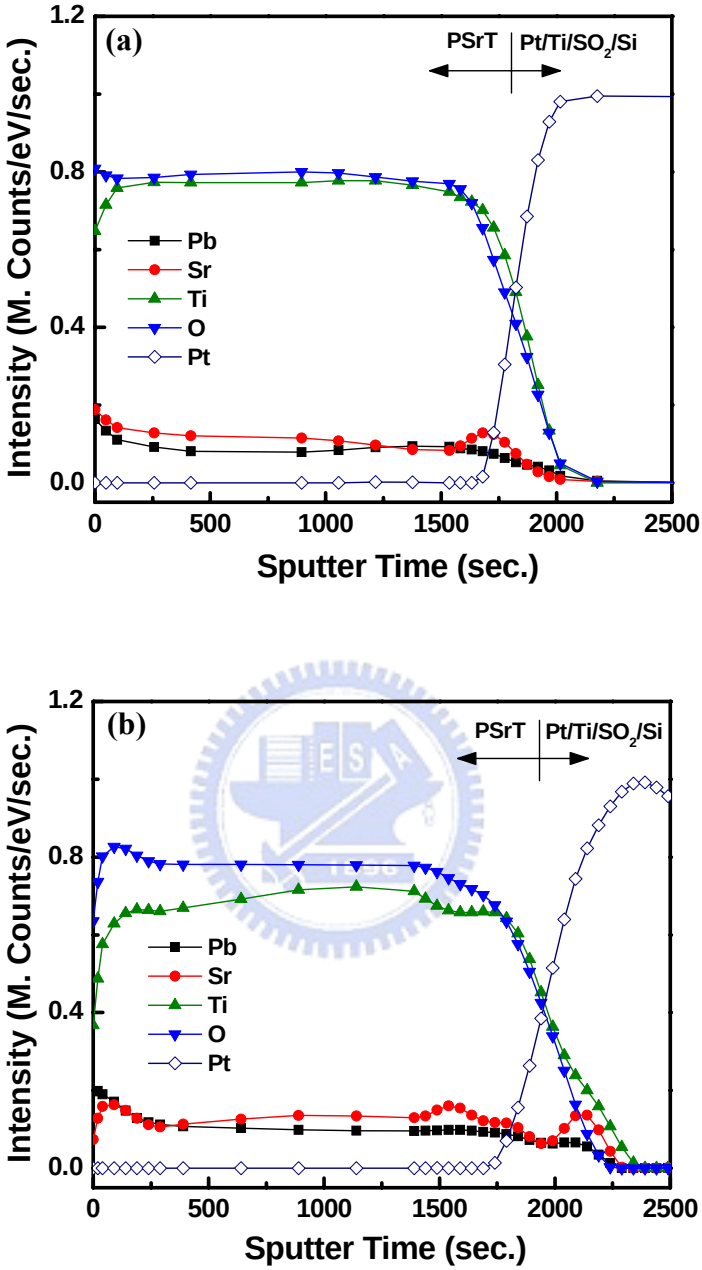


Figure 3-18 AES depth profiles of PSrT films deposited on Pt/Ti/SiO_2/Si substrate: (a) post-ELA and (b) post-ELA + RTA at 600 °C.

3-5-2 Electrical analysis

Figure 3-19(a) gives the C-E hysteresis loops of PSrT films un-annealed, post-ELA, and post-ELA + RTA at 450 and 600 °C. It indicates that the distinct C-E hysteresis loops can be obtained for films post-ELA and post-ELA + RTA. The larger capacitance and better ferroelectricity can be exhibited with the higher annealing temperature of subsequent RTA. Figure 3-19(b) demonstrates the corresponding dielectric constants extracted from the zero-field capacitance for films un-annealed, post-ELA, post-RTA and post-ELA + RTA at 450 and 600 °C. It is observed that the dielectric constant of films can be slightly increased by post-ELA and strongly enlarged after RTA process. The large dielectric constant can be found for both of films post-RTA and post-ELA + RTA at the high annealing temperature. In general, films post-ELA + RTA exhibit superior dielectric constant (i.e. 325 - 492 at 450 - 600 °C) opposed to films post-RTA do (i.e. 81 - 387 at 450 - 600 °C). Furthermore, the evolution of dielectric constant is compatible with the results of XRD and GIXRD (Fig. 3-2, Fig. 3-9 and Fig. 3-16) Thus, the dielectric properties and ferroelectricity of films are obviously dependent on the crystallinity, influenced by the annealing conditions.

Figure 3-20(a) displays the J-E characteristics of films un-annealed, post-ELA, and post-ELA + RTA at 450 and 600 °C. It reveals that the leakage current increases by post-ELA and post-ELA + RTA. The deteriorative leakage current can be seen for films post-ELA + RTA at the higher annealing temperature as like the find of films post-RTA, which can be attributed to the interfacial diffusion at high temperature (600 °C) (Fig. 3-18). Figure 3-20(b) provides the comparison of leakage current density biased at +100/+150 kV/cm for PSrT films un-annealed, post-ELA, post-RTA, and post-ELA + RTA at 450 and 600 °C. The leakage current density of films is the functions of applied biases and annealing conditions. It is observed that the leakage

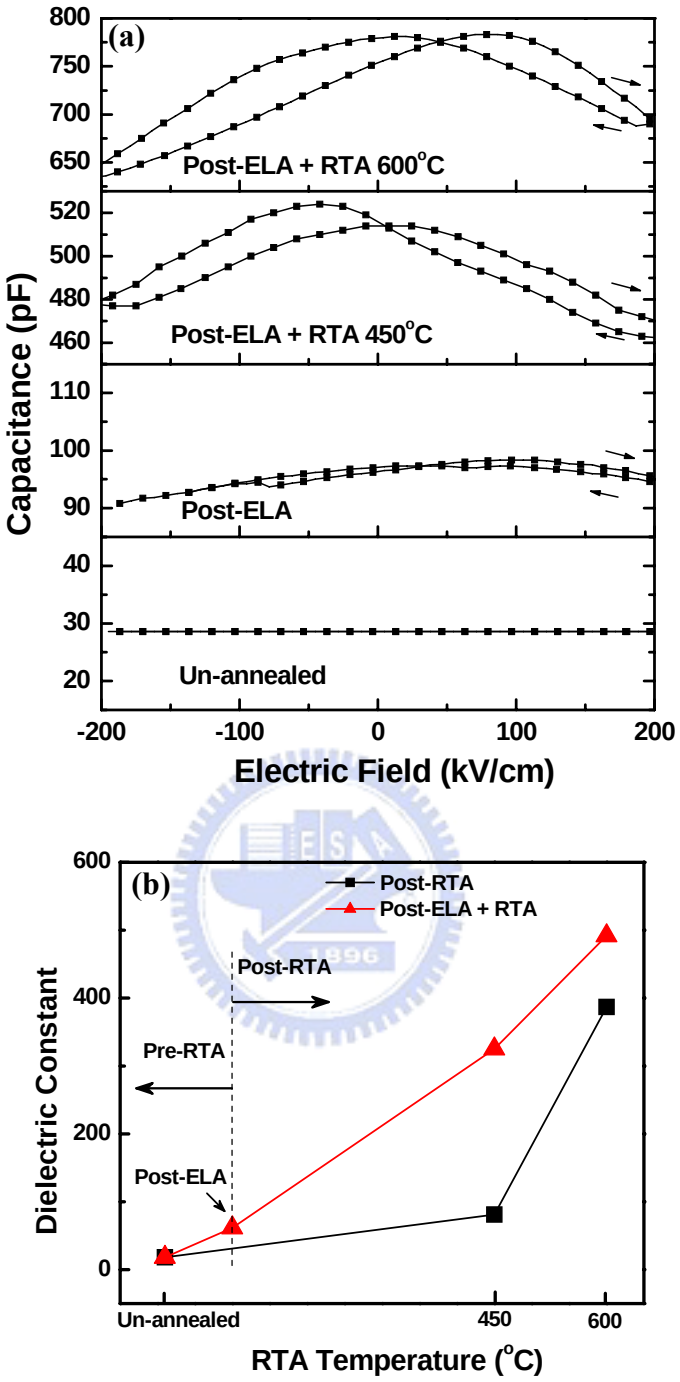


Figure 3-19 (a) Capacitance-electric field (C-E) hysteresis loops of PSrT films un-annealed, post-ELA, and post-ELA + RTA at 450 and 600 °C. (b) The corresponding dielectric constants of PSrT films un-annealed, post-ELA, post-RTA, and post-ELA + RTA at 450 and 600 °C.

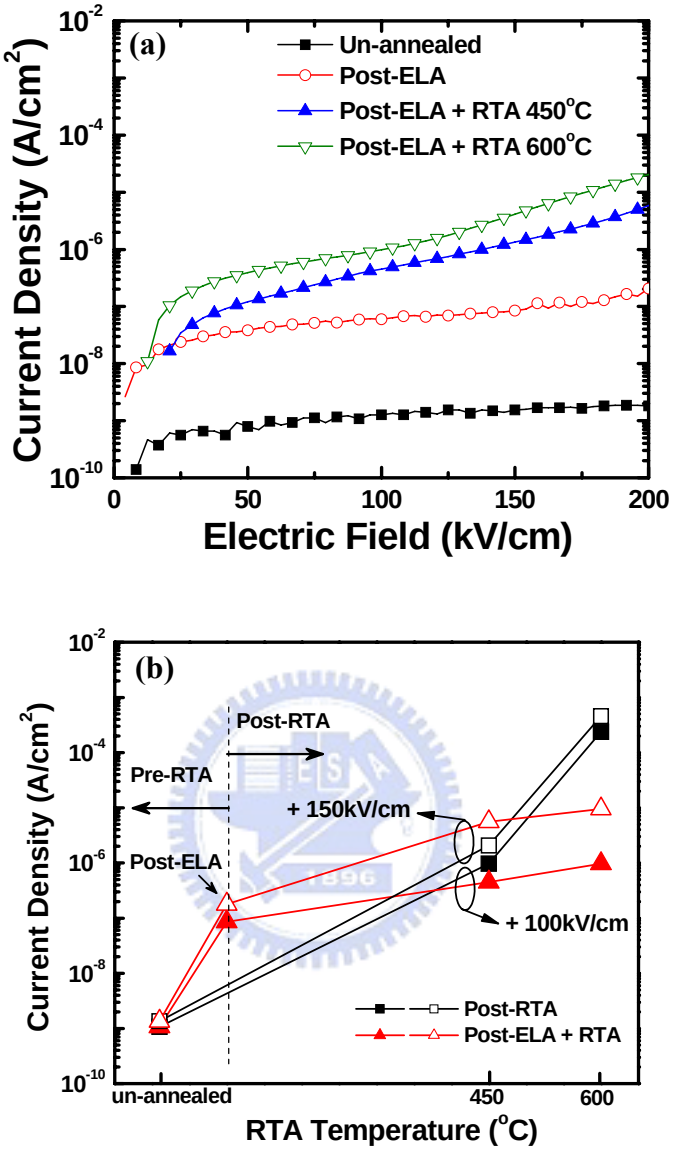


Figure 3-20 (a) Current density versus electric field (J-E) characteristics of PSrT films un-annealed, post-ELA, and post-ELA + RTA at 450 and 600 °C. (b) The comparison of leakage current density biased at +100/+150 kV/cm for PSrT films un-annealed, post-ELA, post-RTA at 450 and 600 °C, and post-ELA + RTA at 450 and 600 °C.

current density of films post-ELA + RTA at 600 °C is inhibited (i.e. 0.97 - 9.55 μA/cm² at +100 - +150 kV/cm) and 1.7-2.4 order of magnitude smaller than that of films post-RTA at 600 °C (i.e. 238 - 454 μA/cm² at +100 - +150 kV/cm). This inhibited leakage current may associate with the specific two regions of film microstructure caused by the process of post-ELA + RTA (Fig. 3-17).

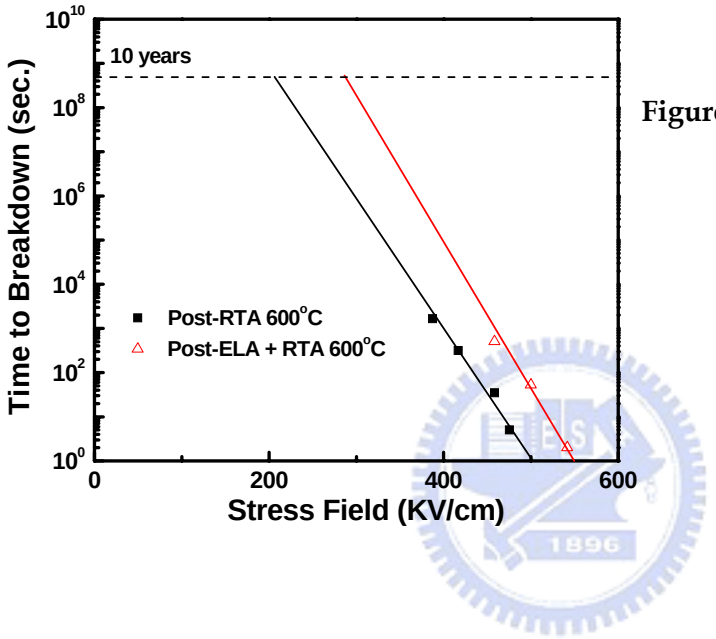


Figure 3-21 TDDB (time to breakdown as a function of stress field) characteristics of PSrT films post-RTA and post-ELA + RTA at 600 °C.

Figure 3-21 displays the characteristics of time-dependent dielectric breakdown (TDDB) to predict the 10 year lifetime. TDDB is regarded as the resistance degradation of dielectric films, which slowly increases the leakage current under constant temperature and dc field stress. The mechanism of resistance degradations in perovskite films could be categorized into the grain boundary model and the reduction model [64-66]. A large potential barrier across the grain boundary will result in shared drop in voltage and suppressed resistance degradation. On the other hand, the reduction model suggests that oxygen vacancies and injection electrons cause resistance degradation. Since the experiment of post-ELA was executed in oxygen ambience and could reduce the oxygen deficiency on the surface of films, reflecting the fewer oxygen vacancies. Therefore, PSrT films post-ELA + RTA exhibit

the longer lifetime and higher breakdown field due to their smaller leakage current density (Fig. 3-20(b)), which result is ascribed to the specific two regions of film microstructure (Fig. 3-17), the improved surface (Fig. 3-1(c) and Fig. 3-15(c)) and the fewer oxygen vacancies in terms of the reduction of defects.

3-6 Summary

The surface morphologies, crystallinity, microstructure and electrical characteristics of PSrT films are noticeably dependent on the annealing conditions. The un-annealed films are amorphous and reveal a smooth and dense surface, an indistinct C-E hysteresis loop, the smallest leakage current. Films post-ELA show the rougher surface morphology, larger value of O/(Pb+Sr) and the enhanced crystallinity of the upper region of films, resulting in the slight increase of dielectric constant and leakage current. The conduction mechanisms of PSrT films are mainly governed by *SE* (Schottky emission) at the applied field range, except the films post-ELA with more laser pulses (≥ 120) reveal *SE*/*PFE* (Schottky emission/Poole-Frenkel emission) behavior at low/high applied fields. As the annealing temperature increases, films indicate a surface image of distinctive grain clusters with pin holes, clear diffraction peaks of provskite structure, distinct C-E hysteresis loops and larger dielectric constant, suggesting that the ferroelectricity is evidently improved by post-RTA. However, the leakage current of films is seriously increased due to the defects and interfacial diffusion induced by post-RTA. Furthermore, films post-ELA and subsequent RTA at 600 °C exhibit the dense surface, well crystallinity, specific two regions of microstructure, distinct C-E hysteresis loops, the largest dielectric constant of 492, and the inhibited leakage current density, which biased at +100-150 kV/cm is 1.7-2.4 order of magnitude smaller than that of films

post-RTA at 600 ^{o}C. Concisely, the well crystallinity, superior ferroelectricity, longer lifetime and higher breakdown field of PSrT films can be achieved by this annealing technique of laser-assisted two-step process.

Chapter 4 Explorations of Pulse-Laser-Deposited $(Pb,Sr)TiO_3$ Films at Low Temperatures

4-1 Concepts of Low-Temperature PLD PSrT Films

There has been an upsurge of activities regarding the integration of ferroelectric devices, integrated circuits (IC), and micro-electro-mechanical systems (MEMS). Thin ferroelectric films, with perovskite structure, have received much attention lately for their potential applications in the nonvolatile random access memory (NVRAM) and the optical switch [1-5]. Depositions of ferroelectric films, such as $PbTiO_3$ (PTO), $Pb(Zr,Ti)O_3$ (PZT), and $SrBi_2Ta_2O_9$ (SBT), are usually conducted at high-temperatures (> 600 ^oC) to obtain the good crystallinity of a perovskite structure [61, 73]. However, the high-temperature process will damage formerly-fabricated structure, especially in the deep submicron regime. In addition, the volatilization of lead oxide (Pb-O compounds) in lead-titanate-based thin films, processing over 490 ± 50 ^oC, can degrade the microstructure and reliability of ferroelectric devices [4, 62]. Hence, a low-temperature process (≤ 450 ^oC) is indeed required for the deposition of ferroelectric thin films for IC and MEMS applications.

$PbTiO_3$ (PTO) film has been considered for the applications of NVRAM, but many drawbacks of this film must be improved, such as high coercive field, high crystallization temperature and poor microstructure. The $(Pb,Sr)TiO_3$ (PSrT) solid-solution film is constituted by PTO and $SrTiO_3$ (STO). PTO and STO films, at room temperature, have a tetragonal structure (ferroelectric phase) and a cubic structure (paraelectric phase), respectively, because the Curie temperature (T_c) of PTO is 490 ^oC and the T_c of STO is -220 ^oC. The effect of lead substituted by strontium

(Sr) in the PTO film will decrease the crystallization temperature and offers a good control of dielectric properties at room temperature [47, 48]. In this work, the (Pb,Sr)TiO_3 films are prepared using the pulsed-laser deposition (PLD), which is excellent for fabricating the ceramic films with complex compounds.

The technique of the PLD is simple, versatile, and capable for growing a wide variety of stoichiometric oxide films without subsequent high-temperature annealing. Hence, PLD is a potential technique, which could be integrated into low-temperature semiconductor processing. Pulsed laser deposition process consists of three steps [31]: (i) vaporization of a target material by laser beam, (ii) transport and interaction of a vapor plume with a background ambient, and (iii) condensation of the ablated material onto a substrate where a thin film nucleates and grows. Therefore, the structural and the electrical characteristics of PLD ferroelectric films are strongly affected by the processing parameters, such as substrate temperature, laser energy fluence, and oxygen ambience. PSrT films using the conductive oxide-electrode, such as (La,Sr)CoO_3, (La,Sr)MnO_3, or RuO_2, could obtain a good crystallinity and well-controlled preferred orientations at high deposition temperatures (> 500 ^oC), as reported in previous works [56, 57], but the drawbacks of the ferroelectric capacitor using oxide-based electrodes are high power consumption and large delay time for the device applications [4]. Thus, the noble metal platinum (Pt), with low resistivity, is considered as the electrode for Pt/PSrT/Pt capacitors because of its low power consumption and RC delay [4]. To data, only a few works reported the properties of PLD PSrT films deposited on the Pt/SiO_2 substrate at the temperatures, over 550 ^oC [56-58]. Thus, the ferroelectric characteristics of PLD PSrT deposited at a relatively low-temperature, under 450 ^oC, are indeed further studied. In this work, the relationship between physical properties and electrical characteristics of PSrT capacitors deposited by low-temperature PLD will be addressed.

4-2 Experiments

P-type silicon wafers with (100) orientation were employed as the substrates in this study. A 100 nm-thick SiO_2 film was grown after the initial RCA cleaning process. Platinum film of 100 nm thickness was sputtered onto SiO_2 as the bottom electrode. The annealing condition for Pt bottom electrode was 450 ^oC for 30 min in N_2 ambient.

Thin PSrT films (200 nm thick) were then deposited on the $Pt/SiO_2/Si$ substrate by a PLD system (Lambda Physik Excimer Laser LPX 210i, using KrF, λ=248 nm). A set of optical lens was used to focus the laser beam over the $(Pb_{0.6}Sr_{0.4})TiO_3$ target in vacuum. The PSrT target was prepared with conventional ceramic fabrication process [31]. The vacuum chamber was pumped down to a base pressure of 0.1 mTorr and then refilled with O_2 as working gas. The vaporized species of the target transferred and deposited on the substrate heated by thermal heater. The deposition temperature (substrate temperature, T_s) varied from 300 ^oC to 450 ^oC, calibrated at the wafer upper surface. It means that a thermal couple, connected to a temperature controller, was used to touch the surface of samples and sense the temperature of $Pt/SiO_2/Si$ substrate, denoted as T_s. During the PLD process, the oxygen partial pressure, target to substrate distance, laser pulsed rate, and average laser power density (laser energy fluence) were 80 mTorr, 4 cm, 5 Hz, and 1.55 J/cm^2 per pulse, respectively.

The physical properties of PSrT films were analyzed before Pt top electrode deposition. The film thickness and the surface morphology of PSrT films were examined by field emission scanning electron microscopy (FESEM) (S-4000, Hitachi). An Auger electron spectroscope (AES) (Microlab 310F, Fison (VG)) was used to analyze the elemental depth profile of PSrT films. An X-ray diffractometer (D5000, Siemens, using Cu Kα, $\lambda \sim 0.154$ nm) was employed to analyze the crystallinity of the

films. The Pt top electrodes, with a thickness of 100 nm and a diameter 75 μm, were then deposited by sputtering and patterned by shadow mask process to form a metal/ferroelectric/metal (MFM) capacitor structure.

An automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station was used to measure the leakage current (I-V) characteristics and breakdown properties. The conductance and tangent loss were measured by an impedance/gain-phase analyzer (4194A, Hewlett Packard). A capacitance-voltage (C-V) analyzer (Package 82 system C-V 590, Keithley) was also used to measure C-V curves at 100 kHz, and the dielectric constant was extracted from C-V measurement. The ferroelectric polarization-electric field (P-E) characteristics of the PSrT films were determined directly from virtual ground circuits (RT-66A standardized ferroelectric testing system, Radiant Technologies). The pulse with a triangle-shaped wave at 10 kHz trains was conducted to measure the polarization [74]. The P-E curve was obtained analytically by calculating the polarization P from the relative permittivity ε_r (dielectric constant) versus electric field E data, addressed as *Eq. (2-2)*. A pulse generator (8110A, Hewlett Packard) and a pulse/function generator (8116A, Hewlett Packard) were connected together with low noise BNC cables to generate +3 V/-3 V bipolar wave pulsed at 1 MHz, confirmed by an oscilloscope (54645A, Hewlett Packard), as an input signal for the measurement of polarization switching degradation (fatigue).

4-3 Physical Analysis

Figure 4-1 shows that the deposition rate of PSrT films is maximal at T_s = 350 °C and then decreases as T_s increases, which may be connected to the volatilization of Pb-O compounds at higher T_s [62]. Figure 4-2 presents a cross-sectional SEM micrograph of of PLD PSrT films deposited at T_s = 400 °C on Pt/SiO_2/Si, with the column-like structure obtained in around 200 nm thickness. It infers that the growth of PSrT films can be strongly influenced by the properties of bottom electrode and the deposition conditions during PLD. Figs. 4-3(a)-(d) show SEM surface morphologies of PLD PSrT films deposited on Pt/SiO_2/Si (100) wafers at various substrate temperatures, ranging from 300 °C to 450 °C. As the T_s increases, the clusters gradually grow and became more uniform and rounded. The surfaces of PSrT films are mostly dense, smooth, and uniform without any cracks at T_s from 300 to 450 °C.

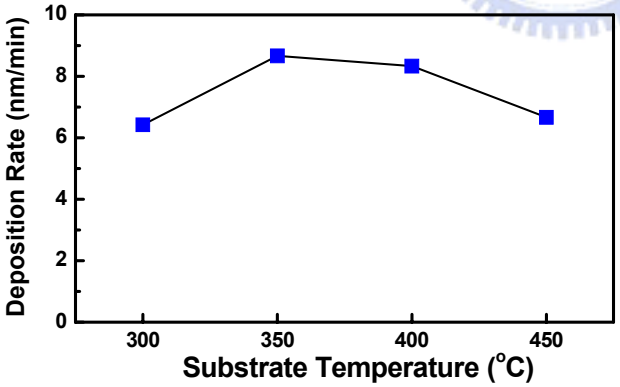


Figure 4-1 Deposition rate of PSrT films deposited at various substrate temperatures (T_s) on Pt/SiO_2/Si (100) wafers.

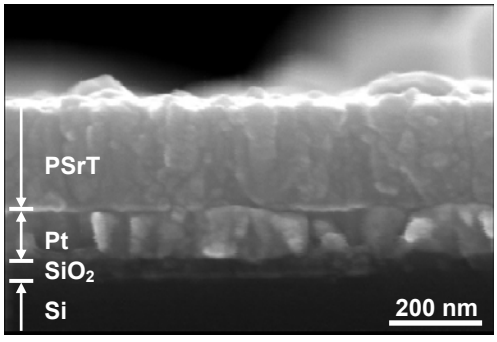


Figure 4-2 SEM cross-sectional micrograph of PLD PSrT films deposited at T_s = 400 °C on Pt/SiO_2/Si (100) wafers.

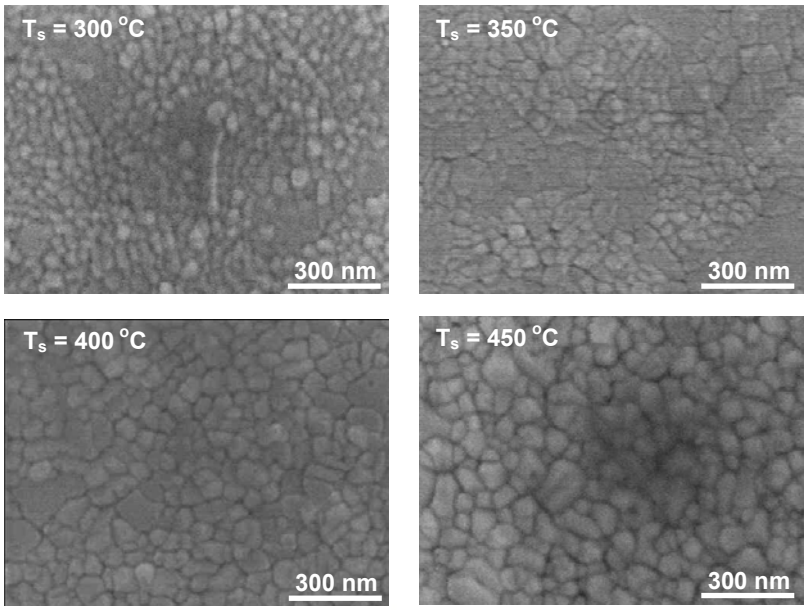


Figure 4-3 SEM surface morphologies of PLD PSrT films deposited at various substrate temperatures (T_s) on Pt/SiO_2/Si (100) wafers.

Figure 4-4 reveals AES depth profiles of PLD PSrT films deposited on Pt/SiO_2/Si (100) wafers at various T_s. Without standard samples to calibrate the sensitivity factor, the count intensity of elements presented here can only be semi-quantitative, but not absolute. For visibility, the intensities of elemental Pb and Sr are distended as five times (5×) and ten times (10×), accordingly. No evident difference is observed between the depth profiles of films deposited from 300 °C to 450 °C. As can be seen from the abrupt interface profile, no significant elemental inter-diffusion of O, Ti, Pb, Sr and Pt between PSrT films and Pt bottom electrode occurs at such low temperatures.

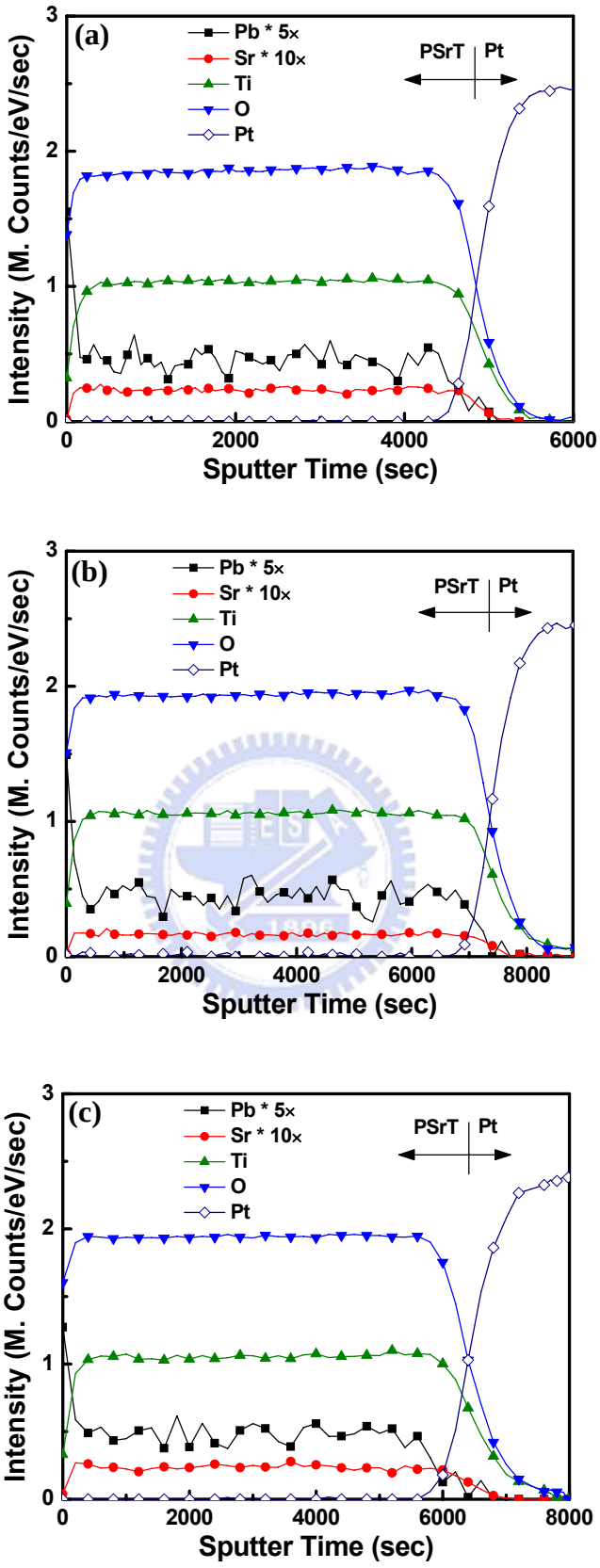


Figure 4-4 AES depth profiles of PLD PSrT films deposited on Pt/SiO_2/Si (100) wafers at (a) 300 °C, (b) 400 °C, and (c) 450 °C.

Figure 4-5(a) displays X-ray diffraction pattern of PSrT films deposited on $Pt/SiO_2/Si$ (100) wafers at various T_s. All of these spectra exhibit diffraction peaks of $(Pb_{1-x}Sr_x)TiO_3$ perovskite phases [47, 48, 58-60, 75]. There are two reasons for the crystallization of PSrT perovskite phase at low temperatures (≤ 450 °C): (i) the addition of strontium (Sr) makes the crystallization temperature of PSrT lower than that of PZT [62], and (ii) the PLD technique could preserve the crystalline phase and stoichiometric ratio of the target material [31]. Moreover, the intensity of (100) and (110) orientations varied significantly as the T_s increases. The PSrT films had a tetragonal structure with a clear (100) peak for $x < 0.5$ and a cubic structure with a strong (110) peak for $x \geq 0.5$, as reported in previous works [47, 48]. Kang *et al.* [47] also stated that the split (110) peaks near $31^o < 2\theta < 33^o$ tended to merge at $x > 0.5$, suggesting that the structure of PSrT films is tetragonal and the composition may be close to the stoichiometric composition (i.e. $(Pb_{0.6}Sr_{0.4})TiO_3$), used for the PLD target herein. Figure 4-5(b) quantizes the XRD data, using the following formula,

$$X_{100} = I_{100} / (I_{100} + I_{110}), \qquad (4\text{-}1)$$

where X_{100} is the relative proportion of the (100) orientation, I_{100} is the integrated area under the (100)-oriented peak, and I_{110} is the integrated area under the (110)-oriented peak. All the films are highly textured. In Fig. 4-5(b), X_{100} is estimated as 31.4%, 65.4%, 55.8% and 49.3% at T_s = 300, 350, 400, and 400 °C, respectively. X_{100} is maximal at T_s = 350 °C and exhibits strong (100) preferred orientation, consistent with the result of polarization versus T_s as described below. Restated substrate heating can not effectively improve the crystallinity of PLD PSrT films when T_s is high (450 °C). Therefore, the properties of PLD PSrT films must be further studied to clarify the decline in diffraction intensities of (100) and (110) as T_s increases from 400 to 450 °C.

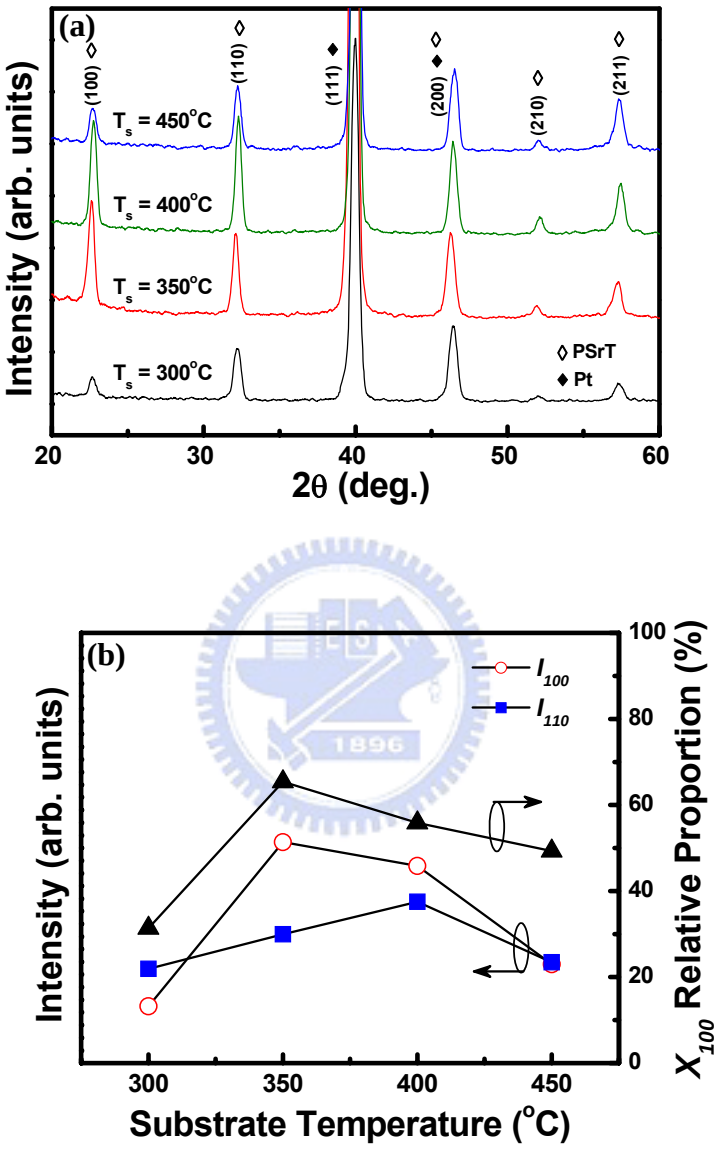


Figure 4-5 X-ray diffraction analyses of PLD PSrT films deposited at various substrate temperatures on $Pt/SiO_2/Si$ (100) wafers: (a) diffraction pattern and (b) texture characteristics.

4-4 Electrical Analysis

Later, leakage current characteristics are interpreted as Schottky emission (*SE*) at low electric fields, and Poole-Frenkel emission (*PFE*) at high electric fields, given by the following equations [16-18], which are used to analyze the interface-limited and bulk-limited conductions of Pt/PSrT/Pt capacitors, respectively.

$$\textbf{SE}: \log(J_{SE}/T^2) = -q\left[\varphi_B - (qE/4\pi\varepsilon_d\varepsilon_0)^{1/2}\right]/(kT\ln 10) + \log(A^*), \quad (4\text{-}2)$$

$$\textbf{PFE}: \log(J_{PF}/E) = -q\left[\varphi_t - (qE/\pi\varepsilon_d\varepsilon_0)^{1/2}\right]/(kT\ln 10) + \log(B), \quad (4\text{-}3)$$

where A^* is the effective Richardson's constant, φ_B is the potential barrier height in the interface, B is a constant, φ_t is the trapped energy level, ε_d is the dynamic dielectric constant of the ferroelectric material in the infrared region, q is the unit charge, k is Boltzmann's constant, J is current density, T is absolute temperature, and E is the external electric field. If the conduction current follows the *SE* behavior, then a log (J/T^2) against $E^{1/2}$ plot should be linear. Similarly, a log (J/E) against $E^{1/2}$ plot can be made for *PFE*. Figure 4-6(a) presents the *SE* plot for Pt/PSrT/Pt capacitors at various T_s. The dashed lines represent the fitted results. The curves of log (J/T^2) versus $E^{1/2}$ closely match the dashed lines, as denoted in *SE1* and *SE2* regions, according to T_s = 300 °C and $T_s \geq$ 350 °C. Figure 4-6(b) draws the electron energy band in the interface of substrate electrodes and reveals PSrT films act as n-type semiconductors due to the generation of oxygen vacancies in ABO_3 perovskites [2, 18]. The space charge density of the interfacial depletion region is assumed to be almost equal to the concentration of oxygen vacancies. In the case of T_s = 300 °C (*SE1*), more interface states result in more charge accumulation and severe image-force effect at the edge of electrodes, decreasing the height of Schottky barrier [2, 76, 77].

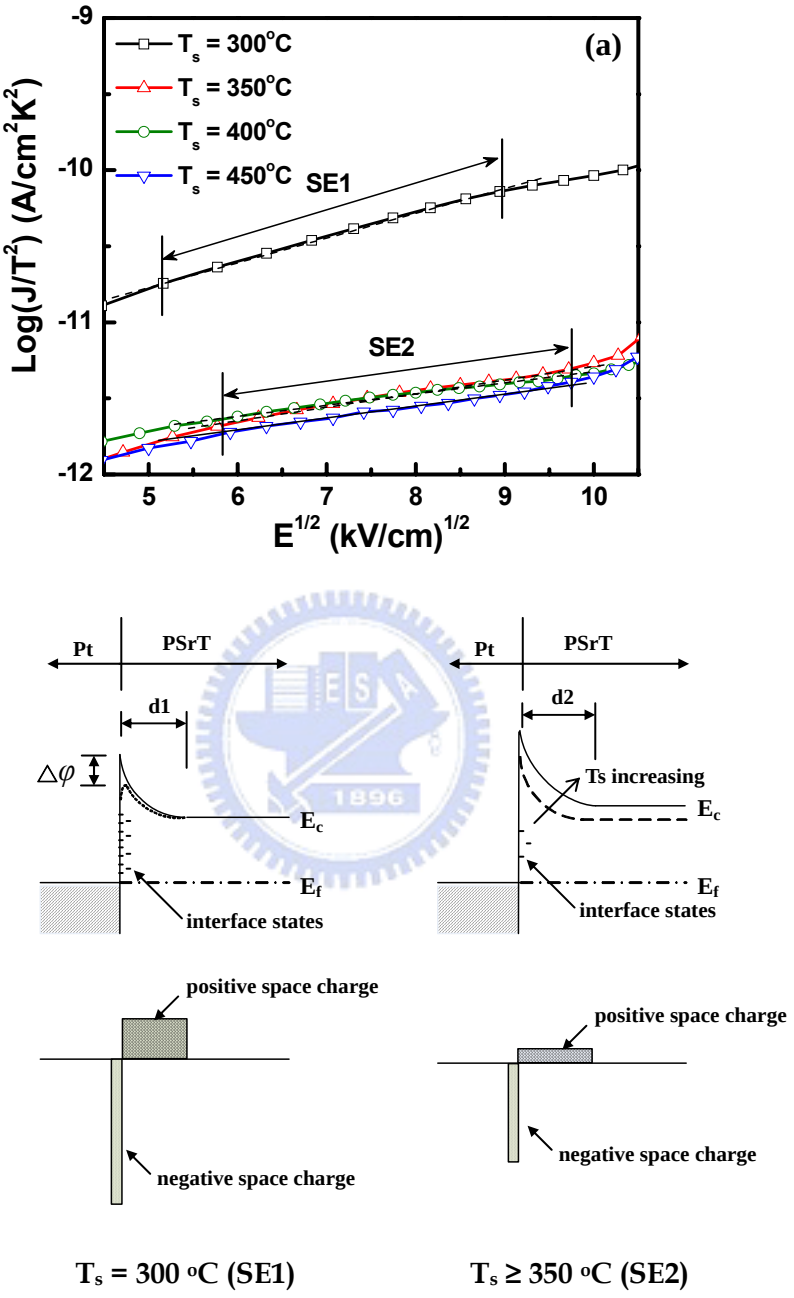


Figure 4-6 (a) Schottky emission (*SE*) plot fitting of log (J/T^2) versus $E^{1/2}$, and (b) the electron energy band in the interface of substrate electrodes at T_s = 300 °C and $T_s \geq$ 350 °C.

The image-force lowering $\Delta\varphi$ can be also expressed as

$$\Delta\varphi = (nqE / 4\pi\varepsilon_s\varepsilon_0)^{1/2}, \quad (4\text{-}4)$$

where n is the amount of charges and ε_s is the static dielectric constant (relative permittivity, ε_r) of the ferroelectric material. The barrier thickness d (foot note *1* and *2* present the cases of *SE1* and *SE2*, respectively) of the interfacial depletion region can be derived as

$$d_1 / d_2 = \left[N_{VO2} / N_{VO1} \times (1 + kT / \Delta\varphi_{MF} \times ln(N_{VO1} / N_{VO2})\right]^{1/2}, \quad (4\text{-}5)$$

where N_{VO1} *and* N_{VO2} are the concentrations of oxygen vacancies for *SE1* and *SE2* cases, accordingly. $\Delta\varphi_{MF}$ is the work function difference between Pt and PSrT, revealing that decreasing the concentration of oxygen vacancies increases the barrier thickness of the interfacial depletion region [18]. In the case of T_s ≥350 °C (*SE2*), increasing T_s yields fewer interface states, a fewer space charge density in interfacial depletion region, and a higher and thicker Schottky barrier, resulting in a small leakage current. Furthermore, the measured conductance G can be utilized to determine the interface state density N_{is} addressed as [19, 77]

$$G/\omega = C_s\omega\tau / (1 + \omega^2\tau^2), \quad (4\text{-}6)$$

$$N_{is} = C_s / qA, \quad (4\text{-}7)$$

where ω is the angular frequency, C_s is the interface state capacitance, and τ is the time constant. When the conductance goes through a maximum, $\omega\tau$ = 1, which C_s = $2G/\omega$, then N_{is} can be obtained by using the following formula:

$$N_{is} = 2G_{max} / \omega qA, \qquad (4\text{-}8)$$

The results obtained show that N_{is} is around 4.3 × 10^{14} and 2.4 × 10^{14} ($cm^{-2}eV^{-1}$) for films deposited at T_s = 300 °C and 450 °C, respectively. The quantitative values of interface state density are consistent with the fitting analysis of *SE* behavior.

Figure 4-7(a) shows the *PFE* plot using the same experimental current-voltage (I-V) data, suggestive of the *PFE* behavior when the bias exceeds +165 kV/cm and the presence of trapping states in PLD PSrT films deposited from 300 °C to 450 °C. The magnitude of leakage currents is governed by the balance of trapping and de-trapping rate. The field-assisted emission of trapped charged carriers follows *PFE* emission rate, revealing bulk-limited conduction as the dominant leakage mechanism at higher applied field. Figure 4-7(b) indicates that samples deposited at high substrate temperatures (T_s ≥ 350 °C) yield fewer trapping states inside PSrT films. Comparing the data at T_s = 400 °C and T_s = 450 °C, it reveals that a larger value of log (J/E) at 450 °C corresponds to more trapping states of the 450 °C-deposited PSrT films. The leakage current of the Pt/PSrT/Pt capacitor degrades at 450 °C may be inferred from the more serious volatilization of Pb-O compounds at higher T_s (≥ 450 °C) [4, 62], corresponding to more oxygen vacancies (OVs) and defects in the film. The OVs will act as charged defects to degrade leakage currents and also deteriorate the composition and crystallinity of films, according to the following reaction [78]

$$O_O \leftrightarrow V_O^{\bullet\bullet} + 2e' + \frac{1}{2}O_2, \qquad (4\text{-}9)$$

where O_O, $V_O^{\bullet\bullet}$ and e' represent the oxygen ion on its normal site, the oxygen vacancy, and the electron, respectively. This may be the cause of the drop in X-ray intensity of the (100) and (110) orientations from T_s = 400 °C to 450 °C (Fig. 4-5(b)).

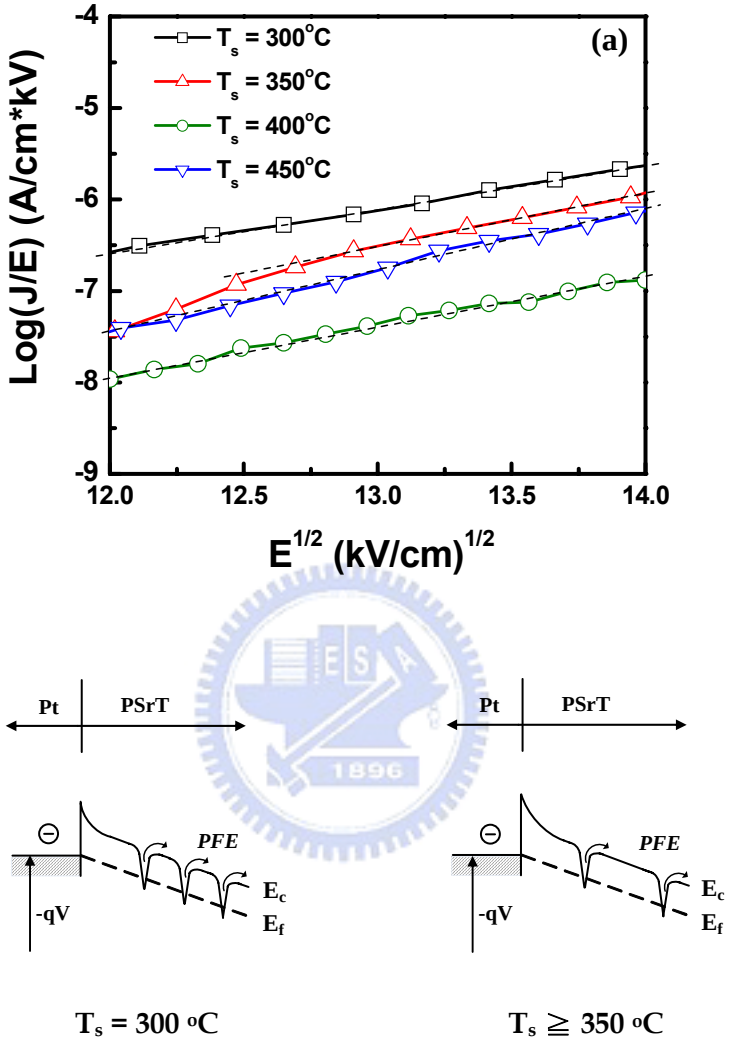


Figure 4-7 (a) Poole-Frenkel emission (*PFE*) plot fitting of log (J/E) versus $E^{1/2}$, and (b) the electron energy band inside PSrT films prepared at T_s = 300 °C and $T_s \geq 350$ °C.

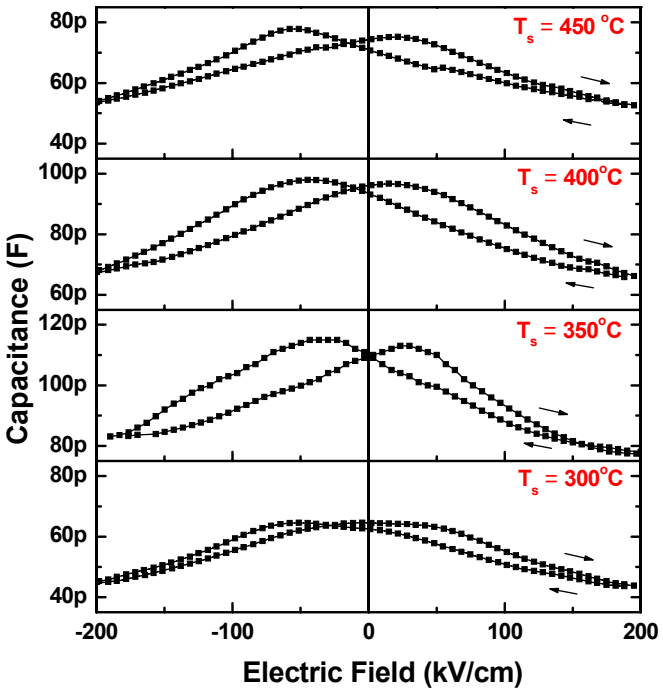


Figure 4-8 Capacitance-electric field (C-E) hysteresis loops of Pt/PSrT/Pt capacitors prepared at various T_s.

Figure 4-8 plots the capacitance-electric field (C-E) characteristics measured at 100 kHz for PSrT films deposited at various T_s. The figure presents the typical C-E hysteretic characteristics of ferroelectric materials. The capacitance is maximal at negative bias corresponding to the coercive field (E_c) of the hysteresis loop as the applied field sweeps from +200 kV/cm to -200 kV/cm. It is maximal at positive E_c when the applied field sweeps in the opposite direction. The zero-field capacitance, in terms of the dielectric constant, depends considerably on the T_s. The asymmetric C-E curves are probably due to different configuration of electrodes used in the measurement (i.e. the area of the bottom electrode is larger than that of the top electrode, as defined by shadow mask).

Figure 4-9(a) plots the saturation polarization ($2P_s$) and capacitance of Pt/PSrT/Pt capacitors deposited at various T_s. The 350 °C-deposited PSrT capacitor has the greatest saturation polarization ($2P_s$) and capacitance. The evolution of the $2P_s$ as a function of T_s is fully consistent with that of capacitance, supporting the claim that the polarization corresponding to each applied field can be obtained

numerically by integrating the dielectric constant, using *Eq. (2-2)* as stated above. Figure 4-9(b) plots the remnant polarization ($2P_r$) and coercive field ($2E_c$) of Pt/PSrT/Pt capacitors as a function of T_s. For PSrT films prepared at 350 °C, $2P_s$, $2P_r$, and $2E_c$ values are 30.71 μC/cm², 6.29 μC/cm², and 84.91 kV/cm, respectively, which values are similar to those of PSrT films prepared by the sol-gel process at 700 °C [42, 47]. The E_c varies with T_s in a direction opposite to that of P_r. This fact is very important as it allows P_r to be maximized and E_c to be minimized simultaneously.

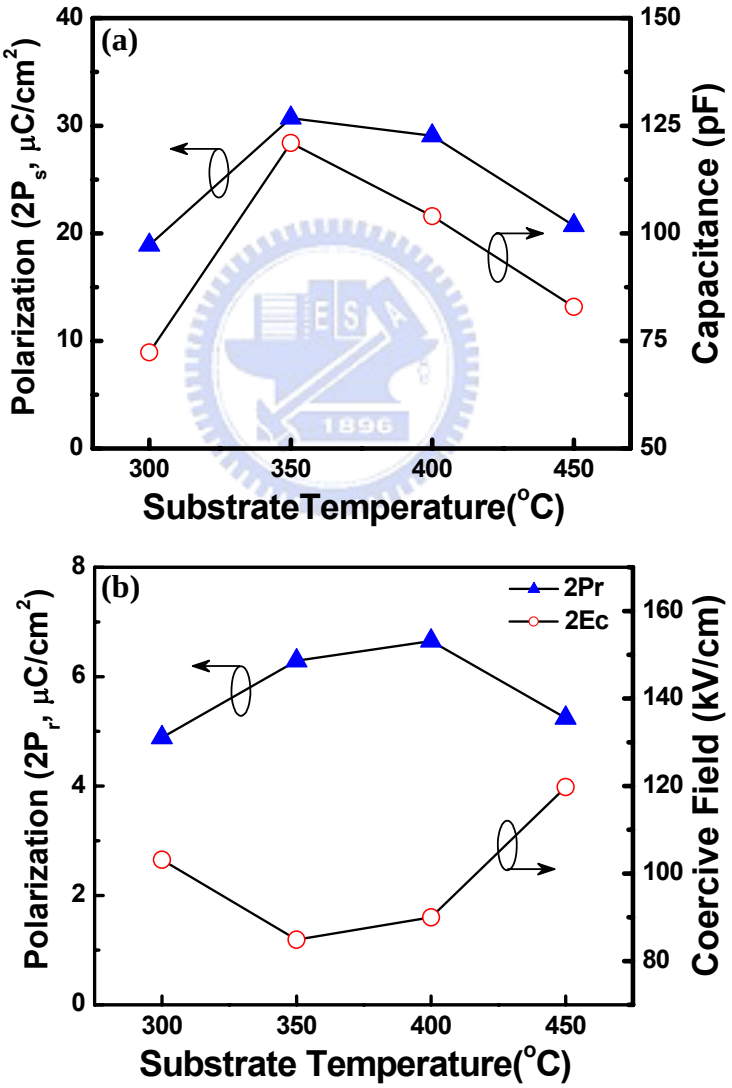


Figure 4-9 (a) Comparison of saturation polarization ($2P_s$) and capacitance, and (b) evolutions of remnant polarization ($2P_r$) and coercive field ($2E_c$) of Pt/PSrT/Pt capacitors prepared at various substrate temperatures.

Table 4-1 summaries the detail comparisons of ferroelectric characteristics for the PSrT films fabricated from different kinds of substrate material and by various deposition techniques. The polarization of the lead-titanate-based crystal is maximal in the [100] direction, so the polarizations of the film with the preferred (110) texture are weaker than those of the films with the preferred (100) texture [4, 46]. The PSrT films, deposited at low T_s (i.e. 350 - 400 °C), exhibit good ferroelectricity and enhanced (100) preferred orientation. Accordingly, the polarization properties of PSrT capacitors are very consistent with the texture characteristics presented in Fig. 4-5(b).

Table 4-1 Comparisons of ferroelectric characteristics for the PSrT films fabricated from different kinds of substrate material and by various deposition techniques.

	This Work	Ref. 56 and 57	Ref. 56-58	Ref. 47	Ref. 42	Ref. 59 and 60
Bottom Electrode	$Pt/SiO_2/Si$	$Pt/Ti/SiO_2/Si$	$LSCO/Pt/SiO_2/Si$ $LSMO/Pt/SiO_2/Si$ [b]	$Pt/Ti/SiO_2/Si$	$Ir/SiO_2/Si$	$Pt/SiO_2/Si$
Film Thickness (nm)	200	NA [a]	NA [a]	400	250	100 - 250
Deposition Method	PLD (KrF, λ= 248nm)	PLD (XeCl, λ= 308nm)	PLD (XeCl, λ= 308nm)	Sol-gel	Sol-gel	LSMCD [c]
Process Temperature	300 - 450 °C	550 - 640 °C	550 - 640 °C	380 - 700 °C curing + 650 -750 °C Annealing	400 °C curing + 650 -735 °C RTA	500 °C baking + 550 - 650 °C Annealing
Saturation Polariztion ($2P_s$, μC/cm^2)	18.9 - 30.7	75	60 - 120	20 - 45	10	NA [a]
Remanent Polarization ($2P_r$, μC/cm^2)	4.9 - 6.7	30	10 - 40	5 - 28	5	NA [a]
Coercive Field ($2E_c$, kV/cm)	84.9 - 103.1	100	50 - 90	60 - 150	240	NA [a]
Dielectric Constant	357.8 - 616.5	NA [a]	NA [a]	1370	NA [a]	481 - 560
Current Density (μA/cm^2) at 100kV/cm	0.39 - 8.29	NA [a]	NA [a]	0.2	NA [a]	~ 200
Residual Contamination of Organic Material	No	No	No	Yes	Yes	Yes

[a] NA: Not available
[b] LSCO: $(La,Sr)CoO_3$, LSMO: $(La,Sr)MnO_3$
[c] LSMCD: Liquid Source Misted Chemical Deposition

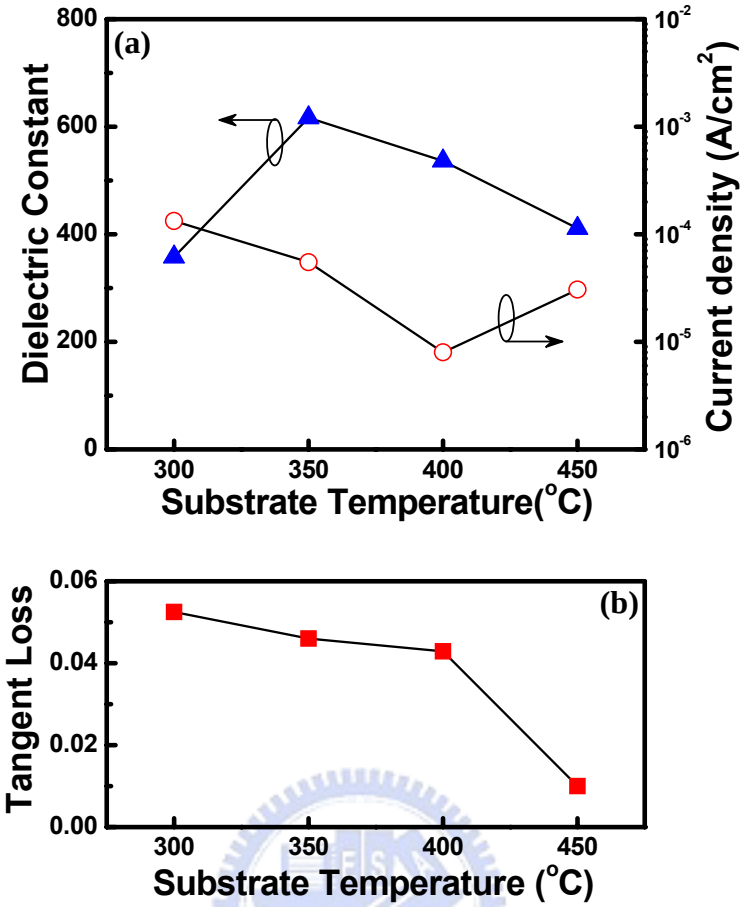


Figure 4-10 Effect of substrate temperatures on (a) dielectric constant and leakage current density biased at +170 kV/cm, and (b) tangent loss characteristics measured at 100 kHz.

Figure 4-10(a) displays the effect of T_s on dielectric constant and leakage current density biased at +170 kV/cm, extracted from Fig. 4-7(a). The leakage current density decreases and reaches a minimum at 400 °C. In contrast the dielectric constant decreases at 350 °C with a maximum value of 617. The dependence of the dielectric constant on the T_s is consistent with the ferroelectricity properties and preferred orientation [78]. Two mechanisms, resistive loss and relaxation loss, are applied for loss tanδ [79]. Since the dielectric constant and leakage current varies with T_s, the tangent loss also depends significantly on T_s, as shown in Fig. 4-10(b). For the resistive loss mechanism, energy is dissipated by mobile charges, and the tangent

loss depends on the magnitude of leakage current. In contrast, for relaxation loss mechanism, energy is dissipated by relaxation of dipoles, and the tangent loss is proportional to the dielectric constant. Thus, resistive loss and relaxation loss are the dominate mechanisms of tangent loss for films deposited under 350 °C and over 400 °C, accordingly. When T_s is between 350 °C and 400 °C, the evolution of the tangent loss demonstrates a transition region of mechanisms dominated by resistive loss and relaxation loss. As described above, the dielectric constant and leakage current of PSrT films are related to the preferred orientation and trapping states. Consequently, the dominate mechanism of tangent loss markedly depends on the preferred orientation and trapping states.

4-5 Reliability Analysis

4-5-1 Breakdown Properties

Figure 4-11(a) shows the time-zero dielectric breakdown (TZDB) and the leakage current density of PSrT films deposited at various T_s, which are extracted from the inset figure under a high electric field of 170 kV/cm. TZDB is influenced by oxygen stoichiometry, composition, crystallinity and interfacial properties of the films. As mentioned, PSrT film deposited at high T_s (450 °C) may produce serious volatilization of Pb-O compounds, resulting in more vacancies and defects in the films, which may deteriorate the crystallinity, leading to a higher leakage current than that of 400°C-deposited films. Hence, TZDB is maximal at T_s = 400 °C due to the suppressed Pb-O volatilization, good stoichiometric composition, fewer interface states and fewer defects inside films. Figure 4-11(b) displays the characteristics of time-dependent dielectric breakdown (TDDB) to predict the 10 year lifetime. TDDB

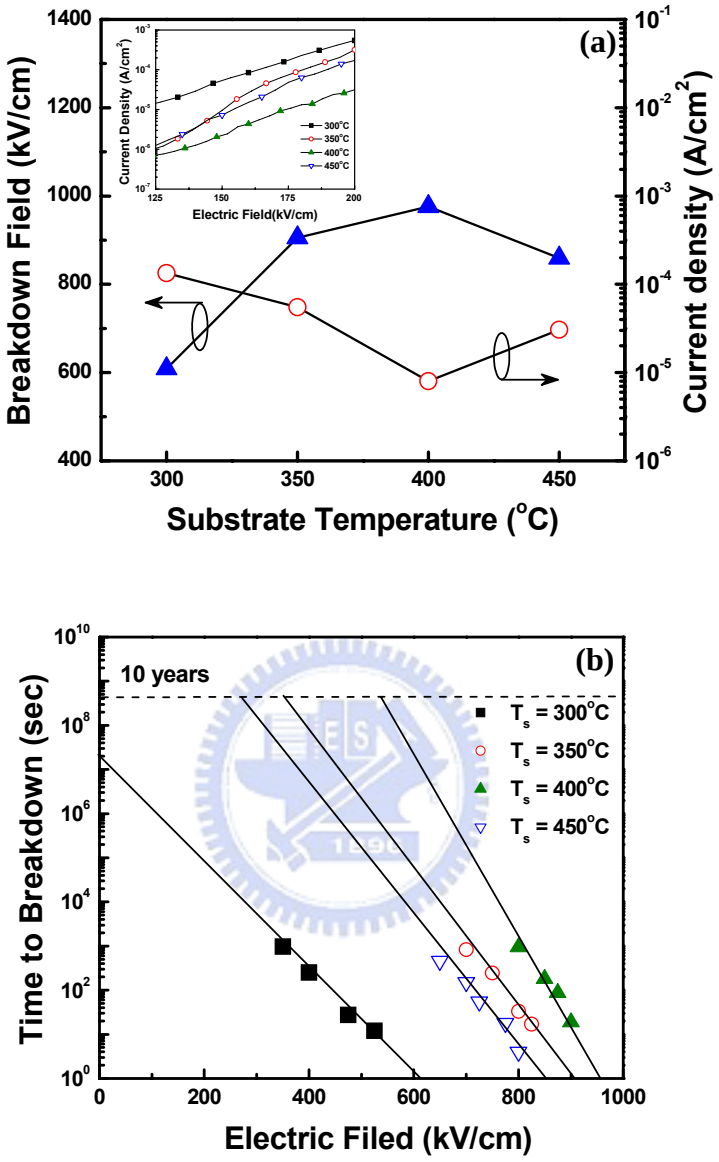


Figure 4-11 (a) TZDB field and leakage current density biased at +170 kV/cm, and (b) TDDB characteristics (as a function of electric field) of PSrT films deposited at various substrate temperatures.

is considered as the resistance degradation of dielectric films, which slowly increases the leakage current under constant temperature and dc field stress. The mechanism of resistance degradations in perovskite films could be categorized into the grain boundary model and the reduction model [18, 78, 65]. A large potential barrier across the grain boundary will result in shared drop in voltage and suppressed resistance degradation. The presence of grain boundaries also contribute to the trap distribution, through structural and chemical defects. On the other hand, the reduction model suggests that OVs and injection electrons cause resistance degradation. The defect chemistry is the key for the breakdown characteristics. Hence, PSrT films deposited at temperatures higher than 350 °C exhibit longer lifetime and higher breakdown field due to their smaller leakage current density, which result is attributed to the reduction of defects, fewer OVs and an improved interface.

4-5-2 Fatigue Properties

Figure 4-12(a) shows the properties of remnant polarization (P_r) fatigue of the switching operation of Pt/PST/Pt capacitors. The initial $2P_r$ value of fresh PST films is ~ 6 C/cm² as large as that of strontium bismuth tantalite (SBT), which is one of the famous ferroelectric materials and had been used to demonstrate NVRAM by Matsushita [73, 80]. This value is also comparable to that of PST films prepared by the sol-gel process at the temperature higher than 700 °C [47, 42]. The small remnant polarization may be connected to two causes. First, since PST films deposited at relatively low temperatures ranging from 300 – 450 °C, the crystallization of films may not be fully complete. Second, the thickness of films, in this work, is designed as 200 nm. From previous reports [81, 82], the grain size could be strongly limited by thickness. It was empirically observed that domain widths become much smaller as

the grain size or film thickness decreases. Furthermore, the interfaces of film, usually containing lots of defects, could act more important role to degrade electric properties of ferroelectrics as opposed to those of thick film or bulk. In short, the ferroelectric properties vary as a function of film thickness [83]. As a result, the thinner PST thin films may have a smaller remnant polarization as compared to thicker films or bulk. The 400 °C-deposited films start to fatigue from 10^8 switching cycles and demonstrate a slight degradation in P_r after 10^{10} switching cycles. For numerical analysis, Fig. 4-12(b) gives the normalized degradation of P_r and coercive field (E_c) before/after 10^{10} switching cycles. The fatigue endurance of PST films could be improved when T_s is higher than 350 °C. The loss in P_r and E_c is found to be less than 17 % after 10^{10} switching cycles. From previous works [25, 27], it has been pointed out that the space charge of OVs can be the major fatigue contributor, especial for OVs located at the interface of electrodes. The fatigue process will alter the space charge distribution and reduce the Schottky barrier height at the interface of electrodes, leading to the change of leakage currents. This result reveals that the fatigue behavior of PST films is evidently affected by the interfacial characteristics.

Figure 4-13 presents the log (J/T^2) versus $E^{1/2}$ plot of fresh and fatigued PST films deposited at 300 °C and 400 °C. The linear dependence of log (J/T^2) versus $E^{1/2}$ is identified as Schottky emission. It is suggested that the 400 °C-deposited PST film has fewer interface states before fatigued and exhibit nearly fatigued-free J-E characteristics. This result is consistent with the fatigue properties shown in Fig. 4-12(b). The SEM images shown in Fig. 4-3 confirm that the 400 °C-deposited films reveal a dense and uniform morphology, as well as an improved interface.

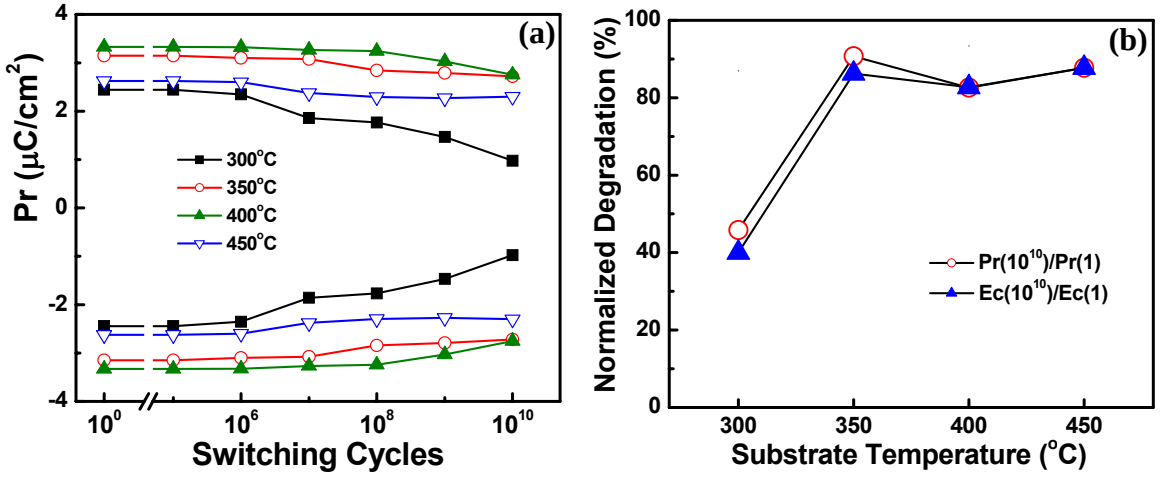


Figure 4-12 (a) Remnant polarization (P_r) vs switching cycles, and (b) normalized degradation of P_r and coercive field (E_c) of PSrT films deposited at various T_s before/after 10^{10} switching cycles.

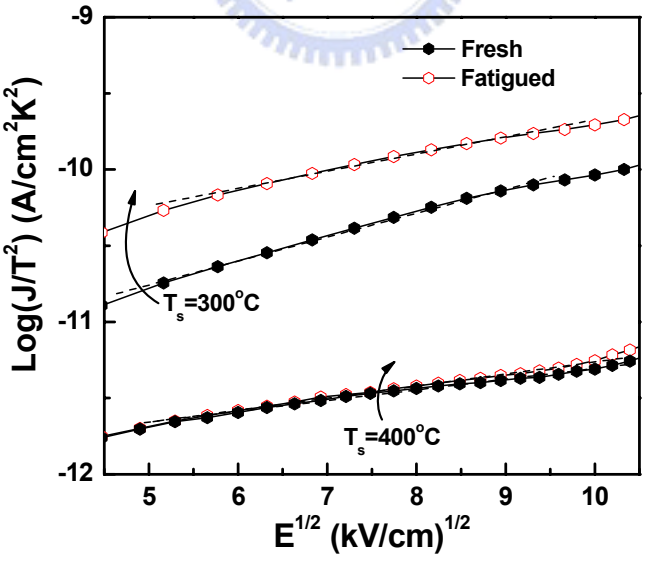


Figure 4-13 Schottky emission plot fitting of log (J/T^2) vs $E^{1/2}$ for the fresh and fatigued PSrT films prepared at substrate temperatures of 300 and 400 °C.

4-6 Summary

Low-temperature PLD PSrT films, deposited from 300 to 450 °C, have been demonstrated with dense and crack-free surface morphologies, evident crystallinity, and excellent ferroelectric properties, hence, can be integrated into IC-compatible process. Among the Pt/PSrT/Pt capacitors, the 350 °C-deposited one exhibits strong (100) preferred orientation, maximum dielectric constant of 617 and good ferroelectricity. The dependence of dielectric constant on T_s is consistent with the ferroelectricity properties and preferred orientation. The leakage mechanism of Pt/PSrT/Pt capacitors reveals SE/PFE at lower/higher applied field. The high substrate temperature ($T_s \geq 350$ °C) yields fewer interface states and better interfacial properties, and also shows fewer trapping states inside PSrT films, revealing that increasing T_s decreases the leakage current. This initial $2P_r$ value (~ 6 μC/cm^2) of fresh PSrT films is also comparable to that of PSrT films prepared by the sol-gel process at temperature higher than 700 °C. Furthermore, the 400 °C-deposited PSrT films reveal minimal leakage current density biased at +170 kV/cm, nearly fatigued-free J-E characteristics after 10^{10} switching cycles, the highest breakdown field, and the best TDDB behavior, which are well explained by the defect chemistry. But the excessively high T_s (450 °C) may produce serious volatilization of Pb-O compounds, resulting in more vacancies and defects in the films, which may be the cause of degradation in crystallinity, high-field leakage currents and reliability properties. On the other hand, the dominate mechanism of tangent loss for PSrT capacitors also significantly depends on the preferred orientation and trap states, corresponding to the dielectric constant and leakage current. In summary, the texture control and excellent electric characteristics of the PSrT films can be achieved with the PLD technique at low T_s.

Chapter 5 Investigations of Pulse-Laser-Deposited $(Pb,Sr)TiO_3$ Films at Various Ambient Oxygen Pressures

5-1 Concepts of Ambient Oxygen Influence on PLD PSrT Films

$PbTiO_3$ (PTO) film has been considered for applications in nonvolatile random access memory (NVRAM), but many drawbacks of this film must be improved, such as high coercive field, high crystallization temperature, and poor microstructure. The $(Pb,Sr)TiO_3$ (PSrT) is composed of the solid solutions: the $PbTiO_3$ (PTO) and the $SrTiO_3$ (STO). PTO and STO films, at room temperature, behave a tetragonal structure (ferroelectric phase) and a cubic structure (paraelectric phase), respectively, because PTO has the Curie temperature (T_c) at 490 ^oC and STO has the T_c at -220 ^oC. The effects of lead substituted by strontium (Sr) in the PTO film decrease the crystallization temperature and offer a good control of the dielectric properties at room temperature [47, 48]. Therefore, PSrT is suitable for memory, sensor, frequency tuning devices and microwave applications due to its large electric-field-dependent dielectric constant and composition-dependent Curie temperature [47, 48, 56-58, 84]. In this work, $(Pb,Sr)TiO_3$ films were prepared using the pulsed-laser deposition (PLD), which is simple, versatile, and capable of growing a wide variety of stoichiometric oxide films without subsequent high-temperature annealing and excellent for fabricating ceramic films with complex compounds. Hence, PLD is a potential technique, which could be integrated into low-temperature semiconductor processing to suppress the formerly-deposited underlayers from damage and eliminate the volatilization of PbO in lead-titanate-based thin films, which always degrades the crystallinity of perovskite phases and electric properties of ferroelectric

device [62].

Pulsed-laser deposition process consists of three steps [31]: (i) vaporization of a target material by laser beam, (ii) transport and interaction of a vapor plume with a background ambient, and (iii) condensation of the ablated material onto a substrate where a thin film nucleates and grows. Hence, the structural and electrical characteristics of the PLD ferroelectric films are strongly affected by processing parameters, such as substrate temperature, laser energy fluence (laser power density) and oxygen ambience.

To our knowledge, much less is known about the ambient oxygen effect on PLD ferroelectric films [85-88] and only a few works studied the properties of PLD PSrT films prepared on Pt/SiO_2 substrate [56-58]. Therefore, this chapter will investigate the influence of ambient oxygen pressure on structural and electrical characteristics of PSrT films deposited by low-temperature PLD. Moreover, the relationship between the texture and the corresponding ferroelectricity of PLD PSrT films will also be addressed.

5-2 Experiments

The 100 nm-thick platinum (Pt) film was sputtered onto SiO_2/p-type Si as the bottom electrode and followed by annealing at 450 ^oC for 30 min in N_2 ambient. Thin PSrT films with 200 nm in thickness were deposited on Pt/SiO_2/Si substrate electrodes with a KrF pulsed-laser deposition system (Lambda Physik Excimer Laser LPX 210i, λ = 248 nm). A set of optical lens was used to focus the excimer laser beam onto the $(Pb_{0.6},Sr_{0.4})TiO_3$ target in vacuum. The PSrT target was prepared with conventional ceramic fabrication process [31]. The vacuum chamber was pumped down to a base pressure of 0.1 mTorr and then refilled O_2 as working gas. The

vaporized species of the target transferred and deposited on the substrate heated by thermal heater. The target to substrate distance was 4 cm. The deposition temperature was fixed at a relative low substrate temperature of 400 °C, calibrated at the wafer upper surface. The ambient oxygen pressure (P_{O_2}) was varied from 50 mTorr to 200 mTorr. The laser pulsed rate and the average energy fluence were 5 Hz and 1.55 J/cm² per pulse, respectively.

The film thickness and the surface morphology of PSrT films were examined by field emission scanning electron microscopy (FESEM) (S-4000, Hitachi). The surface roughness of PSrT films were inspected by atomic force microscope (AFM) (DI Nano-Scope III, Digital Instruments). An Auger electron spectroscope (AES) (Auger 670 PHI Xi, Physical Electronics) was used to analyze the elemental ratios on the surface and the elemental depth profile of PSrT films. The crystallinity of the film was analyzed by X-ray diffractometer (D5000, Siemens, using Cu Kα, λ ~ 0.154 nm). The transmission electron microscopy (TEM) samples were prepared by standard sample preparation techniques with tripod polishing and ion milling using the Gatan PIPS system operated at 3 kV. The TEM experiments were carried out on JEM-2000FX (JEOL Ltd.) operated at 200 keV.

After the physical examinations, the Pt top electrodes, with a thickness of 100 nm and a diameter 75 μm, were deposited by sputtering and patterned by shadow mask process to form a Pt/PSrT/Pt capacitor structure. An automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station was used to measure the leakage current (I-V) characteristics and breakdown properties. A capacitance-voltage (C-V) analyzer (Package 82 system C-V 590, Keithley Co.) was also used to measure C-V curves at 100 kHz, and the dielectric constant was extracted from the C-V measurement. The

ferroelectric polarization versus electric field (P-E) characteristics of the PSrT film were determined directly by virtual ground circuits (RT-66A standardized ferroelectric testing system, Radiant Technologies). A pulse generator (8110A, Hewlett Packard) and a pulse/function generator (8116A, Hewlett Packard) were connected together with low noise BNC cables to generate +3 V/-3 V bipolar wave pulsed at 1 MHz, confirmed by an oscilloscope (54645A, Hewlett Packard), as an input signal for the measurement of polarization switching degradation (fatigue).

5-3 Physical Analysis

PLD PSrT films were prepared at various ambient oxygen pressures (P_{O_2}). Figure 5-1 shows that the deposition rate of PSrT films is maximum at P_{O_2} = 50 mTorr and then decreases as P_{O_2} increases due to the increasing collisions between ejected species and the ambient oxygen gas. Moreover, film thickness could be controlled and roughly considered as a time-based function for different P_{O_2}. In general, the situation of collisions affects the stacking of clusters during PLD, which directly associates with morphologies and structural characteristics of films [31].

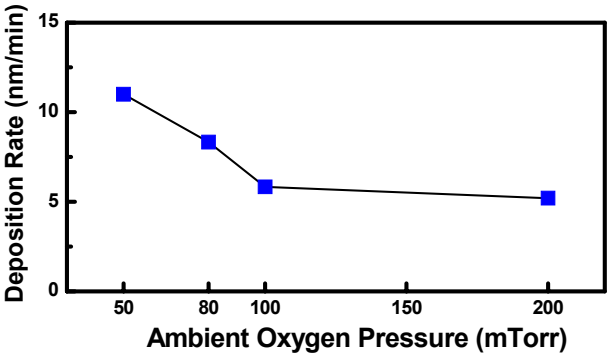


Figure 5-1 Deposition rate of PLD PSrT films prepared at various ambient oxygen pressures (P_{O_2}) on Pt/SiO_2/Si.

Figure 5-2 shows SEM surface morphologies of PLD PSrT films deposited at various P_{O_2} on Pt/SiO_2/Si (100) wafers. As the P_{O_2} increases, the morphology becomes denser and less porous, and the clusters gradually became more uniform, rounded and small, which reflects the better stacking of clusters and fewer defects. Usually, the grain size may be confined by the size of a cluster. Thus, a larger cluster may connect to larger grain size and fewer grain boundaries. We will address later, as a result of the electrical characteristics, that the dense morphology of PSrT films deposited at higher P_{O_2} exhibits fewer interfacial states and fewer deep trapping states inside films.

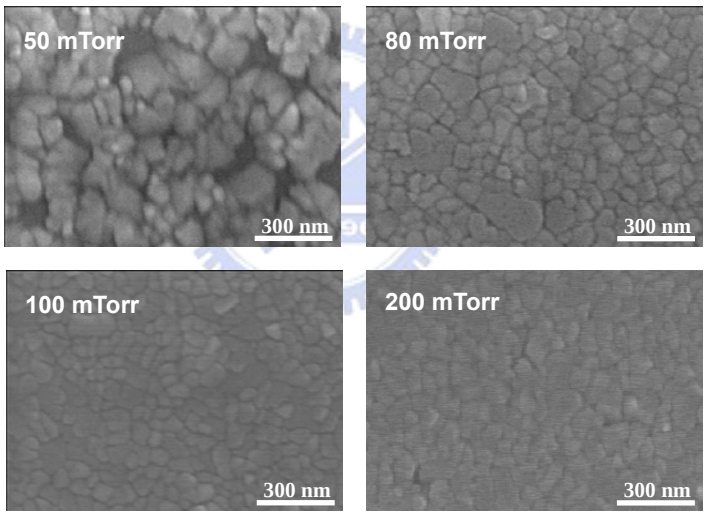


Figure 5-2 SEM surface morphologies of PLD PSrT films deposited at various ambient oxygen pressures on Pt/SiO_2/Si.

Figure 5-3(a) shows AFM images of PLD PSrT films deposited on Pt/SiO_2/Si (100) wafers and indicates the surface morphology is a function of P_{O_2} associated with increasing collisions between ejected species and the ambient gas. For numerical analysis, Fig. 5-3(b) gives the normalized root-mean-square roughness

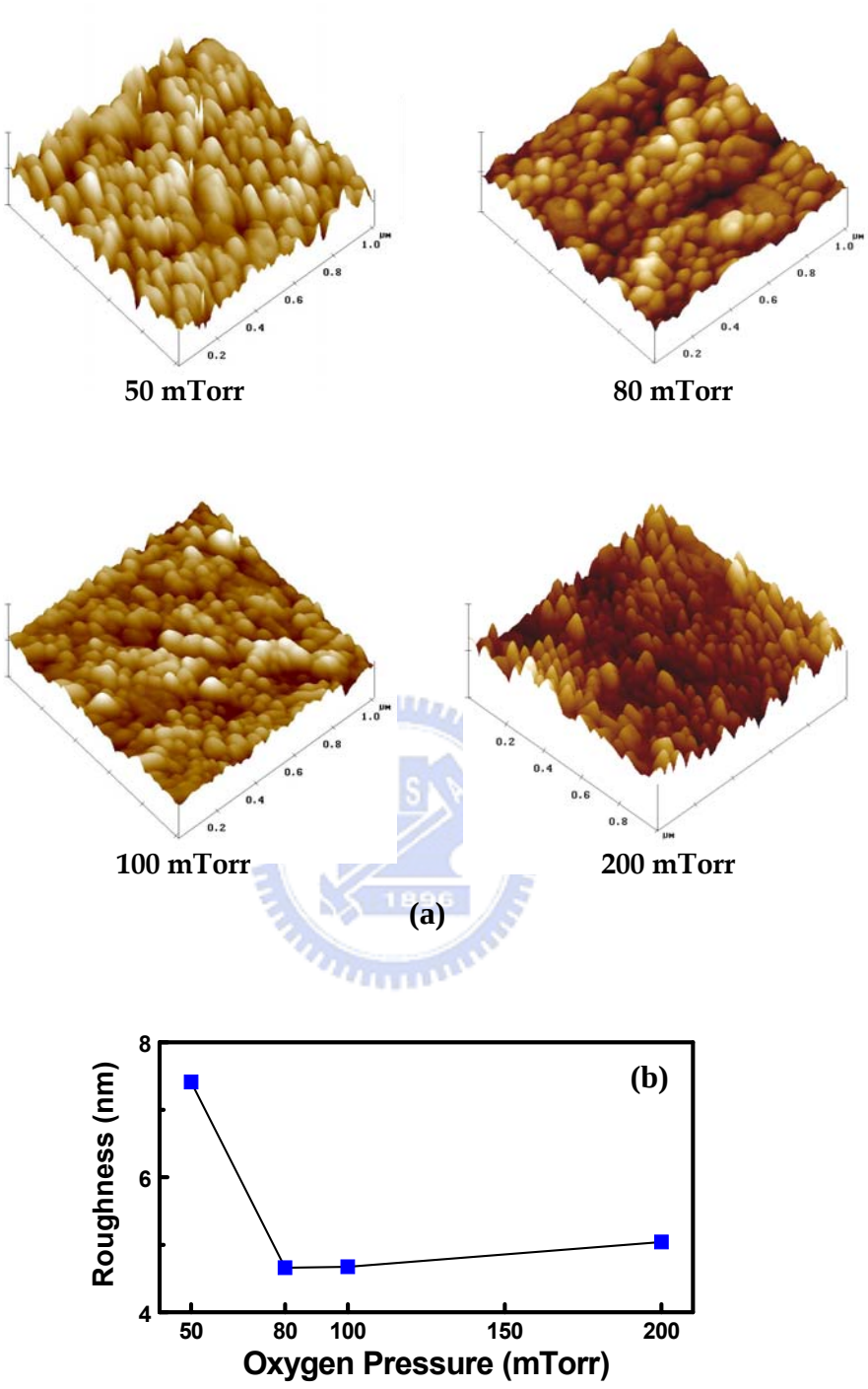


Figure 5-3 (a) AFM images and (b) surface roughness of PLD PSrT films deposited at various ambient oxygen pressures (P_{O_2}) on Pt/SiO_2/Si (100) wafers.

(R_{RMS}), revealing that the maximum R_{RMS} and minimum R_{RMS} are 7.41 nm and 4.66 nm as P_{O_2} equals to 50 and 80 mTorr, respectively, and then R_{RMS} increases very slightly as P_{O_2} increases. As a result of Fig. 5-2 and Fig. 5-3, films deposited at a higher P_{O_2} have denser, less porous and smoother surface morphology.

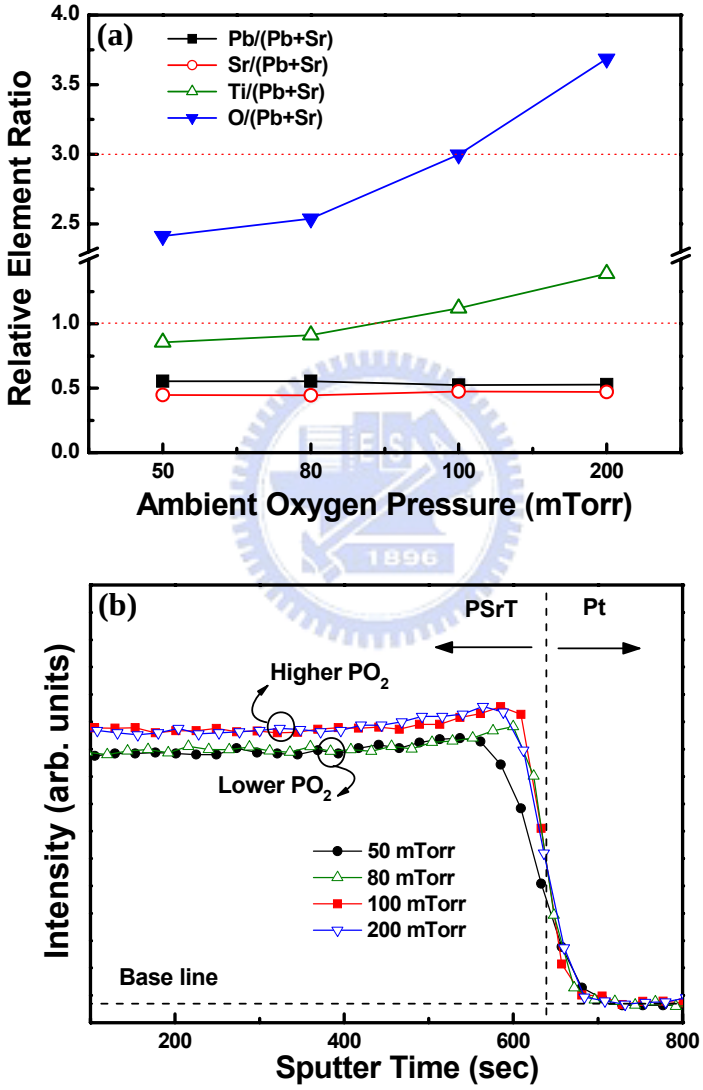


Figure 5-4 (a) Surface relative element ratios and (b) intensity of oxygen element in AES depth profiles of PSrT films deposited at various ambient oxygen pressures on Pt/SiO_2/Si (100) wafers.

Figure 5-4(a) presents the element ratios, calibrated with the stoichiometric composition of $(Pb_{0.6},Sr_{0.4})TiO_3$ target, on the surface of PSrT films analyzed by AES technique and reveals the film composition is a function of P_{O_2}. It can be seen that the element ratio of Ti/(Pb+Sr) increases markedly with the increase of P_{O_2} as opposed to the element ratio of Pb/(Pb+Sr). Besides, the element ratio of Sr/(Pb+Sr) slightly varies with P_{O_2}. It also indicates that the element ratio of O/(Pb+Sr) increases from 2.41 to 3.69 as P_{O_2} increases. Figure 5-4(b) presents the intensity of oxygen element in AES depth profiles and indicates higher oxygen concentration for films deposited at higher P_{O_2}. Thus, it suggests that the oxygen content of films can be strongly compensated at higher P_{O_2}.

Figure 5-5(a) displays the X-ray diffraction (XRD) pattern of PSrT films deposited at various P_{O_2} on $Pt/SiO_2/Si$ (100) wafers. All the diffraction peaks are indexed as (100), (110), (210) and (211) planes of $(Pb_{1-x}Sr_x)TiO_3$ perovskite phases [47, 48, 50, 58, 59, 75]. The crystalline PSrT films are observed at such low temperature (400 °C) because (i) the addition of strontium (Sr) induces a lower crystallization temperature of PSrT than that of PZT [47], and (ii) the PLD technique can preserves the crystalline phases and stoichiometric ratio of the target material at low substrate temperature [31]. Furthermore, the intensity of the (100) and (110) diffraction peaks varies significantly as the ambient oxygen pressure increases. Figure 5-5(b) quantifies the XRD spectral analysis using *Eq. (4-1)*. In Fig. 5-5(b), I_{110} increases with increasing P_{O_2} and shows a maximum at P_{O_2} = 200 mTorr. In contrast, I_{100} exhibits the maximum at P_{O_2} = 80 mTorr and then decreases dramatically with increasing P_{O_2}. Thus, X_{100}, the relative proportion of the (100) orientation, shows the values as 51 ~

55 % with a little variation at P_{O_2} ≤ 100 mTorr and then decreases noticeably as P_{O_2} increases from 100 to 200 mTorr. A transition from (100) preferred orientation to (110) preferred orientation of PSrT films is observed as P_{O_2} increases above 100 mTorr. According to the XRD result, it reveals the possibility to control the texture characteristics of PLD PSrT films by ambient oxygen pressure.

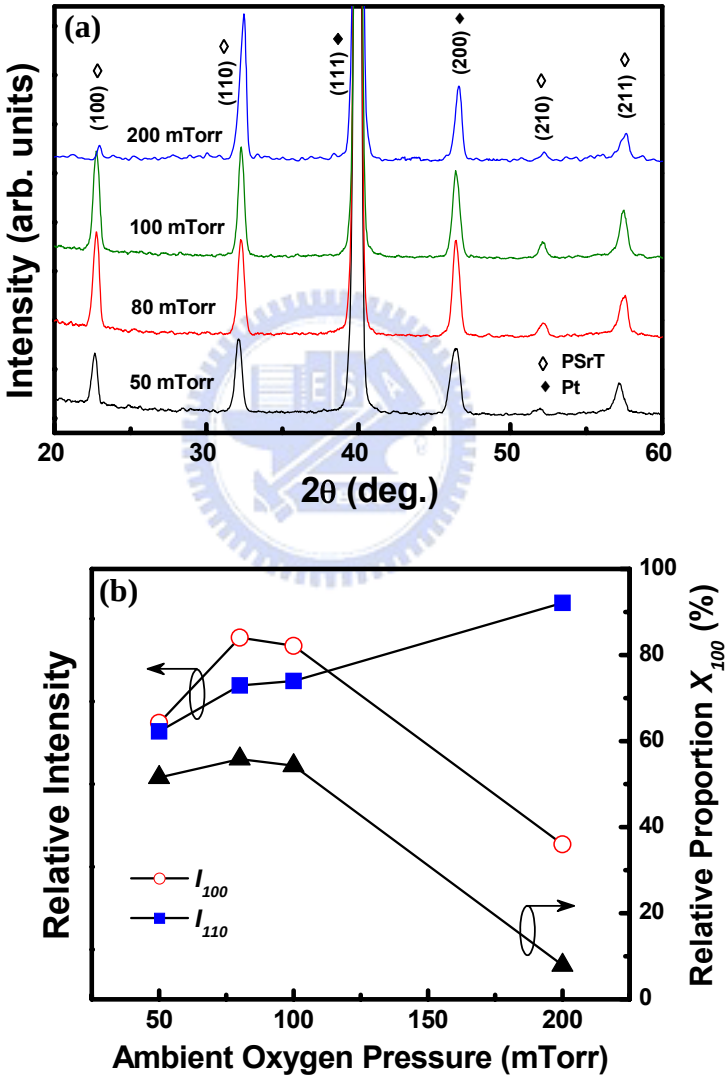


Figure 5-5 X-ray diffraction analyses of PSrT films deposited at various ambient oxygen pressures on Pt/SiO_2/Si (100) wafers: (a) diffraction pattern and (b) texture characteristics.

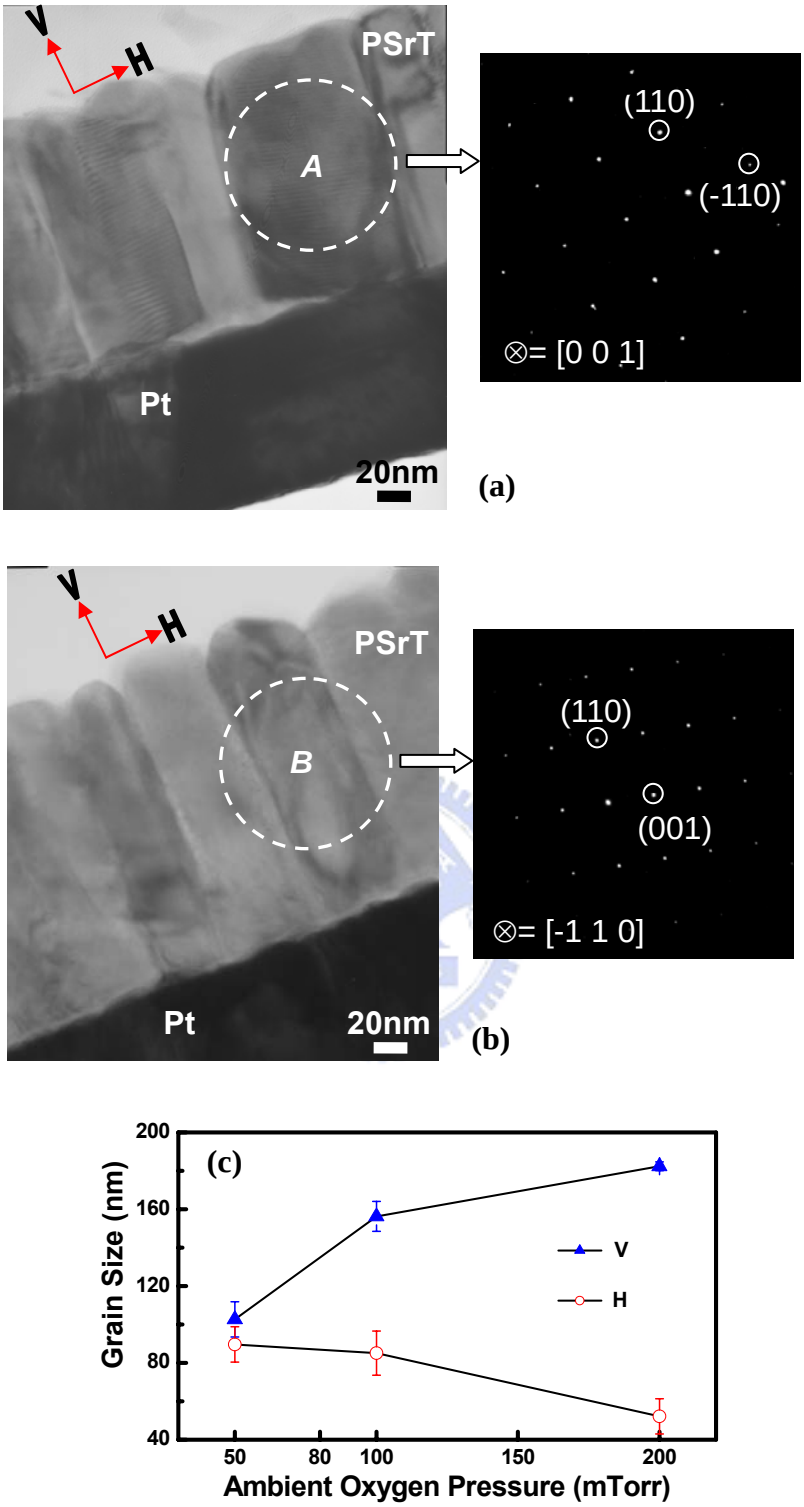


Figure 5-6 Cross-sectional TEM images and selected-area diffraction patterns of PLD PSrT films deposited at (a) P_{O_2} = 100 mTorr and (b) P_{O_2} = 200 mTorr. (c) Grain size in the vertical (V) and horizontal (H) directions of columnar structures.

Figures 5-6(a) and 5-6(b) show the cross-sectional TEM images of PSrT films deposited at 100 mTorr and 200 mTorr, respectively. It also indicates that the morphology of PSrT grains reveals a column-like granular shape. The corresponding selected-area diffraction patterns obtained from granular *A* and *B* (inserted in Figs. 5-6(a) and 5-6(b)) also reveal that the granular grains are single crystal grains. Furthermore, the grain size of PSrT in the vertical (V) and horizontal (H) directions of columnar structures are strongly influenced by P_{O_2}. Fig. 5-6(c) presents the grain size in the vertical and horizontal directions of granular PSrT grains from the TEM images. The grain size in vertical direction increases with increasing P_{O_2} and the maximum grain size is close to film thickness (200 nm) as P_{O_2} = 200 mTorr. In contrast, the horizontal grain size shrinks as P_{O_2} increases and reaches the minimum at 200 mTorr, in agreement with the surface morphologies shown in Fig. 5-2 and Fig. 5-3(a). The plan-view TEM images of films deposited at 50 mTorr and 200 mTorr are shown in Figs. 5-7(a) and 5-7(b), respectively. PSrT film deposited at 50 mTorr shows poly grains structure with uneven grain size. Furthermore, some regions reveal the amorphous state and can be observed on electron diffraction pattern with diffused ring (inset in Fig. 5-7(a)). The images of films deposited at 200 mTorr reveals denser and more uniform poly grains with 60 - 80 nm in diameter (consistent with the observations of Fig. 5-2 and Fig. 5-6) and less amorphous regions comparing to films deposited at 50 mTorr. In addition, high-resolution TEM (HRTEM) images of PSrT films deposited at 50 mTorr and 200 mTorr were shown in Figures 5-7(c) and 5-7(d), respectively. Both of them reveal the clear lattice images along the PSrT $[1\bar{1}0]$ zone axis. An enlarged zone from square marks in Figs. 5-7(c) and 5-7(d) are calculated by using multislice image simulations (using Diamond 2.1c,

Crystal Impact) and good agreement is observed between the calculated and experimental contrasts at a crystal thickness of 7 nm and a defocus length of -48 nm. The slice image simulations used BST reference cell as basis, where Ba atom was replaced by Pb atom. As mentioned above, it is clear that the surface morphology, surface roughness, oxygen composition, preferred orientation, and microstructure of PSrT films could apparently be affected by ambient oxygen pressures during PLD.

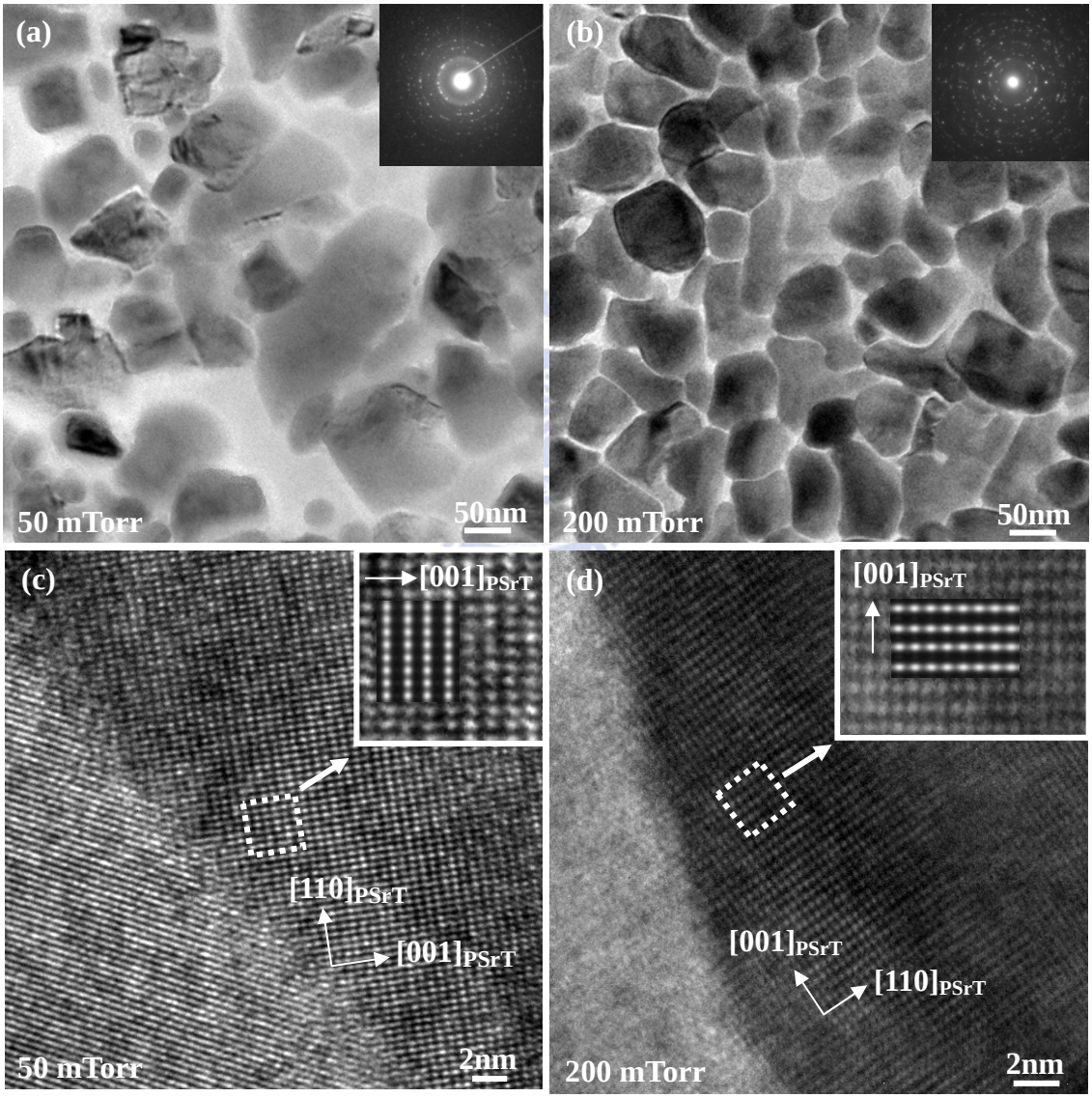


Figure 5-7 (a)-(b) Plane-view TEM images and electron diffraction patterns, and (c)-(d) high-resolution TEM (HRTEM) images and multi-slice image simulations for PSrT films deposited at 50 mTorr and 200 mTorr.

5-4 Electrical Analysis

Figure 5-8(a) plots the capacitance versus electric field (C-E) characteristics of the PSrT films deposited at various P_{O_2} and presents the typical C-E hysteresis characteristics of ferroelectric materials. The capacitance shows a maximum value at negative bias corresponding to the coercive field (E_c) of the hystersis loop as the applied field sweeps from +200 kV/cm to -200 kV/cm. On the other hand, the maximum capacitance appears at positive E_c when the applied field sweeps in the opposite direction. The four C-E curves are not symmetric, probably because of the difference in the configuration of electrodes used in the measurement, since the bottom electrode has a large area and the other, defined by shadow mask, is small. Furthermore, the C-E hysteresis loop expands from P_{O_2} = 50 mTorr to 100 mTorr and then shrinks as P_{O_2} is higher than 100 mTorr, suggesting that the ferroelectricity of PSrT films is suppressed at higher P_{O_2} (200 mTorr). The zero-field capacitance, used in the dielectric constant calculation as shown in Fig. 5-8(b), depends considerably on the P_{O_2}. The polarization of the lead-titanate-based crystal is maximum in the [100] direction, so the polarizations of the films enhanced with the preferred (110) orientation are weaker than those of the films with the preferred (100) orientation [4, 5]. Furthermore, the tetragonality (c/a), i.e. the ratio of c-axis/a-axis lattice constant obtained by electron diffraction patterns (inset in Fig. 5-7(a) and 5-7(b)), of the PSrT films deposited at 50 mTorr and 200 mTorr are ~ 1.033 and ~ 1, accordingly. The larger tetragonality for films deposited at lower P_{O_2} may be attributed to the oxygen deficiency [90-92]. Because the ferroelectric dipole originates from ionic displacement in the c-axis direction, large spontaneous polarization is

obtained with the elongated c-axis, the larger tetragonality. However, the lower P_{O_2} -deposited film (most oxygen deficient) exhibits larger leakage current density (addressed later), which usually leads to charge lost of capacitor and degrades the dielectric constant. In other words, the dielectric and ferroelectric properties of PSrT films are the combined effects of the preferred-orientation and oxygen content. Thus, the PSrT film deposited at 100 mTorr exhibits the maximum dielectric constant of 642, which is connected with the enhanced (100) preferred-orientation (Fig. 5-5(b)) and the higher oxygen concentration (Fig. 5-4).

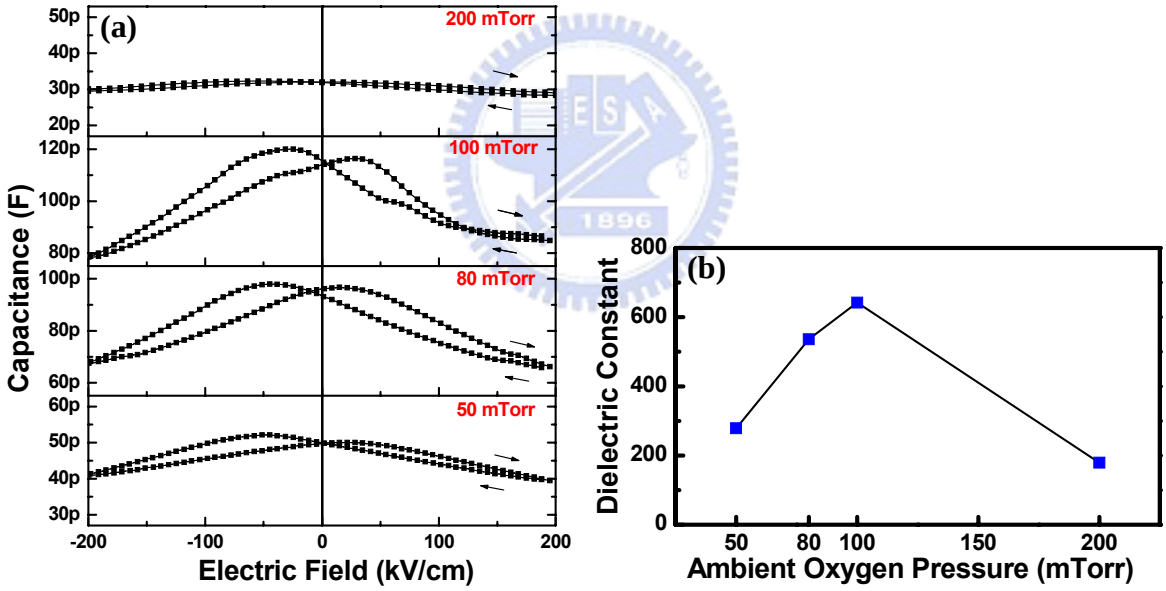
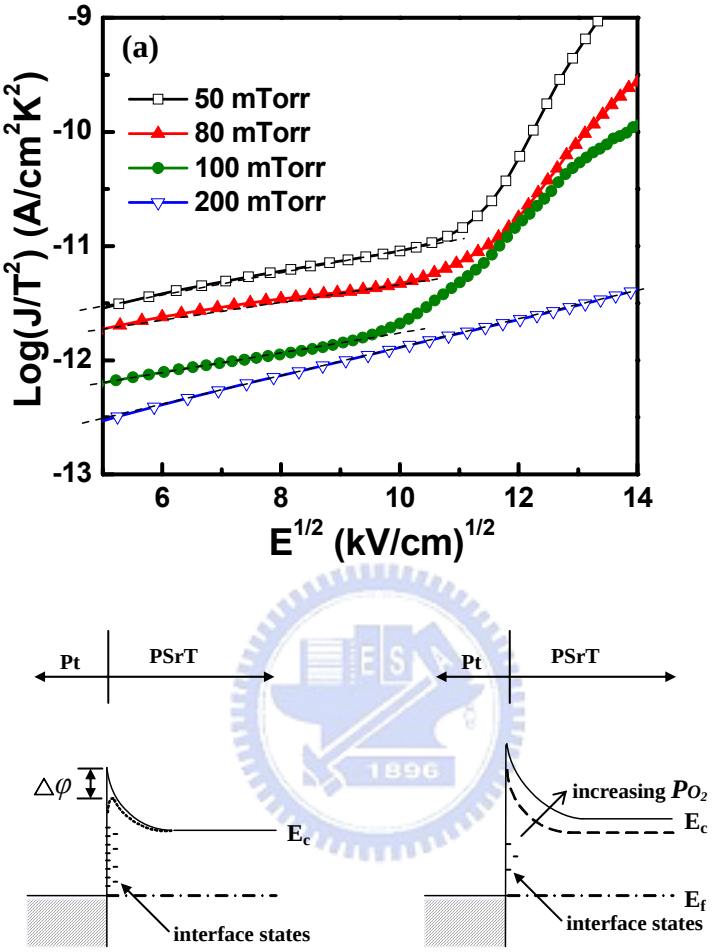


Figure 5-8 (a) Capacitance versus electric field (C-E) hysteresis loops and (b) dielectric constant of Pt/PSrT/Pt capacitors prepared at various ambient oxygen pressures.

The leakage current data are interpreted as Schottky emission (*SE*) at lower electric fields and Poole-Frenkel emission (*PFE*) at higher electric fields, which are used to analyze the interface-limited and bulk-limited characteristics of Pt/PSrT/Pt capacitors, respectively [16-18]. The *SE* behavior and *PFE* behavior are expressed as *Eq. (4-2)* and *Eq. (4-3)*, accordingly. If the conduction current follows *SE* behavior, then a log (J/T^2) against $E^{1/2}$ plot should be linear. Similarly, a log (J/E) against $E^{1/2}$ plot can be made for *PFE*. Figure 5-9(a) presents the *SE* plot of Pt/PSrT/Pt capacitors deposited at various P_{O_2} and the dashed lines represent the fitted results. The inhibited leakage current of PSrT films deposited at higher P_{O_2} is correlated with the lower Schottky barrier, less interface states and fewer space charges (charged defects) due to the denser, smoother surface morphology (Fig. 5-2 and Fig. 5-3) and fewer oxygen vacancies (OVs) (i.e. larger oxygen concentration shown in Fig. 5-4). The OVs will act as charged defects to degrade leakage currents as expressed by *Eq. (4-9)*. As seen in Fig. 5-9(a), it indicates that films deposited at 200 mTorr exhibit *SE* conduction only (without a transition of conduction). Figures 5-9(b) – 5-9(c) draw the electron energy band at the interface of substrate electrodes and reveals PSrT films act as n-type semiconductors due to the generation of oxygen vacancies in ABO_3 perovskites [2, 18]. In the case with lower P_{O_2}, more interface states result in more charge accumulation and severe image-force effect at the edge of electrodes, leading to the decrease ($\Delta\varphi$) of Schottky barrier height [2, 76]. In the case with higher P_{O_2}, the increase of P_{O_2} yields fewer interface states and a higher Schottky barrier, resulting in a small leakage current.



(b) Lower P_{O_2} **(c) Higher** P_{O_2}

Figure 5-9 (a) Experimental and fitted log (J/T^2) versus $E^{1/2}$ (Schottky emission) plots, and the electron energy band at the interface of substrate electrodes for PSrT films deposited at (b) lower P_{O_2} and (c) higher P_{O_2}.

Figure 5-10(a) shows the *PFE* plot using the same experimental current-voltage (I-V) data, indicating that the curves follow *PFE* behavior when the bias exceeds +130 kV/cm and trapping states exist for PLD PSrT films deposited at 50-100 mTorr. In contrast, the leakage current of PSrT films deposited at P_{O_2} = 200 mTorr is not governed by *PFE*. Figure 5-10(b) reveals that PSrT films deposited at lower P_{O_2} have more OVs and rougher surface than those deposited at higher P_{O_2}, yielding more interfacial states as stated in Fig. 5-9(b) and more trapping states inside PSrT films. Thus, the magnitude of leakage current is governed by the balance between the injected electron current and the trapping/detrapping rate. The field-assisted emission of trapped charged carriers follows *PFE* emission rate, revealing bulk-limited conduction as the dominant mechanism for the lower P_{O_2} case. In contrast, Figure 5-10(c) indicates that higher P_{O_2} yields fewer interfacial states with the higher barrier and fewer trapping states inside PSrT films, caused by smoother surface and fewer OVs. Therefore, thermionic emission (*SE* behavior), i.e. interface-limited conduction, is the dominant mechanism at higher P_{O_2}. Consequently, except the PSrT films deposited at 200 mTorr reveal *SE* behavior at the applied field range, the conduction mechanism of PLD PSrT films reveals interface-limited (*SE*) conduction at low electric field and changes to bulk-limited (*PFE*) conduction at high electric field.

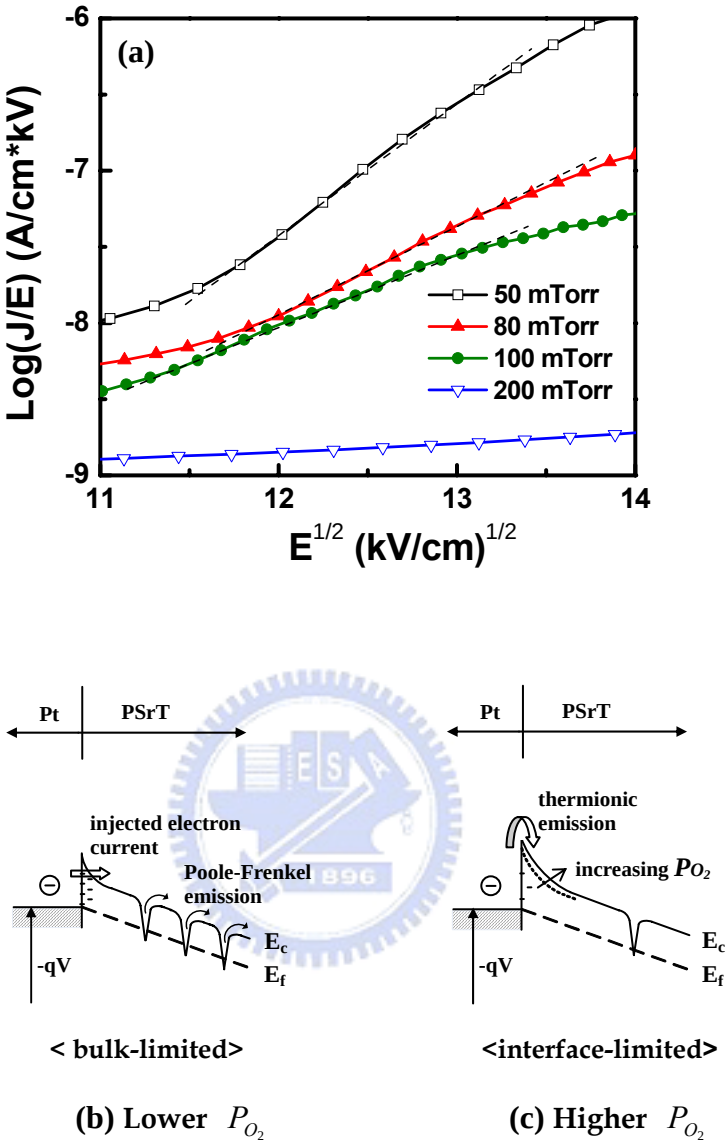


Figure 5-10 (a) Experimental and fitted log (J/E) versus $E^{1/2}$ (Poole-Frenkel emission) plot, and the electron energy band for PSrT films deposited at (b) lower P_{O_2} and (c) higher P_{O_2}.

5-5 Reliability Analysis

5-5-1 Breakdown Properties

Figure 5-11 displays the time-zero dielectric breakdown (TZDB) and the characteristics of time-dependent dielectric breakdown (TDDB) of the Pt/PSrT/Pt capacitors, which are enhanced as P_{O_2} increases. TZDB is influenced by oxygen stoichiometry, crystallinity and interfacial properties of the films. TDDB is regarded as the resistance degradation of dielectric films to predict the 10 year lifetime, which slowly increases the leakage current under constant temperature and dc field stress. The mechanism of resistance degradations in perovskite films could be categorized into the grain boundary model and the reduction model [18, 64, 65]. The grain boundary model indicates that a large potential drop across the high-resistivity grain boundary. Films with smaller grain sizes exhibit more grain boundaries, resulting in the shared drop in voltage and the suppressed resistance degradation. On the other hand, the reduction model suggests that OVs and injection electrons cause resistance degradation. Consequently, PSrT films deposited at higher P_{O_2} exhibit longer lifetime and higher breakdown field due to their smaller leakage current density (inset in Fig. 5-11(a)), in terms of the reduction of defects (Fig. 5-9 and Fig. 5-10), fewer OVs (i.e. larger oxygen concentration shown in Fig. 5-4), an improved interface (i.e. the denser, less porous and more uniform morphology shown in Fig. 5-2), and small cluster sizes.

5-5-2 Fatigue Properties

Figure 5-12 demonstrates the properties of remnant polarization (P_r) fatigue of Pt/PSrT/Pt capacitors after the switching operation. This fatigue examination does

not include the film deposited at 200 mTorr because of its indistinct ferroelectricities. Films deposited at 80 mTorr start to fatigue from 10^8 switching cycles and reveal a slight degradation in P_r (less than 17 %) after 10^{10} switching cycles. From previous works [2, 25-27], it has been pointed out that the space charge of OVs can be the major fatigue contributor. The fatigue process will alter the space charge distribution and reduce the Schottky barrier height at the interface of electrodes, leading to the change of leakage currents.

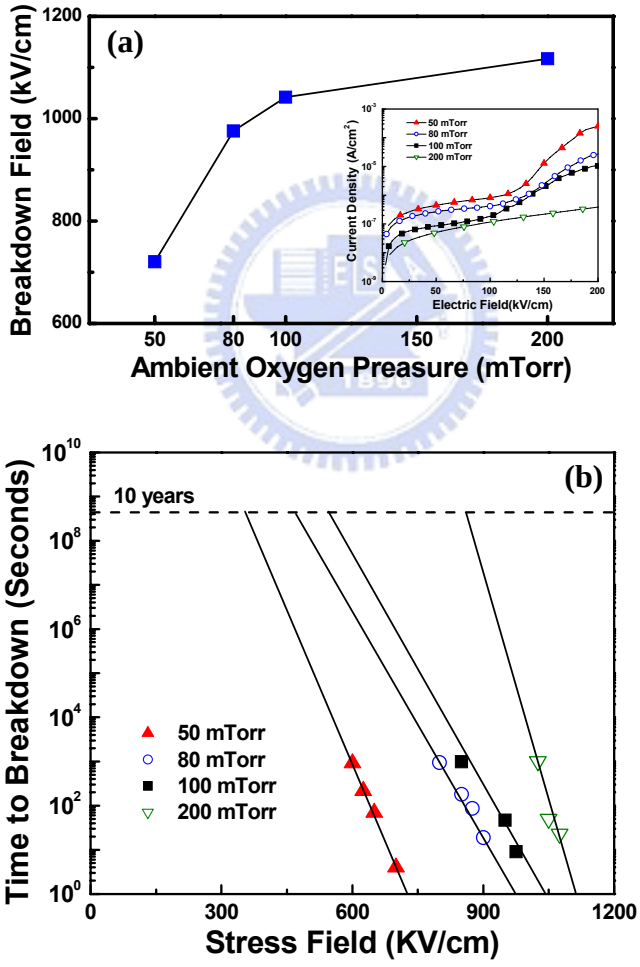


Figure 5-11 (a) TZDB (time-zero dielectric breakdown) and (b) TDDB characteristics (time-dependent dielectric breakdown as a function of electric field) of PSrT films deposited at various ambient oxygen pressures.

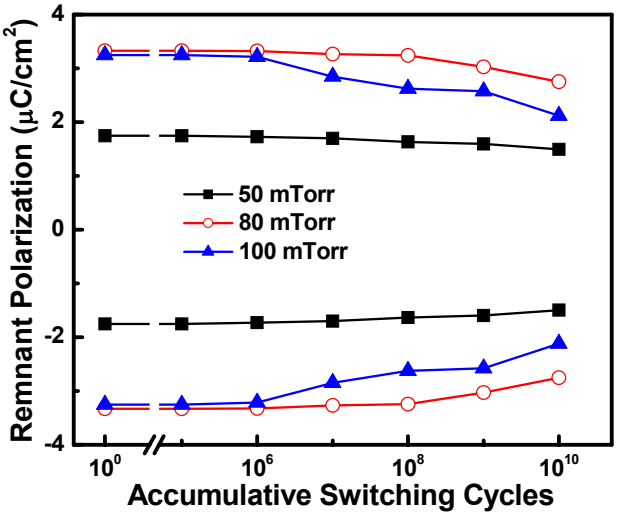


Figure 5-12 The fatigue behaviors of remnant polarization (P_r) versus accumulative switching cycles of Pt/PSrT/Pt capacitors prepared at various P_{O_2}.

Later in the text, the leakage current data before/after fatigued switching operation are interpreted as *SE* (log (J/T^2) against $E^{1/2}$) at lower electric fields and *PFE* (log (J/E) against $E^{1/2}$) at higher electric fields to analyze the space charge correlated to interface-limited and bulk-limited characteristics, accordingly [4, 5, 43]. Figure 5-13(a) presents the *SE* plot of fresh and fatigued Pt/PSrT/Pt capacitors deposited at various P_{O_2} and the dashed lines work as the fitted results. The inhibited leakage current biased at lower electric fields of PSrT films deposited at higher P_{O_2} is correlated with the lower Schottky barrier, less interfacial states and fewer space charges (charged OVs) due to the improved interface (Fig. 5-2) and fewer OVs. It suggests that the films deposited at higher P_{O_2} have fewer interface states before fatigued and exhibit nearly fatigued-free J-E characteristics at lower electric fields. Figure 5-13(b) shows the *PFE* plot using the same experimental current-voltage (I-V) data. Likewise, the inhibited leakage current of films deposited

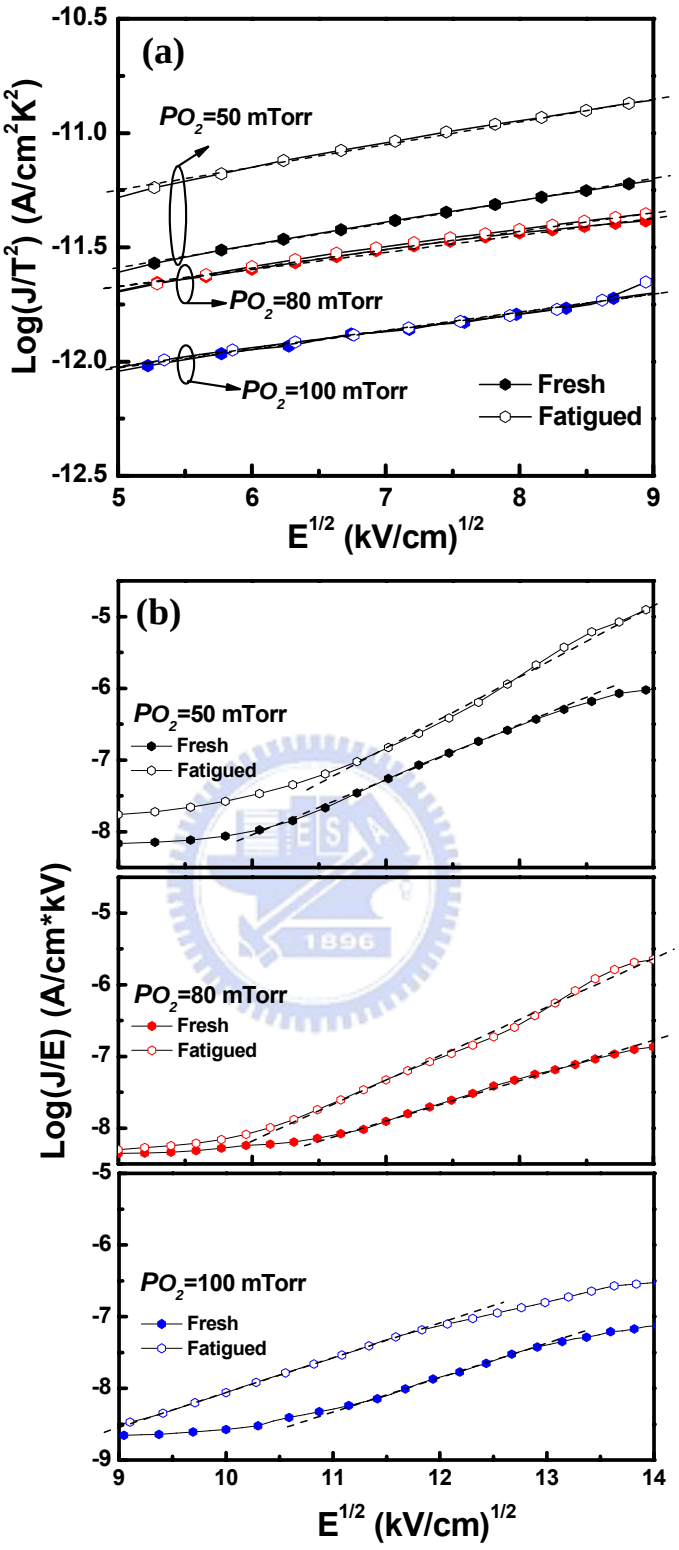


Figure 5-13 (a) Schottky emission plot fitting of log (J/T^2) versus $E^{1/2}$ and (b) Poole-Frenkle emission plot fitting of log (J/E) versus $E^{1/2}$ for the fresh and fatigued Pt/PSrT/Pt capacitors prepared at various P_{O_2}.

at higher P_{O_2} and biased at higher electric fields is associated with less deep trapping states and fewer space charges (charged OVs) inside films due to fewer OVs. It indicates that the onset of *PFE* behaviors of fresh Pt/PSrT/Pt capacitors appears when the bias exceeds +130 kV/cm. In contrast, the onset of *PFE* behaviors of fatigued Pt/PSrT/Pt capacitors changes from above +130 kV/cm to +90 kV/cm when P_{O_2} increases from 50 to 100 mTorr. It suggests that films deposited at higher P_{O_2} exhibit less interfacial states with an improved interface, which inhibit OVs to generate and accumulate at the interface of electrodes, but prefer to create OVs inside films after fatigued.

Figure 5-14 illustrates the electron energy band for the fresh and fatigued Pt/PSrT/Pt capacitors deposited at low and high P_{O_2}. It reveals that PSrT films deposited at lower P_{O_2} have porous surface and more OVs than those deposited at higher P_{O_2}, yielding more interfacial states and more trapping states inside films. As a result, there are more OVs accumulated at the interface and the fatigue properties are dominated by the interfacial states. Conversely, PSrT films deposited at higher P_{O_2} exhibit improved interfaces and fewer OVs, yielding fewer interfacial states and fewer deep trapping states inside films. It suggests that OVs generate inside films and the fatigue properties are dominated by deep trapping states. Hence, films deposited at 80 mTorr exhibit nearly fatigued-free J-E characteristics at lower electric fields and a higher onset field of *PFE* behaviors of fatigued Pt/PSrT/Pt capacitors. The results could be connected with the fewer OVs and a balance distribution of OVs located at the interfaces and inside films, corresponding to the optimum fatigue resistance with fatigue starting from 10^8 switching cycles.

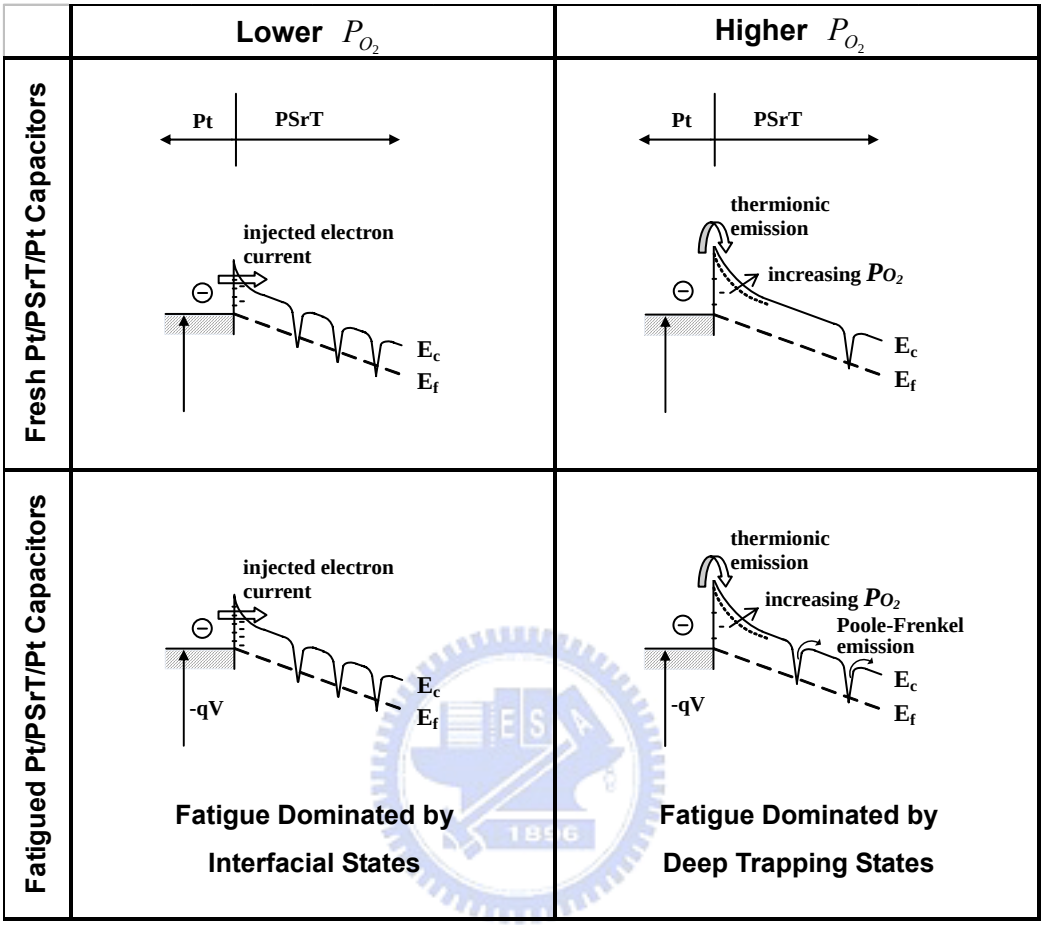


Figure 5-14 Schematic drawings of the electron energy band for the fresh and fatigued Pt/PSrT/Pt capacitors deposited at low and high P_{O_2}.

Finally, Table 5-1 summarizes the physical properties and electrical characteristics of PLD PSrT films deposited at various oxygen partial pressures on $Pt/SiO_2/Si$ (100) wafers.

Table 5-1 Summarized characteristics of PLD PSrT films deposited at various ambient oxygen pressures on $Pt/SiO_2/Si$ (100) wafers.

Ambient Oxygen Pressure (PO_2, mTorr)	**50**	**80**	**100**	**200**
RMS Roughness (R_{RMS}, nm) [a)]	7.41	4.66	4.68	5.04
X_{100} Relative Proportion (%) [b)]	51.5	55.8	54.3	7.9
TZDB Field (kV/cm)	721	976	1042	1117
Dielectric Constant [c)]	279	536	642	180
Current Density ($\mu A/cm^2$) [d)]	0.812	0.416	0.187	0.119

[a)] Evaluated from AFM analysis.

[b)] Evaluated from X-ray diffraction spectra.

[c)] Evaluated from C-E curves at zero-field.

[d)] Evaluated from J-E curves at +100 kV/cm.

5-6 Summary

The preferred orientation, microstructure, and electrical characteristics of PSrT films could be apparently affected by ambient oxygen pressures during low-temperature PLD. The smoother surface morphology, the higher oxygen composition, and the stronger intensity of (110) orientation could be evidently influenced by increasing P_{O_2} during PLD. In addition, the (100) preferred orientation transit to the (110) preferred orientation above 100 mTorr, suggesting that the ferroelectricity of PSrT films is suppressed at higher P_{O_2} . The paraelectricity/ferroelectricity transition and dielectric constant are associated with the preferred orientation, tetragonality (c/a) and oxygen concentration. Films deposited at higher P_{O_2} exhibit longer lifetime and higher breakdown field due to their smaller leakage current density. It is also seen that the leakage current density biased at +100 kV/cm decrease as a function of P_{O_2} . The leakage current analysis of Pt/PSrT/Pt capacitors reveal *SE*/*PFE* (Schottky emission/Poole-Frenkel emission) at low/high applied field, except the PSrT films deposited at P_{O_2} = 200 mTorr only indicate *SE* behavior at the applied field range. It also suggests that PSrT films deposited at lower P_{O_2} have porous surface and more OVs than those deposited at higher P_{O_2}, yielding more interfacial states and more trapping states inside films and the fatigue properties are dominated by the interfacial states. Consequently, PSrT films deposited at higher P_{O_2} show improved interfaces and fewer OVs, yielding fewer interfacial states and fewer deep trapping states inside films and the fatigue properties are dominated by deep trapping states.

Chapter 6 Temperature-Dependent Properties of Pulse-Laser-Deposited $(Pb,Sr)TiO_3$ Films at Low Temperatures

6-1 Brief Concept of Temperature Coefficient of Resistance

Ferroelectric semiconducting materials, with perovskite structure, have received much attention lately for their properties in temperature coefficient of resistance (TCR) [49-55, 93, 94]. Of these materials, $(Pb,Sr)TiO_3$ (PSrT) have aroused considerable interest in the composite effect of negative and positive TCR (NTCR and PTCR), firstly found in 1988 [49]. In addition, PSrT has the relatively low sintering temperature compared to the conventional barium titanate [52]. In the past studies [49, 50, 52-55], PSrT ceramics are found to exhibit a NTCR behavior below Curie temperature (T_c) and the PTCR effect above T_c. Moreover, PSrT solid-solution is constituted by $SrTiO_3$ (STO) and $PbTiO_3$ (PTO) and its T_c can be linearly adjusted from -220 ^oC to 490 ^oC by varying the lead (Pb) content [41, 42]. The substitution of Pb by strontium (Sr) in the PTO film will decrease the crystallization temperature and offers a good control of dielectric properties at room temperature [47, 48]. The TCR effect of PSrT bulk prepared by conventional ceramic solid state sintering processes has been reported [50, 52-55]. However, the TCR properties of PSrT thin films lack for systematically studies, which can be used as thermistor sensor embedded into micro-electro-mechanical systems (MEMS). As a consequence, the subject needs further investigations on the film properties.

Mostly, ferroelectric thin films require low-temperature processes for IC and MEMS applications to prevent the formerly-fabricated structure from thermal

damage. Nevertheless, depositions of ferroelectric lead-titanate films, such as PTO and $Pb(Zr,Ti)O_3$ (PZT), are usually conducted at high-temperatures (> 600 °C) to obtain the good crystallinity of a perovskite structure [61]. The high-temperature (> 450 °C) process will result in the volatilization of lead oxide (Pb-O compounds) in lead-titanate-based thin films [4, 62], which in turn degrades the microstructure and affects the film composition. Thus, a relatively low-temperature process (≤ 450 °C) is certainly required for the deposition of PSrT thin films.

To deposit PSrT films, a pulsed-laser deposition (PLD) technique is conducted because of its simplicity, versatility, and capability of growing a wide variety of stoichiometric oxide films without subsequent high-temperature annealing [31]. PLD process consists of three steps [31]: (i) vaporization of a target material by laser beam, (ii) transport and interaction of a vapor plume with a background ambient, and (iii) condensation of the ablated material onto a substrate where a thin film nucleates and grows. Therefore, the structural and the electrical characteristics of PLD ferroelectric films are strongly affected by the processing parameters, such as deposition temperature, laser energy fluence, and oxygen ambience. In this chapter, the temperature dependent properties of PLD PSrT films deposited at low-temperatures (≤ 450 °C) will be addressed.

6-2 Experiments

The platinum (Pt) film, 100 nm-thick, was sputtered onto SiO_2/p-type Si as the bottom electrode and followed by annealing at 450 °C for 30 min in N_2 ambient. Thin PSrT films (200 nm thick) were then deposited on the $Pt/SiO_2/Si$ substrate by PLD technique. A set of optical lens was used to focus the laser beam over the $(Pb_{0.6}Sr_{0.4})TiO_3$ target. The vacuum chamber was pumped down to a base pressure of

0.1 mTorr and then refilled with O_2 as working gas. The vaporized species of the target transferred and deposited on the substrate heated by a thermal heater. The target to substrate distance was 4 cm. The deposition temperature (substrate temperature, T_s), which was calibrated at the wafer upper surface, varied from 300 °C to 450 °C. During the PLD process, the oxygen partial pressure was kept at 80 mTorr. The laser pulsed rate and average laser power density (laser energy fluence) were 5 Hz, and 1.55 J/cm^2 per pulse, respectively.

An automatic measurement system that combines IBM PC/AT, semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station with embedded heater was used to measure the current-voltage (I-V) characteristics as a function of measurement temperature (T_m) ranging from 30 to 390 °C. The TCR values were evaluated from the temperature dependent leakage current data.

6-3 Temperature Dependent Properties of Pt/(Pb,Sr)TiO3/Pt Capacitors

Low-temperature PLD PSrT films, deposited from 300 to 450 °C, have been demonstrated in ***Chapter 4*** with the dense and crack-free surface morphologies, evident crystallinity, and excellent ferroelectric properties. Here, Table 6-1 summarizes the texture characteristics and electric properties of PLD PSrT films deposited at various substrate temperatures (T_s) on Pt/SiO_2/Si (100) wafers. The growth of PSrT films is strongly influenced by the deposition temperatures (T_s). A mono phase of $(Pb_{1-x}Sr_x)TiO_3$ perovskite structure is exhibited for PLD PSrT films prepared at low substrate temperatures (≤ 450 °C). The intensities of the (100) and (110) orientations significantly vary with T_s. Thus, the X_{100} relative proportion, addressed as $I_{100}/(I_{100}+I_{110})$, are 31.4%, 65.4%, 55.8% and 49.3% at T_s = 300, 350, 400, and 400 °C, respectively. Since the polarization of the lead-titanate-based crystal

is maximal in the [100] direction, the polarization of the film with stronger (110) orientation is weaker than that with stronger (100) orientation [4, 5]. Hence, it suggests that the better ferroelectricity and larger dielectric constant can be obtained for films prepared at T_s = 350 – 400 °C due to the strong (100) preferred orientation.

Table 6-1 Summarized texture characteristics and electric properties of PLD PSrT films deposited at various substrate temperatures (T_s) on Pt/SiO_2/Si (100) wafers.

Substrate Temperature (T_s, °C)	300	350	400	450
X_{100} Relative Proportion (%) [a]	31.4	65.4	55.8	49.3
Saturation Polariztion ($2P_s$, μC/cm^2) [b]	18.90	30.71	29.08	20.72
Remanent Polarization ($2P_r$, μC/cm^2) [b]	4.89	6.29	6.65	5.24
Coercive Field ($2E_c$, kV/cm) [b]	103.13	84.91	90	119.76
Dielectric Constant [c]	357.8	616.5	536	411

[a] Evaluated from X-ray diffraction spectra.
[b] Evaluated from P-E curves.
[c] Evaluated from C-E curves at zero-field.

Figure 6-1 reveals that the temperature dependence of current density (J) versus the applied field for films deposited at various T_s. The current density increases as the temperature of measurement (T_m) and electric field increase. It is seen that the variation of J-T_m curves biased at +50 kV/cm is around 6 orders of magnitude (i.e. from 0.02 μA/cm^2 at T_m = 30 °C to 0.08 A/cm^2 at T_m = 390 °C for 450 °C-deposited film), which is larger than that of approximate 4 orders of magnitude at +150 kV/cm (i.e. from 2.12 μA/cm^2 at T_m = 30 °C to 0.18 A/cm^2 at T_m = 390 °C for 450 °C-deposited film), indicating that J is more sensitive to T_m when films are biased at low field. In addition, the substrate temperature (T_s) affects the film resistance while

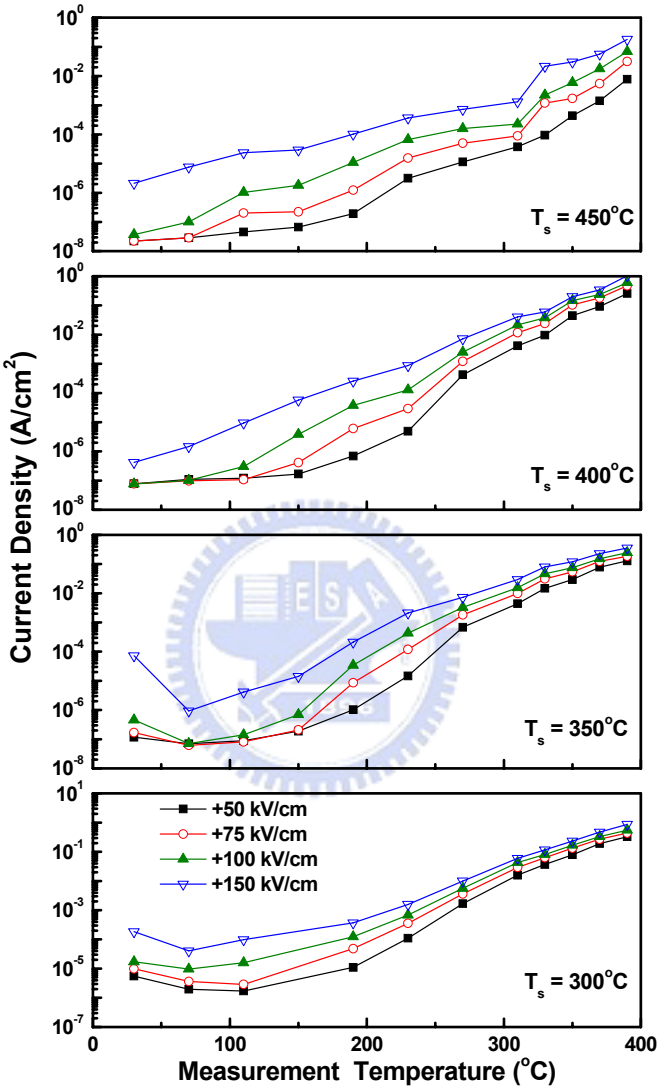


Figure 6-1 Current density versus measurement temperature characteristics of Pt/PSrT/Pt capacitors prepared at various temperatures (T_s) as a function of biased field.

the J-T_m curves biased at different fields vary as T_s increases. Figures 6-2 show the effects of temperature (T_m) and biased field on the current density, dc resistance (R) and temperature coefficient of resistance (TCR) for Pt/PSrT/Pt capacitors prepared at 300 °C. The leakage current density increases with the increase of temperature (T_m) and biased fields (Fig. 6-2(a)), while the resistance also decreases with the increase of applied bias field (Fig. 6-2(b)), where the symbols at each applied field are extracted from J-E curves and the lines represent fitted results. The values of R increase slightly with increasing T_m from room temperature to ~ 100 °C (i.e. a positive TCR, PTCR) and then decrease with T_m (i.e. a negative TCR, NTCR), as exhibited in Fig. 5(c). The TCR, described as following equation [93]

$$TCR = \frac{1}{R}\left(\frac{dR}{dT_m}\right), \qquad (6\text{-}1)$$

exhibits a minimum at T_m ~ 250 °C except for that at +25 kV/cm, possibly due to the unstable J-E measurement biased at such ultra-low electrical field. Thus, the J-E data at +50 and +150 kV/cm were selected to analyze the effect of deposition temperature (T_s) on the temperature dependence of R and the TCR properties (Fig. 6-3). It is observed that the variation of temperature-dependent resistance is very small at T_m = 30 – 150 °C (i.e. 0.36 – 2.31 and 0.08 – 1.3 times of magnitude for films biased at +50 kV/cm and +150 kV/cm, correspondingly). In general, the junction temperature of IC is designed not higher than 125 °C. It means that the ferroelectricity of PSrT films will be stable for memory application during the operation temperature of IC. Films deposited at lower temperatures (T_s) have smaller insulation resistances, larger TCR and more sensitive to temperature change. The bias field effects the temperature dependence of film resistance, especially at higher temperatures (T_m > 100 °C). As

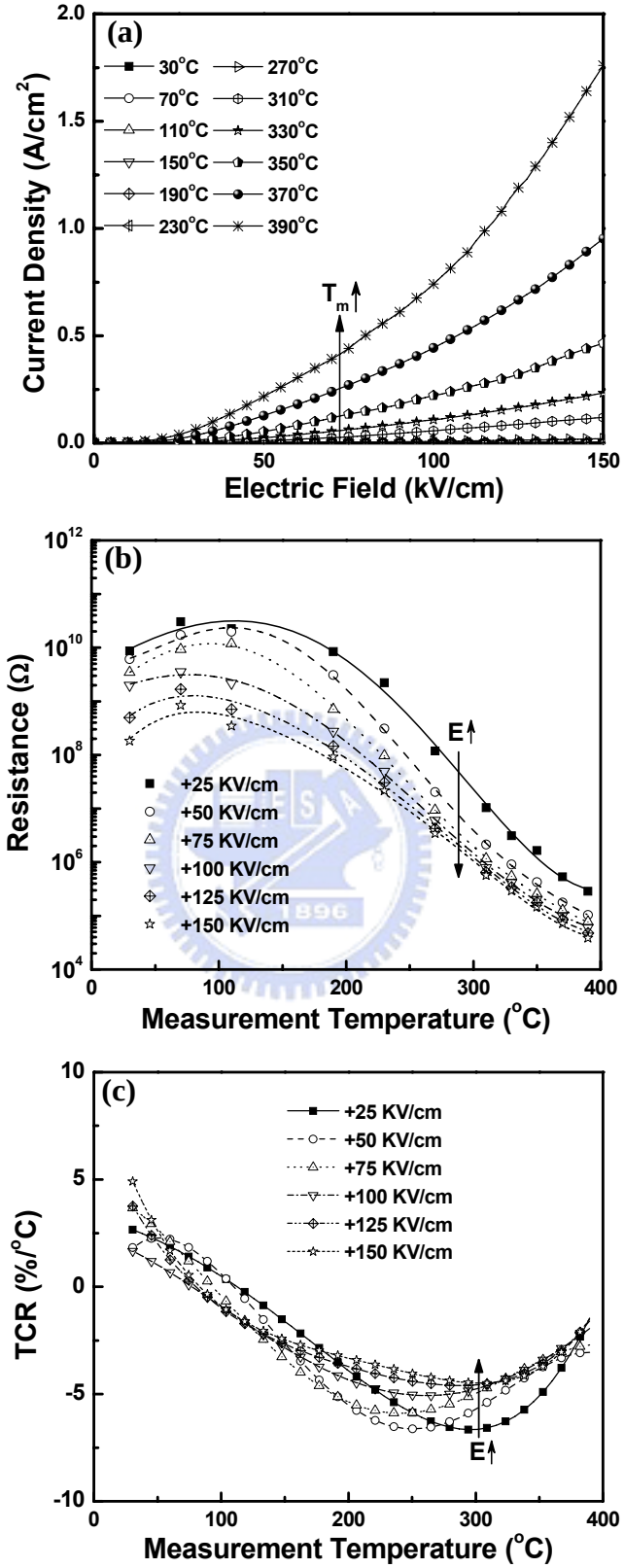


Figure 6-2 (a) Current density versus electric field curves, (b) resistance-temperature curves, and (c) TCR plots of Pt/PSrT/Pt capacitors prepared at 300 °C.

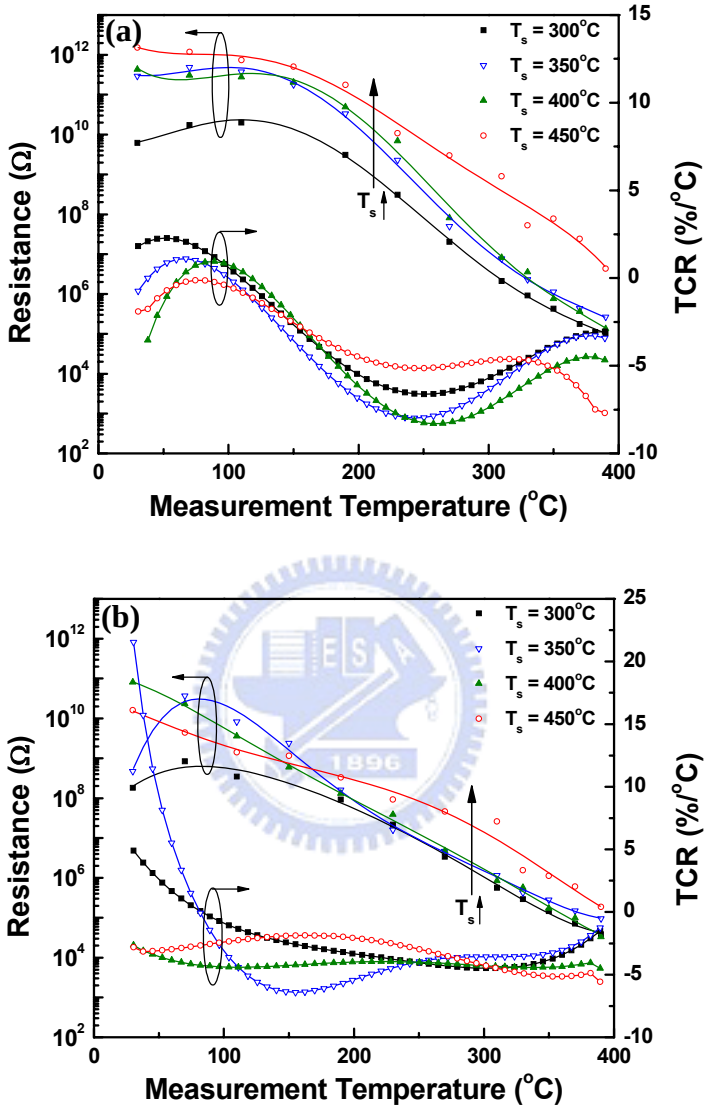


Figure 6-3 Resistance-temperature curves and TCR plots of Pt/PSrT/Pt capacitors prepared at various temperatures (T_s) biased at (a) +50 kV/cm and (b) +150 kV/cm.

seen in Fig. 6-3, the TCRs of films biased at +50 kV/cm are larger than those at +150 kV/cm, and this is important for PSrT films utilized for thermistor component in MEMS application. The PLD PSrT films exhibit apparent NTCR behavior which is different from the bulk PSrT ceramics where a NTCR-PTCR transition is observed in the temperature range of 100 – 390 °C [50, 52-55]. It is possible that the PTCR effect of PLD PSrT films appear only at temperatures above 390 °C, as reported by Chou *et al.* in their work on PSrT bulk ceramics [50]. The evolution of temperature-resistance of PSrT films, which can estimate the Curie temperature (T_c) of PSrT by electrical measurement, has been reported by Lu, and Tseng [54], and Zhao *et al* [53]. Thus, it implies that the T_c of PSrT films is higher than 390 °C and no phase transition of ferroelectric-paraelectric would occur at temperatures below 390 °C. In this study, due to the hardware limit, the maximum of measurement temperature (T_m) is 390 °C, hence, no ferroelectric-paraelectric transition is observed. Thus, without the phase transition, the effects of deposition temperature (T_s) on resistance and TCR are attributed to films' physical characteristics, originating from the changes of crystallinity, microstructure and composition (i.e. preferred orientations, grain boundaries and oxygen vacancies).

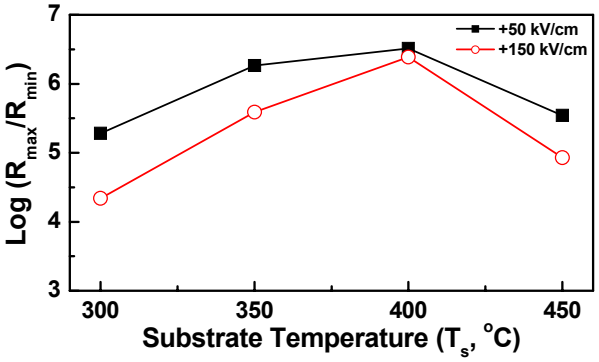


Figure 6-4 Log resistance ratio, log (Rmax/Rmin), of PSrT films deposited at various substrate temperatures (T_s), where R_{max} and R_{min} are the maximum and minimum of film resistance measured from 30 to 390 °C.

Figure 6-4 shows resistance ratio, (R_{max}/R_{min}), as a function of T_s, where R_{max} and R_{min} are the maximum and minimum of film resistance, respectively, measured from 30 to 390 °C as given in Fig. 6-3. Larger (R_{max}/R_{min}) are obtained when films biased at +50 kV/cm than those at +150 kV/cm, which is consistent with what is observed in Fig. 6-1. Besides, films deposited at 400 °C show the maximal (R_{max}/R_{min}) value. Table 6-2 summarizes the Curie temperature, resistance ratio, and TCR of PLD PSrT films in this study and the PSrT bulk ceramics reported in literatures. It is noticed that the low temperature prepared PLD PSrT films exhibit strong NTCR behavior with the larger values of (R_{max}/R_{min}) than the PSrT ceramics do [50, 52-55]. This suggests that film-type PSrT is a better candidate for the applications of thermistor sensor due to its large resistance range in the temperature range of interest (30 – 390 °C).

6-4 Summary

Low-temperature PLD PSrT films, deposited at temperatures ranging from 300 to 450 °C, exhibit the perovskite phases. The deposition temperature (substrate temperature, T_s) strongly affects the crystallinity, morphologies and electrical properties of PSrT films. The current density increases with temperature (T_m) and biased fields. Low-temperature PLD PSrT films exhibit high stability of leakage current and film resistance below 150 °C, which is important and well for memory application. The NTCR behavior is observed in the temperature range of 100 – 390 °C. Furthermore, PLD PSrT films exhibit strong NTCR behavior with a larger resistance range (log (R_{max}/R_{min}) values of 4.3 – 6.5) than the PSrT ceramics do. In addition, T_s affects both the leakage current density and the temperature dependence of leakage current density of the films. The larger resistance range of the PLD PSrT films renders them a better candidate for the application of thermistor sensor.

Table 6-2 Curie temperature (T_c), log resistance ratio (log (R_{max}/R_{min})), and TCR of PSrT films in this thsis and PSrT bulk ceramics reported in literatures.

	This Work	Ref. 52	Ref. 53	Ref. 54	Ref. 55	Ref. 50
Composition	PSrT	PSrT	PSrT	Y-doped PSrT	Y-SiO_2-doped PSrT	Y-SiO_2-doped PSrT
Film/Ceramic Bulk	Film	Ceramic Bulk	Ceramic Bulk	Ceramic Bulk	Ceramic Bulk	Ceramic Bulk
Preparation Method	PLD	CS **	CS **	CS **	CS **	CS or MS **
Electrode Material	Pt	In-Ga Alloy	In-Ga Alloy	In-Ga Alloy	NA *	In-Ga Alloy
Process Temperature (°C)	300 - 450	1100	950	1250	1080 - 1180	1150 or 1220
Measurment Temperature (T_m, °C)	30 - 390	RT - 400	RT - 400	RT - 500	RT - 450	RT - 700
Curie Temperature (T_c, °C)	NA *	150 - 200	123 - 212	140 - 280	165	CS: 210 MS: 390 **
NTCR/PTCR effect	Strong NTCR	NTCR - PTCR Composite	NTCR - PTCR Composite	NTCR - PTCR Composite	NTCR - PTCR Composite	NTCR - PTCR Composite
log (R_{max}/R_{min})	NTCR: 4.34 - 6.51	NTCR: 0.45 - 1.38 PTCR: 4.85 - 5.25	NTCR: 0.11 - 1.86 PTCR: 3.23 - 4.5	NTCR: 0.7 - 1.5 PTCR: 3.6 - 5	NTCR: 2.7 PTCR: 4.7	NTCR: 1 PTCR: 2.5
TCR (%/°C)	-8.3 - +21.5	NA *	NA *	NA *	-3.54 - +6.61	NA *

* NA: Not Available

** CS: Coventionally Sintered , MS: Microwave Sintered

Chapter 7 Characteristics of Low-temperature Pulse-Laser-Deposited $(Pb,Sr)TiO_3$ Films in Metal/Ferroelectric/Silicon Structure

7-1 Brief Concept of Metal/Ferroelectric/Silicon (MFS) Structure

Ferroelectric based gate insulator field-effect transistors (FETs) have been investigated as future nondestructive read-out (NDRO) nonvolatile memory devices [19, 20, 95-100]. Among several kinds of ferroelectric gate FET structures, a metal/ferroelectric/semiconductor (MFS) configuration is particularly promising due to the advantages of simple fabrication processes, low power consumption (without the voltage drop across the buffer insulator) and small memory cell size compared to its alternatives. MFS-FET exploits the ferroelectric field effect, which is the modulation of conductivity by the electrostatic charges induced by ferroelectric polarization, and thus requires the direct deposition of ferroelectric thin films on silicon (Si) wafer. Thin films of various ferroelectric materials, such as $Pb(Zr,Ti)O_3$ (PZT), $YMnO_3$ (YMO), $SrBi_2Ta_2O_9$ (SBT), $Bi_4Ti_3O_{12}$ (BIT), and $CaBi_2Nb_2O_9$ (CBN) have been investigated for MFS-FET devices [19, 20, 96-100]. These materials are usually processed at high-temperatures (> 600 ^oC) to obtain the good crystallinity of a perovskite structure [19, 20, 96-99]. However, the high-temperature process will cause the diffusion of constituent elements and/or the chemical reactions between ferroelectric film and underlying silicon [4, 101, 102], which produce undesirably high density of interfacial trap states [19, 20, 97-100]. In addition, the volatilization of Pb-O in lead-titanate-based films and the loss of Bi content in bismuth-tatanate-based films, processing at high temperatures, always degrade the microstructure and

reliability of ferroelectric devices [4, 62, 103]. Hence, a relatively low-temperature process is indeed required for the deposition of ferroelectric thin films for MFS-FET applications.

(Pb,Sr)TiO_3 (PSrT) is feasible for memory applications due to its large electric-field-dependent dielectric constant and composition-dependent Curie temperature [47, 48, 84]. The (Pb,Sr)TiO_3 (PSrT) solid-solution film is constituted by $PbTiO_3$ and $SrTiO_3$. The effect of lead (Pb) substituted by strontium (Sr) in the $PbTiO_3$ film will decrease the crystallization temperature and offers a good control of dielectric properties at room temperature [47, 84]. To deposit PSrT films, a pulsed-laser deposition (PLD) technique is applied, which is feasible for fabricating films with complex compounds and capable of growing a wide variety of stoichiometric oxide films without subsequent high-temperature annealing. Hence, PLD is a potential technique, which could be integrated into low-temperature semiconductor processing. To date, much less is known about the properties of PLD PSrT films deposited on Si substrate. In this chapter, the low-temperature PLD process can avoid these problems as stated and make several improvements of film properties. Thus, a high-quality MFS structure without the buffer layer between PSrT films and Si substrate has been developed.

7-2 Experiments

Si (100) has the lowest surface state density, which is superior to Si (110) and Si (111). In order to reduce the effect of surface states, (100) orientation p-type Si wafers were employed as the substrates in this study. After initial RCA cleaning process, thin PSrT films (200 nm thick) were then deposited on p-type Si substrates by a PLD system (LPX 210i, Lambda Physik) utilizing KrF excimer laser (λ=248 nm) radiation.

A set of optical lens was used to focus the laser beam over the $(Pb_{0.6}Sr_{0.4})TiO_3$ target in vacuum. The vacuum chamber was pumped down to a base pressure of 0.1 mTorr and then refilled O_2 as reactive gas. The vaporized species of the target were transferred and deposited on the substrate heated by a thermal heater. The deposition temperature (substrate temperature, T_s) was used as a variable from 300 ^oC to 450 ^oC, calibrated at the wafer upper surface. The target to substrate distance was 4 cm. During the PLD process, the oxygen ambient pressure was 80 mTorr. The laser pulsed rate and the average energy fluence were 5 Hz and 1.55 J/cm^2 per pulse, respectively.

An Auger electron spectroscope (AES) (Auger 670 PHI Xi, Physical Electronics) was used to analyze the element depth profile of PSrT films. The crystallinity of films was analyzed by X-ray diffractometer (D5000, Siemens). The optical properties of refraction index (n) and extinction coefficient (κ) were investigated by an $n\&\kappa$ analyzer (1280, $n\&\kappa$ Technology). The n and κ are influenced by the electronic structure and/or crystallinity of the film. After the physical examination, patterned platinum (Pt) top electrodes, with a thickness of 100 nm and a diameter of 75 μm, were deposited by sputtering process to form a Pt/PSrT/Si (MFS) capacitor structure. The thickness of PSrT films was controlled as ~ 200 nm to deduct the influence of film thickness on electrical properties. The noble metal platinum, with low resistivity, is considered as the electrode of Pt/PSrT/Si capacitor because of its small leakage current, low power consumption, small RC delay, and good thermal stability to lead-based perovskite materials [4]. Then, the native oxide on the backside of Si wafer was removed by HF etching. An aluminum (Al) film (500 nm thick) was sequentially deposited on wafer backside to form Si/Al bottom electrode. The combination of a semiconductor parameter analyzer (4156C, Agilent Technologies) and a probe station was used to measure the leakage current (I-V characteristics). A

capacitance-voltage (C-V) analyzer (Package 82 system C-V 590, Keithley) was also used to measure C-V curves at 100 kHz. A pulse generator (8110A, Hewlett Packard) and a pulse/function generator (8116A, Hewlett Packard) were connected together with low noise BNC cables to generate +3 V/-3 V bipolar wave pulsed at 1 MHz, confirmed by an oscilloscope (54645A, Hewlett Packard), as an input signal for the measurement of polarization switching degradation (fatigue).

7-3 Physical Analysis

Figure 7-1 reveals AES depth profiles of PLD PSrT films deposited on Si (100). Without standard samples to calibrate the sensitivity factor, the count intensity of elements presented here can only be semi-quantitative, but not absolute. No evident difference is observed between the depth profiles of films deposited at 300 °C and 450 °C. As can be seen from the abrupt interface profile, no significant inter-diffusion of oxygen, titanium, and silicon between PSrT films and Si substrate occurs at such low temperatures.

Figure 7-2(a) presents the X-ray diffraction pattern of PSrT films deposited at various T_s. All the diffraction peaks of these data are indexed as (100), (110), (111), (200), (210) and (211) planes of $(Pb_{1-x}Sr_x)TiO_3$ perovskite phases [47, 48, 56, 84]. The crystalline PSrT films appear at such low temperatures because (i) the addition of strontium makes the crystallization temperature of PSrT lower than that of PZT [47], and (ii) the PLD technique could preserve the crystalline phases and stoichiometric composition of the target material at low T_s [31, 84]. Moreover, the intensities of the (100), (111), (200), (210) and (211) orientations increase significantly with the increasing T_s. Figure 7-2(b) quantizes the XRD spectral analysis using *Eq. (4-1)*. X_{100}, the relative proportion of the (100) orientation, increases as T_s increases and shows

the maximum at T_s = 450 °C, indicative of strong (100) preferred orientation. It infers that the intensity of (100)-oriented peak of PSrT films is strongly enhanced by the using of Si (100) substrate as opposed to that on Pt/SiO_2/Si (Fig. 4-4).

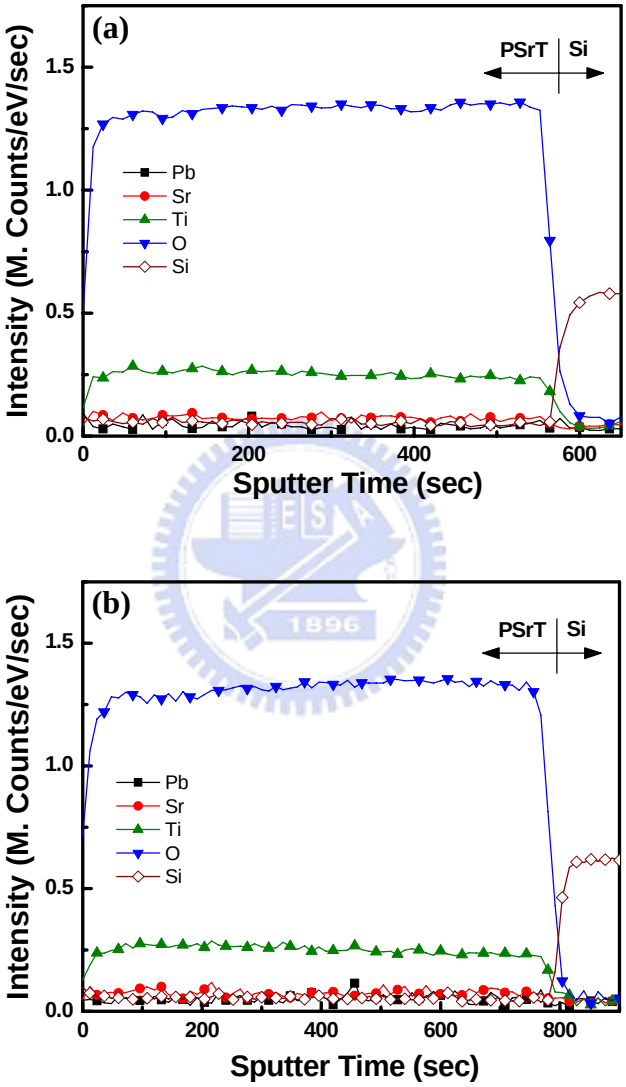


Figure 7-1 AES depth profiles of PLD PSrT films deposited on Si (100) wafers at (a) 300 °C and (b) 450 °C.

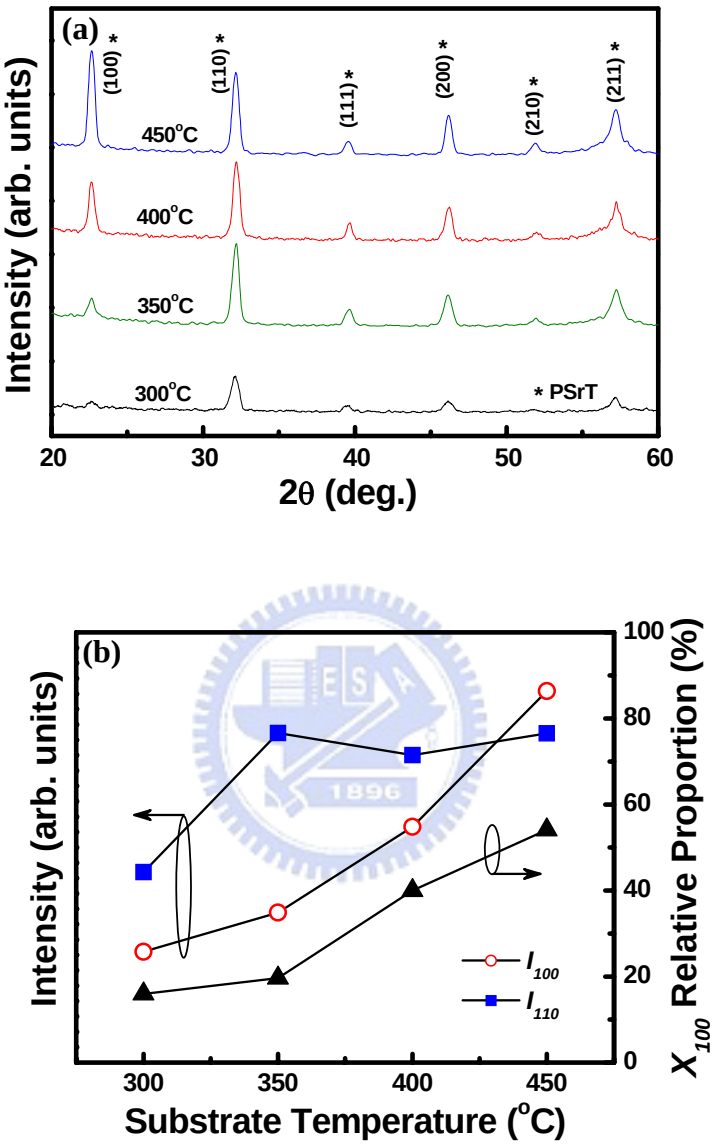


Figure 7-2 (a) X-ray diffraction pattern and (b) texture characteristics of PLD PSrT films deposited on Si at various substrate temperatures.

7-4 Electrical Analysis

The Pt/PSrT/Si capacitor with aluminum backside electrode is used as MFS configuration for electrical measurements. These MFS devices require the ferroelectric film to be deposited on silicon surface directly, and utilize their remnant polarization to control the surface potential of silicon. Thus the interfacial states and the leakage current are very important for normal FET operations. Figure 7-3 displays the curves of current density versus electric field (J-E) and an extraction of slope, α, in different regions of log (J)-log (E) plots, which gives an idea of the conduction process involved under the influence of varying electrical fields. Initially, the leakage current shows an ohmic behavior at low fields ($\alpha \leq 1$). At slightly higher electrical fields ($\alpha \sim 6$ - 8.8), it shows an onset of the linear region, attributed to the space charge limited conduction (SCLC) mechanism [19, 20]. The inhibited leakage current observed in PSrT films deposited at 300 - 400 °C is correlated with the fewer structural defects because of the enhanced crystallinity as shown in Fig. 7-2. Comparing the data at T_s = 400 °C and T_s = 450 °C, the increasing current density may correspond to the more chemical defects due to the more serious volatilization of Pb-O of PSrT films at higher temperature (≥ 450 °C) [4, 62].

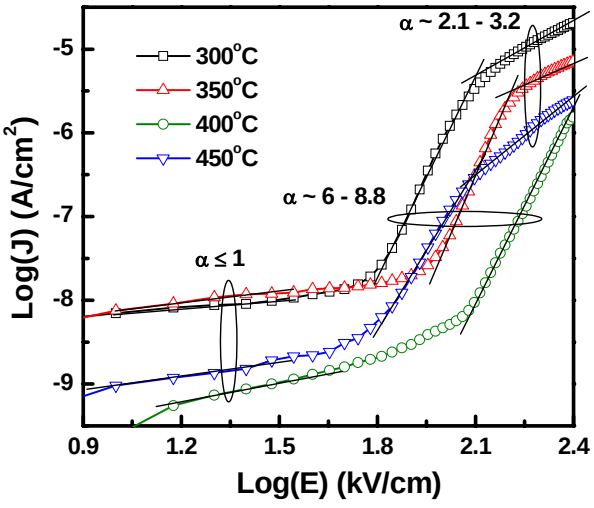


Figure 7-3 Current density versus electric field (log (J)-log (E)) curves of Pt/PSrT/Si capacitors prepared at various substrate temperatures. The corresponding slopes in different regions are denoted as α.

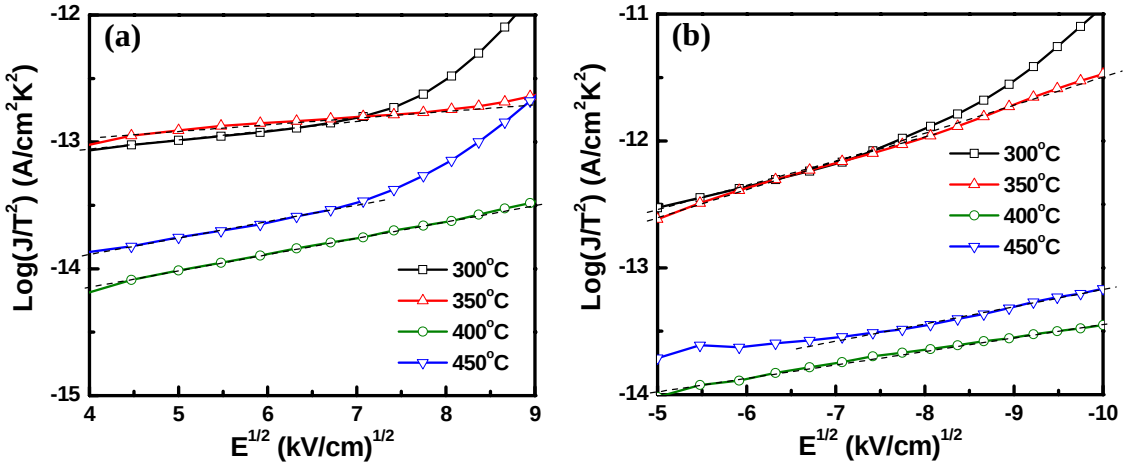


Figure 7-4 Experimental and fitted log (J/T^2) versus $E^{1/2}$ (Schottky emission) plots of Pt/PSrT/Si capacitors at (a) positive bias and (b) negative bias.

Figures 7-4 reveal the experimental and fitted log (J/T^2) versus $E^{1/2}$ (Schottky emission) plots of Pt/PSrT/Si capacitors applied at positive/negative bias. If the leakage current follows Schottky emission behavior, a log (J/T^2) against $E^{1/2}$ plot should be linear and the dashed lines work as the fitted results. It is noted that Figs. 7-4(a) and 7-4(b) reveal a similar tendency. The decreasing values of log (J/T^2) against $E^{1/2}$ present the inhibited interfacial trap states as T_s increases from 300 to 400 °C. As T_s increases to 450 °C, however, the increasing values of log (J/T^2) against $E^{1/2}$ indicate more trap states at both electrode interfaces. A strong polarity dependence of the leakage current is noted due to the different materials used for the top (Pt) and bottom (Si) electrodes as shown in Figs. 7-4(a) and 7-4(b) [100]. The polarity dependence is connected with the different Schottky barrier height (φ_{b1} and φ_{b2}) at the Pt/PSrT and PSrT/Si interfaces, expressed as the following relations [77, 104]

$$\varphi_{b1} = \varphi_m - q\chi_f, \qquad (7\text{-}1)$$

$$\varphi_{b2} = \varphi_{Si} - q\chi_f = \chi_{Si} + \frac{1}{2}E_{Sig} + kTln(N_a/n_i) - q\chi_f, \quad (7\text{-}2)$$

where φ_m is the work function of Pt electrode (φ_m = 5.3 eV), χ_f is the electron affinity of PSrT films, φ_{Si} is the work function of Si substrate, χ_{Si} is the electron affinity of Si (χ_{Si} = 4.05 eV), q is the unit charge, E_{Sig} is the energy gap of Si (E_{Sig} = 1.12 eV), k is the Boltzmann's constant, T is the absolute temperature, n_i is the intrinsic carrier concentration of Si, and the doping concentration (N_a) is about 2×10^{15} cm^{-3}, according to the p-type Si resistivity of 5-10 Ωcm [77, 104, 105]. The values of the electron affinity of PZT, BST, and $SrTiO_3$ are reported as χ_{PZT} = 3.5 eV, χ_{BST} = 4.0 eV, and χ_{STO} = 4.1 eV, accordingly [105, 106]. Thus, the electron affinity of PSrT, χ_f, may be roughly assumed as 3.8 eV. Hence, the Schottky barrier heights could be calculated as φ_{b1} = 1.3 eV and φ_{b2} = 0.8 eV. In addition, the more interfacial trap states result in more charge accumulation and a severe image-force effect at the edge of electrodes, leading to the decrease of Schottky barrier height. The image-force lowering ($\Delta\varphi$) can be expressed as [2, 76]

$$\Delta\varphi = (N_c qE / 4\pi\varepsilon_r\varepsilon_0)^{1/2}, \quad (7\text{-}3)$$

where N_c is the charge amount, ε_0 is the vacuum permittivity, and ε_r is the relative dielectric constant of the ferroelectric material. Figure 7-5 illustrates the schematic drawing of the electron energy band for Pt/PSrT/Si. In general, the electron energy band at the interfaces of electrodes reveal that PSrT films act as n-type semiconductors due to the generation of oxygen vacancies in ABO_3 perovskites [2, 18, 76]. The band gap of PSrT films, E_{fg}, is measured as 3.52 ~ 3.66 eV by optical

investigation of refraction index (n) and extinction coefficient (κ). The values of E_{fg} are approximately close to the reported value of 3.6 eV for $PbTiO_3$ [21].

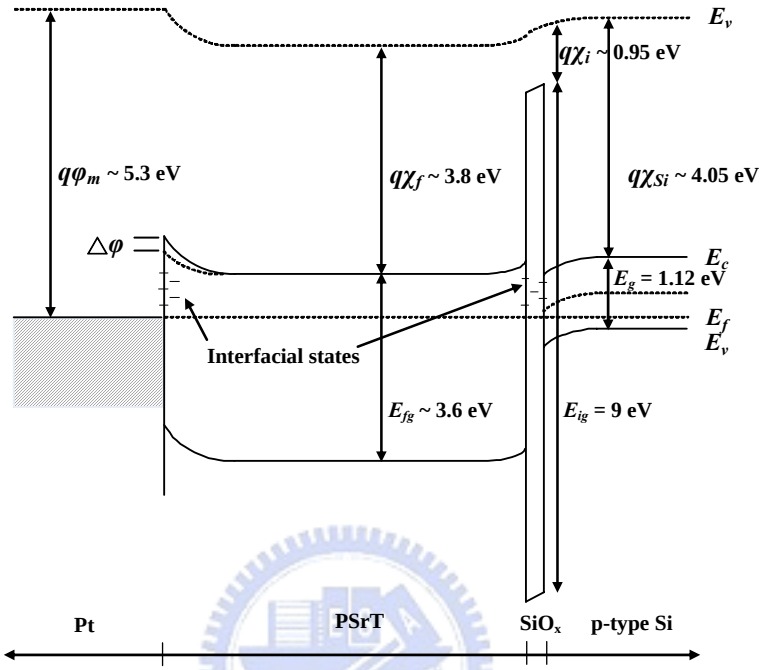


Figure 7-5 Schematic drawing of the electron energy band for the Pt/PSrT/Si structure.

Figure 7-6 displays the hysteresis loops of dielectric constant versus electric field (ε_r-E) for the Pt/PSrT/Si capacitors deposited at various T_s, sweeping at 0.05 V/100 ms from a negative bias to a positive bias and reversing it again. The dielectric constant of hysteresis loops presents the series properties of the capacitor of the Si depletion region and the capacitor of ferroelectric films (C_{PSrT}). The C_{PSrT} can be calculated from maximum dielectric constant of ε_r-E hysteresis loops, expressed as:

$$C_{PSrT} = \varepsilon_{r,max} \times \varepsilon_0 \times A/d \,, \qquad (7\text{-}4)$$

where A is the capacitor area (Pt electrode area), d is the thickness of ferroelectric film,

$\varepsilon_{r,max}$ is the maximum dielectric constant. It is seen that the C_{PSrT} and the width of hysteresis loops increase as T_s increases, which could be ascribed to the enhanced crystallinity of the film (Fig. 7-2) m. In addition, films deposited at higher T_s (≥ 350 °C) show the clockwise hysteresis loops, whereas those deposited at 300 °C reveal the counterclockwise loop. The clockwise hysteresis means that ferroelectric dipole switching governs the surface potential of p-type Si, which is the desired switching mode for the operation in MFS-FET devices [19, 100, 107]. In contrast, the counterclockwise loop could be attributed to the numerous border trap states induced by the poor-quality interfacial native oxide (SiO_x) between ferroelectric film and Si, since SiO_x can be found anywhere in the MFS capacitors [19, 97, 98, 107]. Moreover, 300 °C-deposited films indicates a positive voltage shift of C-E loops compared to those deposited at higher T_s (≥ 350 °C). The negative charge causes the shift toward positive voltage and dominates the electrical properties of the PSrT/Si interface.

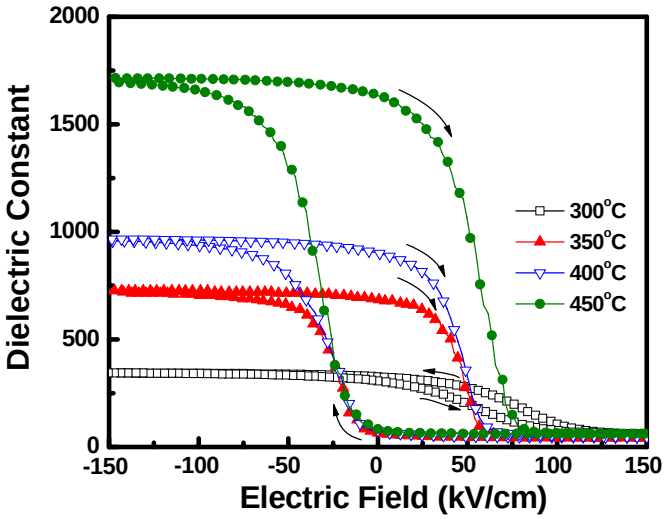


Figure 7-6 Hysteresis loops of dielectric constant-electric field (ε_r-E) for the Pt/PSrT/Si capacitors prepared at various substrate temperatures.

Furthermore, the fixed charge density (N_{fc}) could be estimated from the C-E loops by the following formula [19, 20]:

$$N_{fc} = C_{PSrT}(V_{fb} - \varphi_{ms})/(qA), \quad (7\text{-}5)$$

where V_{fb} is the flatband voltage, φ_{ms} is the effect function remainder between metal (Pt) electrode and semiconductor (Si) substrate, and A is the Pt electrode area. Figure 7-7(a) points out the minimum N_{fc} of ~ 2.85×10^{12} cm^{-2} for films deposited at 400 °C. It is found that the trend of N_{fc} is consistent with that of the leakage current density biased at +150 kV/cm (evaluated from Fig. 7-3), where the conduction is dominated by the SCLC mechanism. Figure 7-7(b) presents the memory windows (V_m), extracted from Fig. 7-6, of Pt/PSrT/Si capacitors prepared at various T_s. The value of V_m increases as T_s increases and shows the maximum of 1.785 V for 450 °C-deposited films, which is associated with the larger C_{PSrT} and the enhanced crystallinity. The V_m can be linked to twice the coercive voltage ($2V_c$) and severely narrows down by the charge injection into the border traps of SiO_x located at the PSrT/Si interface, which can be described as [97, 98]

$$V_m = 2V_c + V_{ci}, \quad (7\text{-}6)$$

where V_{ci} is the flatband voltage shift due to charge injection. Here, the values of $2V_c$ are 2.06 V, 1.7 V, 1.8 V, and 2.4 V (Fig. 4-8), respectively, which could be referred to the polarization versus electric field (P-E) curves of Pt/PSrT/Pt capacitors prepared at T_s = 300 - 450 °C. From *Eq. (7-6)*, the V_{ci} shows the minimum value of ~ -1.57 V for films deposited at 300 °C and the maximum value of ~ -0.3 V for films deposited at 350 - 400 °C. In addition, the V_{ci} slightly changes to -0.61 V as T_s increases from 400 °C to 450 °C. Consequently, the evolution of V_{ci} agrees well with the N_{fc}, the shift of C-E

loop, and leakage currents as mentioned above.

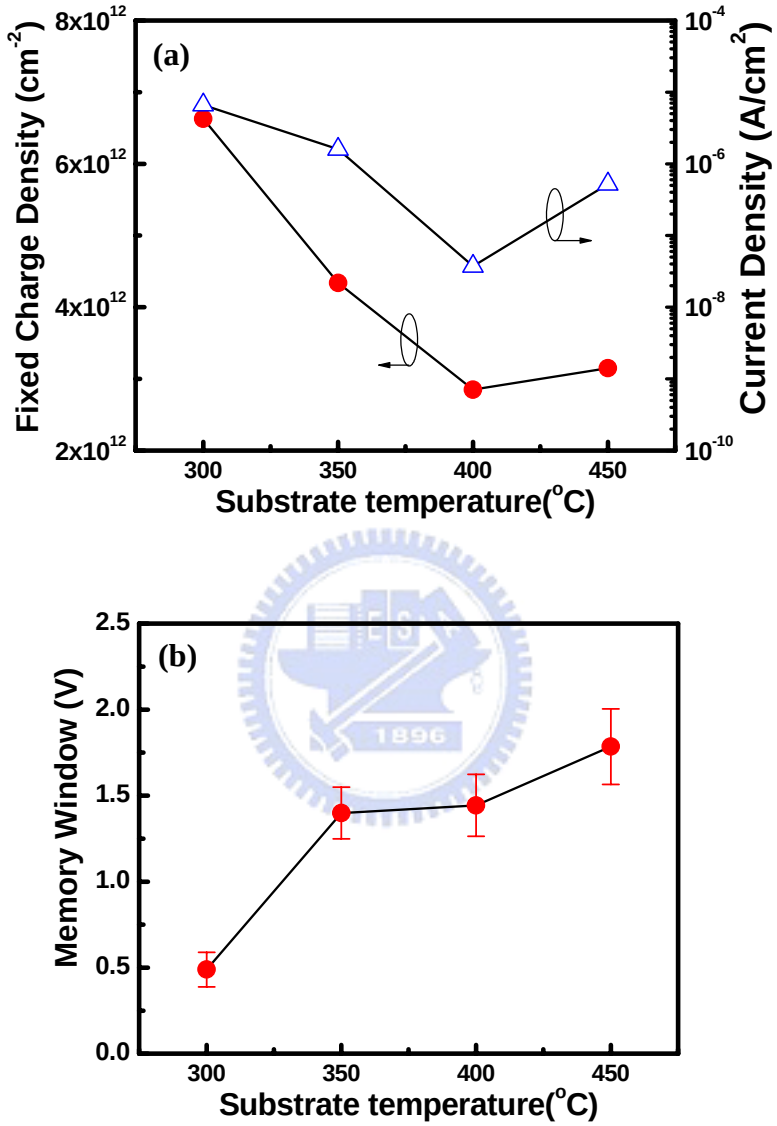


Figure 7-7 (a) Fixed charge density (N_{fc}) and leakage current density (at +150 kV/cm) as a function of substrate temperatures for Pt/PSrT/Si structures. (b) Memory window (V_m) of Pt/PSrT/Si capacitors prepared at various T_s.

7-5 *Fatigue Properties*

Figure 7-8 demonstrates the fatigue properties of ε_r-E hysteresis loops for Pt/PSrT/Si capacitors prepared at 450 °C before/after (fresh/fatigued) 10^{10} switching cycles. The variation of memory windows is less than 11% before/after the fatigued switching cycles. In summary, it suggests that PLD PSrT films deposited at suitable substrate temperatures could be promising for MFS-FET devices.

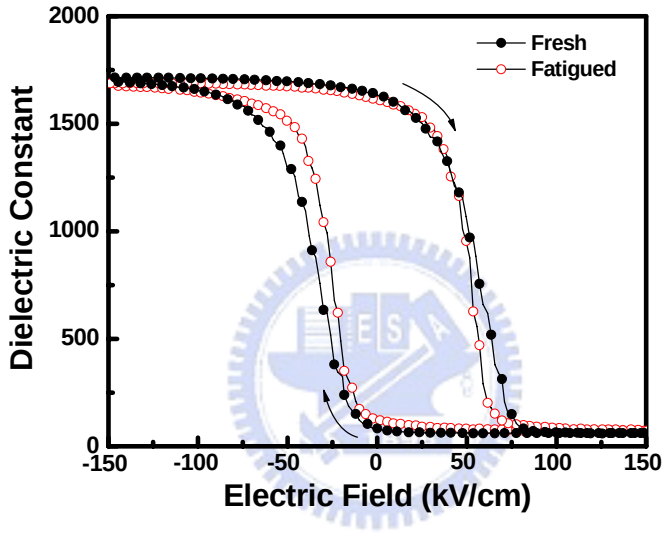


Figure 7-8 ε_r-E hysteresis loops of Pt/PSrT/Si capacitors prepared at 450 °C before/after (fresh/fatigued) 10^{10} fatigued switching cycles.

7-6 Summary

PLD PSrT films, deposited on p-type Si wafers at low substrate temperatures (T_s) from 300 to 450 °C, exhibit the perovskite phases without significant inter-diffusion at PSrT/Si interface. The T_s strongly enhances the film crystallinity and affects electrical properties of Pt/PSrT/Si capacitors. As T_s increases, films have smaller leakage current and fewer interfacial trap states at both electrode interfaces due to the fewer structural defects correlated with enhanced crystallinity. It also reveals the higher ferroelectric gate capacitance, the larger width of ε_r-E hysteresis loops, and larger memory windows (V_m) as T_s increases. In contract, films deposited at lower T_s (300 °C) exhibit the small and counterclockwise loop with the positive voltage shift, which is ascribed to the more negative charges in the trap states. However, films deposited at high T_s (450 °C) may produce serious volatilization of Pb-O compounds, incurring more chemical defects and the leakage degradation. Besides, the fixed charge density (N_{fc}) shows the minimum value of ~ 2.85×10^{12} cm^{-2} for the films deposited at 400 °C. The trend of N_{fc} is consistent with the flatband voltage shift (V_{ci}) and the leakage current density is dominated by space charge limited conduction (SCLC). Furthermore, 450 °C-deposited films disclose excellent fatigue endurance before/after 10^{10} switching cycles with less than 11% variation of V_m. As a consequence, the high-quality MFS structure without buffer layer between the PSrT films and the Si substrate could be realized by the low-temperature PLD.

Chapter 8 Summary and Conclusions

This dissertation concentrates on the studies of the novel low-temperature technologies applied on Pt/PSrT/Pt (MFM) and Pt/PSrT/Si (MFS) capacitors, used as advanced NVRAM devices. Several post-annealing techniques have been conducted to enhance material and electrical performance. The process parameters and consequent film properties are thoroughly studied to acquire the optimal conditions. Superior crystallinity and excellent electrical characteristics can be obtained, and the corresponding relationships for the materials to the electrical characteristics and concerning mechanisms are also explored in this dissertation. Several conclusions are summarized as follows.

The surface morphologies, crystallinity, microstructure and electrical characteristics of PSrT films are noticeably dependent on the annealing conditions. Films post-ELA show a denser and rougher surface morphology, larger value of O/(Pb+Sr) and the enhanced crystallinity of the upper region of films, resulting in the slight increase of dielectric constant and leakage current. As the annealing temperature increases, films indicate a surface image of distinctive grain clusters with pin holes, clear diffraction peaks of provskite structure, distinct C-E hysteresis loops and large dielectric constant, suggesting that the ferroelectricity is evidently improved by post-RTA. However, the leakage current is seriously increased due to the defects and interfacial diffusion induced by post-RTA.

Furthermore, films post-ELA and subsequent RTA at 600 ^{o}C exhibit the dense surface, specific two regions of microstructure, the largest dielectric constant of 492, and the inhibited leakage current density biased at +100-150 kV/cm. Concisely, the

superior crystallinity, improved ferroelectricity, longer lifetime and higher breakdown field of PSrT films can be achieved by the annealing technique of laser-assisted two-step process.

Low-temperature PLD PSrT films, deposited from 300 to 450 ^{o}C (T_s), have been demonstrated with dense and crack-free surface morphologies, evident crystallinity, and excellent ferroelectric properties. Among the Pt/PSrT/Pt capacitors, the 350 ^{o}C-deposited one exhibits strong (100) preferred orientation, maximum dielectric constant and good ferroelectricity. The dependence of dielectric constant on T_s is consistent with the ferroelectricity properties and preferred orientation. The leakage mechanism of Pt/PSrT/Pt capacitors reveals Schottky emission/Poole-Frenkel emission (*SE*/*PFE)* at lower/higher applied field. The high substrate temperature (T_s ≥ 350 ^{o}C) yields fewer interface states and better interfacial properties, and also shows fewer trapping states inside PSrT films, revealing that increasing T_s decreases the leakage current.

Moreover, the 400 ^{o}C-deposited PSrT films reveal minimal leakage current density biased at +170 kV/cm, nearly fatigued-free J-E characteristics after 10^{10} switching cycles, the highest breakdown field, and the best TDDB behavior, which are well explained by the defect chemistry. But the excessively high T_s (450 ^{o}C) may produce serious volatilization of Pb-O compounds, resulting in more vacancies and defects in the films, which may be the cause of degradation in crystallinity, high-field leakage currents and reliability properties.

The current density increases with temperature (T_m) and biased fields. Low-temperature PLD PSrT films exhibit high stability of leakage current and film resistance below 150 ^{o}C, which is important and well for memory application. The NTCR behavior is observed in the temperature range of 100 – 390 ^{o}C. Furthermore, PSrT films exhibit strong NTCR behavior with a larger resistance range (log

(R_{max}/R_{min}) values than the PSrT ceramics do. The larger resistance range of the PLD PSrT films infers a potential application of thermistor sensor.

The preferred orientation, microstructure, and electrical characteristics of PSrT films could be apparently affected by ambient oxygen pressures (P_{O_2}) during low-temperature PLD. The smoother surface morphology, the higher oxygen composition, and the stronger intensity of (110) orientation could be evidently influenced by increasing P_{O_2} during PLD. The paraelectricity/ferroelectricity transition and dielectric constant are associated with the preferred orientation, tetragonality (c/a) and oxygen concentration. Films deposited at higher P_{O_2} also exhibit longer lifetime and higher breakdown field due to their smaller leakage current density. The leakage current analysis of Pt/PSrT/Pt capacitors reveal *SE*/*PFE* at low/high applied field, except the PSrT films deposited at P_{O_2} = 200 mTorr only indicate *SE* behavior at the applied field range. PSrT films deposited at lower P_{O_2} have porous surface and more oxygen vacancies (OVs) than those deposited at higher P_{O_2}, yielding more interfacial states and more trapping states inside films and the fatigue properties are dominated by the interfacial states. Consequently, PSrT films deposited at higher P_{O_2} show improved interfaces and fewer OVs, yielding fewer interfacial states and fewer deep trapping states inside films and the fatigue properties are dominated by deep trapping states.

PLD PSrT films, deposited on p-type Si wafers at low T_s from 300 to 450 ^oC, exhibit the perovskite phases without significant inter-diffusion at PSrT/Si interface. The T_s strongly enhances the film crystallinity and affects electrical properties of Pt/PSrT/Si capacitors. As T_s increases, films have smaller leakage current and fewer

interfacial trap states at both electrode interfaces due to fewer structural defects correlated with enhanced crystallinity. It also reveals the higher ferroelectric gate capacitance, the larger width of ε_r-E hysteresis loops, and larger memory windows (V_m) as T_s increases. In contract, films deposited at lower T_s (300 °C) exhibit the small and counterclockwise loop with the positive voltage shift, which is ascribed to the more negative charges in the trap states. However, films deposited at high T_s (450 °C) may produce serious volatilization of Pb-O compounds, incurring more chemical defects and the leakage degradation.

Besides, the fixed charge density (N_{fc}) shows the minimum value of ~ 2.85×10^{12} cm^{-2} for the films deposited at 400 °C. The trend of N_{fc} is consistent with the flatband voltage shift and the leakage current density is dominated by space charge limited conduction (SCLC). Furthermore, 450 °C-deposited films disclose excellent fatigue endurance before/after 10^{10} switching cycles with less than 11% variation of V_m. As a consequence, the high-quality MFS structure without buffer layer between the PSrT films and the Si substrate could be realized by the low-temperature PLD.

Chapter 9 Future Prospects

PSrT capacitor will be very promising solutions for new generation NVRAM cell capacitor due to its outstanding ferroelectric properties, but the integration issues shall be the big challenges for the practical applications. Therefore, the low temperature is indeed necessary for the implementations of PSrT capacitor. Besides, PSrT film is also a superior candidate for the applications of thermistor sensor due to its strong NTCR behavior and large resistance range in the temperature range of 100 – 390 ^{o}C. Some of the innovative topics are worth to further investigate and listed below.

1. Large area ELA treatment is necessary for practically industrial applications of PSrT thin films due to high throughput and good uniformity requirements. Although scanning ELA system has been widely applied on TFT industry, it still lacks systematical system for PSrT thin film capacitor.

2. Low-temperature PSrT capacitor over a bit-line (COB) can be further integrated with CMOS circuits to recognize its data retention and real operation performance in NVRAM.

3. Low-temperature PSrT film can be further implemented in ferroelectric gate FET (1T FeRAM) to investigate the drain current of I_{on}/I_{off}, data retention and nondestructive read-out (NDRO) in NVRAM.

4. Film-type PSrT can be further studied the mechanisms of TCR and integrated with MEMS devices to recognize the application of thermistor sensor.

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論文題目：**準分子雷射低溫製備之鈦酸鍶鉛薄膜元件特性分析之研究**

Study on the Characterization of Devices with Perovskite Lead-Strontium-Titanate Thin Films Fabricated by Excimer Laser Deposition at Low-Temperatures

Publication List

A. International Journal

1. **Jyh-Liang Wang**, Yi-Sheng Lai, Sz-Chian Liou, Chen-Chia Chou, Chun-Chien Tsai, Chuan-Ping Juan, Huai-Yuan Tseng, Chueh-Kuei Jan, and Huang-Chung Cheng, "Structural and Electrical Investigations of Pulse-Laser-Deposited (Pb,Sr)TiO_3 Films at Various Oxygen Partial Pressures", **accepted** by ***J. Electrochem. Soc.***, 2007.

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4. **Jyh-Liang Wang**, Yi-Sheng Lai, Bi-Shiou Chiou, Huai-Yuan Tseng, Chun-Chien Tsai, Chuan-Ping Juan, Chueh-Kuei Jan, and Huang-Chung Cheng, "Study on Fatigue and Breakdown Properties of Pt/(Pb,Sr)TiO_3/Pt Capacitors", ***J. Phys.: Condens. Matter***, vol. **18**, pp. 10457-10467, 2006.

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2. **J. L. Wang**, and J. S. Chen, "TiB_2 as a Diffusion Barrier for Cu/<Si> Metallization", ***Mat. Res. Soc. Symp. Proc.***, vol. **563**, pp.33-38, 1999.

3. Chun-Chien Tsai, Hsu-Hsin Chen, Yao-Jen Lee, Kai-Fang Wei, **Jyh-Liang Wang**, Bo-Ting Chen, and Huang-Chung Cheng, "High-Performance Double-Gate LTPS Thin Film Transistors Fabricated by Excimer Laser Irradiation", ***2007 International Thin Film Transistors Conference (ITC'07 in conjunction with SID-Mid Europe Chapter Spring Meeting)***, Rome Italy, pp. 44-47, January 25-26, 2007.

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C. Patents

1. 鄭晃忠, **王志良**, 詹爵魁, 史德智, 郭孟維："鐵電元件之製造方法及鐵電材料之熱處理方法", 中華民國專利, 證號：I247045, 公告日期：95 年 1 月 11 日。 ("A Method for Ferroelectric Device Fabrication and Thermal Treatment of Ferroelectric Material", ROC Patent, No. I247045.)

2. 鄭晃忠, 邱碧秀, 史德智, 郭孟維, **王志良**, 陳志信："一種超低漏電流與高熱穩定性之新型鐵電薄膜電容器", 中華民國專利申請中。 ("A novel ultra-low-leakage and high thermal stable ferroelectric capacitor", ROC Patent.)