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Temperature-dependent memory characteristics of silicon–oxide–nitride–oxide–silicon thin-film-transistors

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ABSTRACT

This study investigates the temperature-dependent memory characteristics of polycrystalline silicon thin-film transistors with oxide/nitride/oxide stack gate dielectrics and N^+ poly-Si gate structures for nonvolatile memory application. As the device was programmed by Fowler–Nordheim tunneling at high temperature, some electrons captured in shallow traps could obtain enough thermal energy to de-trap to the gate, resulting in low programming efficiency. As the programming time increases, the hole injection through the blocking oxide from the gate would further lead the threshold voltage to decrease. In addition, the retention characteristic of the device programmed at higher temperature exhibits better charge storage ability. Because the electrons trapped in the shallow traps of the nitride layer can be easily de-trapped when temperature rises, the memory characteristics are mainly dominated by charges stored in the deep traps.

1. Introduction

Polysilicon thin-film transistors (poly-Si TFTs) have attracted considerable attention owing to their wide applications in active matrix liquid-crystal-displays (AMLCD) and memory devices, such as dynamic random access memories [1], static random access memories [2], and electrically erasable programmable read-only memories [3]. In particular, the application in AMLCDs is the primary trend, leading to rapid development of poly-Si TFT technology. Recently, high performance polycrystalline silicon thin-film transistors (poly-Si TFTs) have been designed as functional devices for system-on-panel display technology [4,5]. The functional devices in an LCD panel, including the timing controller and memory, have been developed to make displays more compact and reliable and to reduce their cost [6,7]. Since SOP technology is primarily used for portable electronics, low power consumption is a basic requirement to ensure a long battery life. Therefore, TFT-LCDs integrated with dynamic memory devices [7] or static memory devices [8] have been reported to reduce power consumption when the display is showing a static image. It is well known that nonvolatile memory is widely utilized for data storage in portable electronics systems due to its low power consumption and nonvolatility properties. Unlike the conventional nonvolatile floating gate memory, memory with the silicon/oxide/nitride/oxide/silicon (SONOS) structure has great potential for SOP applications because it is fully compatible with the poly-Si TFTs fabrication process [9]. A SONOS memory array using Fowler–Nordheim (FN) tunneling for program/erase (P/E) operation has been demonstrated to achieve the low power consumption requirement compared with channel hot electron injection scheme [10]. However, SONOS memory still has several performance challenges such as insufficient program/erase (P/E) efficiency and an undesirable gate injection phenomenon [11]. Additionally, in most nonvolatile memory works, the program/erase characteristics are usually investigated at room-temperature [12,13]. However, direct experimental observations of temperature-dependent P/E characteristics are very rare.

This work studies the poly-Si TFT combined with nonvolatile SONOS memory, named as SONOS-TFT. The gate injection phenomenon, the temperature-dependent program/erase and the retention characteristics are discussed.

2. Experiment

In this study, the SONOS-TFT with a gate length of 5 μm and a channel width of 1 μm was fabricated. Firstly, a 400 nm-thick thermal oxide layer was grown on the Si wafer by a furnace system to replace a glass substrate. Then an undoped 50 nm-thick amorphous silicon (a-Si) layer was deposited on the oxidized silicon wafer by low-pressure

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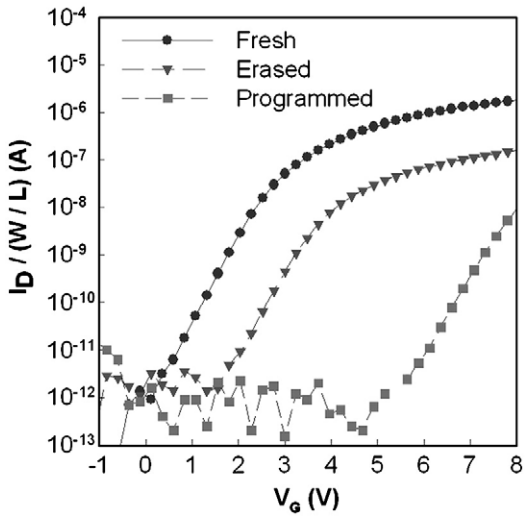

Fig. 1. The I_D–V_G curves of device before memory operation (fresh) and after the programming/erasing operations.

chemical vapor deposition (LPCVD) at 550 °C. Subsequently, the deposited a-Si layer was recrystallized by solid-phase crystallization at 600 °C for 24 h under N_2 ambient. After the patterning of the active region with electron beam lithography and a dry etch process, the 25-nm-thick oxide–nitride–oxide (ONO) multilayer gate dielectric layers were formed by LPCVD sequentially as the 5-nm tunnel oxide (TO), the 10-nm silicon nitride and the 10-nm blocking oxide (BO). A 150-nm-thick in-situ n^+ doped poly-Si layer was then deposited at 550 °C with flow rates of SiH_4 of 490 sccm and PH_3 of 100 sccm are at 600 mTorr, and defined. After S/D formation by self-aligned phosphorous implantation, a 200-nm oxide passivation layer was deposited and contact holes were patterned. Finally, Al metallization was performed and the devices were annealed at 400 °C in nitrogen ambient for 30 min.

3. Results and discussion

Fig. 1 plots the I_D–V_G curves of the SONOS-TFT before and after the program/erase operations by FN tunneling. During the program/erase operation, the device was operated for 10 s with a gate voltage of 18 V/−18 V and grounded source/drain. The proposed device exhibits not only the transistor characteristics, but also the nonvolatile memory characteristics because the nitride layer is used as a charge trapping layer. However, the threshold voltage (V_{th}) of a fresh memory device is different from that of the memory device after the erasing operation.

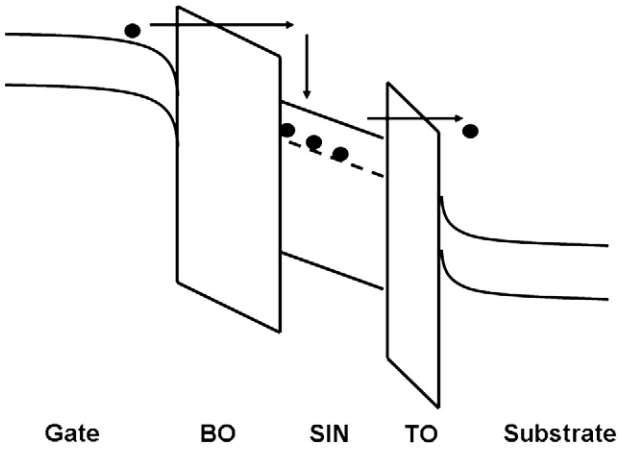

Fig. 2. Schematic band diagram during erasing operation with FN-tunneling mechanism.

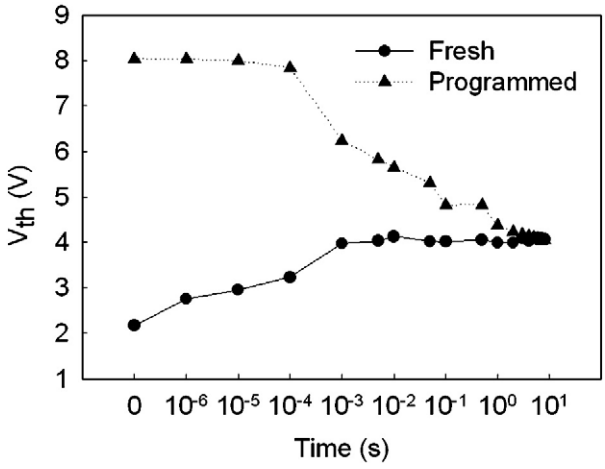

Fig. 3. Self-convergent characteristics of the device with a −18 V erasing bias.

The results indicate that the charge stored in the nitride layer cannot be erased completely.

In general, electrons are injected from the poly-Si channel into the nitride layer and are captured by the traps in the nitride layer resulting in the V_{th} increase during the programming operation: conversely, the captured electrons are injected back into the poly-Si channel from the nitride layer during the erasing operation. Usually, the erased V_{th} is the same as the initial one in the fresh device. However, as the device is erased by the FN-tunneling mechanism, the electrons that are captured in the nitride layer cannot be completely removed because the electrons are injected from the control gate into the nitride layer. Therefore, after the erase operation, the new erased V_{th} is dominated by the dynamic balance between the gate injection into the nitride layer and the charge de-trapping out of the nitride layer. The schematic band diagram is shown in Fig. 2.

To determine the erased V_{th}, the fresh device and the programmed device were both erased using a −18 V erasing gate bias, as shown in Fig. 3. As the erasing time increases, the V_{th} of the fresh device initially increases and then saturates at a time of longer than 1 s. On the other hand, the V_{th} of the programmed device declines to a saturation value. As is clearly seen in Fig. 3, both threshold voltages tend to converge to the saturated threshold voltages. Indeed, the erased V_{th} is determined by the dynamic balance of the injection of electrons from the gate and the de-trapping of electrons to the Si channel; this phenomenon is the so-called self-convergent characteristic [14].

Fig. 4 shows the program characteristics of the SONOS-TFT obtained by using an 18 V programming gate bias at different temperatures.

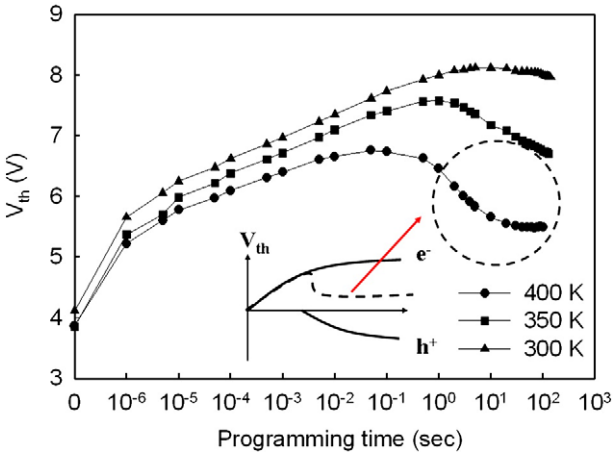

Fig. 4. Program characteristics of the SONOS-TFTs at different temperatures over time. Inset is the schematic threshold voltage shift of electron and hole behavior.

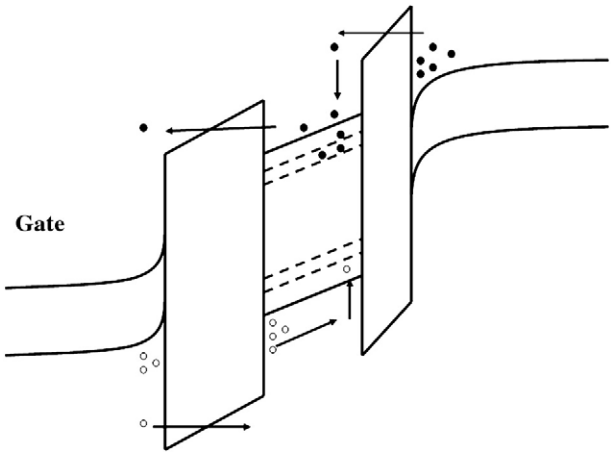

Fig. 5. Schematic band diagrams across ONO layer of programming characteristic at high temperature.

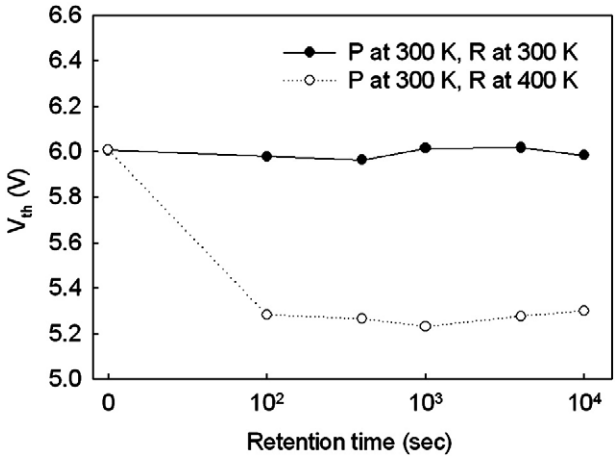

Fig. 7. Retention characteristics the SONOS-TFT at different retention temperatures.

Clearly, the programming efficiency decreases as the temperature increases. For general programming operations, the electrons are injected from the channel by tunneling through the tunnel oxide and are then captured by the traps in the nitride (either deep traps or shallow traps). When the device is programmed at high temperature, electrons captured in shallow traps may obtain thermal energy and are de-trapped, and then moved to the blocking oxide by field-enhanced Poole–Frenkel (P–F) emission. The de-trapped electrons are then injected to the gate by FN tunneling. Since the de-trapping phenomenon is more pronounced at higher temperature, the threshold voltage shift (ΔV_{th}) declines as the temperature increases. Therefore, the reduction of the threshold voltage shift of the device is greatest at 400 K. Because the hole gate injection in SONOS memory was considered as a possible parasitic effect [15], the hole may play an important role in the programming process at high temperature. At a sufficiently long programming time (>0.05 s), the holes which are injected from the gate by FN tunneling can migrate to the tunnel oxide, resulting in a lowering of ΔV_{th}. Fig. 5 shows the schematic band diagram and carrier transport. The migration of holes in the nitride layer, as well as the migration of electrons, is based on the PF emission. Accordingly, as temperature increases, the injected holes more easily move to the interface between the nitride and tunnel oxide layers. As the programming time is extended to 100 s, the shift of V_{th} tends to saturate. The saturated V_{th} can be regarded as representing the dynamic balance of the electron and hole currents through the ONO layer. As shown in the inset in Fig. 4, the threshold voltage shift can be seen as the superimposition of electron and hole injections.

Fig. 6 shows the erasing characteristics of the SONOS-TFT at different temperatures with a −18 V erasing voltage. The device was programmed to the same V_{th} by using a 20 V programming gate bias. During the erase process, the electrons that were captured in the nitride layer were de-trapped and then moved to the tunneling oxide by the field-enhanced Poole–Frenkel (P–F) emission. Finally, the de-trapped electrons were injected back to the poly-Si channel by the tunneling mechanism. The threshold voltage shift increased with the temperature. Moreover, the erased threshold voltages for 350 K and 400 K are lower than that for 300 K, which is determined by the dynamic balance as shown in Fig. 3. The results in Figs. 4 and 6 demonstrate that the high temperature makes the electrons de-trap more easily from traps during both the program and the erase operations, resulting in the better erasing efficiency but the smaller threshold voltage shift.

Temperature-dependent retention characteristics were also discussed in this work. Fig. 7 presents the retention characteristics of the device at 300 K and 400 K for a device that was programmed with a gate bias of 18 V for 10 μs at 300 K. When retention is measured at 400 K, the threshold voltage decreases quickly from 6 V to 5.2 V during the first 100 s, and then remains unchanged to 10,000 s. This result is caused by the de-trapping of the electrons from the shallow traps during the first 100 s, and the retention of electrons in the deep traps throughout the remaining time period. The retention characteristics associated with programming at various temperatures (300 K, 350 K, and 400 K) were measured at 400 K and analyzed, as shown in Fig. 8. Clearly, the degradation of the threshold voltage was suppressed as the programming temperature increased. For devices programmed at 300 K or 350 K, the degradation of V_{th} is caused by the de-trapping of the

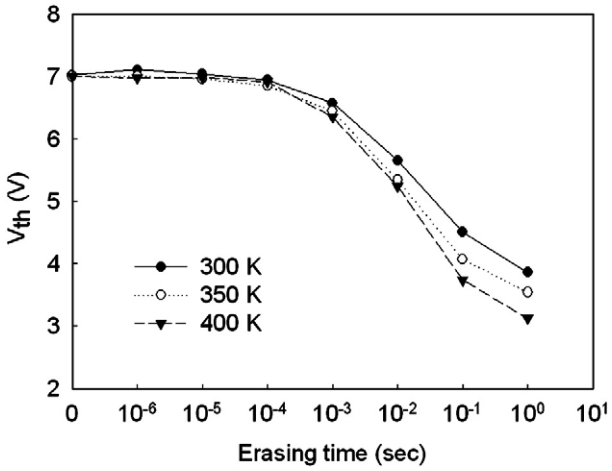

Fig. 6. Erasing characteristics of the SONOS-TFT at different erasing temperatures.

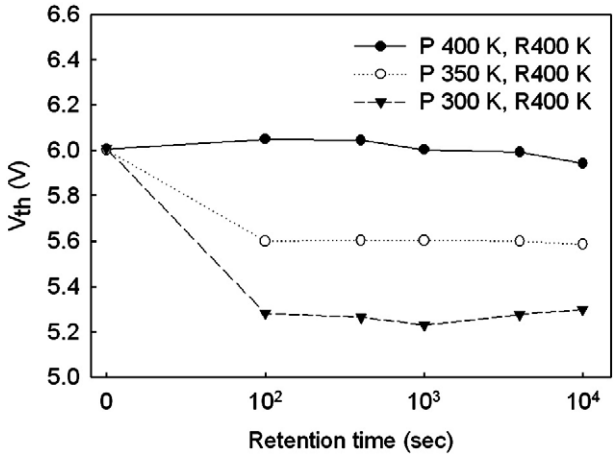

Fig. 8. Retention characteristics the SONOS-TFT at different programming temperatures.

electrons trapped in the shallow traps. For 400 K programming, the electrons that are trapped in shallow traps can be easily de-trapped to the gate, as mentioned above. This result reveals that most of the electrons are trapped in the deep states when the device programmed at high temperature.

4. Conclusion

We have demonstrated poly-Si TFT combined with nonvolatile SONOS memory. As the SONOS-TFT memory operated by FN-tunneling mechanism, the erased threshold voltage is different from the threshold voltage of a fresh SONOS-TFT due to the undesirable gate injection. Furthermore, as the device is programmed at high temperature, both the de-trapping of the electrons trapped in the shallow traps and the hole injection from the gate lead to the reduction in the threshold voltage shift. The retention results reveal that the electrons in the nitride layer at high temperature are mainly trapped in the deep traps. Hence, the device programmed at high temperature has the better retention characteristic.

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