國立交通大學

電子工程學系 電子研究所

博士論文

超薄電漿氮化氧化層與高介電常數氧化鉿於閘極介電層之研究

Study on Ultrathin Plasma Nitrided Oxide and HfO$_2$ High-κ Gate Dielectrics

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中華民國九十四年六月

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摘要

在以超薄電漿氮化氧化層作為閘極介電層的 N 型金氧半場效電晶體中，由通道熱電子與基板熱電子注入而引起的元件劣化效應是本論文研究的主題之一。相較於一般傳統使用的熱氧化層，可以發現超薄氮化閘極介電層比較容易受到通道熱電子與基板熱電子效應的影響，導致更大的臨界電壓偏移與轉移電導值降低。劣化增加的嚴重性會隨著在閘極介電層因氮化時間增長所致的氮元素含量增加而增加。儘管對於傳統的熱氧化層或是電漿氮化氧化層二者而言，由基板熱電子所引起的劣化是與注入電子的能量強烈相關，但是氮化氧化層表現在臨界電壓偏移的明顯劣化情況卻是發生於較熱氧化層為低的基板偏壓值。在以電漿氮化氧化層作為閘極介電層的 N 型金氧半場效電晶體中，這種經由基板負偏壓致使的劣化增加現象，可歸因於在電漿氮化製程程序中導入的一個較高濃度的順磁性電子陷阱先驅物。另一方面，在以超薄電漿氮化氧化層作為閘極介電層的 P 型金氧半場效

電晶體元件中，也可以發現類似的劣化趨勢。在通道熱電子壓迫測試之後，可以發現更嚴重的臨界電壓偏移與轉導值降低現象。不過，氮化氧化層作為閘極介電層的 P 型金氧半場效電晶體，會受到相較於傳統熱氧化層為大的負偏壓溫度不穩定效應。這種由於受偏壓與溫度壓迫測試導致的不穩定現象，在 N 型金氧半場效電晶體元件中是不顯著的。

本論文探討的另一個主題是氧化鉿，一個作為金氧半場效電晶體閘極介電層的最佳高介電常數材料。在金絕半電容器的製作中，採用原子汽相沉積氧化鉿介電層，搭配以濺鍍方式沉積銅或鋁金屬作為閘極所組成的。為了便於比較，同時也製作了以二氧化矽介電層所組成的金絕半電容器對照組。利用偏壓溫度壓迫測試與崩潰電荷測試方法，可以對電容器的穩定性與可靠性進行檢驗。相對於在二氧化矽介電層中的高漂移速率，銅金屬在氧化鉿介電層的組成中顯得相當穩定。銅金屬閘極的氧化鉿電容器也具有比鋁金屬閘極較高的電容值，而且沒有可靠性降低的問題。此實驗結果顯示具有高密度 $9.68\ \mathrm{g/cm^3}$ 的氧化鉿是一個很好的阻擋銅金屬擴散的阻障層。而這也意味著銅金屬在積體電路閘極介電層後續製程整合的可行性。

氧化鉿高介電常數材料的另一個重要應用是作為金絕金電容器的絕緣層。利用一標準的後段金屬層作為下電極，金絕金電容器已經成為微處理器、高頻電路與混合信號積體電路之一關鍵被動元件。為了增加電路密度與減少晶胞面積與成本，高電容密度是金絕金電容器一項很重要的考量因素。因此採用高介電常數材料像是氧化鉿，就是增加電容密度的一個很有效的方式。在金絕金電容器的實驗結果可以得到約 $5\times10^{-9}\ \mathrm{A/cm^2}$ 的低漏電流密度與約 $3.4\ \mathrm{fF/\mu m^2}$ 的高電容密度，達到很小的溫度係數與頻散效應。一些不同的金屬電極像是鉭、鋁、銅等也加以比較。最後氧化鉿金絕金電容器的電性傳導機制可被推導出來並歸類為Frenkel-Poole形式。

Study on Ultrathin Plasma Nitrided Oxide and HfO_2 High-κ Gate Dielectrics

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Abstract

The degradation induced by channel hot electron (CHE) and substrate hot electron (SHE) injection in nMOSFETs with ultrathin plasma nitrided gate dielectric was studied in this thesis. Compared to the conventional thermal oxide, the ultrathin nitrided gate dielectric is found to be more vulnerable to CHE and SHE stress, resulting in enhanced threshold voltage shift and transconductance reduction. The severity of the enhanced degradation increases with increasing nitrogen content in gate dielectric with prolonged nitridation time. While the SHE-induced degradation is found to strongly relate to the injected electron energy for both conventional oxide and plasma-nitrided oxide, dramatic degradation in threshold voltage shift for nitrided oxide is found to occur at a lower substrate bias magnitude, compared to thermal oxide. This enhanced degradation by negative substrate bias in nMOSFETs with plasma-nitrided gate dielectric is attributed to a higher concentration of paramagnetic electron trap precursors introduced

during plasma nitridation. On the other hand, similar degradation trend was also found in the pMOSFET devices with ultrathin plasma nitrided gate dielectric. Enhanced threshold voltage shift and transconductance reduction were observed after CHE stress for the nitrided devices. Nevertheless, the pMOSFETs with nitrided gate dielectric suffer larger negative bias temperature instability (NBTI), comparing to that with conventional thermal oxide. Such instability owing to bias-temperature stressing is inconspicuous in nMOSFET devices.

The other subject included in this thesis is HfO_2, a promising high-*k* material in gate dielectric of MOSFETs. Metal-insulator-semiconductor (MIS) capacitors were fabricated using atomic vapor deposition (AVD) HfO_2 dielectric with sputtered copper and aluminum gate electrodes. The counterparts with SiO_2 dielectric were also fabricated for comparison. Bias-temperature stress (BTS) and charge-to-breakdown (Q_{BD}) test were conducted to examine the stability and reliability of these capacitors. In contrast with the high Cu drift rate in SiO_2 dielectric, Cu in contact with HfO_2 seems to be very stable. The HfO_2 capacitors with Cu-gate also depict higher capacitance without showing any reliability degradation, compared to the Al-gate counterparts. These results indicate that HfO_2 with its considerably high density of 9.68 g/cm^3 is acting as a good barrier to Cu diffusion, and it thus appears feasible to integrate Cu metal with the post-gate-dielectric ULSI manufacturing processes.

Another application for HfO_2 high-*k* dielectrics is metal-insulator-metal (MIM) capacitors. MIM capacitors using one of the standard back-end metal layers as bottom electrode have emerged as key passive components for microprocessors, high frequency circuits, and mixed-signal integrated circuits applications. A high capacitance density is important for a MIM capacitor to increase the circuit density and reduce the cell area

and cost. Therefore, adoption of high-*k* material like HfO_2 is a very efficient way to increase the capacitance density. Experimental results show low leakage current densities of ~5×10^{-9} A/cm^2 and high capacitance density of ~3.4 fF/μm^2 at 100 kHz in the MIM capacitors. The temperature coefficient and frequency dispersion effect for these MIM capacitors were very small. Different metal electrodes like tantalum, aluminum, and copper were also investigated and compared. Finally, the mechanism of electrical transport was extracted for the HfO_2 MIM capacitors to be Frenkel-Poole type conduction mechanism.

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Chapter 1

Introduction

1.1 Overview of Ultrathin Gate Oxide Reliability

The IC industry has been rapidly and consistently scaling the design rule, increasing the chip and wafer size, and cleverly improving the design of devices and circuits for over 35 years. As a result, the industry has enjoyed exponential increases in chip speed and functional density versus time combined with exponential decreases in power dissipation and cost per function versus time, as projected by Moore's Law [1]-[3]. As metal-oxide semiconductor field-effect transistors (MOSFETs) are scaled to deep submicron dimensions, the integrated circuit (IC) industry is running into increasing difficulties in continuing to scale at the accustomed rate, owing to the small dimensions and certain key device, material, and process limits that are being approached.

For the past three decades, CMOS technology has powered a revolution and leads the industry to enjoy a great success due to its highly integrated performance in both dimension and density with scaling. The great advances made in ULSI technology in recent years have been underpinned by rapid developments in the design and fabrication of CMOS devices. It is often said that the real magic in silicon technology lies not in the silicon crystalline material but in silicon dioxide, since silicon dioxide is employed as many critical components of silicon devices [4]. Due mainly to formation of nearly perfect interface property of silicon and silicon dioxide, SiO_2 has been treated as an ideal gate insulator of MOS devices for several generations. However, as CMOS technology scales aggressively into deep submicron regime and beyond, gate oxide reliability becomes of a critical issue. Though physical gate length is the most important factor in scaling CMOS transistor density and performance, aggressive scaling of gate oxide thickness is required. For a MOSFET to behave as a transistor, the gate must exert greater control over the channel than the drain dose, i.e., the gate to channel capacitance must be larger than the drain to channel capacitance [5]. Furthermore, scaling of gate oxide thickness not only benefits the driving capability of transistor but suppresses the short channel effect, which is known as a stumbling stone for CMOS scaling. Therefore, to ensure the continued shrinkage of CMOS technologies down to deep submicron regime and beyond, ultrathin gate dielectric with low defect density and high reliability is indispensable.

Since Momose *et al.* from Toshiba group first proposed the use of 1.5 nm direct-tunneling gate oxide for nMOSFETs with extremely high device performance in 1994 [6], many aggressive studies regarding direct tunneling gate oxide for sub-quarter micron devices have been carried out [7]-[14]. The application of direct-tunneling gate oxide not only achieves high speed for logic circuits, its use is also essential for high-performance RF applications [13], [14]. In addition, the use of thinner oxides is also critical to meet the demands of lower programming voltage for future nonvolatile memories [15]. However, the application of direct-tunneling gate oxide to ULSI devices faces many challenges. Firstly, the presence of large quantum-mechanical (QM) tunneling current is a serious scaling limitation in terms of standby power consumption [16]. Secondly, breakdown characteristics for ultrathin oxides become even more critical due to the dramatic increase in electric field across the oxide during normal device operation. Whether oxide becomes inherently more robust or more vulnerable to electric stress as it thins down therefore plays a very crucial role for its applications to ULSI devices. Thirdly, poly-gate depletion effects are known to get worse with oxide scaling. This is because the operating gate voltage normally does not scale proportionally to the oxide thickness, and therefore the average surface field increases. The additional voltage drop at the poly depletion layer results in undesirable drive current degradation [17]. Since these effects worsen for thinner oxides, it could become a limiting factor for future device scaling.

A number of difficult challenges for MOSFET scaling are pointed out in the 2003 ITRS, and these are exacerbated by the previously mentioned rapid scaling. These challenges include several that are the result of the scaling down of the gate dielectric thickness: excessive gate leakage current, boron penetration from the p+ polysilicon gate electrode into the channel of the MOSFET, and increasing deleterious impact of polysilicon depletion in the polysilicon gate electrodes. Also, with scaling, the mobility of electrons and holes in the inversion layer is projected to become inadequate to meet the transistor performance goals. Finally, the classical planar bulk MOSFET itself will likely eventually become inadequate to meet transistor requirements, mainly because of the inability to adequately control short-channel and quantum effects and statistical variability for very small transistors.

1.2 Challenge of Gate Dielectric Scaling

As discussed in the previous section, the challenge inherent is associated with the rapid scaling of the gate dielectric thickness, T_d for high-performance and low-power logic technologies. The first difficulty is a susceptibility to boron penetration, which is the uncontrolled diffusion of boron from the heavily doped p+ poly gate of the pMOSFETs through the thin gate dielectric and into the MOSFET channel. The result is an uncontrollable but positive shift in the pMOSFET V_t. Lightly doping the gate oxide with nitrogen to form oxy-nitride generally controls this problem [18] and is the standard approach for current leading-edge IC technologies. The other major difficulty is excessive gate leakage current, as the oxy-nitride becomes very thin with scaling. The predominant conduction mode for very thin dielectrics is direct tunneling, where the gate leakage current increases exponentially with decreasing dielectric thickness. In Figure 1.1 [2], the 2003 ITRS projections for EOT and $J_{g,\,\mathrm{limit}}$ are plotted for low-standby-power (LSTP) logic. Also plotted are simulations of the expected gate leakage current density assuming the gate dielectric is oxy-nitride. As indicated in the figure, by 2006 oxy-nitride is incapable of satisfying the limit ($J_{g,\,\mathrm{limit}}$) on gate leakage current density. Carrying out a similar analysis for low-operating-power (LOP) and high-performance logic, oxy-nitride is incapable of satisfying the limit on gate leakage current density by 2006 for LOP logic also, and by 2007 for high-performance logic [2].

In 2006 or 2007, when oxy-nitride gate dielectric becomes incapable of meeting the maximum gate leakage limit, the preferred approach to reducing gate leakage in order to satisfy the limit is to replace the oxy-nitride with a “high-κ” dielectric. Such a dielectric has a significantly higher relative dielectric constant k than the k_{ox} = 3.9 value of silicon dioxide (the k for lightly nitrogen doped oxy-nitride is also close to 3.9). For a dielectric of thickness T_d, the equivalent oxide thickness, EOT, is:

$$EOT = T_d / (k / k_{ox}) = T_d / (k / 3.9). \tag{1.1}$$

To first order, a transistor with such a gate dielectric has a gate capacitance per unit area,

$$C_{g,\,\mathrm{area}} = k\varepsilon_0 / T_d = k_{ox}\varepsilon_0 / EOT, \tag{1.2}$$

where ε_0 is the dielectric constant of vacuum. $k_{ox}\varepsilon_0/EOT$ is also the value of the gate capacitance per unit area for an otherwise identical transistor with a silicon dioxide gate dielectric of thickness EOT. Hence, to first order, the major electrical characteristics such as

I_{on} should be the same for both transistors (except the gate leakage current, which should be significantly reduced for the transistor with high-κ gate dielectric). For silicon dioxide, with $k = 3.9$, $EOT = T_d$, while for high-κ gate dielectric, where $k > 3.9$, T_d is significantly larger than EOT. Since direct tunneling is strongly dependent on T_d, the gate leakage current density will generally be significantly smaller for the high-κ gate dielectric, if the energy barrier between the dielectric and silicon is large enough [19]. Extending current approaches using lightly nitrogen-doped oxy-nitride with $k \sim 3.9$, heavily nitrogen doped oxy-nitride has been shown to have $k > 5$, and as a result, gate leakage current reduced by more than an order of magnitude relative to silicon dioxide [20]. In simulating the gate leakage of oxy-nitride dielectric, as in Figure 1.1, such extended, heavily nitrogen doped oxy-nitride is assumed. Per the analysis above, high-κ gate dielectric is projected to be needed for low-power logic in 2006 and for high-performance logic in 2007. Very active research and development is being carried out on high-κ materials for the gate dielectric, and the current leading candidates are hafnium oxide, hafnium silicate, and hafnium oxy-nitride [21].

Another major front-end issue is polysilicon depletion in the gate electrode. When gate voltage is applied to turn on a MOSFET, a depletion region of thickness W_d forms adjacent to the polysilicon-oxide interface (see Figure 1.2). This depletion region increases the effective electrical thickness of the gate dielectric in inversion, EOT_{elec}:

$$EOT_{elec} = EOT + \Delta\text{poly} = EOT + (k_{ox} / k_{Si})W_d \sim EOT + W_d / 3, \qquad (1.3)$$

where $k_{Si} = 11.9$ is the relative dielectric constant of silicon and Δpoly encapsulates the impact of polysilicon depletion. According to Wilk *et al.* [19], Δpoly can be as much as 0.4 nm. As a result of the polysilicon depletion, EOT is replaced by EOT_{elec} in (1.2) for the gate capacitance per unit area, reducing the capacitance. Consequently, for any given gate voltage, the inversion layer charge and I_{on} are reduced. The impact of polysilicon depletion becomes more severe with the smaller *EOT* in succeeding technology generations. Increased doping of the polysilicon reduces the depletion, since W_d is inversely proportional to the square root of the polysilicon doping. However, with the limited solubility of the dopants, particularly boron for the p+ polysilicon gate of the pMOSFET, this solution will eventually become inadequate, even if germanium-doped polysilicon, which has higher solid solubility for boron, is used [22]. The preferred solution is metal-gate electrodes, since with metal gates there is virtually no depletion, no boron penetration, and sheet resistance is very low. According to 2003 ITRS projections, metal-gate electrodes will need to be implemented for high-performance logic by 2007 [2]. However, CMOS optimization requires a work function ~ 5.0 eV (near the silicon valence band edge) for pMOSFETs and ~ 4.1 eV (near the silicon conduction band edge) for nMOSFETs [23] to set the desired symmetric threshold voltages of 0.2 to 0.5 V for NMOS and −0.2 to −0.5 V for PMOS. One approach involves utilizing different metals with different work functions, one for the pMOSFET [24], [25], and one for the nMOSFET [26], [27] device. This would present difficult process integration problems and would tend to increase the chip processing complexity and cost. An alternative approach that aims to reduce the process complexity and cost is to utilize one material system for both metal electrodes, and use doping or alloy composition to vary the work function as necessary [25], [28].

1.3 Scope and Organization of the thesis

This thesis investigates promising candidates of alternative gate dielectrics containing nitrided oxide and hafnium oxide.

The thesis is organized as follows:

Chapter 2 reviews recent trends in gate oxide scaling to show that further scaling of SiO_2 is limited by static power dissipation and other fundamental considerations. As an alternative to continuing to scale SiO_2, the use of alternative high-*k* gate dielectrics is discussed. Several of the most important material properties for such high-*k* dielectrics are also reviewed.

Chapter 3 investigates the hot carrier injection reliability of nMOSFET's with ultrathin plasma nitrided gate oxide. The devices with plasma nitrided oxide suffer more trans-conductance reduction and threshold voltage shift. The degradation is direct proportional to the plasma nitridation time. We report, for the first time, an enhanced degradation under negative substrate bias in nMOSFETs with ultrathin plasma nitrided gate dielectric. The enhanced degradation is attributed to the introduction of paramagnetic electron trap precursors during plasma nitridation.

Chapter 4 investigates the hot carrier injection reliability and negative bias temperature instability of pMOSFET's with ultrathin plasma nitrided gate oxide. For channel hot-carrier stressing, the most efficient stressing condition is located corresponding to the region of maximum gate current. The negative threshold voltage shift indicates a positive charge build-up in the gate dielectric. For negative bias temperature stressing, appreciable enhancement of the threshold voltage shift can be observed through the raising of temperature. The enhanced device degradation is attributed to the H-related species and the interface trap generated during NBT stressing. NBTI is an important issue for pMOSFETs from the reliability point of view.

Chapter 5 presents the hafnium oxide film as alternative material to replace SiO_2 for gate dielectric in complementary metal-oxide-semiconductor technology. AVD^{TM}-deposited HfO_2 capacitors using Cu and Al as the gate electrode have been fabricated and investigated for the first time. Our results clearly show that HfO_2 dielectric depicts superior resistance against Cu diffusion after BTS test, compared to SiO_2. Moreover, the presence of Cu metal in direct contact with HfO_2 has negligible impact on the reliability of the HfO_2 capacitor. The fact that HfO_2 can behave as a good barrier against Cu diffusion is attributed to its considerably high density. This finding is important as it suggests the feasibility of a Cu integration process from the gate electrode to BEOL interconnect.

Chapter 6 investigates HfO_2 MIM capacitors with different metal electrodes. The MIM capacitor with Al top electrode exhibits the lowest capacitance density, while that with Cu top electrode exhibits the highest capacitance value. Due to the Al_2O_3 layer formed between Al and HfO_2, the capacitance density and the leakage current density were reduced. On the other hand, the successful fabrication of the Cu top electrode capacitor implies the possibility of integrating Cu with HfO_2 dielectrics.

Chapter 7 describes the conclusions of the thesis and the suggestions for future work.

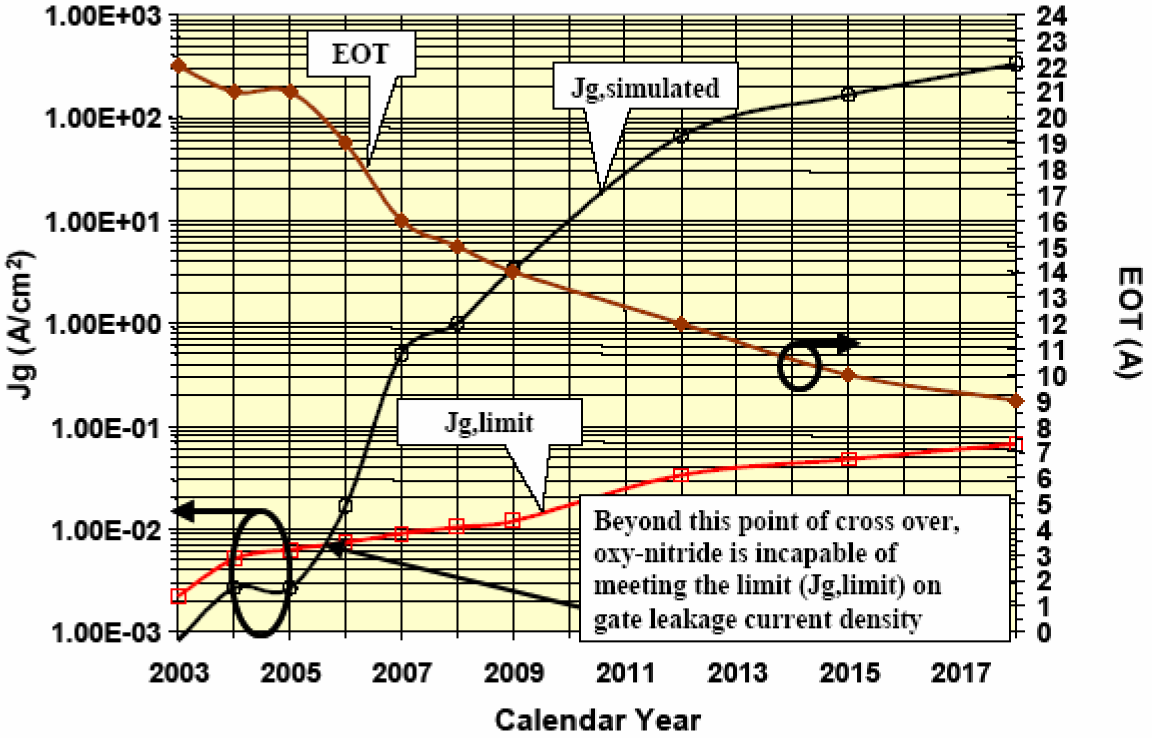


Fig. 1.1 LSTP logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling. [ITRS 2003]

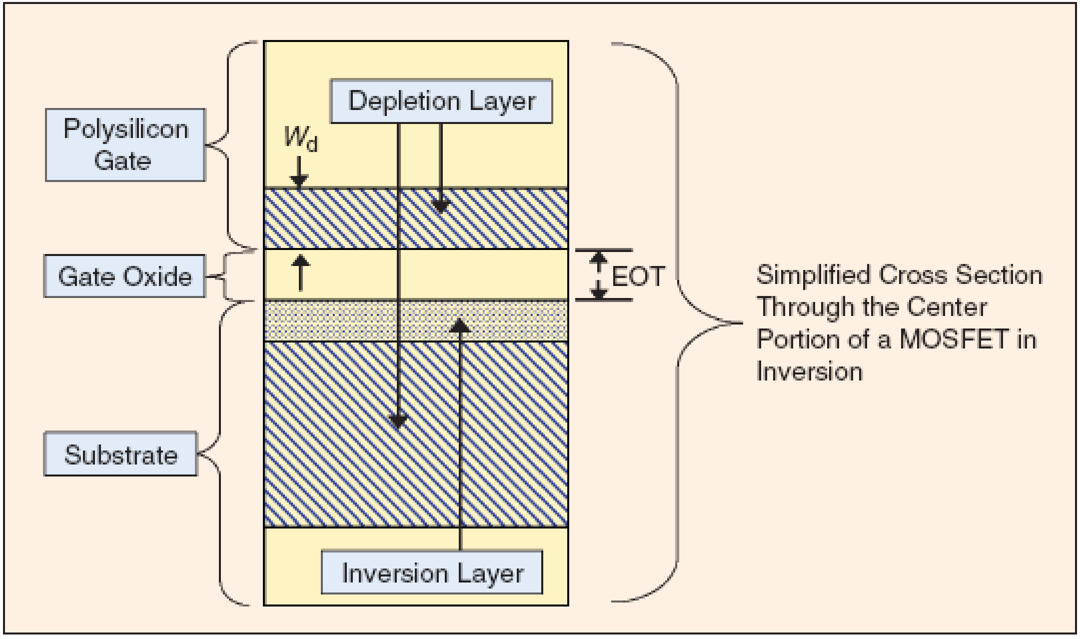


Fig. 1.2 Polysilicon depletion effects

Chapter 2

Trends in Gate Oxide Scaling

2.1 MOSFET Scaling

Recall that a MOSFET ideally acts as a three-terminal switch, either connecting or isolating the drain (D) and source (S) terminals based on the voltage applied to the controlling gate (G) terminal, as illustrated in Figure 2.1(a). In practice, this switching action is achieved through the use of a gate capacitor, as illustrated in Figure 2.1(b). Depending on the polarity of the voltage applied to the gate terminal, either positive or negative charge is induced in the channel region along the bottom plate of the gate capacitor. The channel charge either connects or isolates the drain and source nodes depending on the type of carrier contained in those regions.

The operation of the MOSFET depends critically on several properties of the gate dielectric material, SiO_2. The wide insulating bandgap (E_g) of SiO_2 electrically isolates charges in the gate and channel regions, so that the controlling gate terminal does not interfere with the flow of current in the channel region, as illustrated in Figure 2.2(a). Also, the interface between SiO_2 and the underlying Si substrate is electrically of very high quality, allowing electric field lines originating at the gate electrode to penetrate into the channel region to accumulate or invert the surface charge. Prior to the development of the Si/SiO_2 system, attempts to realize a field-effect transistor (FET) were hampered by the abundance of electrically active defects at the dielectric/semiconductor interface.

The amount of charge (Q) induced in the channel region is given by the product of the gate oxide capacitance per unit area (C_{ox}) and the voltage drop across the gate capacitor (V),

$$Q = C_{ox} V \,. \tag{2.1}$$

Since C_{ox} can be modeled as a parallel-plate capacitor, its value is given by

$$C_{ox} = \frac{k_{ox} \varepsilon_0}{t_{ox}} \,, \tag{2.2}$$

where k_{ox} is the relative dielectric constant, ε_0 is the permittivity of free space, and t_{ox} is the physical thickness of the dielectric material. Based on these relations, the drain-source current for a long-channel MOSFET operating in the saturation region can be expressed as

$$I_{ds} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)^2 \,, \tag{2.3}$$

where μ is the channel mobility, W and L are the width and length of the channel region, respectively, V_{gs} is the gate-source potential, and V_t is the threshold voltage. Equations 2.2 and 2.3 reveal that reducing the lateral (L) and vertical (t_{ox}) dimensions of the device increases the current flow between the drain and source. Intuitively, this is because reducing t_{ox} increases C_{ox} and hence the amount of channel charge, and reducing L decreases the distance the channel charge must travel to conduct a current. Reducing the gate oxide thickness (t_{ox}) along with the channel length (L) also helps to maintain the gate electrode’s control over short channel effects. Increased gate capacitance allows the gate potential to modulate more channel charge and is especially important as the supply voltage scales down. Much of the progress in Si microelectronics has been driven by the ability to continually shrink these and other critical dimensions of the MOSFET to increase performance and decrease die area, a process referred to as scaling [29].

2.2 Recent Gate Oxide Scaling Trends

The gate oxide has been aggressively scaled in recent generations. Figure 2.3 shows extrapolated gate oxide scaling targets based on published data from recent Intel technologies [30]. The technology node refers to the smallest poly-Si gate length which can be defined by photolithography and roughly corresponds to the minimum channel length for a given process technology. A more complete list of projected transistor parameters is given in Table 2.1. The predictions are based on extrapolations of published state-of-the-art 180 nm technologies assuming channel length, supply voltage, and gate oxide thickness scaling factors of 0.7, 0.8, and 0.8, respectively [31]-[33]. These projections, representative of the current targets for high-performance logic technology, aggressively outpace those compiled in the 2000 update of the International Technology Roadmap for Semiconductors (ITRS). However, these data have been included and revised in the 2004 update of the ITRS, as shown in Table 2.2.

The two data sets in Figure 2.3 refer to the equivalent electrical and physical thickness of the gate oxide. The equivalent oxide thickness (*EOT*) refers to how thin a pure SiO_2 layer would need to be in order to meet the gate capacitance requirements of a given technology. In a modern MOSFET device, the gate oxide behaves electrically as if it were 0.8–1.0 nm thicker than its physical thickness, because depletion in the poly-Si gate and quantization in the inversion layer each extend the centroids of charge modulated by the gate voltage by 0.4–0.5 nm [34].

2.2.1 Gate Leakage and Static Power Dissipation

A significant consequence of aggressively scaling the gate oxide is the resulting direct tunneling of carriers through the potential barrier presented by the insulator layer. As illustrated in Figure 2.2(b), when the thickness of the potential barrier becomes less than approximately 3.0 nm, substantial tunneling currents can flow through the gate oxide, leading to large static power dissipation. In addition, the gate and channel regions are no longer isolated from each other when tunneling occurs. Recent studies have shown that gate leakage can significantly impact circuit performance as a consequence, especially for analog and dynamic logic circuits.

Figure 2.4 shows extrapolated trends in power dissipation for high-performance CMOS logic based on published data from recent Intel technologies [30], [35]. Both active and static power components are shown. Traditionally, the main source of power dissipation in CMOS circuits has been active switching, which depends on the rate at which node capacitances are charged and discharged,

$$P_{active} = NCV^2 f \ . \tag{2.4}$$

N is the number of switching transistors, C is the total switched capacitance, V is the supply voltage, and f is the frequency of operation. The observed increase in active power with each generation reflects the trend towards higher levels of integration and higher frequency of operation, which more than offsets the reduction in device capacitance and supply voltage. Much more alarming is the rapid increase in static (i.e. standby) power dissipation beyond the 180 nm technology node. Static power is primarily due to subthreshold (I_{off}) and gate (I_{gate}) leakage currents. The extrapolation of the I_{gate} component is based on quantum mechanical modeling of gate tunneling currents through ultrathin SiO_2 layers by Lo *et al.* [34], [36]. As shown in Figure 2.4, standby power has been increasing much more rapidly than active power in recent generations, and if current trends continue, standby power will actually surpass active power beyond the 65 nm generation. Clearly, the exponential increase in the gate leakage, which arises from direct tunneling of carriers through the gate oxide, presents a serious limit to future CMOS scaling.

2.2.2 Scaling Limit of SiO_2

In addition to limitations arising from static power dissipation, there has recently been great interest in determining if a more fundamental limit to scaling SiO_2 exists. One of the most convincing experiments which demonstrated that such a fundamental limit indeed exists is the work of Muller *et al.* from Bell Labs [37], [38]. Using a scanning transmission electron microscope (STEM) probe with 0.2 nm resolution, they studied the chemical composition and electronic structure of oxide layers as thin as 0.7–1.2 nm through detailed electron-energy-loss spectroscopy (EELS) measurements. By moving the probe site-by-site through the ultrathin SiO_2 layers, they mapped the local unoccupied density of electronic states, which provides insight into the local energy gap of the material, as a function of the probe position. In their work, the local energy gap was given by the separation between the highest occupied and lowest unoccupied states. They found that three to four monolayers of SiO_2 were needed to ensure that at least one monolayer maintained a fully bulk-like bonding environment, giving rise to the wide, insulating bandgap of SiO_2. Since the first and last monolayers form interfaces with Si and poly-Si respectively, they have bonding arrangements intermediate to those of bulk Si and bulk SiO_2 and hence have energy gaps smaller than that of bulk SiO_2. Based on these insights, Muller *et al.* concluded that the fundamental scaling limit of SiO_2 is likely to be in the range of 0.7 to 1.2 nm. Another important insight from their study was that for a 1.0 nm oxide, a 0.1 nm increase in the root-mean-square (RMS) interface roughness can lead to a factor of 10 increase in the gate leakage current, showing that the growth of such thin layers must be precisely controlled on atomic scales.

There has been remarkable agreement between experiment and theory regarding the scaling limit of SiO_2. Theoretical studies by Tang *et al.* employing a Si/SiO_2 interface model based on the β-cristobalite form of SiO_2 showed that the band offset at the interface degraded substantially when the SiO_2 layer was scaled to less than three monolayers [39]. The large reduction in the band offset was attributed to a reduction in the SiO_2 bandgap and also suggested 0.7 nm as the scaling limit of SiO_2. A more recent study by Kaneta *et al.* using a Si/SiO_2 interface model based on β-quartz SiO_2 directly computed the local energy gap as a function of position through the interface [40]. While the transition from bulk Si to bulk SiO_2 in their model was structurally abrupt, it was found that the full bandgap of SiO_2 was not obtained until the second monolayer of SiO_2 was reached. Again, these calculations suggest that approximately 0.7 nm of SiO_2 is the minimum required for substantial band offsets to develop at the interface, indicating the formation of a large bandgap.

Thus, both experiment and theory suggest that the bulk properties of SiO_2, including the wide, insulating bandgap needed to isolate the gate and channel regions, cannot be obtained for films less than 0.7 nm thick. Since technology roadmaps predict the need for sub-0.6 nm gate oxides in future generations, it is unlikely that SiO_2 will scale beyond the 70 nm generation, both from static power dissipation and fundamental materials science points of view.

2.3 High-*k* Gate Dielectrics

As an alternative to continuing to scale SiO_2, recent effort has focused on the development of alternative high-*k* gate dielectrics. Recall that the traditional approach to scaling the gate dielectric has been to reduce t_{ox} to increase C_{ox},

$$C_{ox} = \frac{k_{ox}\varepsilon_0}{t_{ox}}, \tag{2.5}$$

But now that gate leakage currents due to direct tunneling have reached unacceptably high levels, the more recent high-*k* approach is to increase the physical thickness of the film ($t_{high\text{-}k}$) to reduce the tunneling currents, yet at the same time obtain higher values of gate capacitance by using a dielectric material with a higher dielectric constant ($k_{high\text{-}k}$) relative to SiO_2,

$$C_{high-k} = \frac{k_{high-k}\varepsilon_0}{t_{high-k}}. \tag{2.6}$$

Over the past several years, a wide variety of high-*k* dielectrics have been investigated as possible replacements for SiO_2. Compared to just five or six years ago, a much shorter list of candidates is still being pursued today, due to the stringent requirements placed on the MOS dielectric material. In considering candidate gate dielectrics, it should be recalled that the dominance of the Si MOSFET over competing technologies has largely been attributed to the high quality of thermally grown SiO_2 and the resulting Si/SiO_2 interface. Other substrate materials provide higher intrinsic carrier mobilities or concentrations, yet none can match the electrical performance of the Si/SiO_2 interface. Not surprisingly then, the most stringent requirements arise from the need to develop an alternative dielectric material whose Si interface properties match the high quality of the Si/SiO_2 interface.

In the following sections, some of the important materials properties required of high-*k* dielectrics are reviewed. Such considerations lead to the conclusion that only a few basic classes of materials are capable of meeting the requirements for a replacement dielectric material. Several excellent review papers discuss these and other material considerations for high-*k* dielectric applications in further detail [41]–[43]. A particularly important consideration is that the chosen high-*k* dielectric be scalable to future technology generations. Because of the immense costs associated with developing a replacement material for SiO_2, which benefits from nearly 30 years of research, the industry requires a material which will not only meet the requirements for the upcoming 90 nm or 65 nm technologies, but can also be scaled to end-of-the-roadmap technology nodes.

2.3.1 Target Dielectric Constant

To first order, a high-*k* film can be physically thicker than a pure SiO_2 layer by the ratio of its dielectric constant to that of SiO_2, and still provide the same gate capacitance, since

$$C_{ox} = \frac{k_{ox}\varepsilon_0}{t_{ox}} = C_{high-k} = \frac{k_{high-k}\varepsilon_0}{t_{high-k}} \tag{2.7}$$

and

$$t_{high-k} = \left(\frac{k_{high-k}}{k_{ox}}\right)t_{ox}, \tag{2.8}$$

thus potentially reducing direct tunneling currents substantially. Equation (2.8) is often expressed in terms of the equivalent oxide thickness (*EOT*) described in Section 2.2. In the context of high-*k* dielectrics, *EOT* is defined as the thickness of a pure SiO_2 layer which provides the same gate capacitance as a high-*k* layer,

$$EOT = t_{ox} = \left(\frac{k_{ox}}{k_{high-k}} \right) t_{high-k} \, . \qquad (2.9)$$

Recall from Figure 2.3 that the gate capacitance targets for the upcoming 90 nm and 65 nm technologies require dielectrics with physical *EOT* values of 1.0 nm and 0.6 nm, respectively. At first glance, it would seem that an arbitrarily high *k*-value would allow a substantially thick dielectric film to meet very small *EOT* targets. In practice, the extreme gate thickness-length aspect ratio that would result from a very high *k*-value and hence a very thick insulator leads to fringing field effects which undermine the gate electrode's ability to maintain control of the channel. Device simulations have explored the impact of large *k*-values on threshold voltage roll-off and subthreshold swing to determine the upper range of desirable dielectric constants, which generally is believed to be on the order of 30 to 50 [44]. The lower range of acceptable dielectric constants depends on the *EOT* requirements of a given technology generation. It is generally believed that pure or nitrided SiO_2 with dielectric constants close to 4 will provide physical *EOTs* down to about 1.6 nm; near-term alternatives such as Si_3N_4 or oxynitride stacks with nitrided SiO_2 interfaces with *k*-values near 7 will provide physical *EOTs* down to about 1.1 nm; and pure metal oxides or pseudo-binary alloys of metal oxides with dielectric constants in the range of 15 to 25, providing a factor of four to six improvement over SiO_2, will provide physical *EOTs* down to about 0.6 nm.

It should be noted that some of the near-term materials such as Si_3N_4 and the metal oxide Al_2O_3 are attractive from the point of view of integration, since substantial experience and equipment infrastructure for processing both materials exist. Due to the relatively low gains in the dielectric constant relative to SiO_2, however, these materials are likely to be intermediate solutions at best. It is also worth mentioning that the ferroelectric class of materials which has been pursued for 1 Gb and beyond dynamic random access memory (DRAM) storage capacitors provide *k*-values in the range of 100 to 1000, far in excess of the requirements for a gate dielectric [41]. In addition, ferroelectric materials generally require a complex composite structure to promote stability and adhesion to adjoining layers, so that using them as transistor gate dielectrics is not feasible. Hence, substantial new investments in materials research and technology development are needed, above and beyond the existing efforts in the DRAM community, to realize alternative gate dielectrics for logic technologies.

Many high-*k* materials consist of oxides and alloys of d-electron transition metals. Representative transition metal oxides include: column 3B materials such Y_2O_3 and La_2O_3; column 4B materials such as ZrO_2 and HfO_2; and column 5B materials such as Ta_2O_5. It is well-known that the static (i.e. low frequency) dielectric constants of such metal oxides have significant electronic and ionic contributions at the frequencies of interest [45]. The electronic contribution arises from the polarization of electrons in response to an applied electric field, whereas the ionic contribution depends on the displacement of the ions themselves in response to an electric field. To first order, the additional shells of electrons in a heavy transition metal compared to a lighter atom allow for greater electronic polarization for a given electric field strength. It has also been observed that the d-electron metal transfers nearly all of its valence electrons to the oxygen atom, resulting in increased ionicity and hence polarization. In addition, the bonding between many d-electron transition metals and oxygen exhibit a softening of the phonon mode. In other words, the natural vibration frequency associated with the metal-oxygen bond is lowered. This allows the relatively low frequency excitation common in microelectronics applications to couple into the vibrational mode, leading to large displacements of the metal atom. The ability to model both the electronic and ionic components of the dielectric response is thus important for investigation of high-*k* materials.

In addition to pure transition metal oxides, there is also considerable interest in pseudo-binary alloys for high-*k* applications. Representative examples include the silicate system, such as $ZrSi_xO_y$, which can be thought of as an alloy between the pure metal oxide ZrO_2 and SiO_2, $(ZrO_2)_x(SiO_2)_{1-x}$; and the aluminate system, such as $LaAl_xO_y$, which is an alloy between La_2O_3 and Al_2O_3, $(La_2O_3)_x(Al_2O_3)_{1-x}$. The motivation for the use of these alloys over pure metal oxides arises from their interface properties with Si, as described in Section 2.4.

2.3.2 Bandgap and Band Offsets

Since an important function of the gate dielectric is to isolate the gate terminal from the current-carrying channel region, it needs to be a good insulator. SiO_2 provides a wide bandgap on the order of 9 eV, substantially larger than the 1 eV bandgap of Si. A closely related property is the height of the potential barrier presented to tunneling electrons from the conduction band and to tunneling holes from the valence band. At the Si/SiO_2 interface, these band offset energies are relatively symmetric, so that barriers on the order of 4 eV are presented to both electrons and holes. Any degradation of the bandgap results in lower band offset energies which compromise the potential tunneling reduction obtained by using a material with a higher dielectric constant and hence a physically thicker film.

It has been observed that most high-*k* materials have smaller bandgaps relative to SiO_2. Figure 2.5 illustrates the approximately inverse relation between bandgap and static dielectric constant obeyed by a number of representative high-*k* dielectrics. This behavior is expected qualitatively since stronger polarizability implies weaker bonding, and weaker bonding implies a smaller separation between bonding and antibonding energies [46]. The implied tradeoff between dielectric constant and bandgap severely limits the applicability of candidate materials at the upper range of target dielectric constants. For example, early high-*k* efforts focused on Ta_2O_5 and TiO_2, since they provided large dielectric constants and substantial processing experience with the materials existed from DRAM applications [47]–[50]. However, their bandgaps are substantially smaller than that of SiO_2, with estimated values of 4.5 eV and 3.5 eV for Ta_2O_5 and TiO_2, respectively [42]. Interestingly, Al_2O_3 presents an exception to this general trend and provides approximately twice the *k*-value of SiO_2 while maintaining a large bandgap.

2.3.3 Si Interface Properties

The feasibility of any high-*k* dielectric ultimately depends on the quality of its interface with Si. Two particularly important interface considerations are thermal stability and defect formation. Many of the early metal oxides such as Ta_2O_5 and TiO_2 which were pursued because of their previous use in DRAM processes have been found to be thermally unstable in direct contact with Si [48], [50], [51]. For both materials, reactions have been observed in which thick interfacial layers form between the metal oxide and the Si substrate. Specifically, Alers *et al.* observed the formation of a 2.0 nm thick interfacial region after Chemical Vapor Deposition (CVD) of Ta_2O_5 on HF-last-Si at 400°C [48]. Similar observations of interfacial reaction have been made for TiO_2 films deposited directly on HF-last-Si [50]. Since the channel transport properties were determined by nominally Si/SiO_2-like interfaces for both materials, reasonable channel mobilities were obtained. The Si/SiO_2 interface is known to have a very low density of interface states arising from unsaturated surface bonds and other electrically active imperfections. Interface states lead to degradation of on-current, since carrier mobility is limited by scattering at the interface due to the strong vertical electric fields present in the channel. In the case of the TiO_2 device, deliberate efforts to suppress the growth of the interfacial layer led to substantial charging and degradation of peak channel mobility from 150 cm^2/V-sec to 60 cm^2/V-sec.

For both Ta_2O_5 and TiO_2, the formation of an interfacial oxide layer appears inevitable and necessary to maintain good transport properties at the Si interface. In fact, interfacial reaction is expected for these materials based on analysis of equilibrium phase diagrams [42]. While it is difficult to directly determine the chemical composition of such thin layers, it is generally believed that a SiO_2-like layer with a relatively low dielectric constant forms, as illustrated by Figure 2.6. The formation of an interfacial low-*k* layer between the Si substrate and the high-*k* film is highly undesirable, since then the gate dielectric appears electrically as a series capacitance whose effective capacitance is less than that of the high-*k* layer alone,

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}. \tag{2.10}$$

Assuming that the interfacial layer has the dielectric properties of SiO_2, Equation (2.10) can be re-written in terms of the following relation for the *EOT* of the dielectric stack.

$$t_{eq} = t_{SiO_2} + \left(\frac{k_{SiO_2}}{k_{high-k}} \right) t_{high-k} \tag{2.11}$$

For a given *EOT* (t_{eq}) target, any non-zero t_{SiO2} reduces the thickness of the high-*k* film which can be used, thus increasing the tunneling transmission through the stack. Furthermore, the minimum *EOT* can never be less than t_{SiO2}, so that the interfacial oxide layer limits the maximum achievable capacitance of the gate stack.

2.4 Zirconium and Hafnium Silicates

Zirconium (Zr) and hafnium (Hf) silicates are promising high-k dielectrics developed largely to overcome the interface stability issues suffered by many high-k binary metal oxides [52]–[54]. Ternary phase diagrams of the Zr-Si-O system reveal that the binary metal oxide ZrO_2 as well as the compound silicate $ZrSiO_4$ should be thermodynamically stable in direct contact with Si. Since Zr and Hf are isoelectronic elements, it is expected that HfO_2 and $HfSiO_4$ should also be stable on Si.

In practice, interface reactions, much like those described in the previous section for other metal oxides, have been observed for nearly all ZrO_2 and HfO_2 films deposited directly on Si [50], [55], [56]. High resolution transmission electron microscope (HRTEM) measurements by Campbell *et al.* revealed that interfacial layers of 0.9 nm and 1.2 nm thickness were formed when depositing ZrO_2 and HfO_2 directly on Si, respectively [50]. Medium energy ion spectroscopy (MEIS) and x-ray photoelectron spectroscopy (XPS) analysis showed that the interfacial layer was SiO_2-like, not a silicate. In contrast, Lee *et al.* found that ZrO_2 and HfO_2 films deposited directly on Si using a magnetron sputtering technique gave rise to a silicate interfacial layer [55]. Copel *et al.* also found that ZrO_2 deposition by atomic layer chemical vapor deposition (ALCVD) on HF-last-Si led to discontinuous nucleation with islands of ZrO_2 interspersed along the Si interface [56]. Atomic force microscopy also revealed a large RMS roughness of 0.57 nm along the interface.

The variability in the interfacial layer following ZrO_2 and HfO_2 deposition leads to the conclusion that the growth of such layers is difficult to control. Instead, recent efforts toward integrating ZrO_2 and HfO_2 films have focused on first growing a high quality, well controlled, ultrathin SiO_2 layer prior to ZrO_2 deposition. Perkins *et al.* deposited ALCVD ZrO_2 films on chemically grown oxides and obtained $EOT < 1.4$ nm [57]. Having an underlying SiO_2 layer also leads to the desirable electrical properties of a Si/SiO_2 interface which helps to maintain high channel carrier mobility. Of course, the minimum *EOT* is still limited by the extent of the interfacial SiO_2 layer as described previously.

Another potential problem with ZrO_2 and HfO_2 is that they have been observed to crystallize at relatively low temperatures. Polycrystalline films may exhibit high leakage paths along grain boundaries which act as trapping centers. Thus, in general, amorphous dielectrics which resist recrystallization up to relatively high temperature are desirable for gate dielectric applications.

To overcome the challenges of pure ZrO_2 and HfO_2 films, Wilk and Wallace proposed the use of Zr and Hf silicates as promising high-*k* gate dielectrics [42], [52]–[54]. By alloying two different oxides, such as ZrO_2 and SiO_2 in the case of Zr silicate, $(ZrO_2)_x(SiO_2)_{1-x}$, they believed that it may be possible to retain the desirable properties of both oxides while eliminating the undesirable properties of each. By explicitly incorporating SiO_2 during deposition of ZrO_2 precursors, the driving force for reaction between the dielectric and the Si substrate is reduced, so that the interface is more likely to behave like the desirable Si/SiO_2 interface. This allows better control of the Si interface properties. It is generally believed that silicate deposition results in a single, uniform high-*k* layer in direct contact with Si. Combining a poly-crystalline film like ZrO_2 with an amorphous one like SiO_2 also leads to an amorphous silicate phase.

At the same time, by incorporating some amount of ZrO_2 into the SiO_2 film, the enhanced polarizability of Zr-O bonds relative to Si-O bonds leads on average to a higher dielectric constant for material. While many different silicate systems are possible, column IVB elements such as Zr and Hf are expected to substitute well for Si atoms, thus reducing the possibility of forming dangling (i.e. unsaturated) bonds at the Si interface. The notion of doping SiO_2 with Zr or Hf also leads to a natural scaling scenario for the silicate system. By progressively increasing the Zr or Hf concentration, the k-value can be steadily increased, up to a limit, to meet the gate capacitance requirements for future technology generations.

The increased control over interface properties comes at the expense of a lower dielectric constant relative to pure ZrO_2 or HfO_2. Depending on the metal concentration, the dielectric constant is believed to scale between 4, corresponding to pure SiO_2, and approximately 15 to 20 for stoichiometric $ZrSiO_4$ or $HfSiO_4$, since pure ZrO_2 and HfO_2 are thought to have dielectric constants close to 25 and 35, respectively [54]. Si-rich compositions are preferred to maintain thermal stability with the Si substrate. Preliminary theoretical work by Jun *et al.* suggests that both $ZrSiO_4$ and $HfSiO_4$ have dielectric constants near 12, toward the lower end of the above range.

The lower dielectric constant of the silicates relative to the pure metal oxides does not necessarily imply a smaller gate capacitance. To illustrate this point, Figure 2.7 shows two possible gate stack structures. Figure 2.7(a) depicts a pure metal oxide (e.g. ZrO_2 with $k = 25$) which requires a 0.5 nm interfacial SiO_2 layer with $k = 4$. Figure 2.7(b) shows a silicate layer (e.g. Zr silicate with $k = 16$) which forms a single, uniform high-k layer in direct contact with Si. Using Equations (2.9) and (2.11), it is straightforward to show that both gate stack structures achieve the same equivalent gate capacitance, corresponding to *EOT* values of 1.0 nm. Surprisingly, the lower-k silicate layer can be physically thicker than the higher-k ZrO_2 layer, so that less tunneling is expected for the silicate stack. This is due to the fact that the silicate is believed to form a single, uniform high-k layer, thus avoiding the formation of a low-k interfacial region.

2.5 Summary

This chapter has reviewed recent trends in gate oxide scaling. The aggressive scaling requirements for upcoming technologies suggest that SiO_2 cannot be scaled beyond the 65 nm generation. The desirable properties of alternative high-*k* dielectric materials have also been described. An important consideration is that the chosen dielectric material be scalable to future technology nodes. Of the various requirements, it is likely that achieving a high quality interface with the underlying Si substrate will be the most stringent. This requirement has motivated the development of the silicate system, which is believed to form a high quality Si/SiO_2-like interface while eliminating the need for an explicit interfacial oxide layer, which limits the achievable *EOT* values of gate stacks employing pure metal oxides.

Table 2.1 Projected transistor parameters for future technology generations.

Generation (nm)	**180**	**130**	**100**	**70**	**Scaling factor**
L_{gate} (nm)	100	70	50	35	0.7x
Vdd (V)	1.5	1.2	1.0	0.8	0.8x
T_{ox}, electrical (nm)	3.1	2.5	2	1.6	0.8x
T_{ox}, physical (nm)	2.1	15	1.0	0.6	0.8x
I_{off} at 25°C (nA/μm)	20	40	80	160	2x

Table 2.2 Selected excerpts from the 2004 update of the International Technology Roadmap for Semiconductors.

Year	**2001**	**2004**	**2007**	**2010**	**2013**	**2016**
Technology Node	**130nm**	**90nm**	**65nm**	**45nm**	**32nm**	**22nm**
L_{gate} (nm)	**65**	**37**	**25**	**18**	**13**	**9**
Vdd (V)	**1.2**	**1.2**	**1.1**	**1**	**0.9**	**0.8**
$T_{ox,}$physical (nm)	**1.5**	**1.2**	**0.9**	**0.7**	**0.6**	**0.5**
Gate leakage at 100°C (μA/μm)	**0.01**	**0.17**	**0.23**	**0.33**	**1**	**1.67**

Solutions unknown

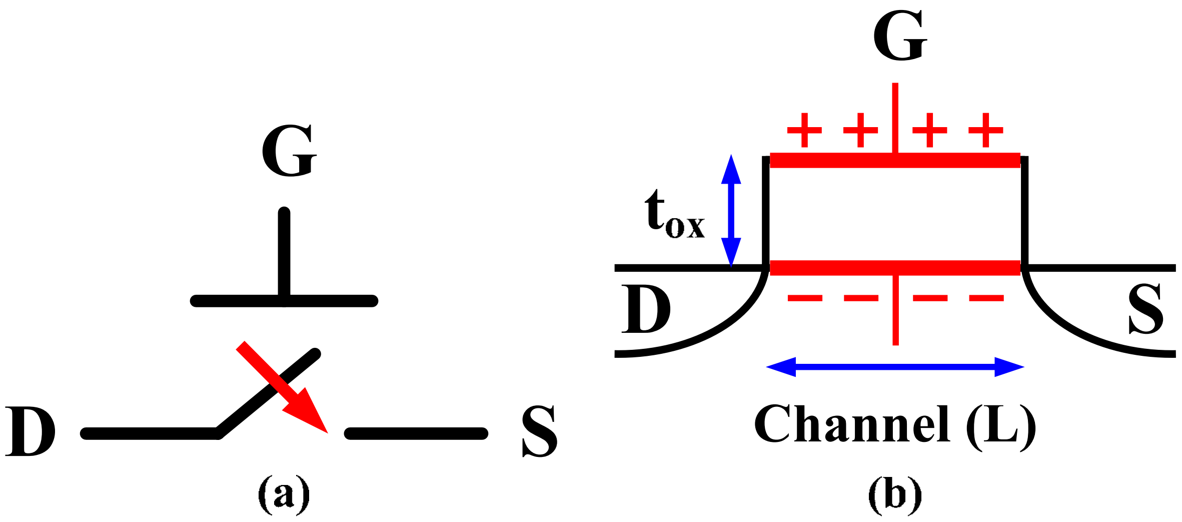


Fig. 2.1 (a) The MOSFET ideally acts as a 3-terminal switch. (b) Practical realization of the MOSFET requires a gate capacitor.

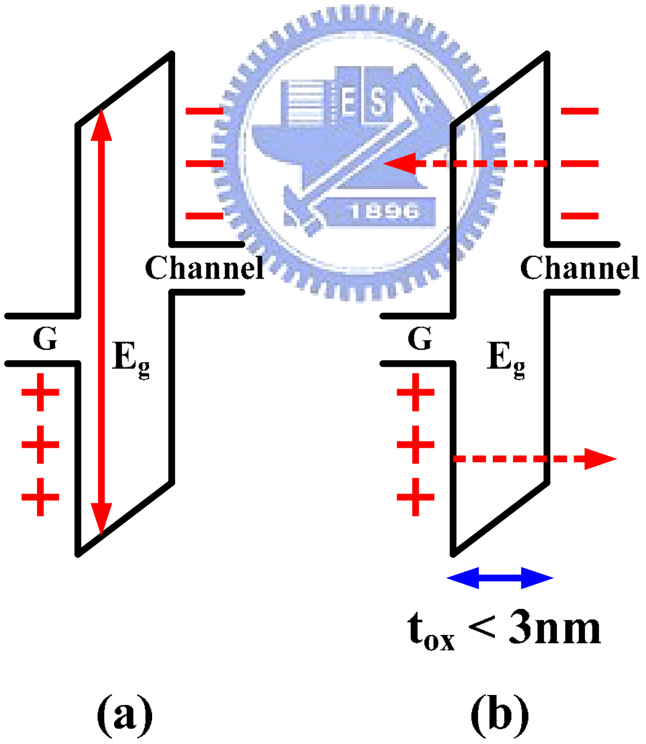


Fig. 2.2 (a) Simplified band diagram of the MOS system. (b) Direct tunneling of carriers through the insulator potential barrier can occur for thin dielectric layers.

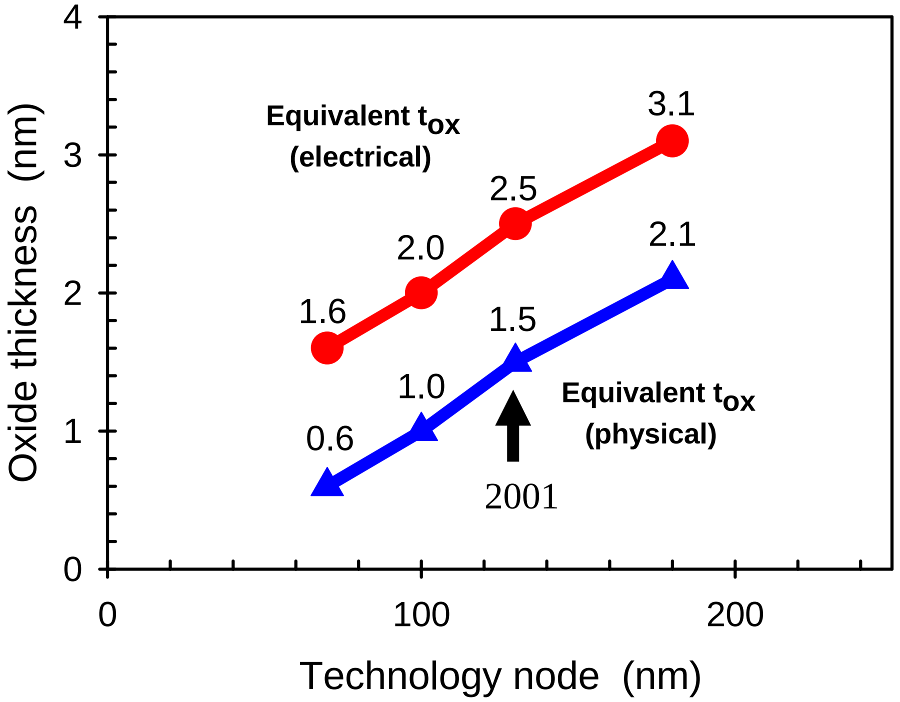


Fig. 2.3 Extrapolated gate oxide scaling trend for recent CMOS technologies.

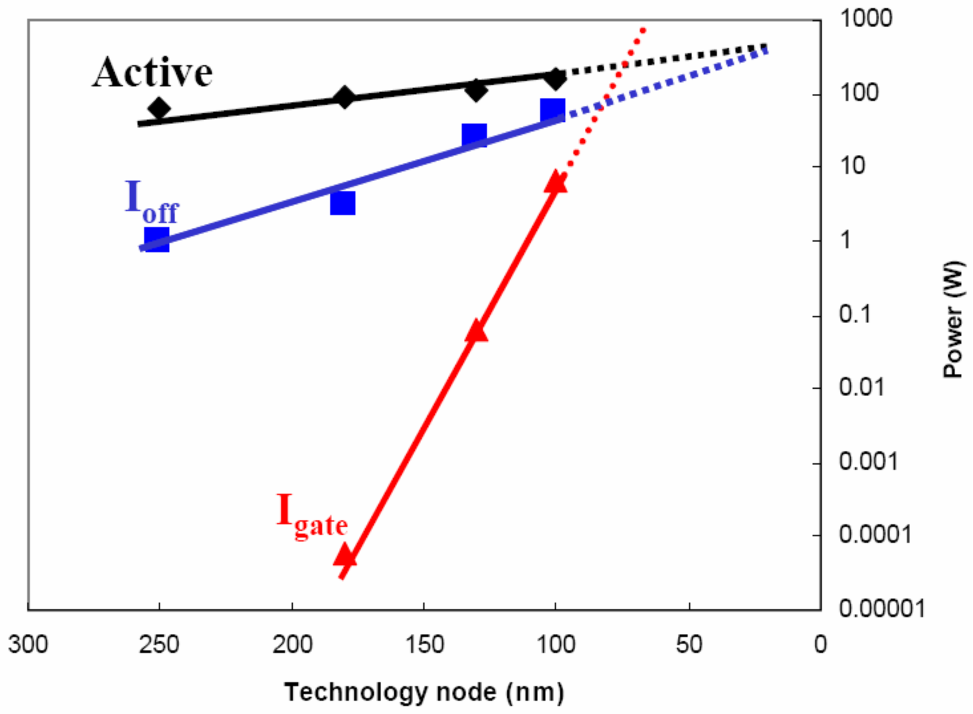


Fig. 2.4 Extrapolated trend of active and leakage power dissipation for state-of-the-art CMOS technologies.

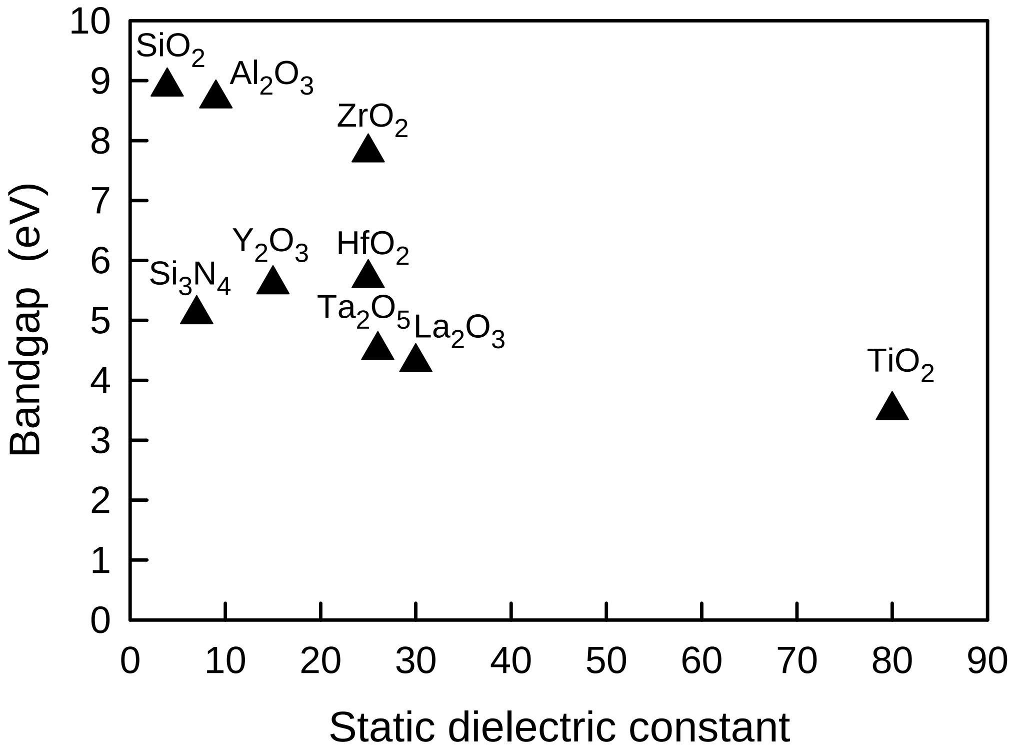


Fig. 2.5 Plot of bandgap versus static dielectric constant for representative high-*k* gate dielectric materials.

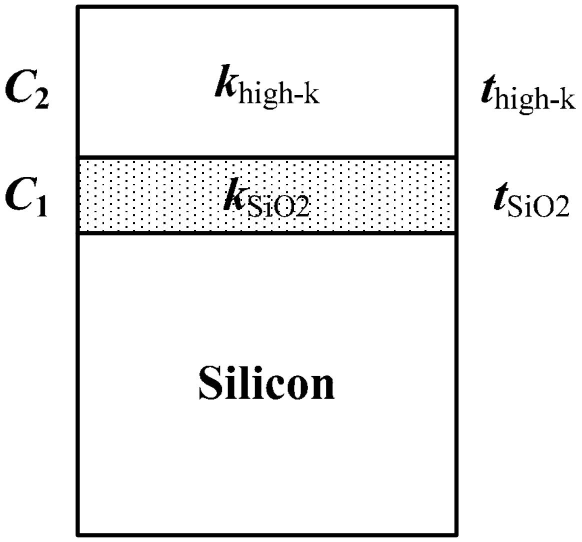


Fig. 2.6 Diagram illustrating a high-*k* gate dielectric stack with a low-*k* interfacial layer.

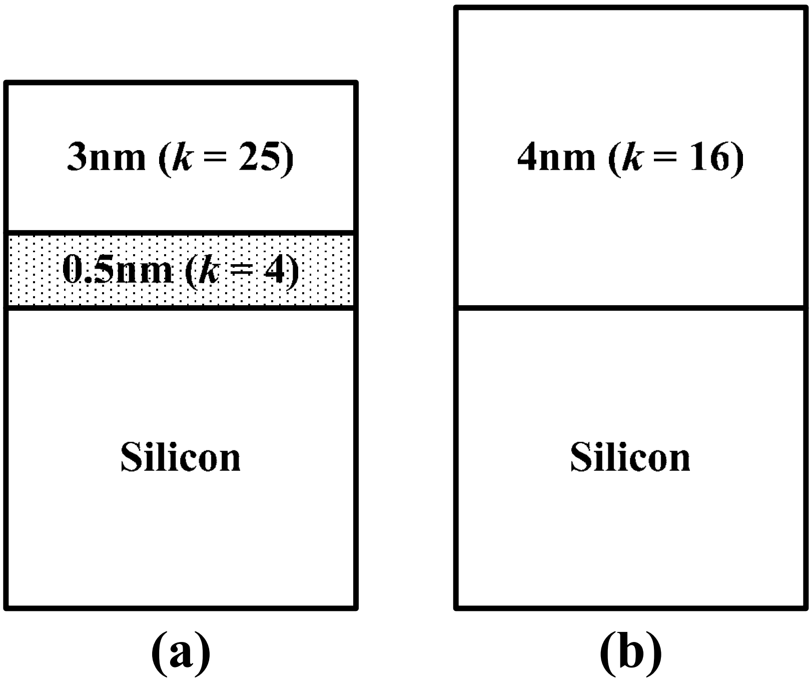


Fig. 2.7 (a) A gate dielectric stack formed of a high-k layer and a low-k interfacial layer. (b) A stack formed of a single, uniform layer with intermediate k-value. Both stacks provide 1.0 nm *EOT*.

Chapter 3

Reliability of Ultrathin Plasma Nitrided Gate Oxides for ULSI Devices

3.1 Backgrounds and Motivation

To ensure the continued shrinkage of CMOS technologies down to deep submicron regime and beyond, ultrathin gate dielectric with low defect density and high reliability is indispensable. In general, high driving capability and well-controlled short channel characteristics require the use of ultrathin gate oxides. As predicted by the ITRS, the oxide thickness (T_{ox}) needs to be less than 2.0 nm for sub-100 nm CMOS technology node. However, for MOSFETs with such ultrathin gate oxides, direct tunneling current and boron penetration through the ultrathin gate oxide will become severe issues for device integration. Numerous researches have been conducted in reducing the direct tunneling current and improving the boron penetration by incorporating nitrogen into the gate oxide or using nitride/oxide stack gate dielectric [58]. The conventional thermal nitridation processes require higher temperatures to incorporate sufficient nitrogen concentration into the gate dielectrics. However, high process temperatures make device integration more difficult as technology scales down continuously. Recently, integrated oxynitride stack [59], jet vapor deposition (JVD) nitride [60], remote plasma nitridation (RPN) and decoupled plasma nitridation (DPN) on SiO_2 [61], [62], and nitride-related candidates such as stacked N/O [63], have been considered. Both RPN and DPN processes could be possible solutions for ultrathin gate dielectric not only because it could control the concentration of nitrogen uniformly but most importantly because it has lower process temperature [64]-[66].

Device degradation by hot-carrier effects is one of the most important reliability issues for short channel MOSFETs. Device characteristics will be degraded by interface-state generation and transconductance degradation during hot-carrier stress [67]. For worse cases, hot-carrier effects may damage gate oxide to cause oxide breakdown. The stronger electric fields will exist near the drain side as device dimension has scaled down without reducing the applied voltage in order to obtain higher performance. Therefore, electrons and holes will be accelerated more easily to gain high energies. Even though the improvement of hot-carrier reliability had been investigated by nitrided oxide and stacked nitride/oxide gate dielectrics [68], nitrogen incorporation induced positive fixed oxide charges and traps will still be another considerations. Carrier injection and trapping in the gate dielectric and trans-conduction degradation by Coulomb charge scattering make the hot-carrier-induced degradation still be a significant reliability problem for devices with ultra-thin nitrided gate dielectrics [69].

In this chapter, issues relating to the reliabilities of ultrathin gate dielectrics for present and future ULSI technologies will be investigated. Gate oxide integrity including gate leakage current, time-dependent dielectric breakdown (TDDB), and evaluation of oxide reliability are comprehensively demonstrated.

3.2 Experimental Procedure

Deep submicron (0.13 μm) nMOSFETs with ultrathin gate dielectrics were used in this study. After active device area definition, conventional thermal oxides were grown at 900°C.

In order to achieve a final equivalent oxide thickness (*EOT*) of approximately 2.0 nm for all splits, thermal oxides with various starting thickness were subjected to various plasma nitridation times. After deposition and patterning of a 150 nm thick un-doped poly-Si film, arsenic dopants were implanted with energy of 5 keV to dope the gate electrode and also to form the shallow source/drain junction. For activation, all samples were annealed using rapid thermal annealing (RTA) in N_2 gas ambient for 30 sec. Subsequently, cobalt salicide, borophosphosilicate glass (BPSG), and metallization processes were performed to complete the device fabrication. The hot-carrier stress of nMOSFETs was carried out subjecting to the drain voltage of 1.8V, 2.0V, and 2.2V with the gate voltage at the condition of maximum substrate current, maximum gate current, and one-half of the drain voltage for comparison. For time-dependent reliability testing, constant positive voltage of 2.2V was applied to the gate with the source and drain grounded and the negative bias ranging from 0 V (i.e., constant voltage stress, CVS) to −2 V was applied to the substrate terminal at room temperature. Device characteristics were recorded at certain time interval for stress time up to 10^4 seconds. The indicators of reliability degradation are transconductance G_m reduction and threshold voltage V_t shift. G_m is defined as the peak value of the transconductance of a device in linear region, while threshold voltage is defined at the interception extrapolated from the peak value.

3.3 Electrical Characteristics of Plasma Nitrided Gate Oxides

Figure 3.1 shows the drain current (I_d) versus drain voltage (V_d) characteristics for (a) long channel (W/L = 10/10 μm) and (b) short channel (W/L = 10/0.13 μm) nMOSFET devices with thermal oxide (N0) and plasma nitrided oxides (with plasma treatment time of 25 sec (N1) and 50 sec (N2), respectively). The drain current is larger for the plasma nitrided devices, and is proportional to the plasma nitridation time. Figure 3.2 shows the drain current (I_d)

versus gate voltage (V_g) characteristics for (a) long channel (W/L = 10/10 μm) and (b) short channel (W/L = 10/0.13 μm) nMOSFET's with thermal oxide (N0) and plasma nitrided oxides (N1, N2). For the long channel devices, the threshold voltage of N0, N1, and N2 are 0.35, 0.32, and 0.32 V, respectively. The swing is about 72mV/dec for all three devices. For the short channel devices, however, the threshold voltage of N0, N1, and N2 are 0.43, 0.35, and 0.33 V, respectively. And the swing of N0, N1, and N2 are 79, 80, and 81mV/dec, respectively. The subthreshold current is obviously larger for the devices with plasma nitrided oxide than that with thermal oxide. Drain induced barrier lowering (DIBL) effect is also observed in the deep submicron devices. For the sake of distinction, Figure 3.2 was re-plotted in Figure 3.3 as a function of the effective gate drive ($V_g - V_t$). The transconductance characteristics corresponding to Figure 3.2 were shown in Figure 3.4. The product of transconductance and oxide thickness ($G_m * T_{ox}$) corresponding to Figure 3.4 were also shown in Figure 3.5. The value for the device with thermal oxide is larger than that for the plasma nitrided ones, which implies the mobility is larger for the device with thermal oxide than that with plasma nitrided ones.

3.4 Channel Hot Carrier Degradation

For nMOSFETs electrons flowing through the high field region in the depletion region near the drain side will obtain sufficient energy to cause impact ionization process and electron-hole pairs are generated, then more hot carriers will be created. Meanwhile, holes will flow toward substrate to be substrate current I_{sub}. In order to monitor the hot-carrier effects for nMOSFETs, devices will be stressed at maximum substrate current ($I_{sub,max}$) and that indicates the most efficient generation of hot carriers [70], [71]. In order to monitor the aging situation, the variation of the maximum transconductance $G_{m,max}$, the threshold voltage

V_t, and the forward-mode drain current I_d were measured at $V_d = 0.05$ V. The stressing experiments were interrupted periodically to measure the degradation monitors by using a Keithley Model 4200-SCS Semiconductor Characterization System. Figure 3.6 shows the comparison of the stress time dependence of $G_{m,max}$ degradation ($\Delta G_{m,max}/G_{m,max}$) among devices stressed at $V_g = I_{sub,max}$ on a double log scale ($\Delta G_{m,max} = (G_{m,max}(t) - G_{m,max}(0)) < 0$). Figure 3.6(a), (b), and (c) are corresponding to the device under the stressing drain voltage V_d = 1.8, 2.0, and 2.2 V, respectively. It can be seen that the device N0 exhibits less degradation than the other two devices N1 and N2, although different stressing voltages were applied. And larger degradation is expected with higher stressing voltage. In general, the $G_{m,max}$ in the linear region is found to be decreased as a result of the carrier mobility degradation, which is associated with the generated interface traps.

The stressing gate voltage at maximum substrate current is roughly two-third of the stressing drain voltage. Specifically, for stressing condition V_d = 1.8 V, the stressing V_g of 1.34, 1.28, and 1.30 V were evaluated for N0, N1, and N2, respectively. For stressing condition V_d = 2.0 V, the stressing V_g of 1.44, 1.28, and 1.26 V were evaluated for N0, N1, and N2, respectively. And for stressing condition V_d = 2.2 V, the stressing V_g of 1.62, 1.44, and 1.56 V were evaluated for N0, N1, and N2, respectively. These V_g values were evaluated through substrate current curves as a function of gate voltage as stressing drain voltage kept constant. Figure 3.7 depicts the typical substrate current curve at drain voltage of 1.8 V. The substrate current curve behaves nearly the same level at higher voltage range ($V_g \geq V_d / 2$). This is different from the conventional devices where the peak of the substrate current is obvious and the voltage of the peak is roughly one-half of V_d. Therefore, the further measurements were conducted with the stressing condition of $V_g = V_d / 2$ and $V_g = V_d$. The results were sketched in Figure 3.8(a) and (b). In Figure 3.9, the transconductance degradation of the devices with different stressing gate voltages of 0.9, 1.3, and 1.8 V at stressing drain voltage of 1.8 V were compared. The larger degradation occurred at $V_g = V_d$, rather than $V_g = I_{sub,max}$ or V_d / 2. Such consequence implies the degradation process was mainly determined by the stressing voltage level applied on the nodes, but not determined by maximum substrate current.

Threshold voltage (V_t) shift is another indicator of hot carrier degradation. V_t shift after stressing mainly results from the charges injected into the volume of the gate oxide, which may serve as the fixed oxide charges and may shift the flat-band voltage. Interface traps exert some influences on V_t shift as well. The created interface traps are apt to lie in the upper half of the bandgap in nMOSFETs, resulting in reduced channel carriers and increased channel series resistance, and thus positive V_t shift. The interface degradation has been proven to be related to hydrogen and to the basic passivation process which involves a silicon-hydrogen bond at the silicon/silicon dioxide (Si/SiO_2) interface [71]-[74]

$$\equiv \text{Si-H} + \text{hot carrier} \rightarrow \equiv \text{Si}^* + \text{H}. \tag{3.1}$$

The asterisk signifies a dangling bond that can subsequently capture an electron and become negatively charged [75]. The positive threshold voltage shift associated with nMOSFET degradation is caused by structural changes involving hydrogen, most probably those described by (3.1). As corresponding to the $G_{m,max}$ degradation in Figure 3.6, Figure 3.10 compares the threshold voltage shift ΔV_t of devices N0, N1, and N2 as a function of the stress time ($\Delta V_t > 0$). Similar tendency correlated to stressing voltage can be observed in these figures. Figure 3.11 also shows the threshold voltage shift data corresponding to the $G_{m,max}$ degradation in Figure 3.8. The measurement results sketched in Figure 3.12 compares the threshold voltage shift of the devices with different stressing gate voltages of 0.9, 1.3, and 1.8 V as stressing drain voltage kept at 1.8 V. Figure 3.13 shows the I_d-V_g characteristics of device N2 before and after 10,000 sec stressing at V_d = 1.8V, V_g = 0.9, 1.3, and 1.8V. It can be seen clearly that higher gate voltage leads to larger threshold voltage shift.

3.5 Enhanced Negative Substrate Bias Degradation

For MOSFETs employing ultrathin gate oxide, the introduction of nitrogen into gate dielectric is known to cause enhanced degradation in negative bias temperature instability (NBTI) for pMOSFETs [76]. For nMOSFETs, however, less significant impact of plasma nitridation on device reliability was commonly reported [77]. In this work, we report, for the first time, that by subjecting the device to substrate hot electron stress [78], nMOSFETs with ultrathin plasma nitrided gate oxide (~ 2.0 nm) suffer an enhanced reliability degradation, compared to the device with conventional thermal oxide in terms of V_t shift and G_m reduction. The enhanced degradation under negative substrate bias is believed to be due to a higher level of paramagnetic electron trap precursors in the gate dielectric created by the plasma nitridation process [79].

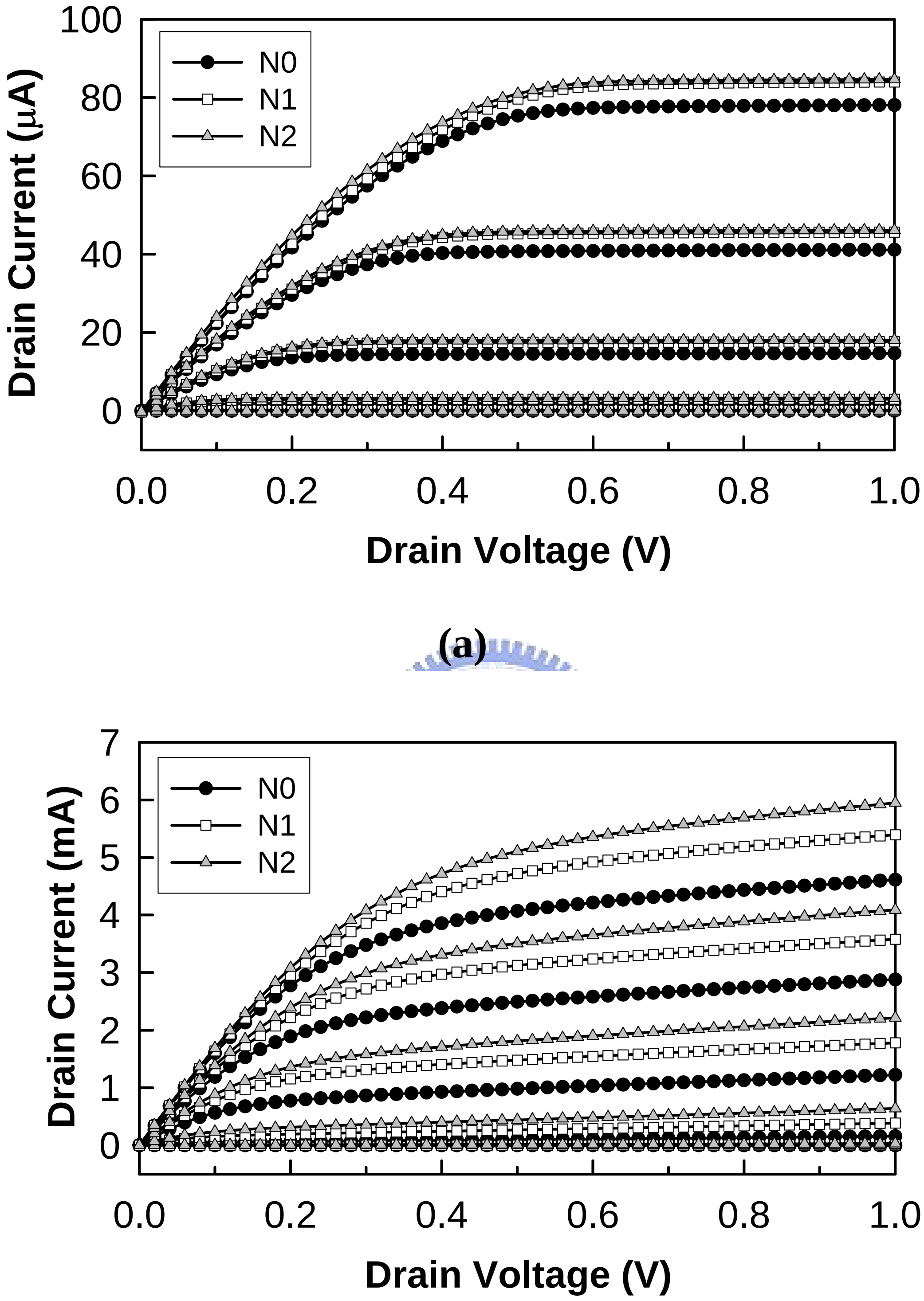
Figure 3.14 and Figure 3.15 compare the stress time dependence of the relative transconductance degradation and threshold voltage shift for the devices subjected to $V_b = 0$ V and $V_b = -2$ V with the gate voltage kept constant of 1.8 V. Both the transconductance and the threshold voltage show little changes under the stress condition of $V_b = 0$ V. After raising the substrate bias from 0 V to –2 V, some degradation of transconductance and threshold voltage shift were observed. However, the curves behave large vibration and the degradation values seem not so distinct. Therefore, similar measurement with higher stressing gate voltage of 2.2 V was employed in order to make more pronounced data. Figure 3.16(a) and (b) depicts the stress time dependence of the transconductance degradation and threshold voltage shift, respectively, for $V_g = 2.2$ V and $V_b = 0$ V (constant voltage stress). Only slightly larger values were observed in the stressing gate voltage of 2.2 V comparing with those in the stressing gate voltage of 1.8 V. Figure 3.17(a), (b), and (c) shows the transconductance degradation, threshold voltage shift, and drain current degradation, respectively, as a function of stress time subjected to $V_g = 2.2$ V and $V_b = -2$ V. It is noticeable that distinct different slope can be seen between the devices with thermal oxide (N0) and nitrided oxide (N1 and N2).

For the sake of ease of comparison, the relative transconductance reduction and threshold voltage shift as a function of stress time are re-plotted in Figure 3.18(a) and (b), respectively. Two substrate biases, i.e., 0 V and −2 V, were employed for comparison. For zero substrate bias, e.g., constant gate voltage stress (CVS), only negligible degradations were observed for all splits, irrespective of the gate dielectric preparation processes. When the magnitude of the substrate bias is raised to −2 V, the device with conventional thermal oxide remains stable and depicts only slight degradations in both G_m and V_t. In contrast, significant G_m reduction and V_t shift are observed for the nitrided devices. The extent of damage increases for samples with longer nitridation time (i.e., 50 sec compared to 25 sec). Figure 3.19 depicts threshold voltage shifts as a function of substrate bias for different splits. Under low substrate bias, only slightly larger threshold voltage shift is observed for the splits with plasma-nitrided oxides. This trend remains unchanged until the magnitude of the substrate bias reaches −1 V, where a dramatic increase in threshold voltage shift occurs for nitrided samples, independent of the incorporated nitrogen content. In contrast, the magnitude of the threshold substrate bias needed for inducing significant V_t shift for the sample with thermal oxide is 0.5 V larger (i.e., at a substrate bias of −1.5 V). Figure 3.20 shows the relative gate current changes for different samples over stress time with a substrate bias of −2 V. A larger electron trapping density can be seen for samples with plasma-nitridation, and increases with increased plasma treatment time.

A plausible cause of the observed exacerbated degradation is plasma-induced damage during nitridation. But, it is ruled out because only insignificant and bias-insensitive degradation has been found at low substrate bias regime, which obviously contradicts with the fact that plasma-induced “latent” defects can be easily re-triggered even under traditional constant voltage stress, i.e., $V_b = 0$ V [80]. As well known, trap filling of the as-fabricated defects in plasma-nitrided oxide, which were speculated to be located near valence band [81], could account for the slightly larger V_t shift in the low substrate bias range. However, trap filling rate should not increase with the increasing energy of the transport carriers. Therefore, we hypothesize that nitrogen incorporation in the thermal oxide by plasma nitridation could introduce more precursors of paramagnetic electron traps into oxide bulk. These precursors (e.g., $\equiv Si_2NH$ or $\equiv Si_2N\text{-}NSi_2\equiv$) can be more easily broken, compared to the dominant precursors ($\equiv$Si-O-O-Si$\equiv$) in thermal oxide, and become paramagnetic electron trap centers after hot electron stress. This explains the substrate-bias-dependent threshold voltage shift, since energy is needed to activate the bond breaking reaction [79].

3.6 Conclusions

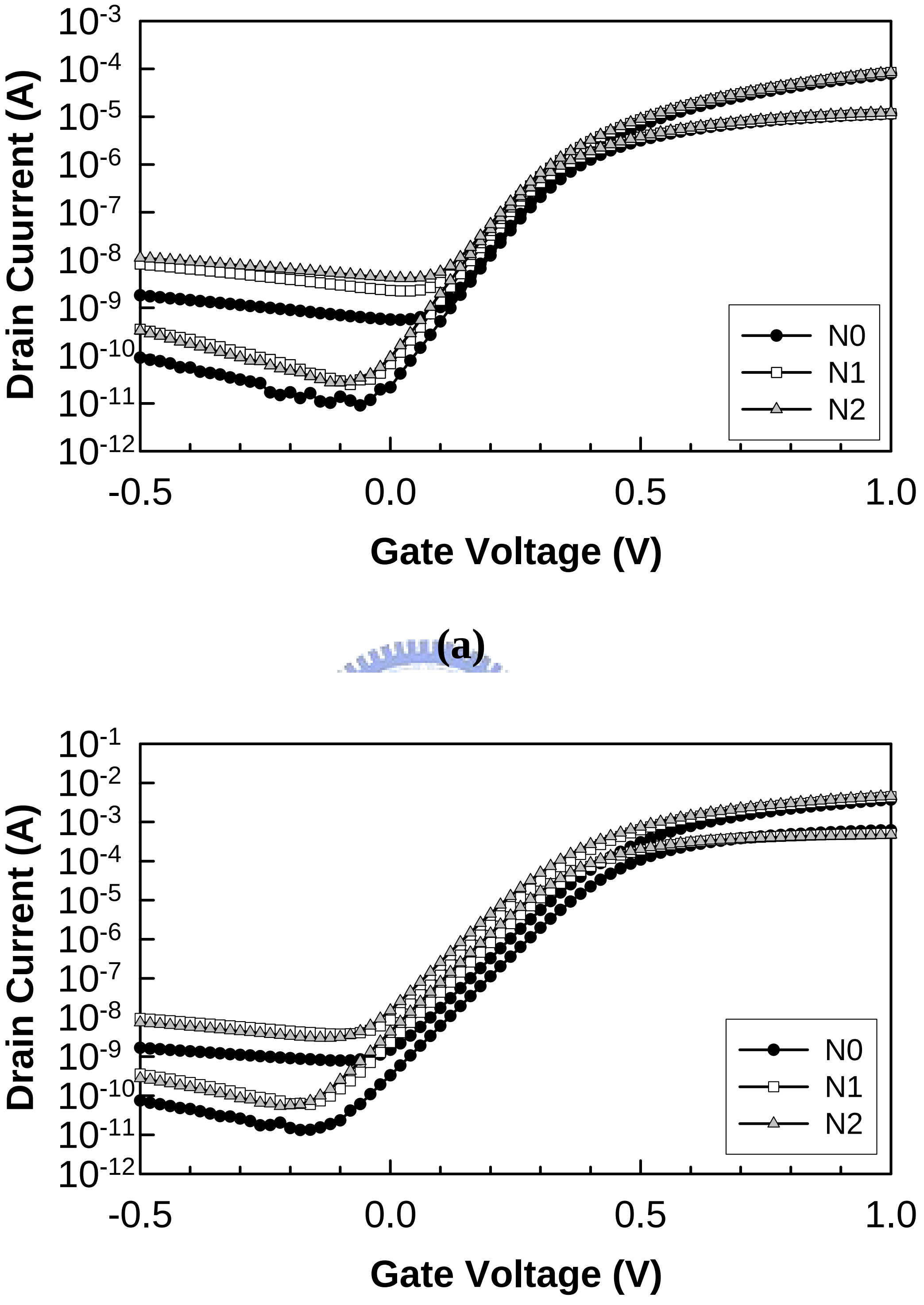
The hot carrier injection reliability of nMOSFET’s with ultrathin plasma nitrided gate oxide is investigated in this chapter. The devices with plasma nitrided oxide suffer more transconductance reduction and threshold voltage shift. The degradation is direct proportional to the plasma nitridation time. For channel hot-carrier stressing, the most efficient stressing condition is located at $V_g = V_d$, rather than maximum substrate current or $V_g = V_d / 2$ which is often utilized for traditional nMOSFETs. For substrate hot-carrier stressing, the raising of substrate voltage can enhance the device degradation considerably. We report, for the first time, an enhanced degradation under negative substrate bias in nMOSFETs with ultrathin plasma nitrided gate dielectric. The enhanced degradation is attributed to the introduction of paramagnetic electron trap precursors during plasma nitridation. Similar to NBTI in pMOSFETs, our findings are important for nMOSFETs from the reliability point of view. Even though the incorporation of nitrogen into thermal oxide is advantageous in many respects, our findings suggest that careful attentions need to be paid to ensure that plasma-nitrided gate dielectric meets the reliability requirements for the sub-100nm device technology node.



(a)

(b)

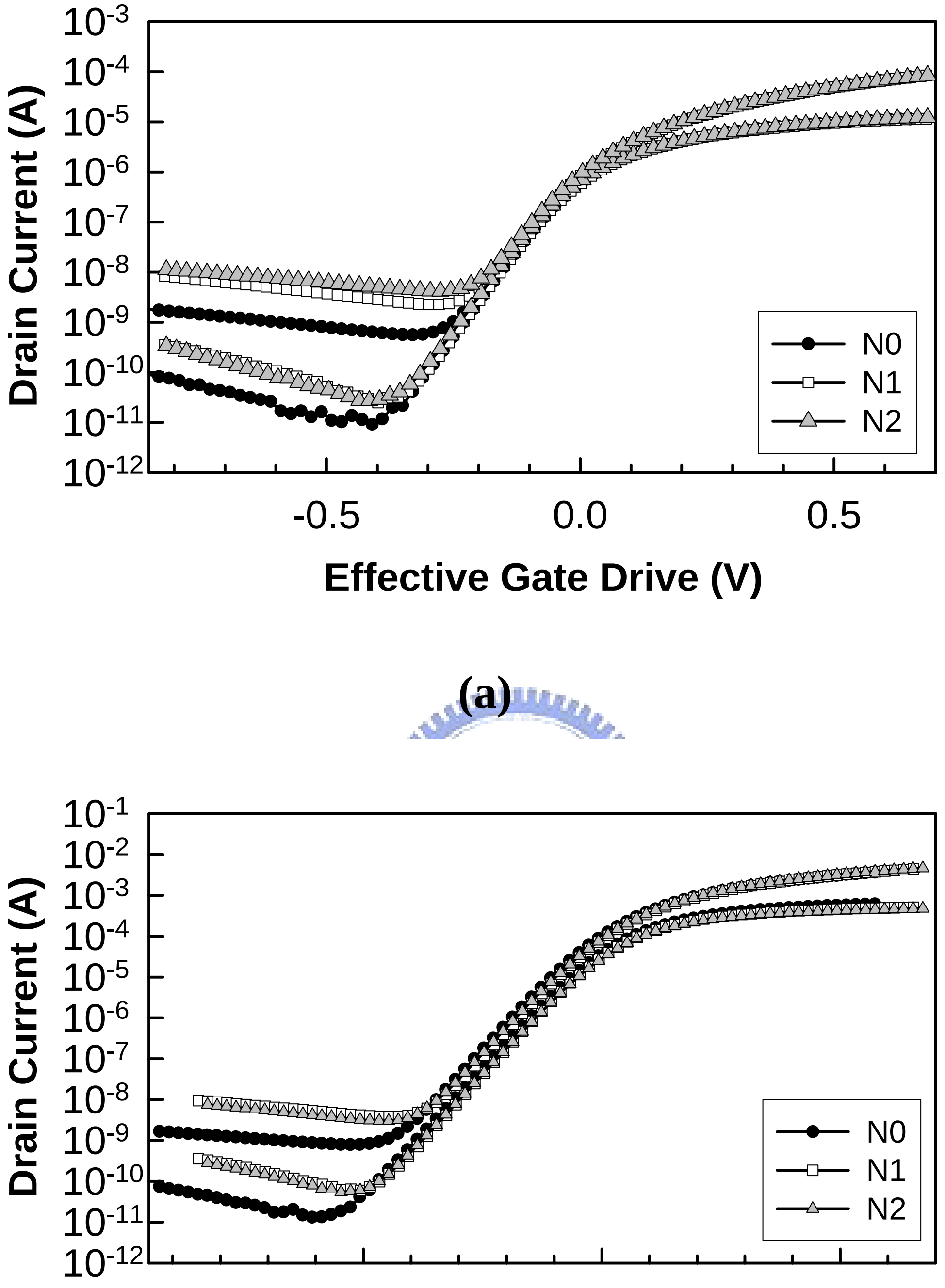
Fig. 3.1 Typical I_d-V_d characteristics for (a) long channel (*W/L* = 10/10 μm) and (b) deep submicron (*W/L* = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).



(a)

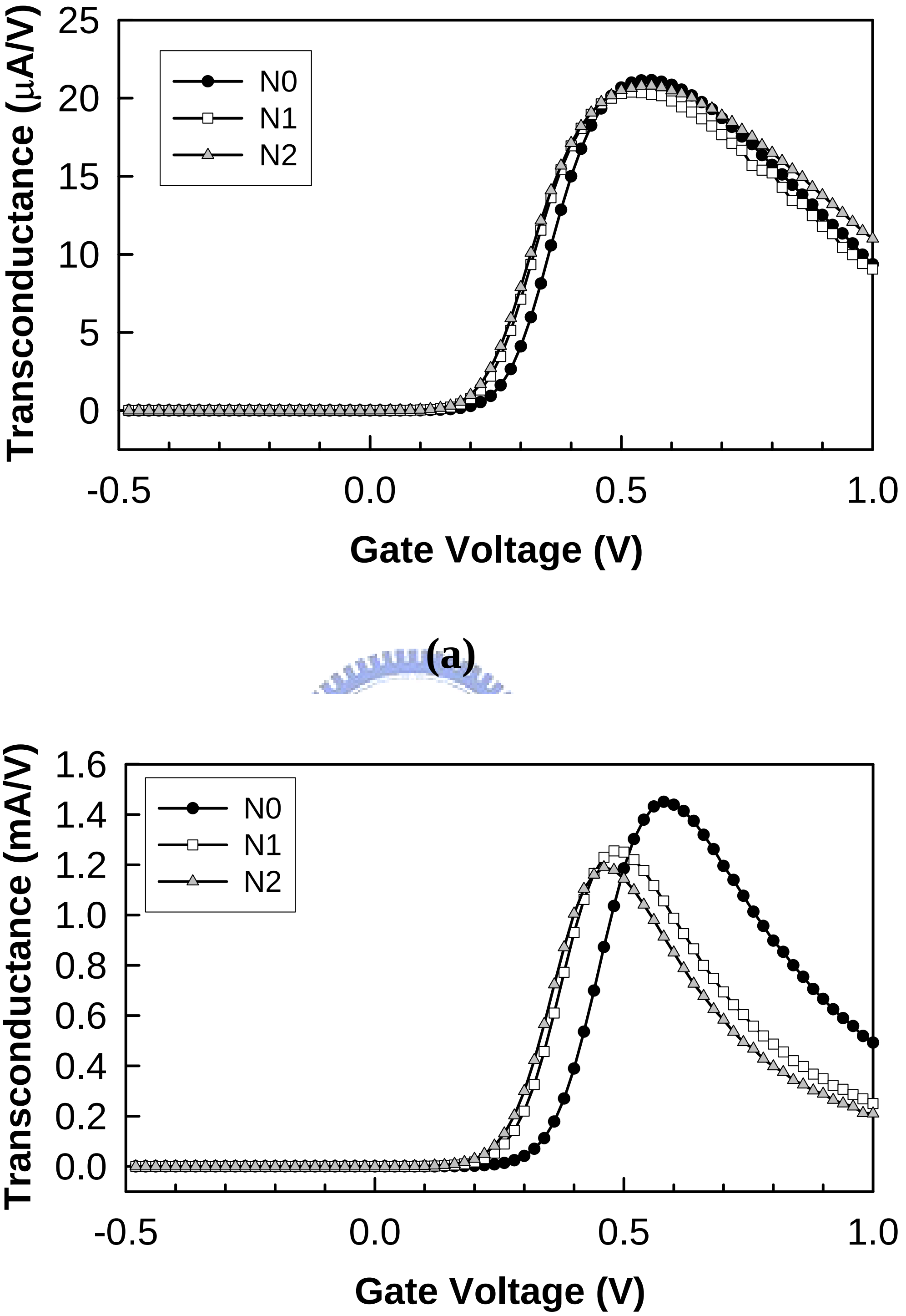
(b)

Fig. 3.2 Typical I_d-V_g characteristics for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).



(b)

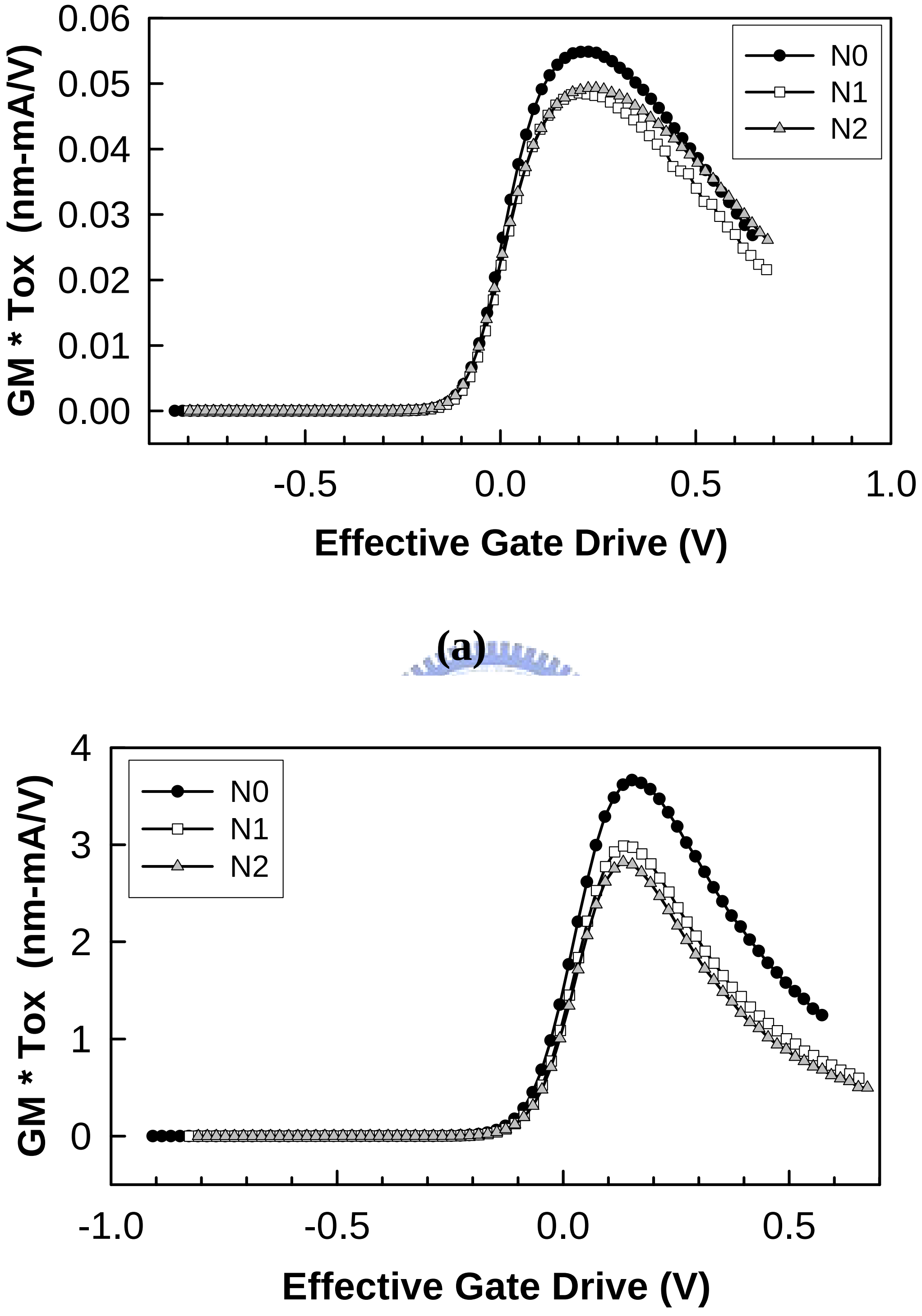
Fig. 3.3 Drain current (I_d) as a function of effective gate drive ($V_g - V_t$) for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).



(a)

(b)

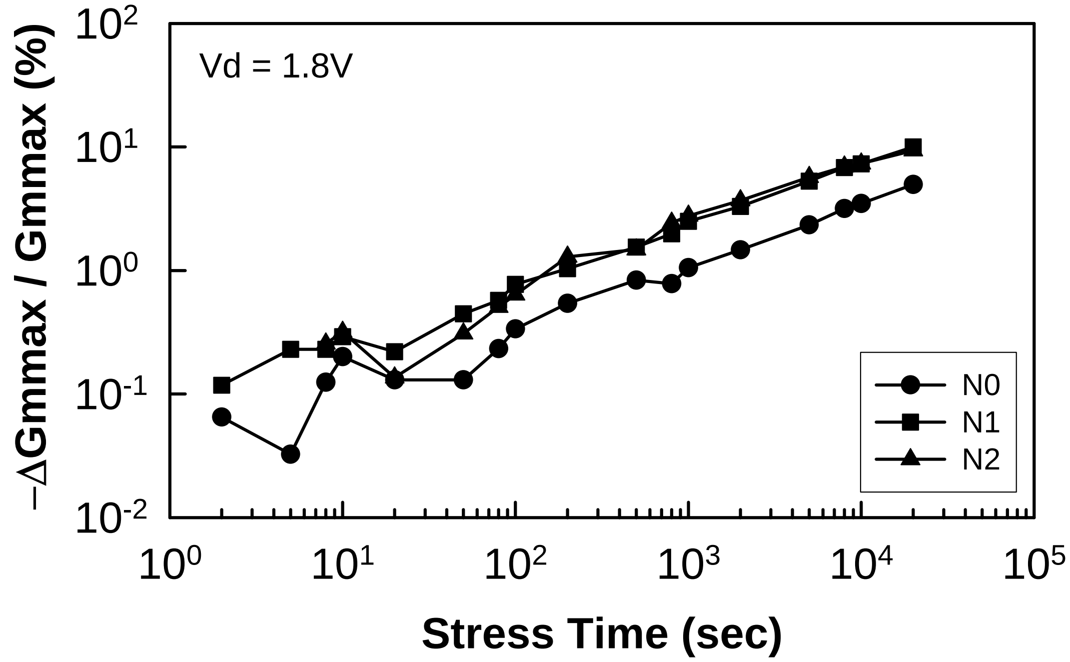
Fig. 3.4 G_m-V_g characteristics for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).



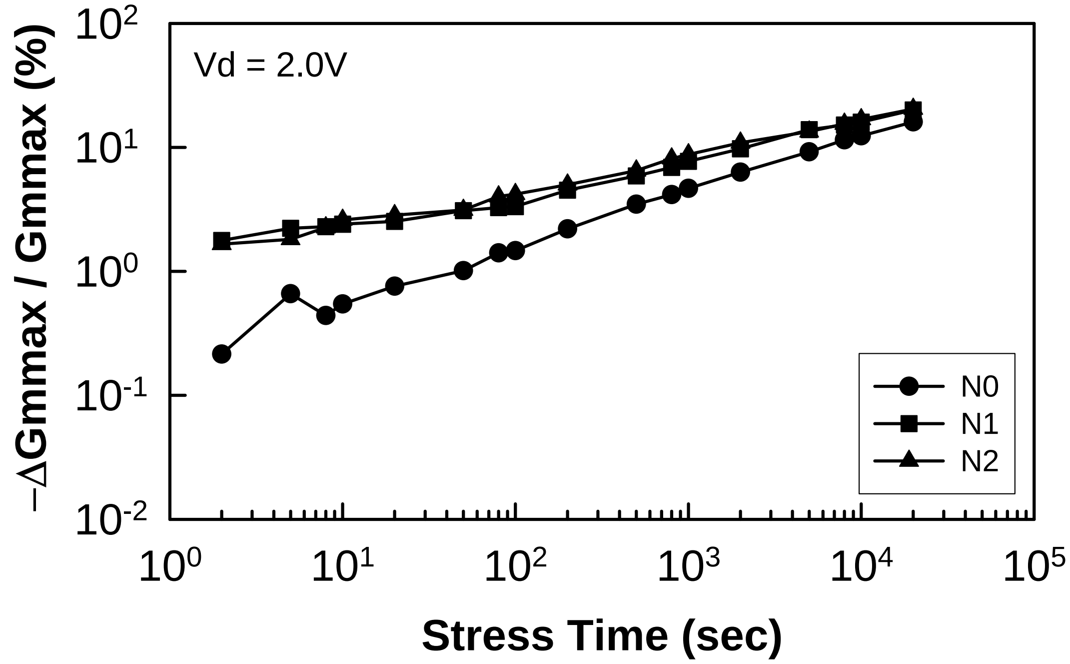
(a)

(b)

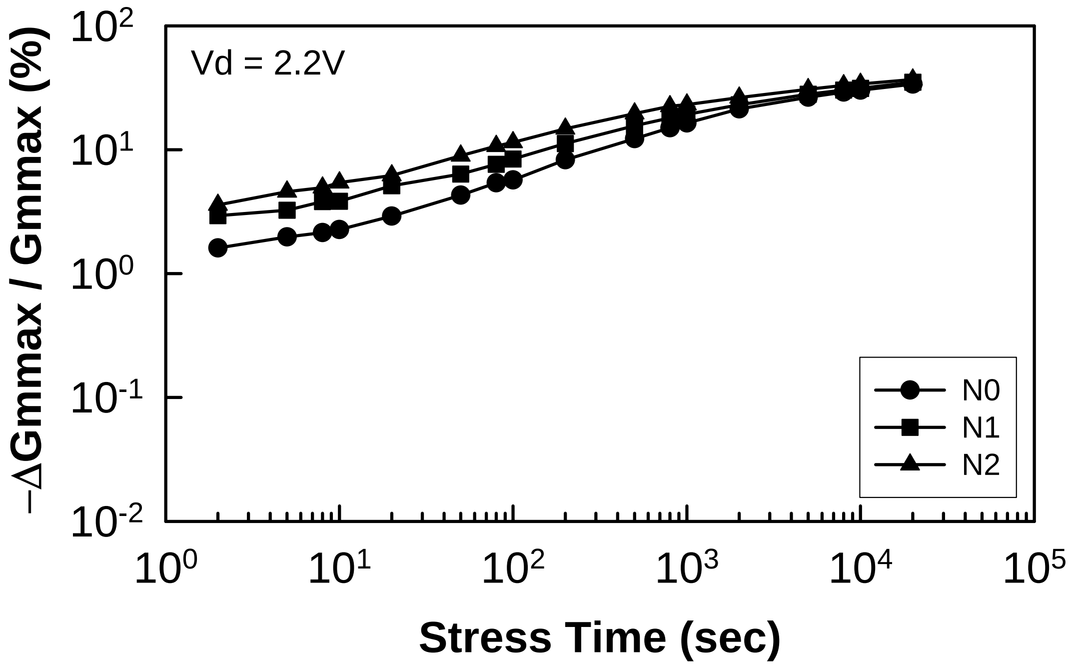
Fig. 3.5 $G_m * T_{ox}$ as a function of effective gate drive ($V_g - V_t$) for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).


Vd = 1.8V
−ΔGmmax / Gmmax (%)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{0}
10^{1}
10^{2}
10^{3}
10^{4}
10^{5}
Stress Time (sec)
N0
N1
N2

(a)


Vd = 2.0V
−ΔGmmax / Gmmax (%)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{0}
10^{1}
10^{2}
10^{3}
10^{4}
10^{5}
Stress Time (sec)
N0
N1
N2

(b)



(c)

Fig. 3.6 Stress time dependence of $G_{m,max}$ degradation ($\Delta G_{m,max}$ / $G_{m,max}(0)$) in devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) at (a) V_d = 1.8V, V_g = $I_{sub,max}$, (b) V_d = 2.0V, V_g = $I_{sub,max}$, and (c) V_d = 2.2V, V_g = $I_{sub,max}$.

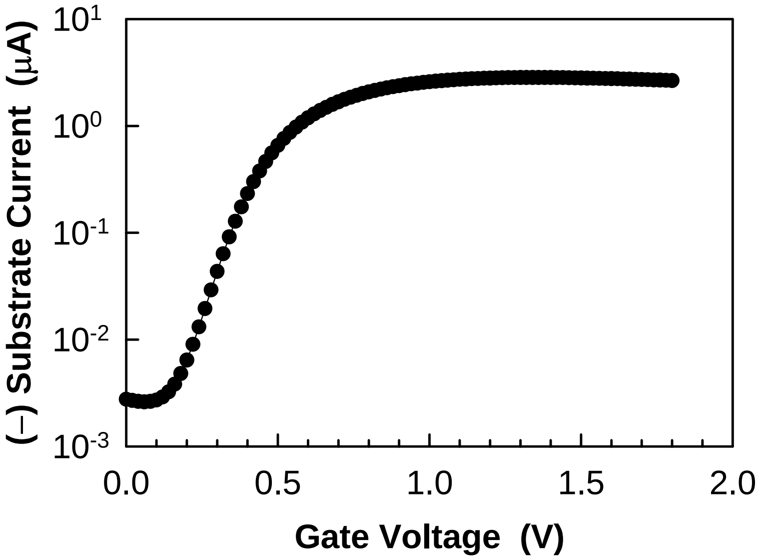


Fig. 3.7 Typical substrate current curve as a function of gate voltage to estimate the stressing condition.

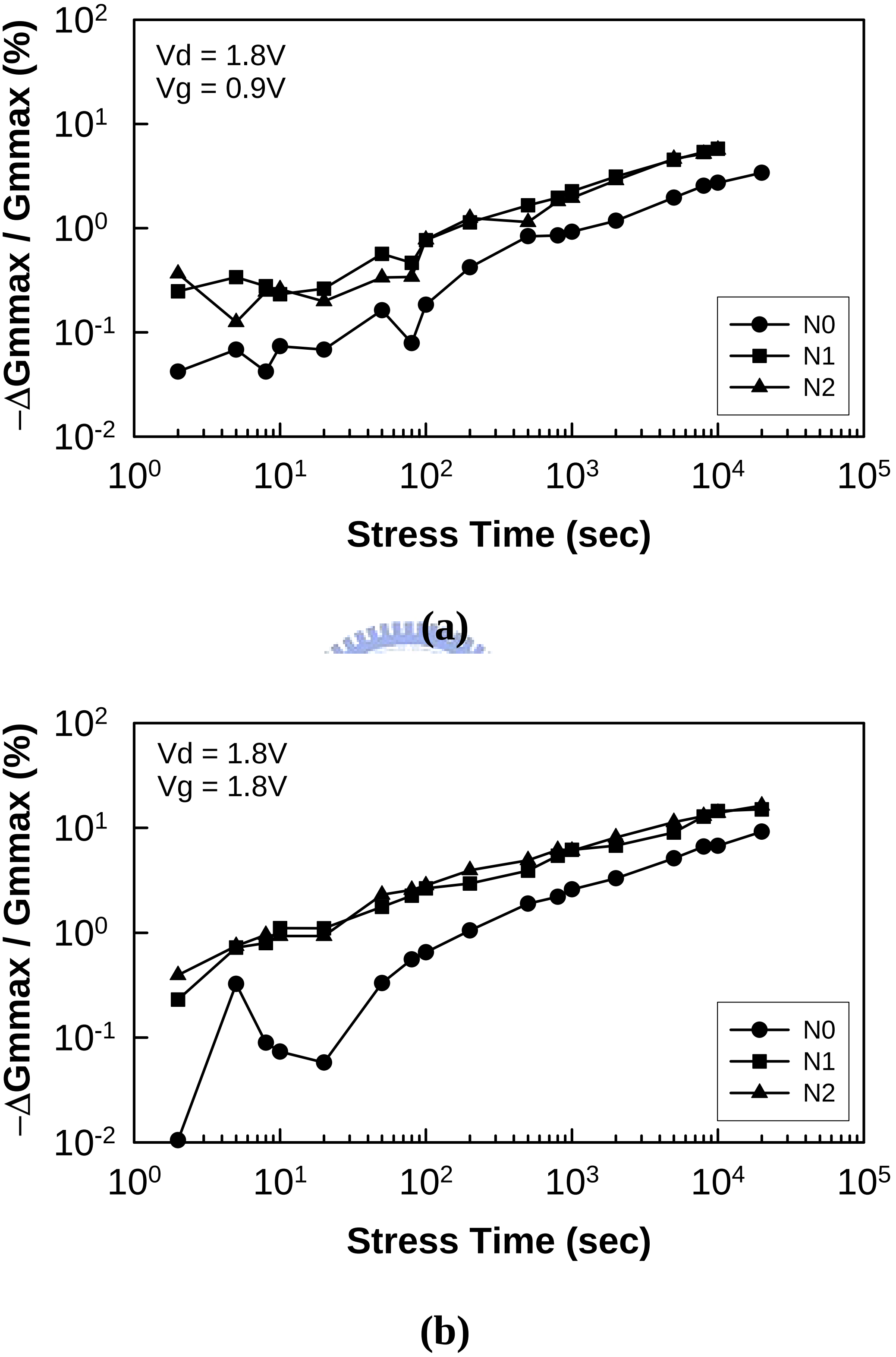


Fig. 3.8 Stress time dependence of $G_{m,max}$ degradation ($\Delta G_{m,max}$ / $G_{m,max}$ (0)) in devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) at (a) V_d = 1.8V, V_g = 0.9V and (b) $V_d = V_g$ = 1.8V.

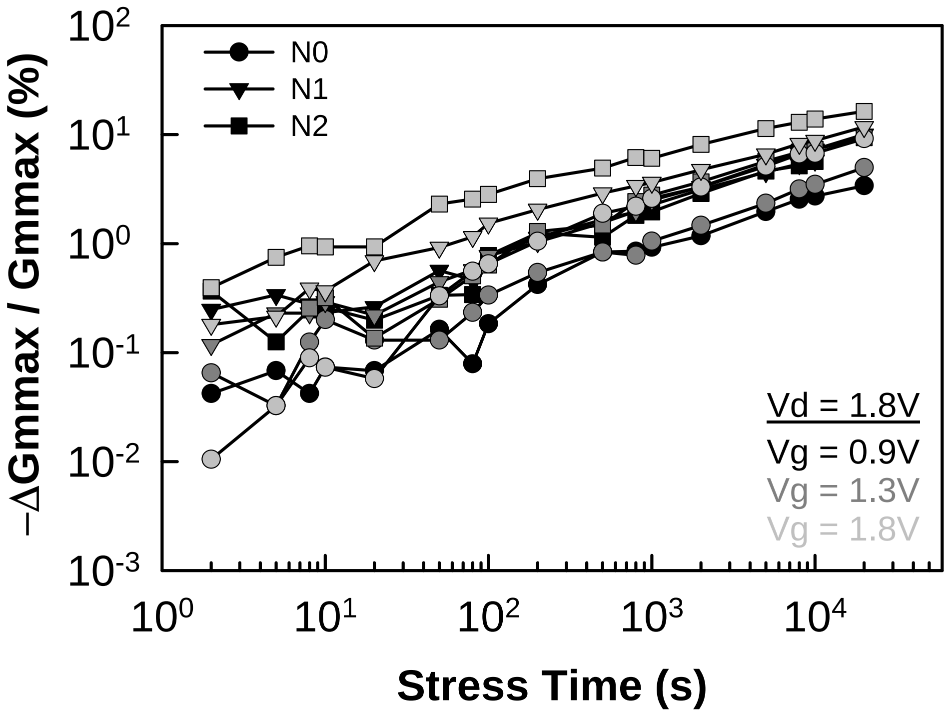
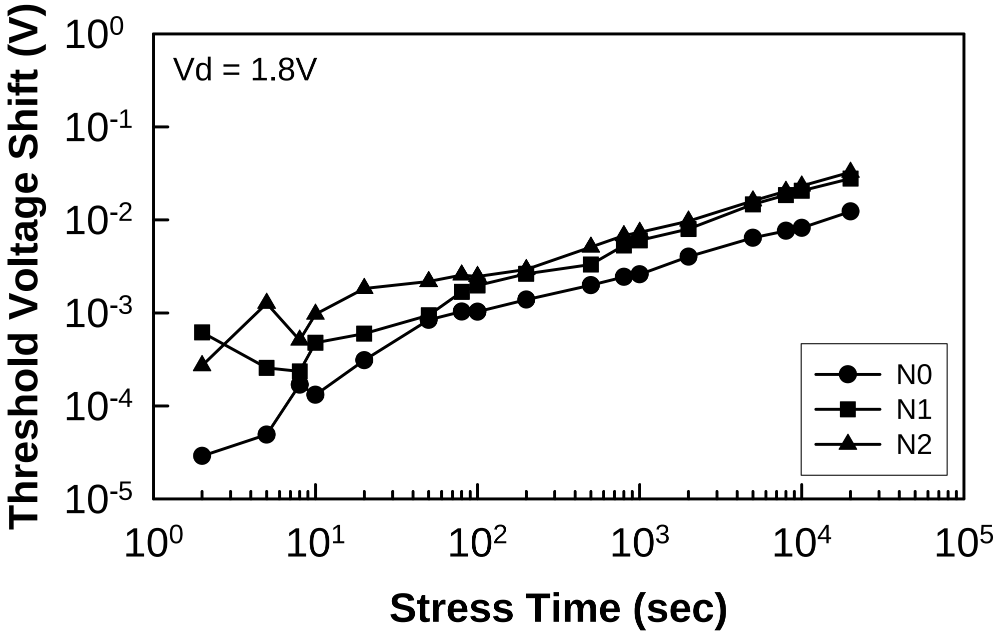
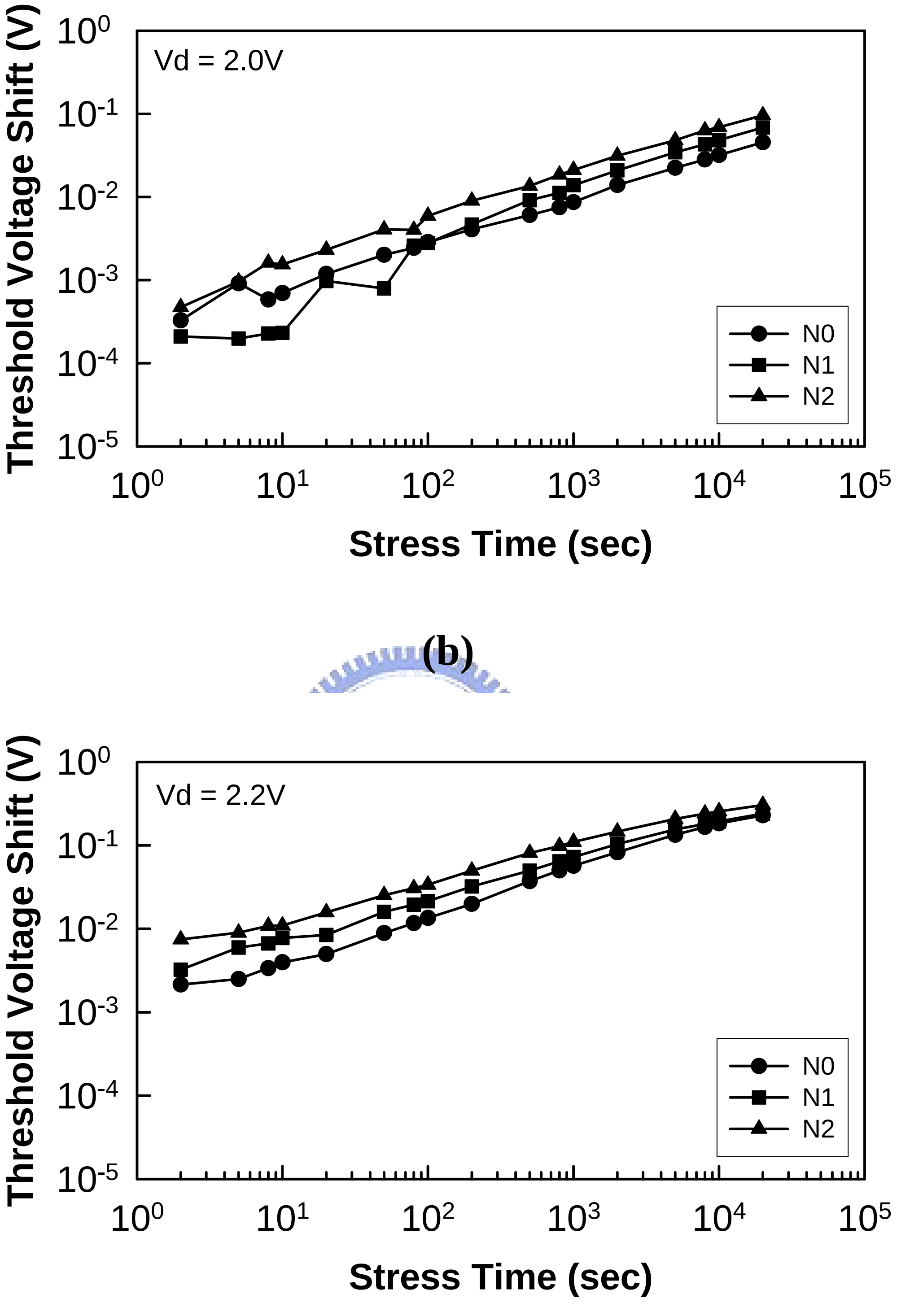


Fig. 3.9 Stress time dependence of $G_{m,max}$ degradation ($\Delta G_{m,max}$ / $G_{m,max}$ (0)) in devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) at V_d = 1.8V and V_g = 0.9, 1.3, and 1.8V.



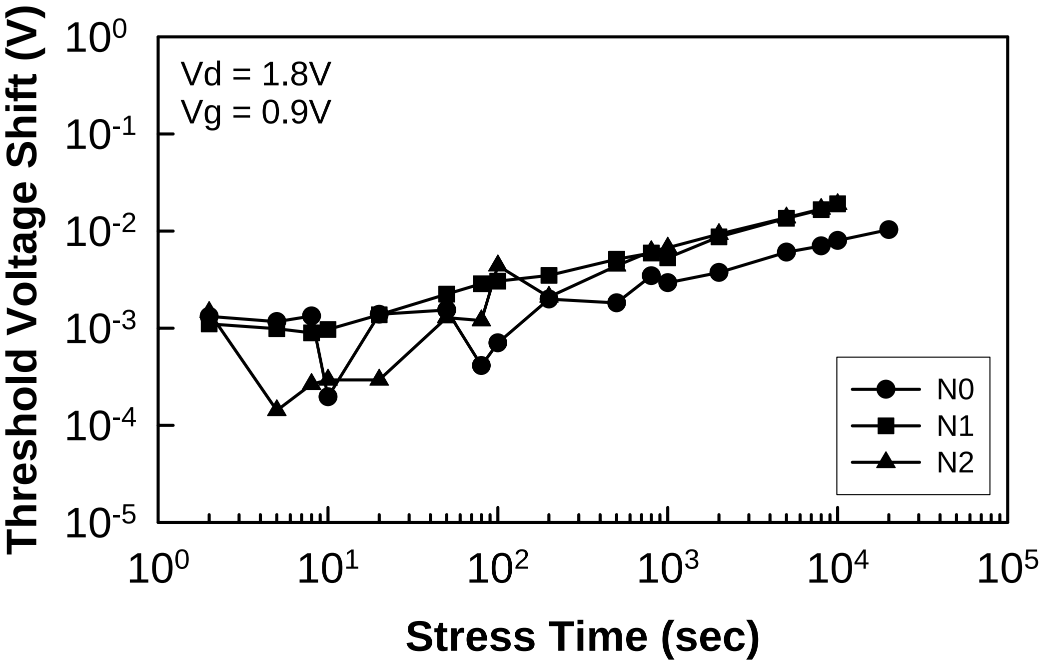
(a)



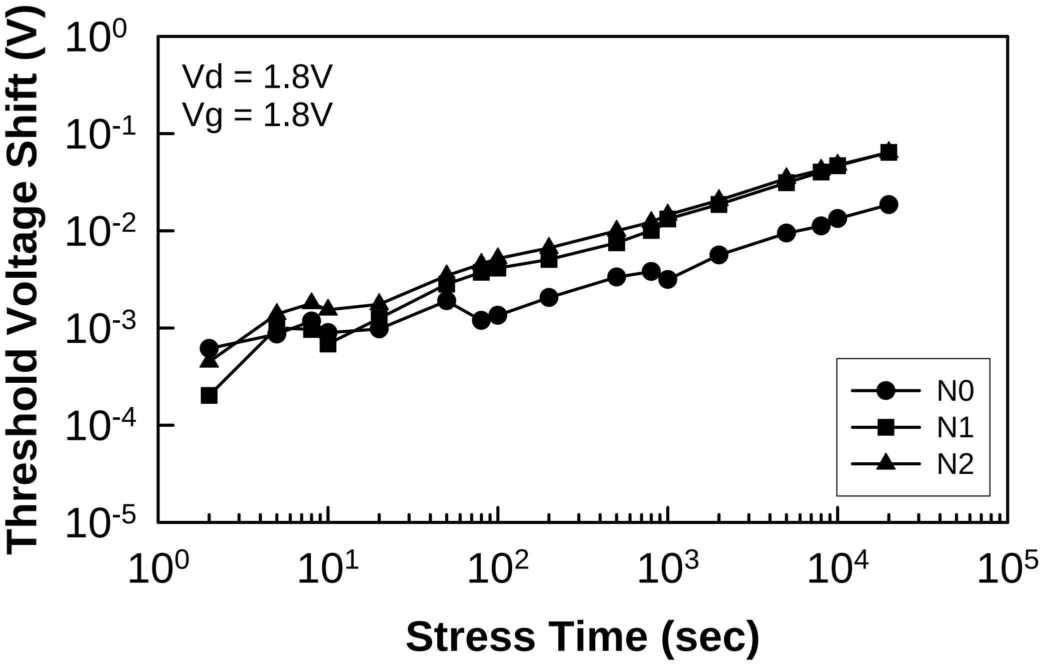
(b)

(c)

Fig. 3.10 Threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time at (a) V_d = 1.8V, $V_g = I_{sub,max}$, (b) V_d = 2.0V, $V_g = I_{sub,max}$, and (c) V_d = 2.2V, $V_g = I_{sub,max}$.



(a)



(b)

Fig. 3.11 Threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time at (a) V_d = 1.8V, V_g = 0.9V and (b) $V_d = V_g$ = 1.8V.

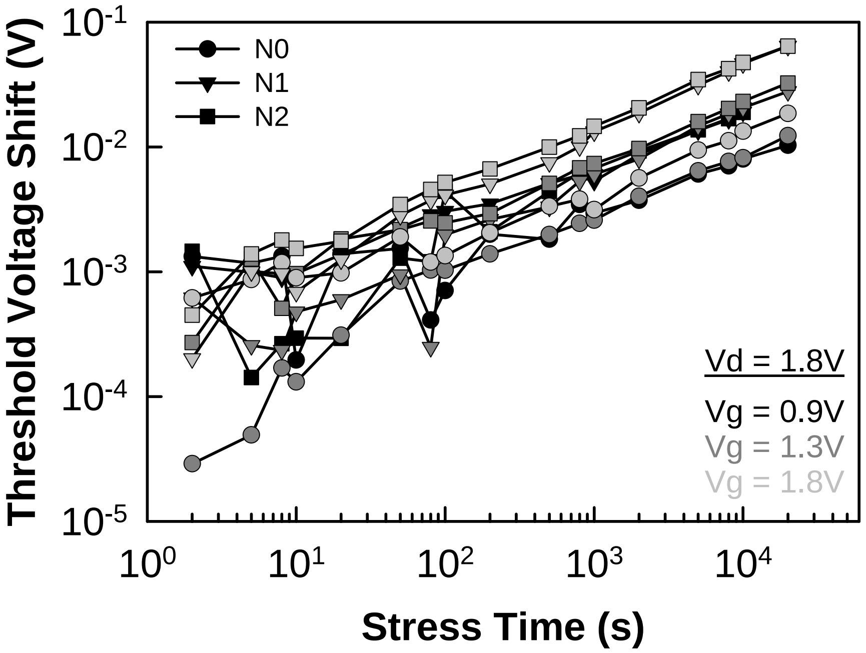


Fig. 3.12 Threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time at V_d = 1.8V and V_g = 0.9, 1.3, and 1.8V.

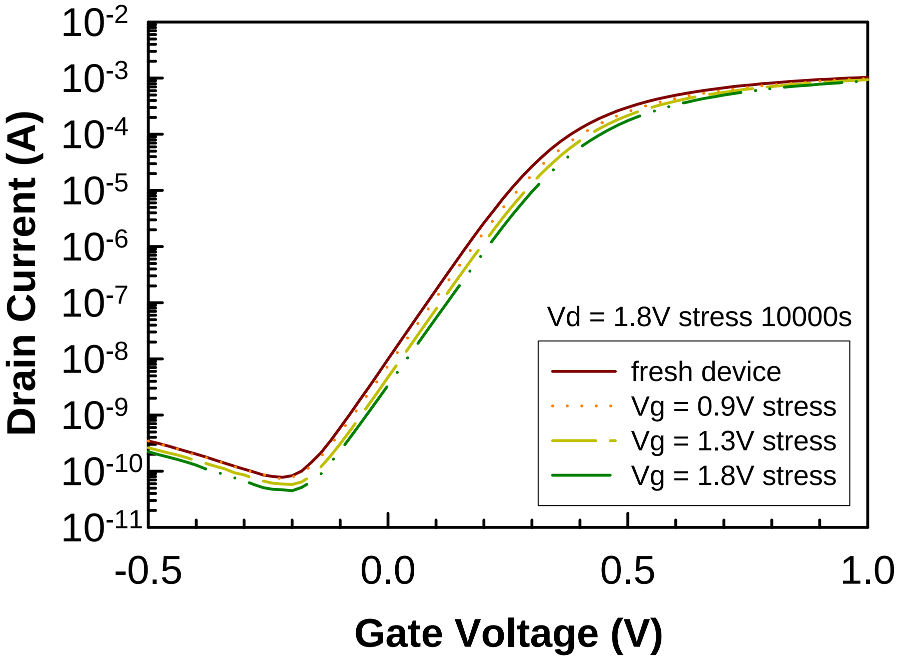
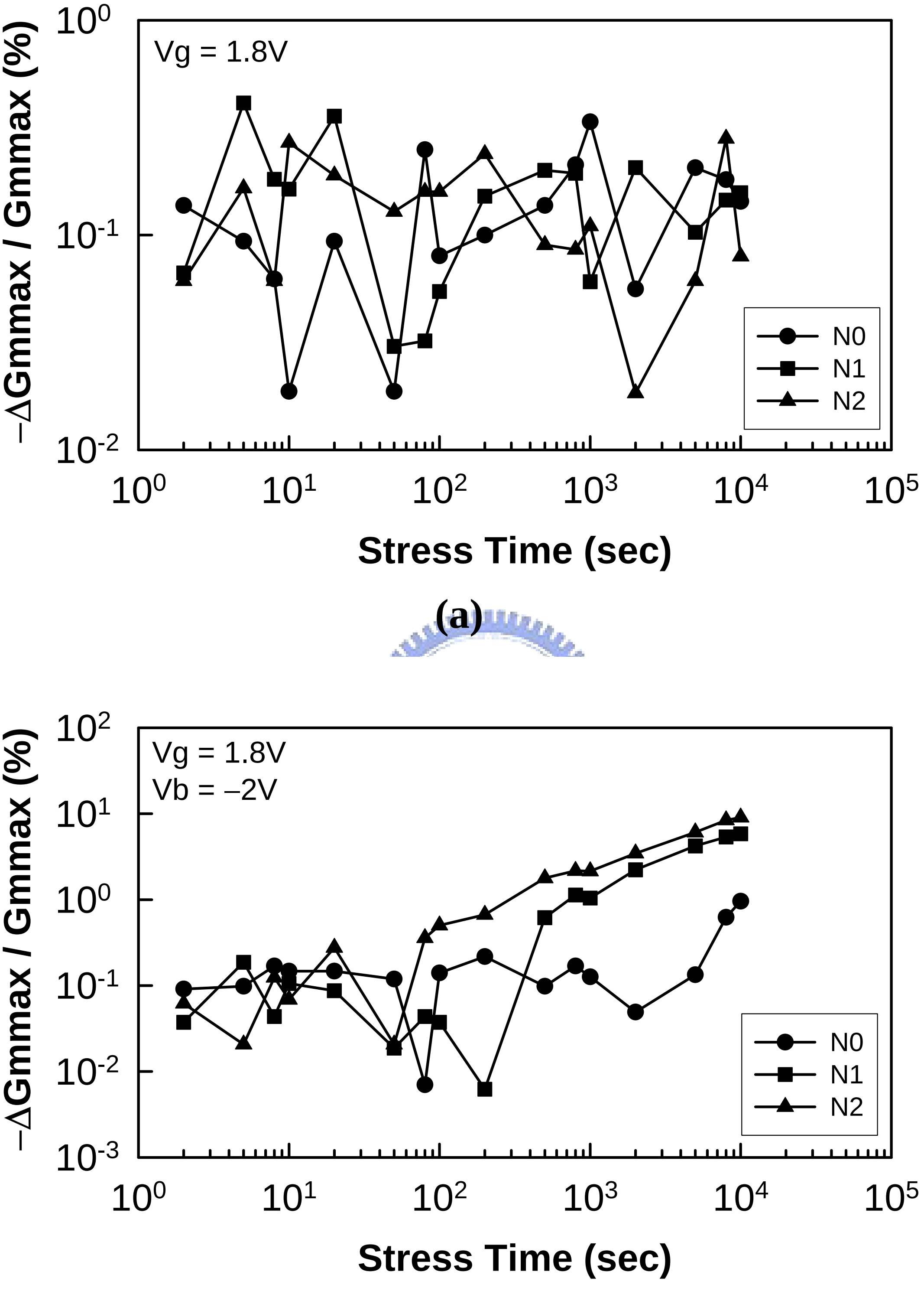


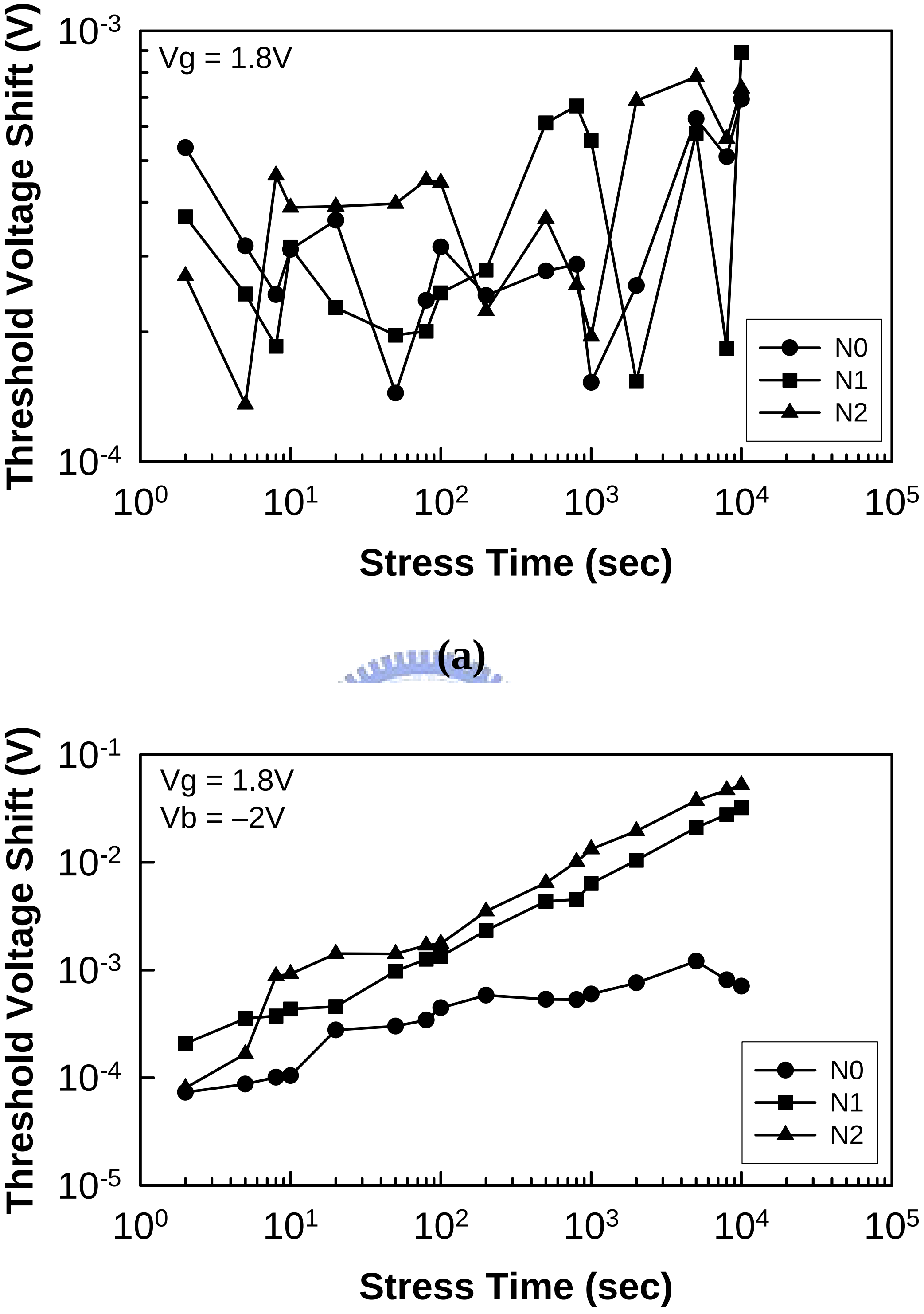
Fig. 3.13 I_d-V_g characteristics of device with plasma nitrided oxide (N2) before and after 10,000 sec stressing at V_d = 1.8V, V_g = 0.9, 1.3, and 1.8V.



(a)

(b)

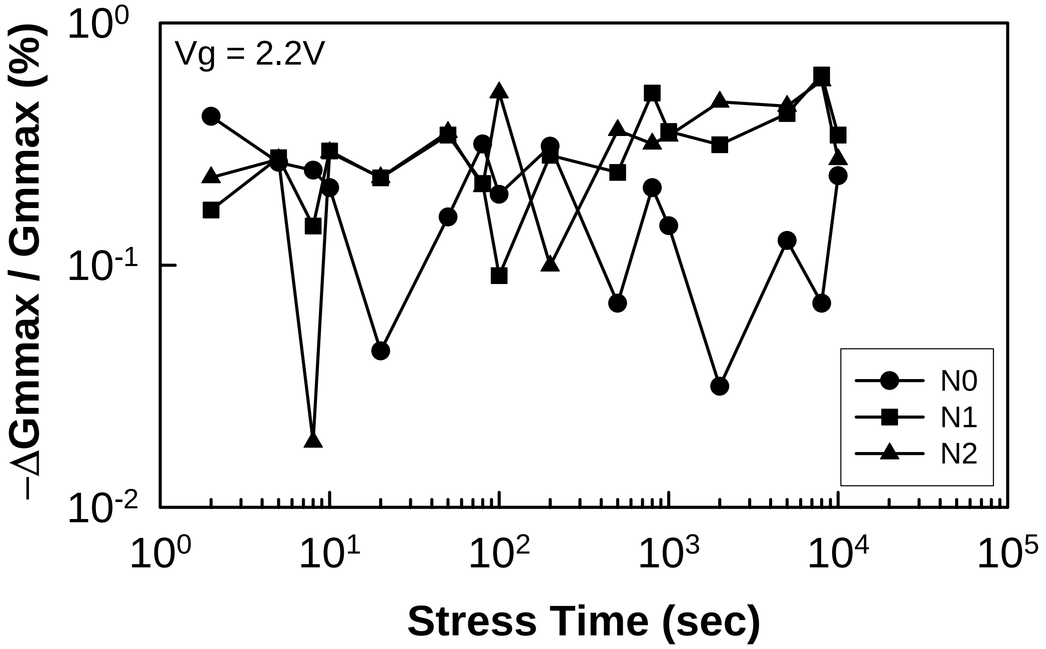
Fig. 3.14 Stress time dependence of $G_{m,max}$ degradation ($\Delta G_{m,max}$ / $G_{m,max}$ (0)) in devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) at (a) V_g = 1.8V, $V_d = V_s = V_b$ = 0V and (b) V_g = 1.8V, V_b = –2V, $V_d = V_s$ = 0V.



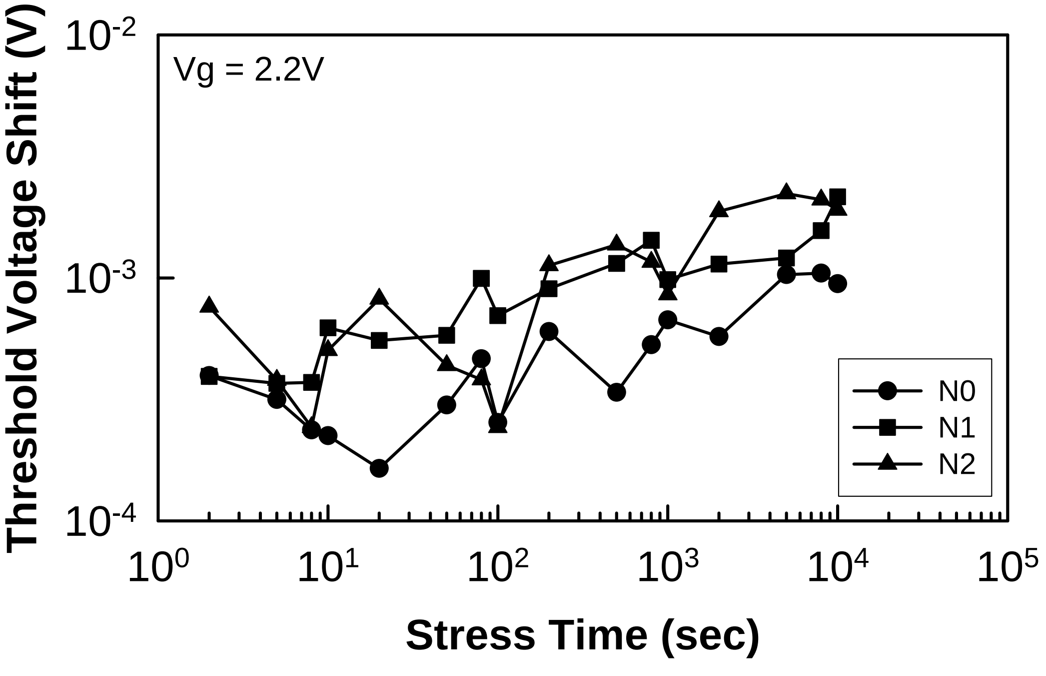
(a)

(b)

Fig. 3.15 Threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time at (a) V_g = 1.8V, $V_d = V_s = V_b$ = 0V and (b) V_g = 1.8V, V_b = –2V, $V_d = V_s$ = 0V.

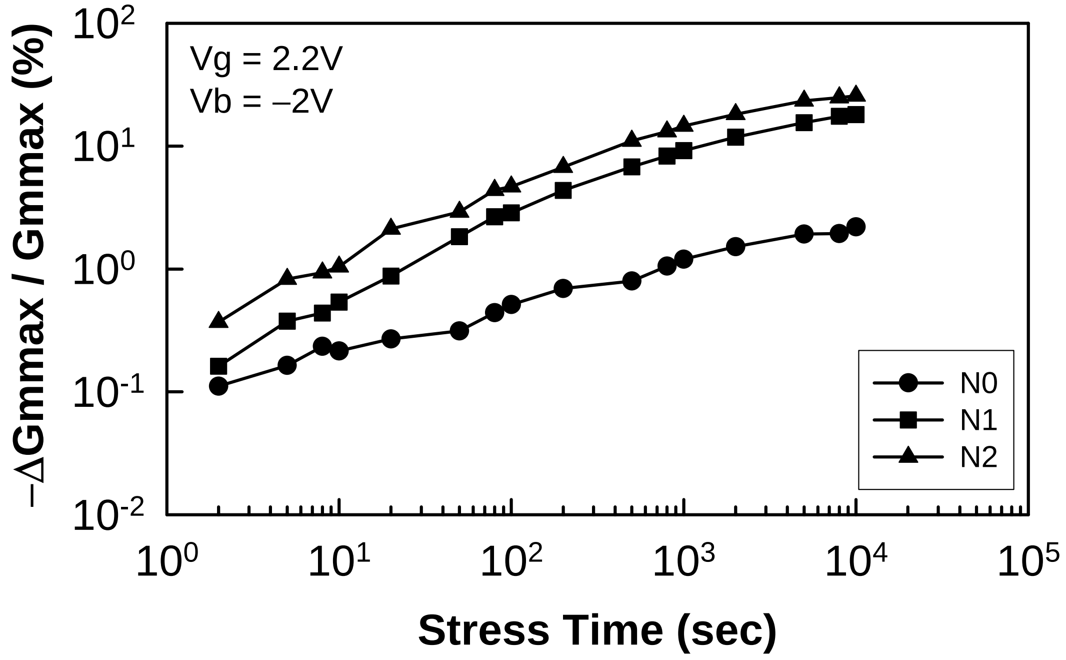


(a)

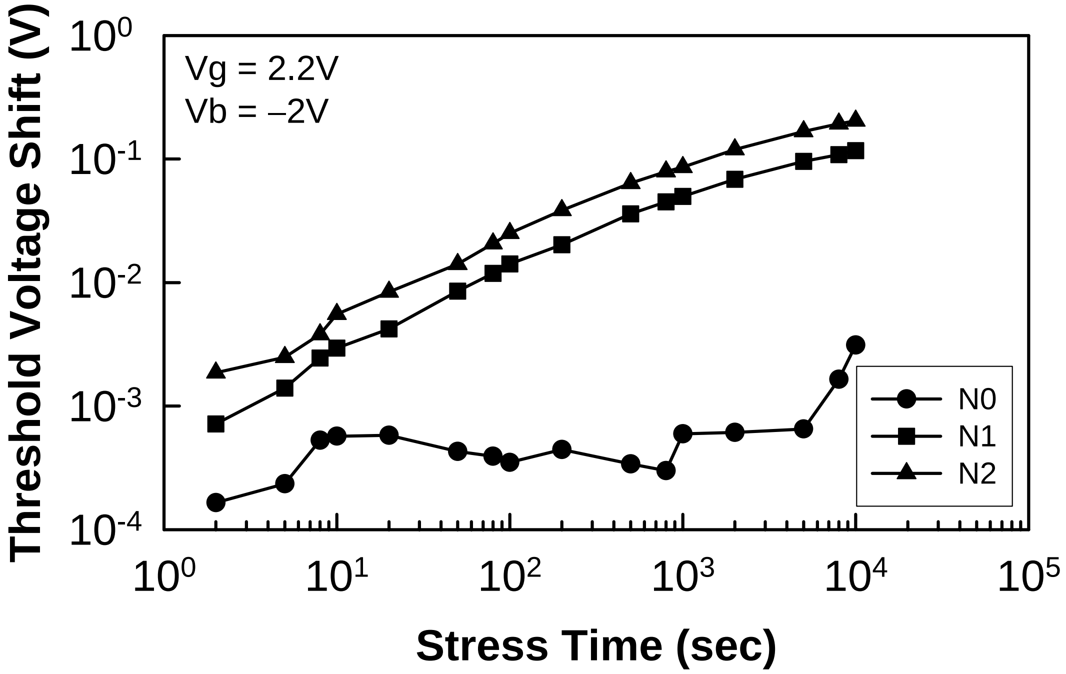


(b)

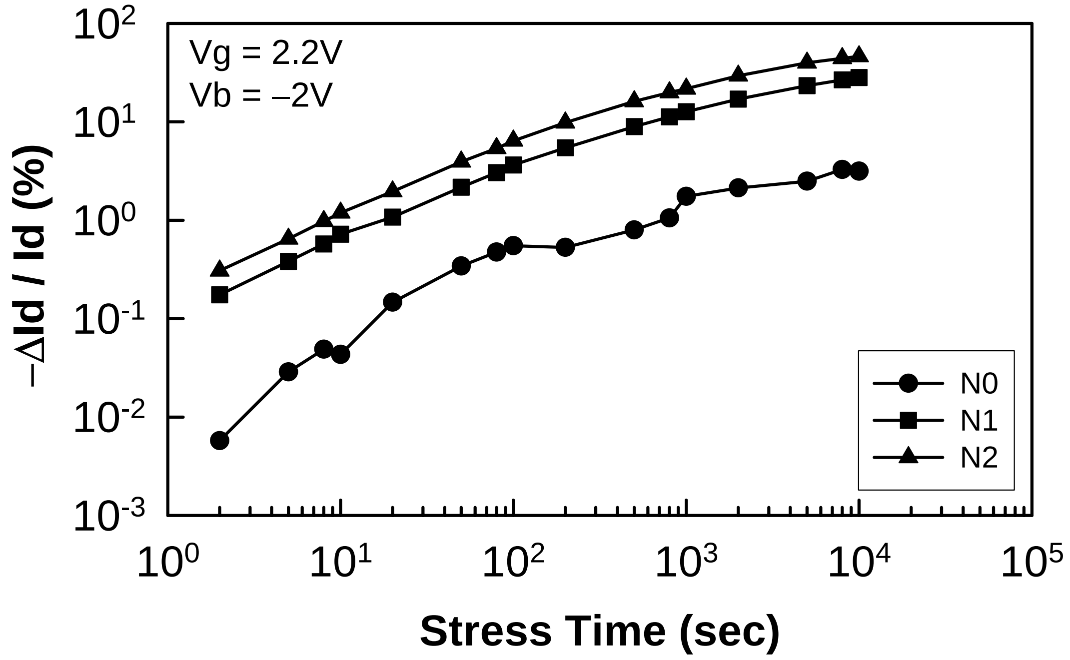
Fig. 3.16 (a) $G_{m,max}$ degradation ($\Delta G_{m,max}$ / $G_{m,max}$ (0)) and (b) threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time at V_g = 2.2V, V_d = V_s = V_b = 0V.


Vg = 2.2V
Vb = –2V
–ΔGmmax / Gmmax (%)
10^{2}
10^{1}
10^{0}
10^{-1}
10^{-2}
10^{0}
10^{1}
10^{2}
10^{3}
10^{4}
10^{5}
Stress Time (sec)
N0
N1
N2

(a)


Vg = 2.2V
Vb = –2V
Threshold Voltage Shift (V)
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{0}
10^{1}
10^{2}
10^{3}
10^{4}
10^{5}
Stress Time (sec)
N0
N1
N2

(b)



(c)

Fig. 3.17 Stress time dependence of (a) $G_{m,max}$ degradation ($\Delta G_{m,max}$ / $G_{m,max}$ (0)), (b) threshold voltage shift, and (c) drain current degradation (ΔI_d / I_d(0)) in devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) at V_g = 2.2V, V_b = –2V, V_d = V_s = 0V.

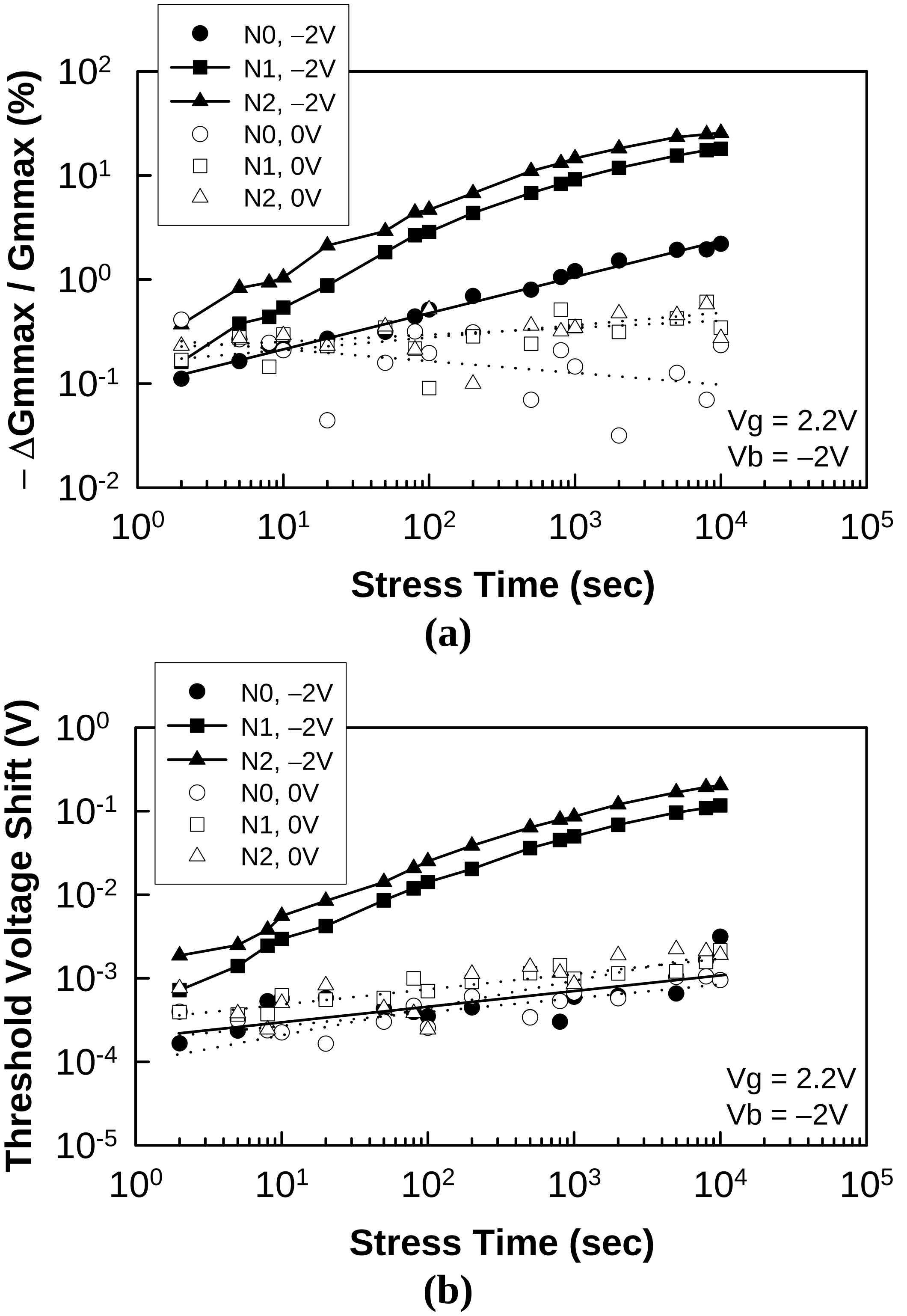


Fig. 3.18 Substrate hot electron (SHE) stress time dependence of (a) relative G_m degradation and (b) threshold voltage (V_t) shift for devices with thermal oxide (N0) and plasma nitrided oxides (N1 and N2). Substrate biases are 0V and –2V.

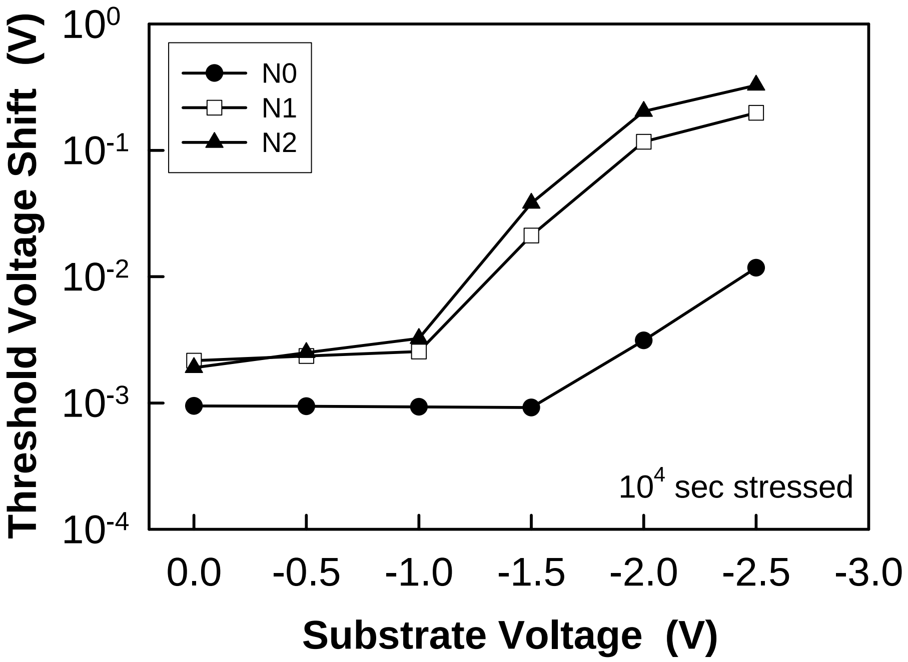


Fig. 3.19 Threshold voltage (V_t) shift of the devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of substrate bias after 10^4 sec of SHE stressing.

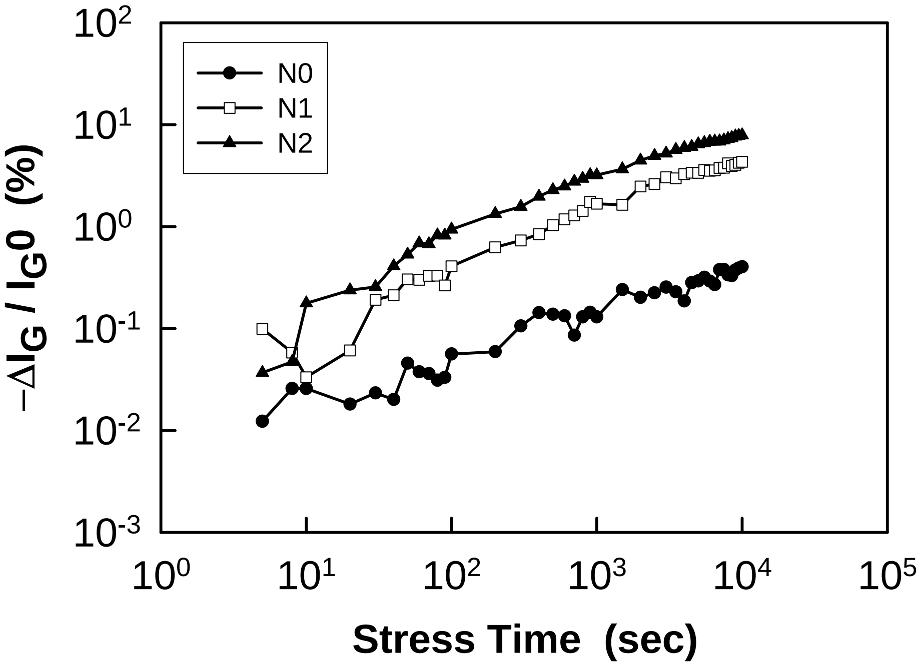


Fig. 3.20 Relative gate leakage current change as a function of SHE stress time for different samples.

Chapter 4

Reliability of pMOSFETs with Ultrathin Plasma Nitrided Gate Dielectric

4.1 Backgrounds and Motivation

For MOSFETs employing ultrathin gate oxide, the drastic increase in standby power consumption as a result of the direct tunneling leakage current in the dielectric is a challenging issue, especially as device scaling leads to higher device density in a chip. In addition, the dopant impurity penetration through the ultrathin gate dielectric represents another major concern on the oxide scaling. In the past, nitrogen incorporation into the ultrathin gate oxide to form oxynitride and/or nitride/oxide stacks have been successfully demonstrated to alleviate the above shortcomings [82]. Among the available nitridation techniques, plasma nitridation is particularly viable and popular for preparing reliable ultrathin gate dielectric due to its uniformity, relatively high nitrogen concentration, low process temperature, and the ability to preserve high quality oxide/Si interface [83]–[85].

As gate oxide thickness in MOS devices is reduced, the increasing gate leakage current poses a major challenge to continued transistor scaling. Reliability of the ultrathin SiO_2 presents another major concern. Thus a transition to a gate material with a higher dielectric constant is critical for further CMOS scaling. A number of high-κ dielectrics, such as Ta_2O_5 [86], Al_2O_3 [87], La_2O_3 [87], ZrO_2 [88], HfO_2 [89] and several silicates have been proposed to replace SiO_2 in the gate stack. Stability of these materials in contact with silicon during high-temperature processing steps remains a major problem. Thus it might be a few years before a successful integration of a high-κ dielectric into CMOS fabrication process becomes reality. At the same time Si_3N_4, which has a relatively high dielectric constant of 7.5 (almost twice that of SiO_2), has been used by the semiconductor industry for decades and is relatively easy to integrate into the fabrication process. Good performance of Si_3N_4 transistors has already been demonstrated [90]. It is necessary to demonstrate good reliability of thin Si_3N_4 before it can replace SiO_2 as gate dielectric, however. Studies of time-dependent dielectric breakdown [90], [91], and time-dependent dielectric wear out [92] indicate that Si_3N_4 under Fowler-Nordheim stress meets reliability requirements. It still remains to be shown that hot-carrier reliability of Si_3N_4 gate dielectrics is acceptable. Earlier work [91] indicates good hot-carrier reliability of nMOSFET JVD nitride transistors with 3.1 nm equivalent oxide thickness. In this chapter we will examine the hot-carrier reliability of Si_3N_4 pMOSFETs as well as SiO_2 pMOSFETs.

We also examine the mechanism responsible for pMOSFET degradation. It has been long known that the mechanism responsible for the device degradation in nMOSFET is interface-state generation. The situation for pMOSFETs is less clear. It had long been believed that hot-carrier reliability of pMOSFETs is not as serious an issue as hot-carrier reliability of nMOSFETs for the following reason: The mean free path of holes in silicon is about one half that of the electrons [93]; therefore holes scatter more frequently and fewer of them reach high enough energies (about 4 eV) to create interface states [94]. However, as the transistor channel length has been scaled down into the deep-sub-micron regime (and supply voltages have been reduced) hot-carrier induced degradation of pMOSFETs has been approaching that of nMOSFETs [95]. Consequently the hot-carrier reliability of pMOSFETs has been studied in more detail. Three hot-carrier degradation mechanisms in pMOSFET's have been identified [96], [97]. The first is negative oxide charge trapping. Electron trapping near the drain region leads to a reduction in the threshold voltage and to the effective channel shortening. As a result, pMOSFET drive current increases. This mechanism is most important in longer channel pMOSFETs, and gate current I_g has been used as a predictor of the device lifetime. The second mechanism is the generation of interface states by hot holes, which leads to channel mobility degradation. In this case the substrate current I_{sub} should be used to predict the device lifetime. And the third mechanism is positive oxide charge trapping. Interface-state generation has been shown to be the dominant degradation mechanism for 0.25 μm surface channel pMOSFETs [96]. We will show that this conclusion remains true for our devices, for both oxide and nitride gate dielectrics.

4.2 Experimental Procedure

Deep submicron (0.13 μm) pMOSFETs with ultrathin gate dielectrics were used in this study. After active device area definition, conventional thermal oxides were grown at 900°C. In order to achieve a final equivalent oxide thickness (*EOT*) of approximately 2.0 nm for all splits, thermal oxides with various starting thickness were subjected to various plasma nitridation times. After deposition and patterning of a 150 nm thick un-doped poly-Si film, boron dopants were implanted with energy of 5 keV to dope the gate electrode and also to form the shallow source/drain junction. For activation, all samples were annealed using rapid thermal annealing (RTA) in N_2 gas ambient for 30 sec. Subsequently, cobalt salicide, borophosphosilicate glass (BPSG), and metallization processes were performed to complete the device fabrication. The hot-carrier stress of pMOSFETs was carried out subjecting to the drain voltage of −2.1V, −2.3V, and −2.5V with the gate voltage at the condition of maximum gate current. For time-dependent reliability testing, constant negative voltage of −2.1V, −2.3V, and −2.5V were applied to the gate with the source, drain, and substrate grounded at room temperature. For negative bias temperature instability (NBTI) testing, the temperature was ranged from room temperature to elevated 100°C. Device characteristics were recorded at certain time interval for stress time up to 10^4 seconds. The indicators of reliability degradation are transconductance G_m reduction and threshold voltage V_t shift. G_m is defined as the peak value of the transconductance of a device in linear region, while threshold voltage is defined at the interception extrapolated from the peak value.

4.3 PMOSFETs with Ultrathin Plasma Nitrided Gate Dielectric

Figure 4.1 shows the drain current (I_d) versus drain voltage (V_d) characteristics for (a) long channel (W/L = 10/10 μm) and (b) short channel (W/L = 10/0.13 μm) pMOSFET devices with thermal oxide (N0) and plasma nitrided oxides (with plasma treatment time of 25 sec (N1) and 50 sec (N2), respectively). The drain current is larger for the thermal oxide device. For the plasma nitrided devices, the drain current is decreased with the plasma nitridation time. Figure 4.2 shows the drain current (I_d) versus gate voltage (V_g) characteristics for (a) long channel (W/L = 10/10 μm) and (b) short channel (W/L = 10/0.13 μm) pMOSFET's with thermal oxide (N0) and plasma nitrided oxides (N1, N2). For the long channel devices, the threshold voltage of N0, N1, and N2 are –0.14, –0.23, and –0.28 V, respectively. The swing is about 68mV/dec for all three devices. For the short channel devices, however, the threshold voltage of N0, N1, and N2 are –0.31, –0.38, and –0.44 V, respectively. And the swing of N0, N1, and N2 are 81, 80, and 79mV/dec, respectively. The subthreshold current is obviously larger for the devices with plasma nitrided oxide than that with thermal oxide at saturated region. Drain induced barrier lowering effect is also observed in the deep submicron devices. For the sake of distinction, Figure 4.2 was re-plotted in Figure 4.3 as a function of the effective gate drive ($V_g - V_t$). The transconductance (G_m) characteristics corresponding to

Figure 4.2 were shown in Figure 4.4. The product of transconductance and oxide thickness (G_m * T_{ox}) corresponding to Figure 4.4 were also shown in Figure 4.5. The value for the device with thermal oxide is larger than that for the plasma nitrided ones, which implies the mobility is larger for the device with thermal oxide than that with plasma nitrided ones. Further, the G_m * T_{ox} values of these pMOSFET's are almost one-third compared with that of the nMOSFET's shown in chapter 3, which is consistent with the ratio of hole and electron mobility listed in literatures.

4.4 Channel Hot Hole Degradation

In order to monitor the hot-carrier effects for pMOSFETs, devices will be stressed at maximum gate current ($I_{g,max}$) and that indicates the most efficient generation of hot carriers. While evaluating V_g values through gate current curves as a function of gate voltage as stressing drain voltage kept constant, the curves show monotonic increase and always reach the maximum at maximum gate voltage. Figure 4.6 depicts the typical substrate current curve at drain voltage of –2.1 V. This makes the situation of stressing condition more simple and straight forward comparing with that for nMOSFET's. In order to monitor the aging situation, the variation of the maximum transconductance $G_{m,max}$, the threshold voltage V_t, and the forward-mode drain current I_d were measured at V_d = 0.05 V. The stressing experiments were interrupted periodically to measure the degradation monitors by using a Keithley Model 4200-SCS Semiconductor Characterization System. Figure 4.7 shows the comparison of the stress time dependence of $G_{m,max}$ degradation ($\Delta G_{m,max}/G_{m,max}$) among devices stressed at V_g = $I_{g,max}$ on a double log scale ($\Delta G_{m,max} = (G_{m,max}(t) - G_{m,max}(0)) < 0$). Figure 4.7(a), (b), and (c) are corresponding to the device under the stressing drain voltage V_d = –2.1, –2.3, and –2.5 V, respectively. It can be seen that the device N0 exhibits less degradation than the other two devices N1 and N2, although different stressing voltages were applied. And larger degradation is expected with higher stressing voltage. In general, the $G_{m,max}$ in the linear region is found to be decreased as a result of the carrier mobility degradation, which is associated with the generated interface traps.

Figure 4.8 depicts the gate current curves as a function of gate voltage at the biasing condition of $V_d = V_g = -2.5$V. Comparing these gate current curves, the current of device N0 shows the smallest value and that of device N1 is the largest. As corresponding to the $G_{m,max}$ degradation in Figure 4.7, Figure 4.9 compares the threshold voltage shift ΔV_t of devices N0, N1, and N2 as a function of the stress time ($\Delta V_t < 0$). Similar tendency correlated to stressing voltage can be observed in these figures. The associated degradation of drive currents with respect to devices N0, N1, and N2 are shown in Figure 4.10. We examine the mechanism responsible for the device degradation by examining the change in the threshold voltage (Fig. 4.9). The negative threshold voltage shift ΔV_t indicates a positive charge build-up in the gate dielectric. The positive charge can result from either hole trapping in the dielectric or the creation of positively charged interface states at the dielectric interface. In practice, it may be hard to draw a distinction between the two phenomena, as it is hard to distinguish between bulk and interface traps in the case of ultrathin dielectrics. However, the mechanism of hole injection into the dielectric indeed plays a significant role for deep-submicron pMOSFETs [96].

4.5 Enhanced Negative Bias Temperature Instability

Negative bias temperature instability (NBTI) of pMOSFETs with p+ poly-Si gate is becoming a more serious problem regarding the reliability of CMOS devices [98]. NBTI is anticipated to be enhanced by scaling down of gate length [99] and also by incorporation of nitrogen into gate oxide [100]. On the other hand, SiON gate dielectrics with a high concentration of nitrogen are expected to be applied for 90-nm-node CMOS devices [101]–[103]. Thus, NBTI may be a critical issue for 90-nm-node CMOS technology. However, several questions regarding the mechanism of NBTI still remain. Figure 4.11 illustrates the NBTI stress configuration.

The degradation of pMOSFETs by NBT stress is represented by a shift of threshold voltage (V_t) in the negative direction. This V_t shift is widely believed to be explained by the following reaction model [104],

$$\mathrm{Si_3\text{-}Si\text{-}H} \rightarrow \mathrm{Si_3\text{-}Si^{\circ}} + \mathrm{X_{interface}} \tag{4.1}$$

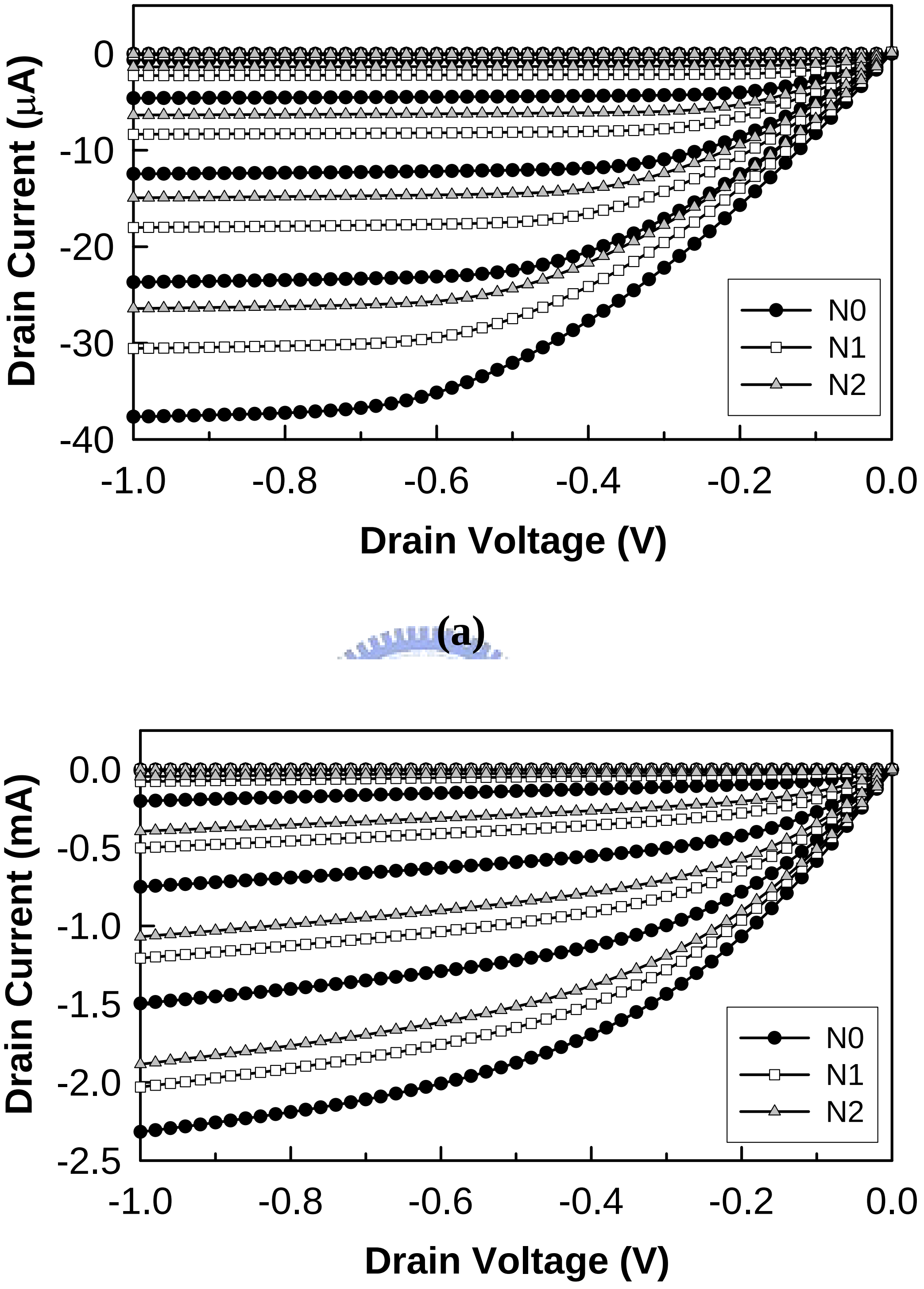
$$\mathrm{X_{interface}} \rightarrow \mathrm{X_{bulk}^{+}} \tag{4.2}$$

where Si_3-Si° is an interface trap and X is a H-related species. Firstly, reaction (4.1) generates an interface trap at the interface. Secondly, according to reaction (4.2), the species X diffuses into the gate dielectric and a positive fixed charge is generated. The H-related species X is possibly a hydrogen atom, a hydrogen molecule, or a positively charged hydrogen ion, but it has not been identified yet.

The phenomenon of NBTI enhancement caused by nitrogen in gate dielectrics can be a critical problem for near-future CMOS technology which requires SiON gate dielectrics with a high concentration of nitrogen. Kimizuka *et al.* reported that the activation energy of NBTI was much smaller for a heavily nitrided NO-oxynitride than for a pure SiO_2 [100]. Figure 4.12(a) shows the threshold voltage shift against stress time for the three devices (N0, N1, and N2) under the bias of V_g = –2.5V at an elevated temperature of 125°C. Appreciable greater shift of threshold voltage was found for the devices with nitrided oxide (N1, N2). Regarding time dependence of NBTI, it can be found that the time-dependent V_t shift caused by NBT stress follows a power law with an exponent around 0.25. Figure 4.12(b) shows the constant voltage stress ($V_g = -2.5$V) at room temperature for the three devices. Appreciable difference between NBT stress and constant voltage stress can be observed. A larger threshold voltage shift was found for the devices under NBT stress. Different stress gate biases of –2.5V and –2.3V at elevated temperature of 125°C for the three devices were compared in Figure 4.13.

4.6 Conclusions

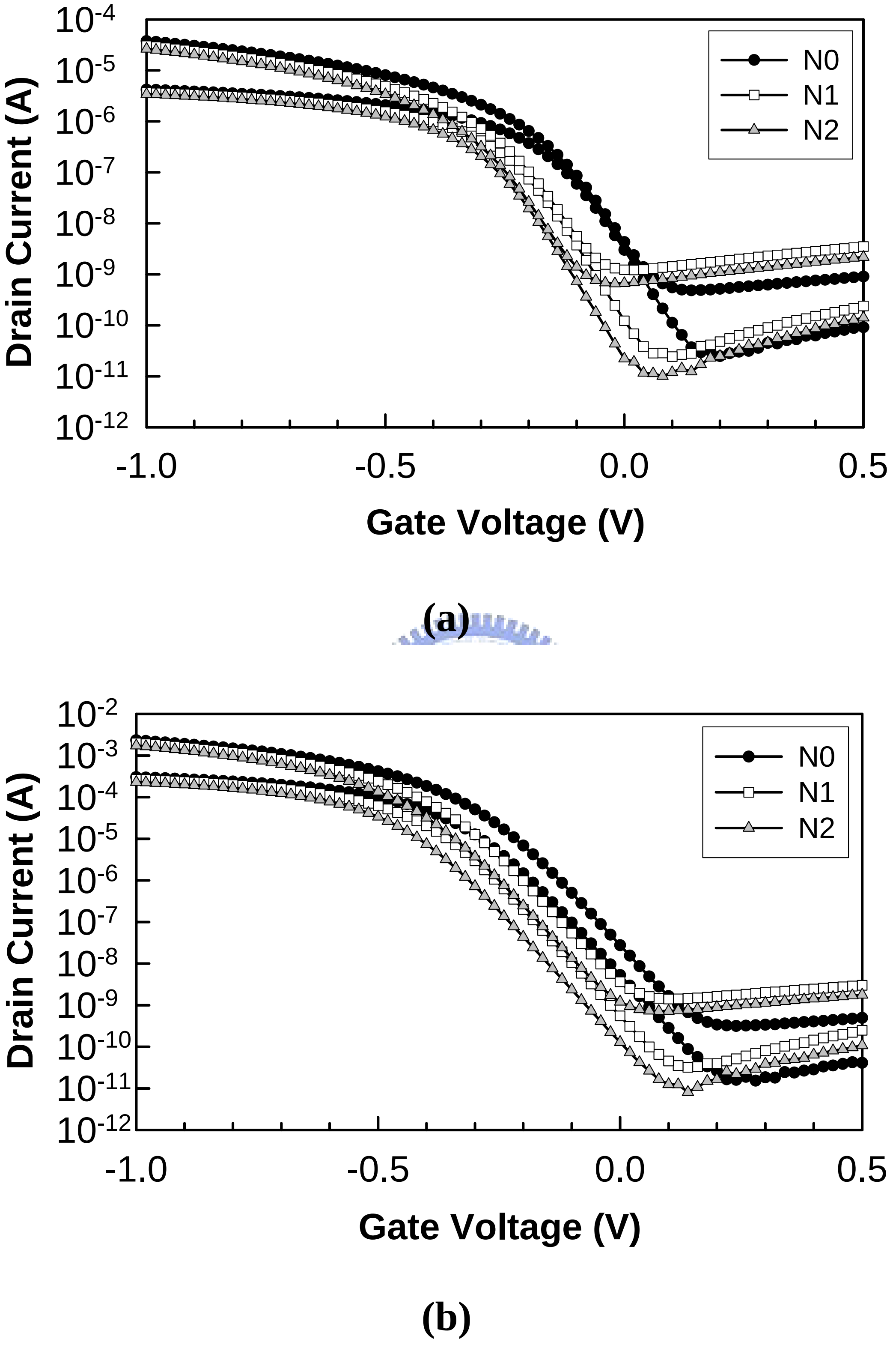
The hot carrier injection reliability and negative bias temperature instability of pMOSFET's with ultrathin plasma nitrided gate oxide was investigated. The devices with plasma nitrided oxide suffer more transconductance reduction and threshold voltage shift. The degradation is direct proportional to the plasma nitridation time. For channel hot-carrier stressing, the most efficient stressing condition is located at $V_g = V_d$, which is corresponding to the region of maximum gate current. The negative threshold voltage shift ΔV_t indicates a positive charge build-up in the gate dielectric. The positive charge can result from either hole trapping in the dielectric or the creation of positively charged interface states at the dielectric interface. For negative bias temperature stressing, appreciable enhancement of the threshold voltage shift can be observed through the raising of temperature. The enhanced device degradation is attributed to the H-related species and the interface trap generated during NBT stressing. NBTI is an important issue for pMOSFET's from the reliability point of view. Even though the incorporation of nitrogen into thermal oxide is advantageous in many respects, our findings suggest that careful attentions need to be paid to ensure that plasma-nitrided gate dielectric meets the reliability requirements for the sub-100nm device technology node.



(a)

(b)

Fig. 4.1 Typical I_d-V_d characteristics for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).



(a)

(b)

Fig. 4.2 Typical I_d-V_g characteristics for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).

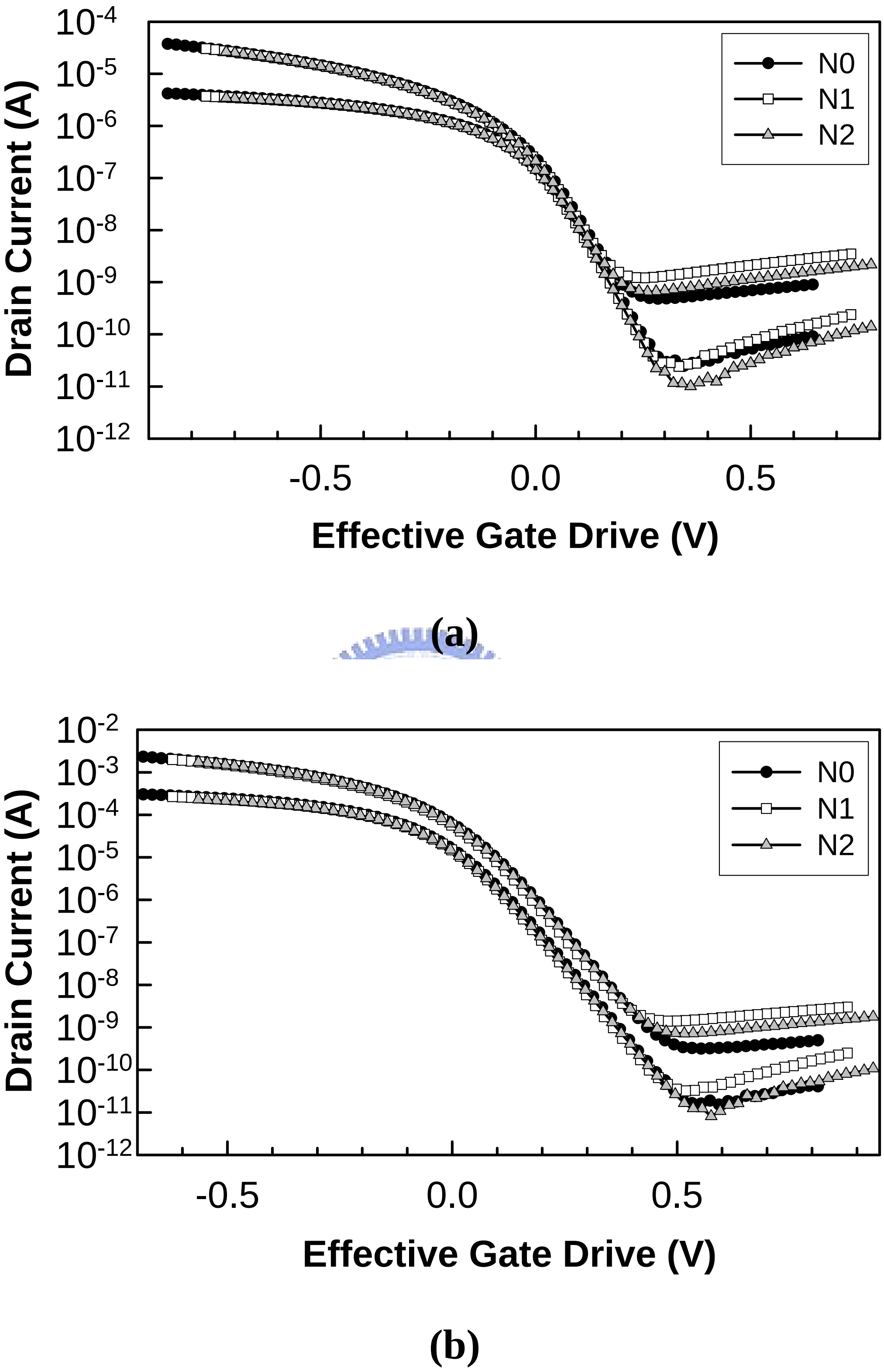


Fig. 4.3 Drain current (I_d) as a function of effective gate drive ($V_g - V_t$) for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).

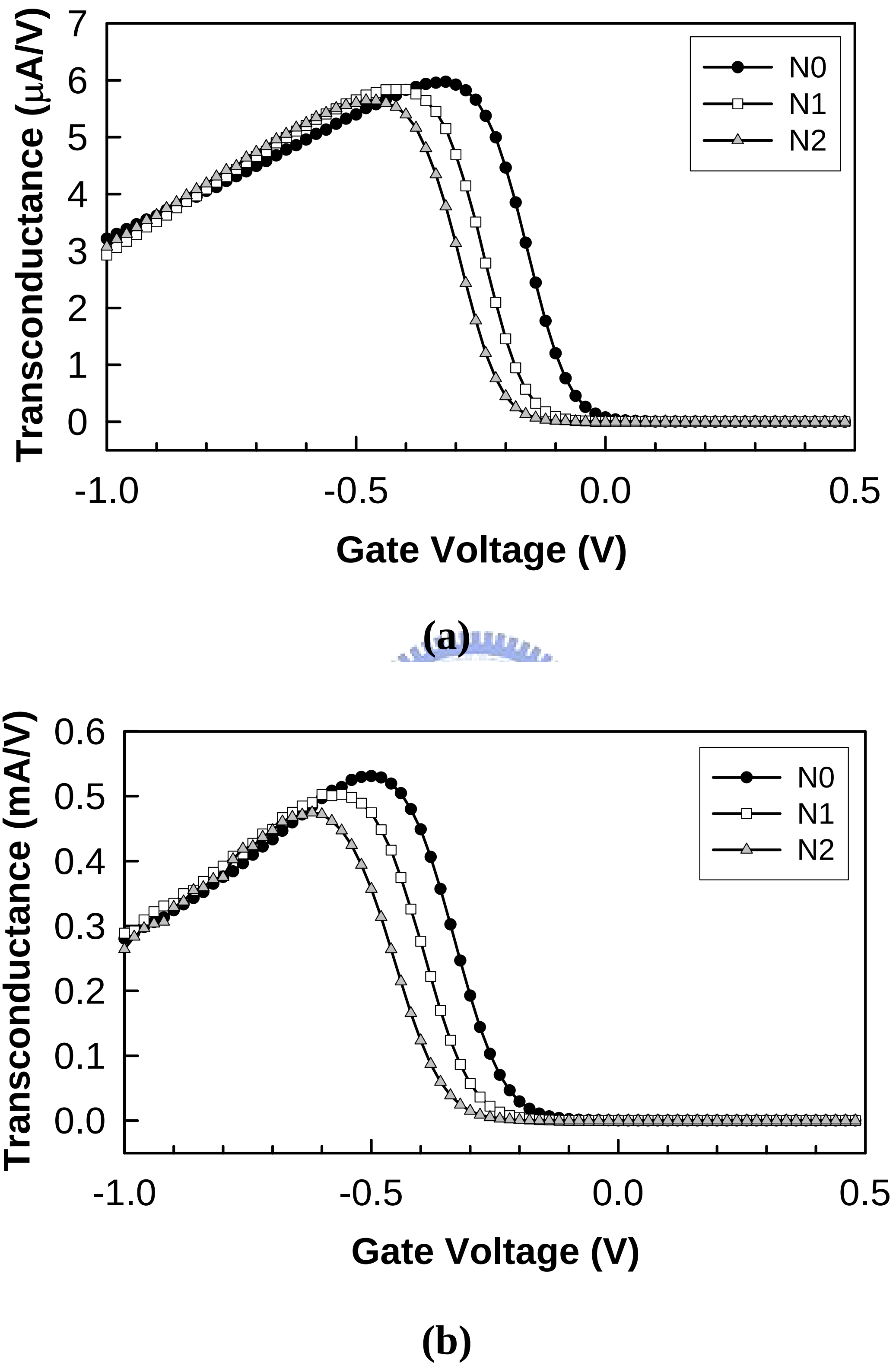
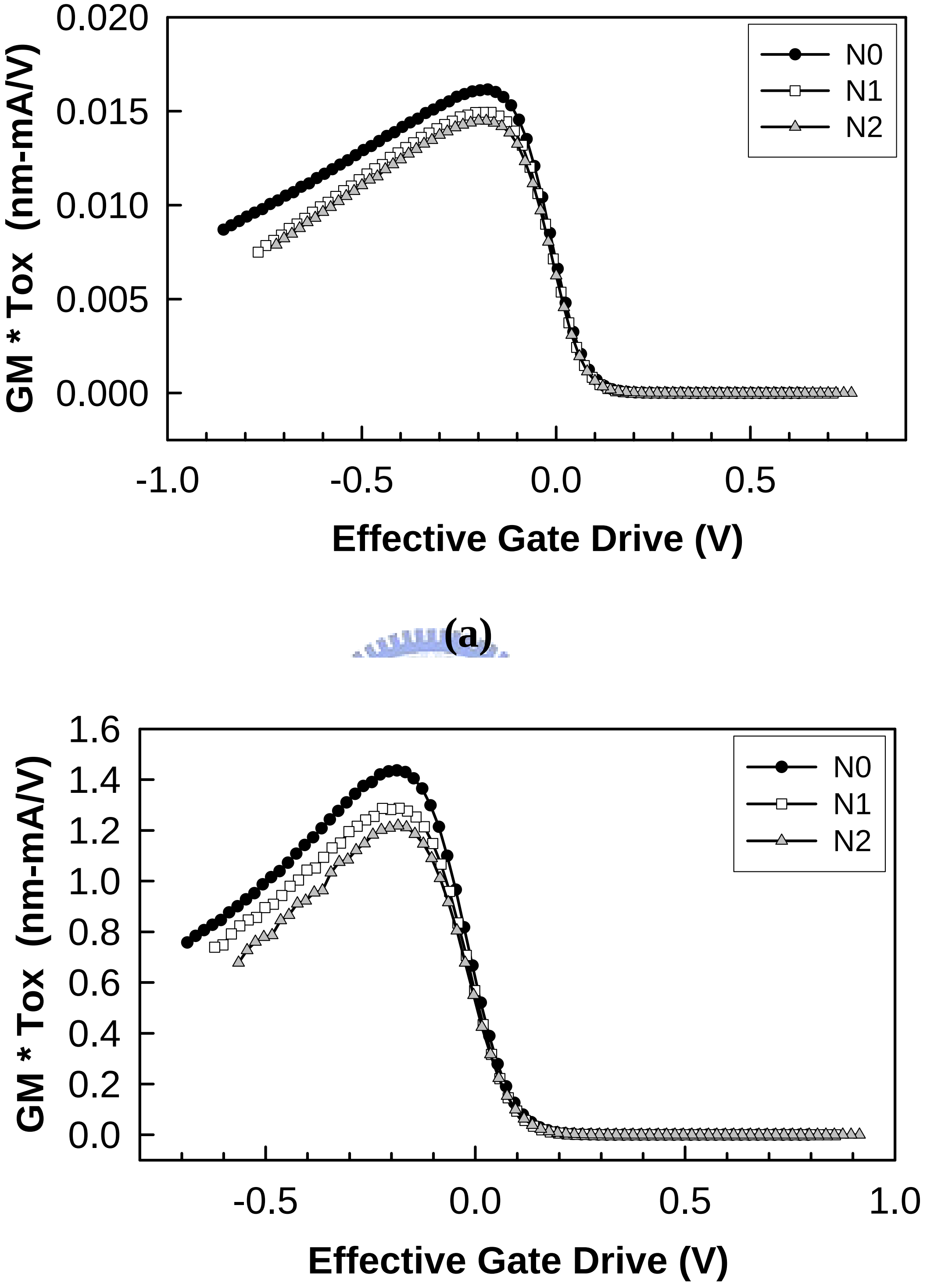


Fig. 4.4 G_m-V_g characteristics for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).



(a)

(b)

Fig. 4.5 $G_m * T_{ox}$ as a function of effective gate drive ($V_g - V_t$) for (a) long channel (W/L = 10/10 μm) and (b) deep submicron (W/L = 10/0.13 μm) devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2).

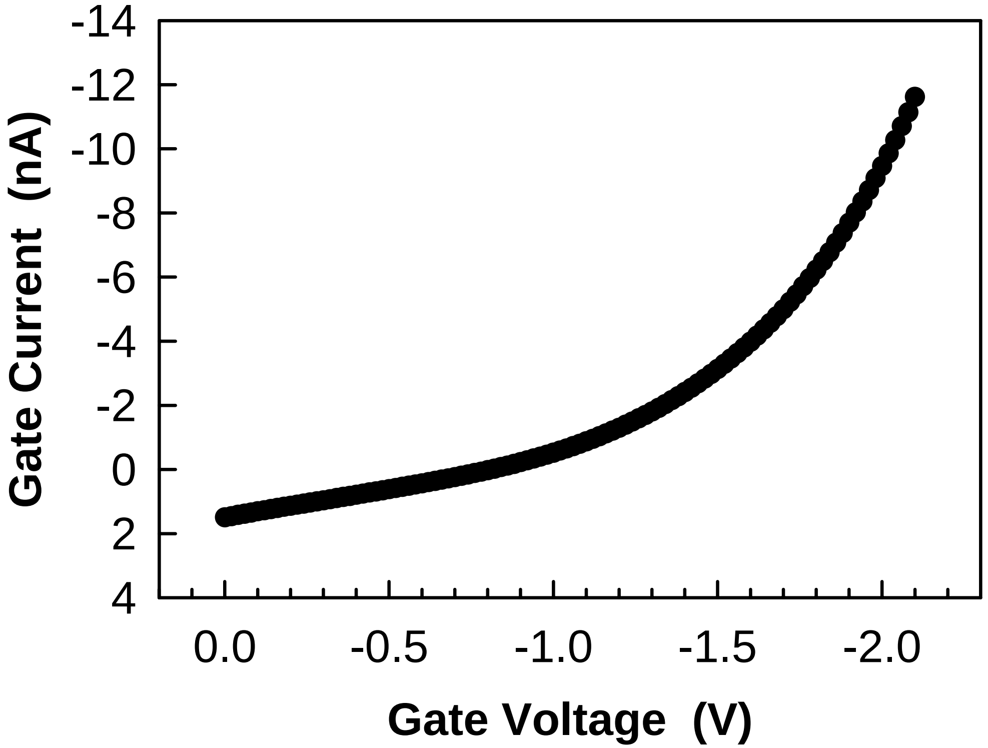
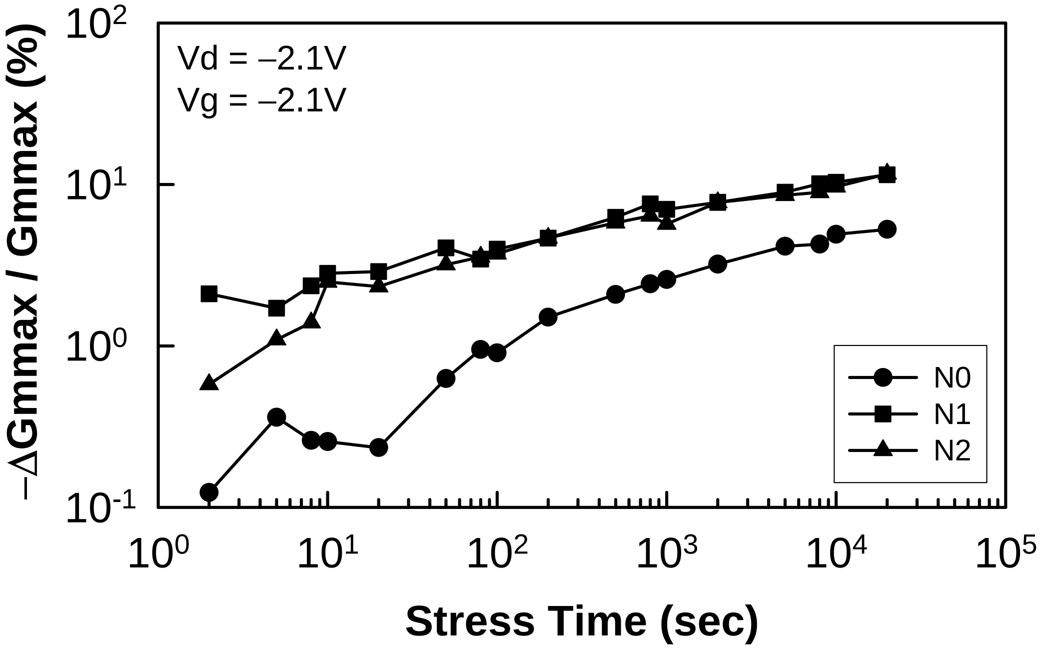
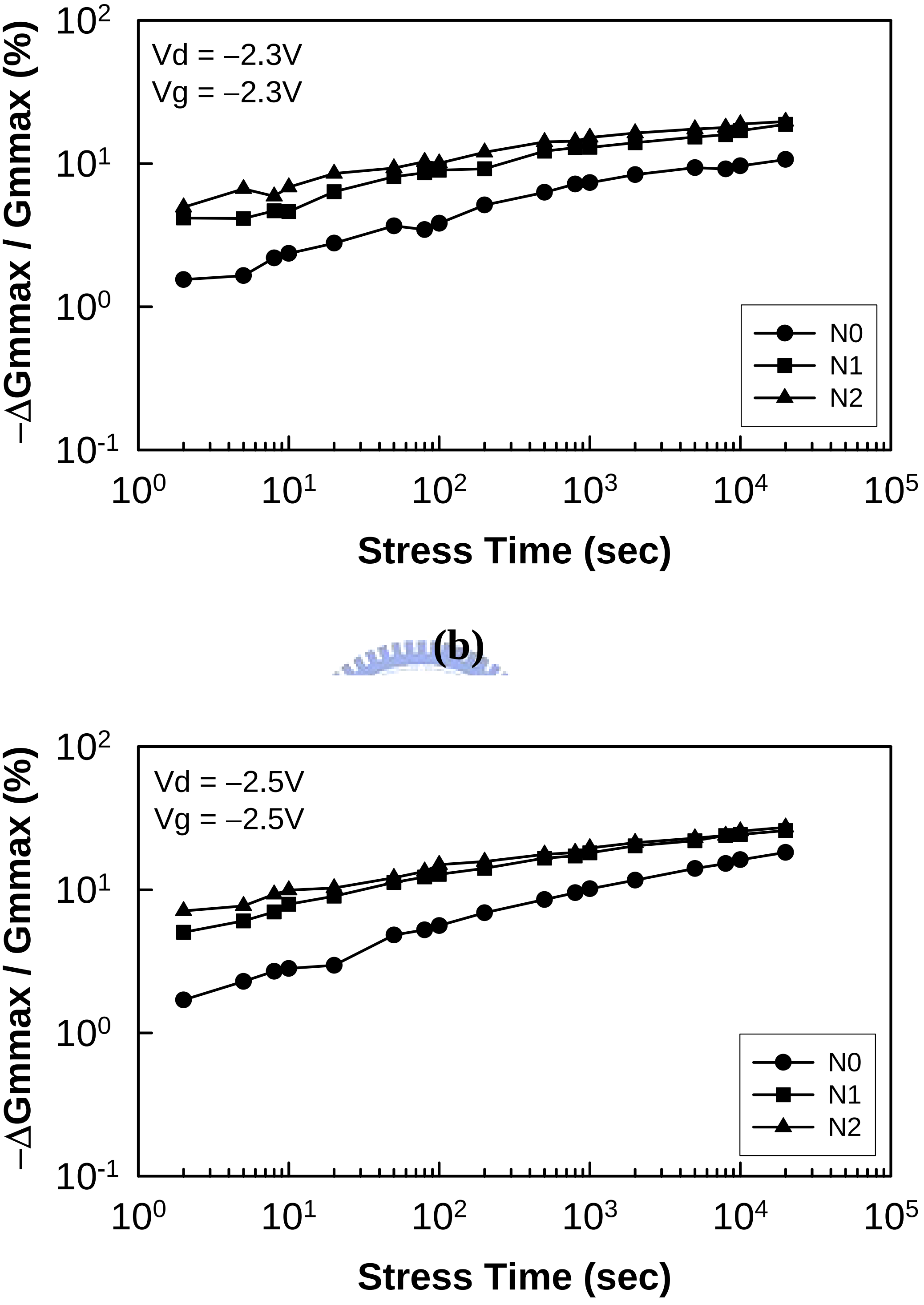


Fig. 4.6 Typical gate current curve as a function of gate voltage to estimate the stressing condition.



(a)



(b)

(c)

Fig. 4.7 Stress time dependence of $G_{m,max}$ degradation ($\Delta G_{m,max} / G_{m,max}$ (0)) in devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) at (a) $V_d = V_g =$ –2.1V, (b) $V_d = V_g =$ –2.3V, and (c) $V_d = V_g =$ –2.5V.

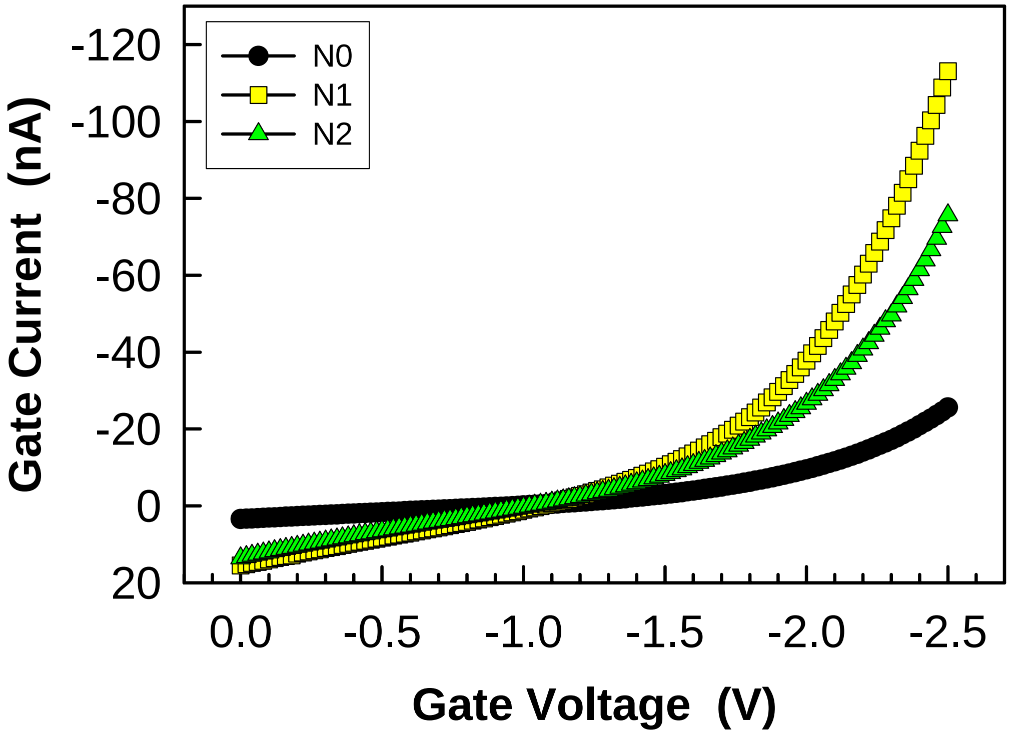
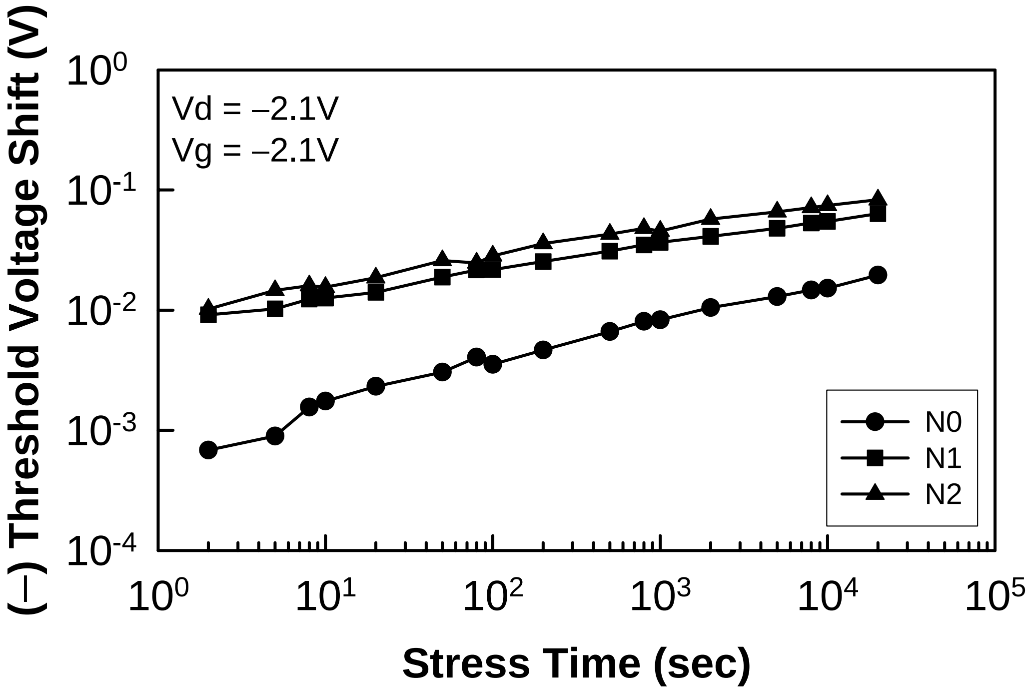
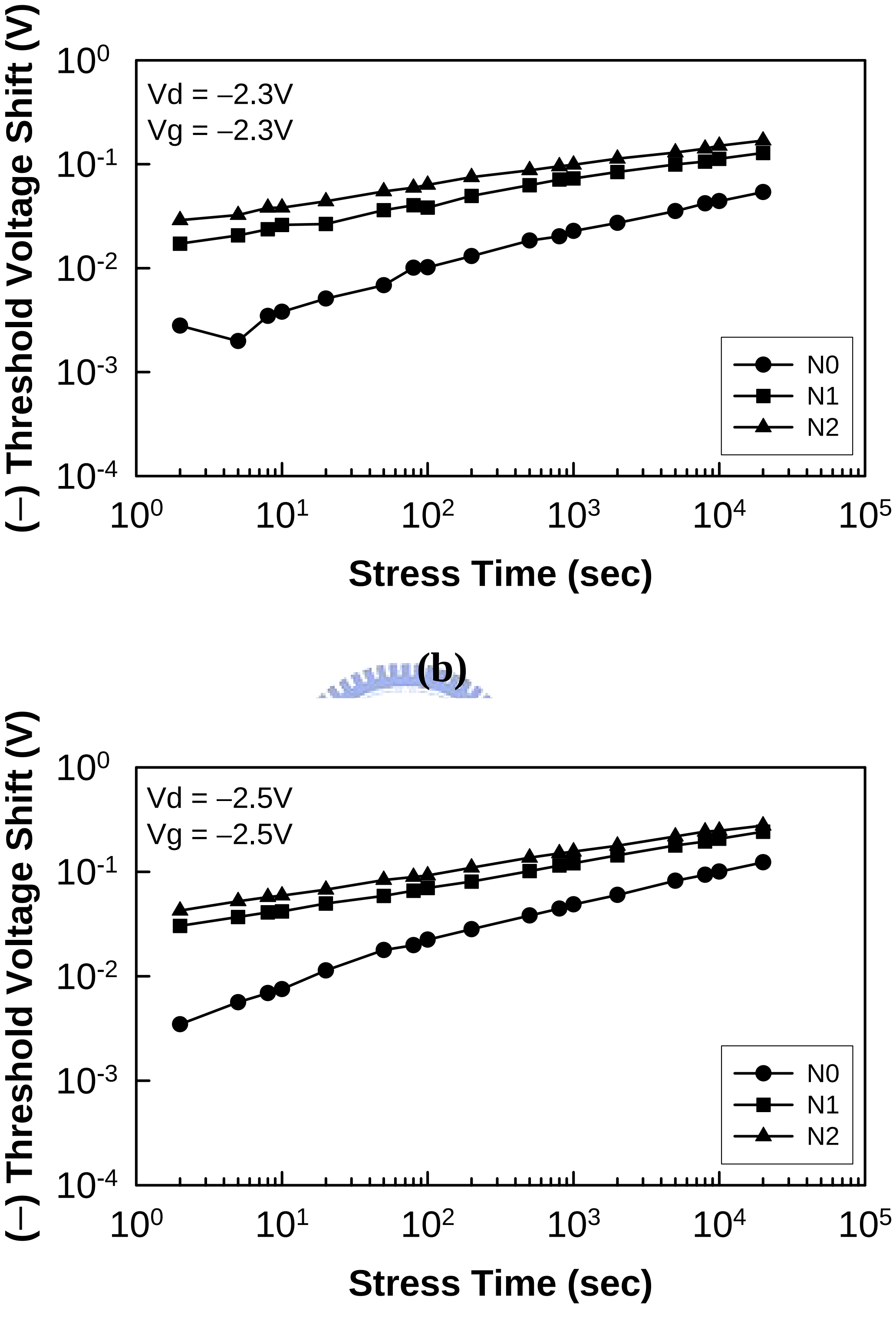


Fig. 4.8 Comparison of the gate current curves as a function of gate voltage biasing at $V_d = V_g = -2.5$ V.

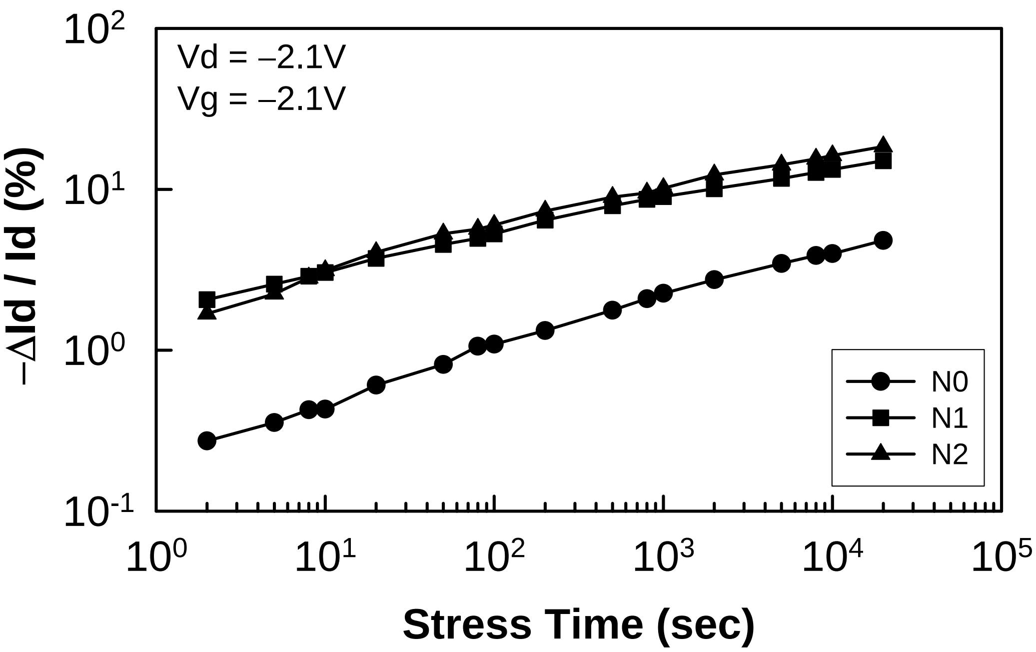


(a)

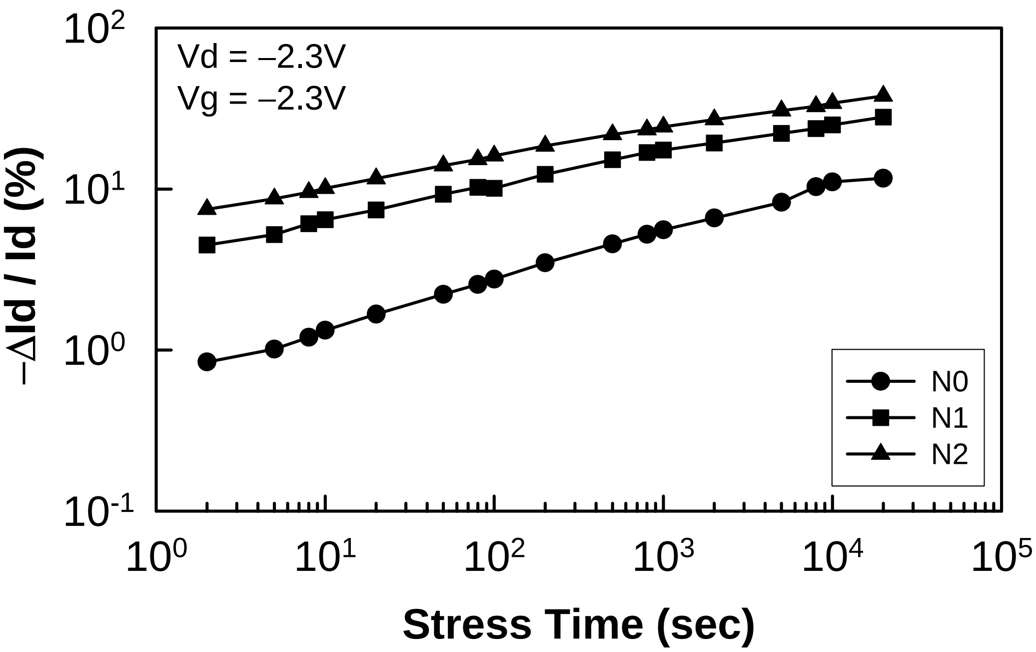


(c)

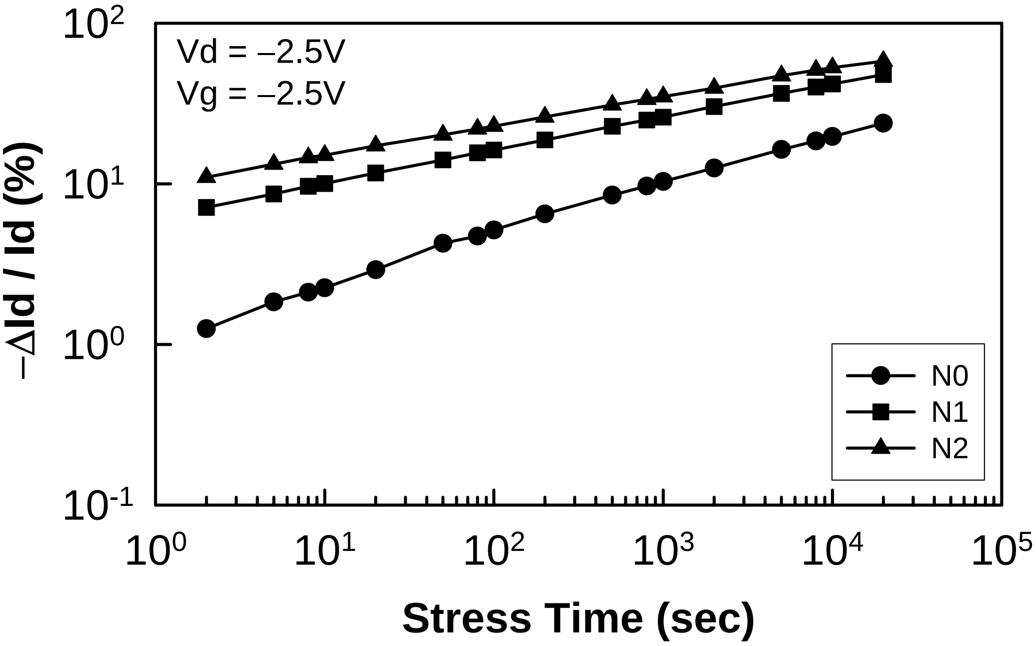
Fig. 4.9 Threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time at (a) $V_d = V_g = -2.1$V, (b) $V_d = V_g = -2.3$V, and (c) $V_d = V_g = -2.5$V.


Vd = –2.1V
Vg = –2.1V
–ΔId / Id (%)
10²
10¹
10⁰
10⁻¹
10⁰
10¹
10²
10³
10⁴
10⁵
Stress Time (sec)
N0
N1
N2

(a)


Vd = –2.3V
Vg = –2.3V
–ΔId / Id (%)
10²
10¹
10⁰
10⁻¹
10⁰
10¹
10²
10³
10⁴
10⁵
Stress Time (sec)
N0
N1
N2

(b)



(c)

Fig. 4.10 Stress time dependence of I_d degradation (ΔI_d / I_d (0)) in devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) at (a) $V_d = V_g = -2.1$V, (b) $V_d = V_g = -2.3$V, and (c) $V_d = V_g = -2.5$V.

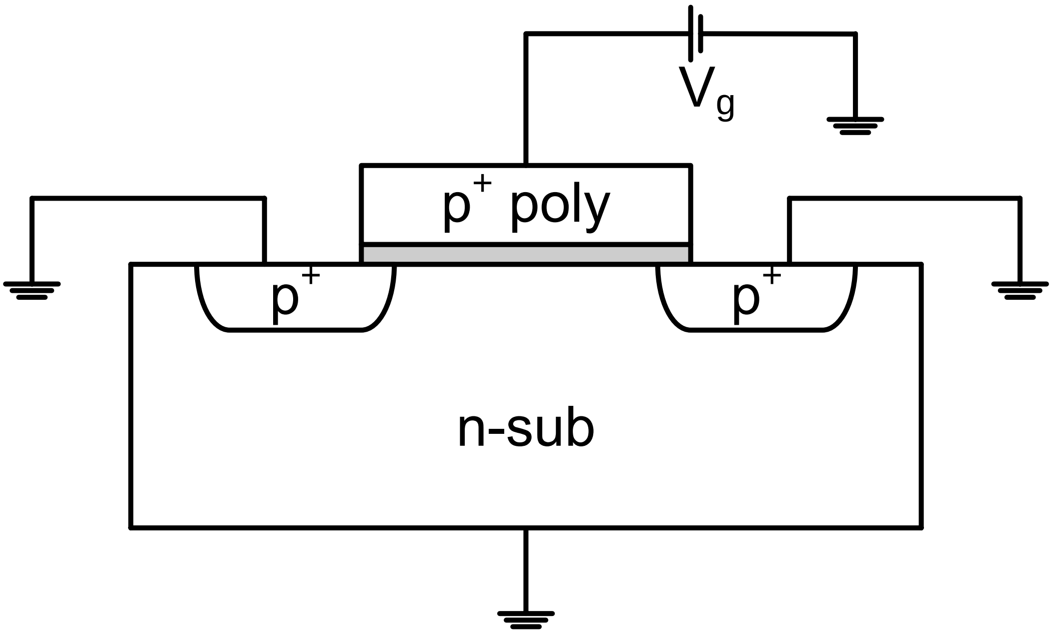
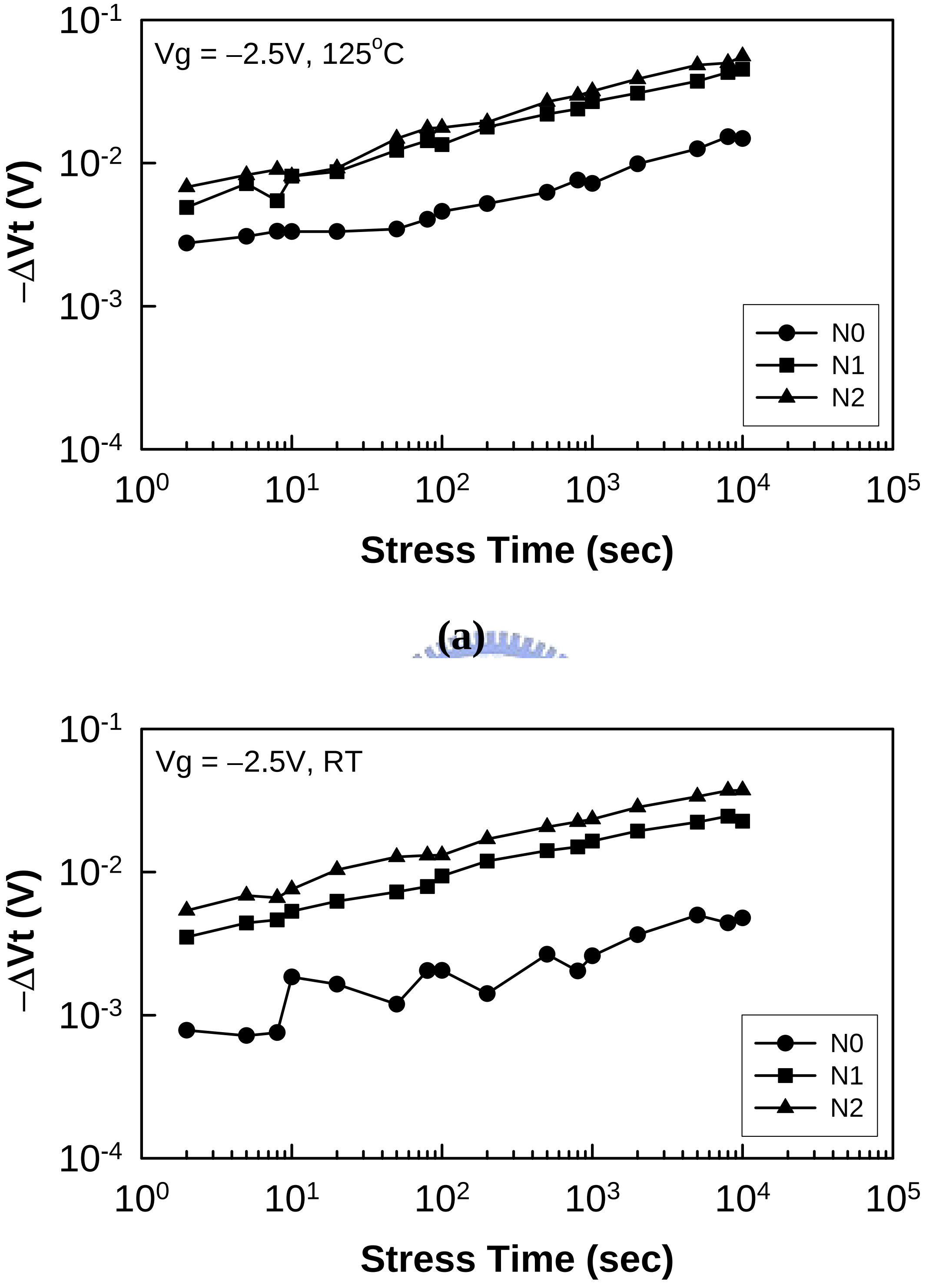


Fig. 4.11 Schematic plot of experimental configuration for NBTI stress.



(a)

(b)

Fig. 4.12 Threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time at (a) under NBTI stress (V_g = –2.5V, T = 125°C) and (b) V_g = –2.5V.

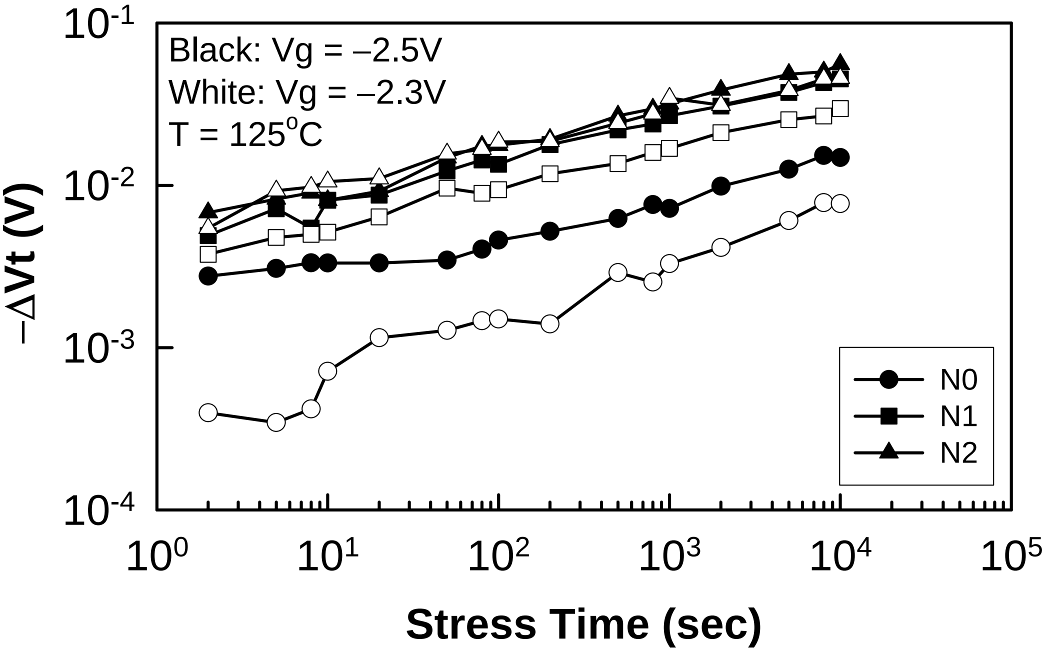


Fig. 4.13 Threshold voltage shift of devices with thermal oxide (N0) and plasma nitrided oxides (N1, N2) as a function of stress time under NBTI stress.

Chapter 5

MIS Capacitors with HfO_2 Dielectrics

5.1 Background and Motivation

When the gate length of MOSFETs is scaled down to 0.1 μm regime with the corresponding gate oxide thickness thinner than 3 nm, some major problems arise in realizing high-performance ULSI circuits. Specifically, device performance and reliability can be seriously degraded by the intolerably high direct-tunneling leakage current, increased gate resistance, worsened polysilicon gate depletion and boron penetration [105], [106]. To alleviate these problems, high dielectric constant (high-κ) gate insulator and metal gate have been proposed to meet the stringent performance requirement [107], [108]. Several metal oxides with dielectric constant in the range of 10–25 have been proposed as potential candidates for SiO_2 gate replacement. Various high-κ dielectric materials, such as Al_2O_3, Ta_2O_5, HfO_2, and ZrO_2, have been extensively studied [108]-[113]. Specifically, Al_2O_3 and La_2O_3 have dielectric constants of ~10 and 20, respectively [109], [113]. Alternatively, Wilk *et al.* [114], [115] proposed the use of silicates as a gate dielectric. Their work focuses mainly on studies of dielectric films formed by reactive sputtering of Zr and Hf. They obtained [115] an equivalent oxide thickness of about 1.6 nm and a $\kappa = 11$ for a Hf silicate film incorporating 6 at.% Hf. Furthermore, they claim that these films are stable on Si up to about 1050°C, consistent with the ternary phase diagram for the Zr–Si–O system which indicates that both ZrO_2 and $ZrSiO_4$, as well as $ZrSi_xO_y$ silicates, are stable in direct contact with Si. However, recent publications showed that several controversial issues remain with these materials, such as high-κ oxide nucleation on a clean Si surface as well as its thermal stability at the poly-Si and Si interfaces. Campbell *et al.* [116] showed that after a high temperature (1000°C) anneal, the metal phase $ZrSi_2$ was formed at the poly-Si/ZrO_2 interface which degraded the electrical properties. On the contrary, Kang *et al.* [117] investigated the thermal stability of the poly-Si/HfO_2 interface and they show good electrical characteristics after a rapid thermal annealing of 1000°C in N_2. Among these dielectrics, HfO_2 is very promising for the next-generation gate dielectric of MOSFETs, because of its high dielectric constant, excellent thermal stability, and large band gap, etc. [118], [119].

5.2 Sample Preparation

Standard 6-inch (100) p-type Si wafers, with resistivity of 15-25 Ω-cm, were used in this study. During the sample preparation, there are two deposition instruments available in the study of HfO_2 film, i.e. physical-vapor-deposition (PVD) and metal-organic-chemical-vapor-deposition (MOCVD). In the beginning, the PVD was used to characterize the physical and material property. Some electrical characteristics were also measured. Before hafnium oxide deposition, standard RCA cleaning process was conducted. The deposition of hafnium oxides was carried out by sputtering through a hafnium target in an Ar/O_2 mixture. Either polysilicon or metal, such as Al, Pt, Ta, TiN, etc., were used as the top electrode. For the hafnium oxides prepared using MOCVD, the tetrakis diethylamido hafnium (TDEAH) precursor was deposited by atomic vapor deposition (AVD^{TM}) on an AIXTRON Tricent® system at a substrate temperature of 400°C in oxygen ambient. Sample characterization was done by using a combination of characterization techniques such as optical reflectivity for film thickness measurements and the determination of the optical band gap, transmission electron microscopy (TEM) to determine the gate stack structure and the thickness of various layers, capacitance–voltage (*C*–*V*) measurements using Agilent 4284A precision LCR meter for measurements of equivalent electrical thickness (defined as the thickness of a SiO_2 layer with equivalent gate capacitance) and current–voltage (*I*–*V*) measurements using Keithley Model 4200-SCS to evaluate the leakage currents. By comparing the results of these techniques, accurate values of the dielectric constant as a function of oxide composition have been achieved. Finally, some attention will be given to the thermal stability of the hafnium oxide on Si.

5.3 Material Analysis of HfO_2 Dielectric Film

5.3.1 TEM Analysis

Cross sectional high-resolution transmission electron microscopy analysis was carried out for hafnium oxide films. Figure 5.1 depicts the thickness of the hafnium oxide as a function of the deposition time. Both the experimental data (dotted) and the linear regression were shown in the figure. The thickness after post-deposition annealing (PDA) of 800°C by rapid-thermal-annealing (RTA) in O_2 and N_2 ambient for 30 sec were also plotted. The film thickness increased after PDA indicates the as-deposited hafnium oxide was not optimized in its bonding and film structure. The film hardness also enhanced after PDA treatment. Figure 5.2 shows the high-resolution TEM images of a 4.5 nm HfO_2 film, which was deposited by sputtering with the power of 100 W for 300 sec. The top electrode is poly-Si and the PDA treatment condition is 800°C in O_2 ambient for 30 sec. The interfacial layer between HfO_2/Si, which is believed to be hafnium silicate comprising HfO_2 and SiO_2, can be seen clearly. This relatively thick layer is likely formed because the HfO_2 is sputtered from a hafnium target in an argon/oxygen gas mixture. This oxidizing ambient favors nucleation of an initial SiO_2 film before the hafnium oxide film is formed. Figure 5.3 shows the high-resolution TEM images of Pt/HfO_2/Si with an HfO_2 thickness of 3.4 nm. Figure 5.3(b) shows the same picture of Figure 5.3(a) with higher resolution. The HfO_2 is amorphous and the interfacial layer is visible in the picture. It should be noted that all of the samples studied showed amorphous HfO_2, which demonstrates the stability of HfO_2 films in direct contact with Si after anneal at high temperature.

5.3.2 Optical Analysis

For optical evaluation an *n* and *k* analyzer [120] was used. From a single reflectance measurement from 190 to 900 nm, this technique computes univocal values of the index of refraction $n(\lambda)$, extinction coefficient $k(\lambda)$, and film thickness *d*. The fitting algorithm utilizes the Forouhi-Bloomer equations [121] for $n(\lambda)$ and $k(\lambda)$. These equations describe the index of refraction, $n(E)$, and the extinction coefficient, $k(E)$, as function of the energy *E* or λ for a wide variety of semiconductors and dielectrics produced under a variety of processing conditions. They are given as

$$k(E)=\sum_{i}^{q}\frac{A_i(E-E_g)^2}{E^2-B_iE+C_i}\text{, and} \tag{5.1}$$

$$n(E)=n(\infty)+\sum_{i}^{q}\frac{B_{0i}E+C_{0i}}{E^2-B_iE+C_i}. \tag{5.2}$$

The integer "*q*" in Equations (5.1) and (5.2) specifies the number of terms. Each term in the sum for $k(E)$ and the sum for $n(E)$ contributes either a peak or a shoulder to their spectra. The first term ($q=1$) describes the spectra of an amorphous material; the higher order terms ($q \geq 2$)

describe a polycrystalline or crystalline material.

In Equation (5.1), E_g is the optical energy band gap. According to this formulation, E_g represents the energy for which $k(E)$ is an absolute minimum. The parameters A_i, B_i, and C_i depend on the electronic configuration of the material [121]. The parameter $n(\infty)$ represents $\lim_{E\to\infty} n(E)$. The quantities B_{0i} and C_{0i} again are not independent parameters, they depend on A_i, B_i, C_i, and E_g. Equations (5.1) and (5.2) are valid over a very wide range of photon energies spanning ultraviolet, visible, and near infrared. Furthermore, $n(E)$ and $k(E)$ in Equations (5.1) and (5.2) are related through Kramers–Kronig dispersion relation [121]. By comparing measurements with the appropriate algorithm, film thickness, $n(\lambda)$ and $k(\lambda)$ spectra, E_g, and interface roughness can be determined.

Figure 5.4 shows the reflectance spectra for thin HfO_2 films deposited at room temperature. As the film thickness increases, the reflectance decreases in the deep ultraviolet region. These spectra correspond to films thickness from about 4.5 to 14.0 nm. In general, for very thin films some disagreement was found with thickness measured by TEM. However, dielectric constant measurements using TEM and n and k thickness were in good agreement.

5.3.3 Surface Analysis

Chemical surface characterization of various HfO_2 films was accomplished by x-ray photoelectron spectroscopy (XPS) utilizing monochromatic and standard Al x-ray sources. Figure 5.5(a) plots the Hf 4f features for HfO_2 film, which shows the sputtered HfO_2 film has typical HfO_2 chemical bonding structure. Figure 5.5(b) shows a comparison of XPS spectra for several HfO_2 films before and after PDA at 600, 700, 800, and 900°C in oxygen ambient for 30 sec. Conformable spectra were observed for the samples after elevated temperature annealing, which implies the thermal stability of HfO_2 films after annealing is rather stable. Figure 5.6 shows the AFM images of the HfO_2 film surface, the RMS roughness is about 0.14 nm.

5.4 Electrical Characterization of HfO_2 Capacitors with Pt Electrode

The plot of capacitance-voltage (*C*-*V*) characteristics of thin HfO_2 film is shown in Figure 5.7. The electrode of the capacitor is Pt, with an electrode area of 4.5×10^{-4} cm^2. The schematic representation of the capacitor structure is sketched in Figure 5.8. The hafnium oxide film was deposited directly on Si at room temperature for 300 sec and post annealed in oxygen ambient for 30 sec. The largest value of measured capacitance in accumulation is C_{max} = 513 pF, which corresponds to an equivalent oxide thickness of t_{ox} = 3.0 nm, where t_{ox} is the electrical thickness equivalent for pure SiO_2. There is a frequency dependence of the capacitance between 10 kHz and 1 MHz in Figure 5.7, especially for the curve of 1 MHz. Such decrease in capacitance value may be due to the series resistance connecting to the capacitor. Figure 5.9 shows 100 kHz curves of both positive and negative *C*-*V* sweeps, which gives a hysteresis of less than 110 mV.

The plot of the corresponding current-voltage (*I*-*V*) characteristics for the film represented in Figure 5.7 is shown in Figure 5.10. The leakage current is about 10^{-2} A/cm^2 at the bias of 1.0 V. This value seems a little bit larger for using as a gate dielectric in the MOSFETs.

5.5 HfO_2 MIS Capacitor with Copper Gate Electrode

5.5.1 Motivation of Incorporating Copper Gate Electrode

Recently, Cu has successfully replaced the conventional aluminum alloys as the interconnect metal in the advanced ULSI manufacturing, due to its superior conductivity and better electromigration resistance. Despite its success as the metal interconnect of choice, Cu has still not gained acceptance as the gate electrode of the transistor because the positively charged Cu ions are known to drift very rapidly in thermal oxide under the influence of electric field, and can cause severe reliability degradation in oxide [122].

For the high-κ dielectrics, replacing the conventional polysilicon gate electrode with metal gate has been proposed because of the interface instability between the high-κ dielectrics and polysilicon gate [119], [123]–[125]. However, Cu has never been under consideration, to the best of our knowledge, mainly because of the concern of the rapid Cu ion drift in the dielectric as mentioned above. In this work, Cu was used for the first time as the metal gate electrode directly on top of a high-κ dielectric, i.e., HfO_2. Based on the results from the bias-temperature stress (BTS) and charge-to-breakdown (Q_{BD}) measurement, the HfO_2-based Cu-gate capacitors show not only enhanced capacitance but also no noticeable reliability degradation compared to Al-gate counterparts. Our results strongly suggest the feasibility of a full Cu process from the gate electrode to the back-end-of-line (BEOL) in future ULSI fabrication.

5.5.2 Experimental Procedure

Standard 6-inch (100) p-type Si wafers, with resistivity of 15-25 Ω-cm, were used in this study. Following a standard RCA cleaning process, a layer of 10-nm-thick HfO_2 using tetrakis diethylamido hafnium (TDEAH) precursor was deposited by atomic vapor deposition (AVD^{TM}) on an AIXTRON Tricent® system at a substrate temperature of 400°C in oxygen ambient. Wafers were subsequently split into two groups. 500-nm-thick Cu was sputtered through a metal mask as the gate electrode for one group, with 500-nm-thick Al for the control group. Finally, all wafers received a 500-nm-thick Al deposition on the wafer backside. The device area is 1.7×10^{-4} cm^2. It is worth noting that control wafers with 10-nm-thick SiO_2 dielectric were also fabricated in this study for comparison. The current-voltage (I-V) characteristics were measured using Keithley Model 4200-SCS Semiconductor Characterization System, and the capacitance was measured using Agilent 4284A precision LCR meter at a frequency of 100 kHz. Constant current stress (CCS) was conducted for evaluating reliability. In order to investigate the thermal stability of HfO_2 film with Cu electrode, an effective electric field of +1 MV/cm at elevated temperatures ranging from 100 to 200°C was applied to the gate stacks for bias-temperature stress (BTS) testing.

5.5.3 Capacitor Characterization and Bias Temperature Stressing

Figure 5.11(a) displays typical capacitance-voltage (C-V) characteristics of Cu/SiO_2/Si and Al/SiO_2/Si capacitors, both before and after BTS test, at 150°C for 1000 sec. The applied field was +1 MV/cm. A significant negative flatband voltage (V_{FB}) shift of about −0.4 V is observed for the Cu/SiO_2/Si capacitor, indicating that positively bulk charges (i.e., Cu ions) are introduced into the dielectric [126]. In contrast, only negligible V_{FB} shift is found for the Al/SiO_2/Si capacitors after BTS test. It is well known that Al is quite stable in contact with SiO_2. This is because a very thin self-limiting Al_2O_3 layer is formed between the Al electrode and SiO_2, and acts as a good diffusion barrier for further element diffusion and/or reaction [127]. Figure 5.11(b) exhibits the *C-V* characteristics of $Cu/HfO_2/Si$ and $Al/HfO_2/Si$ capacitors before and after BTS test at +1 MV/cm, 150°C for 1000 sec. Quite amazingly, there is essentially no V_{FB} shift observed after BTS. Although slightly larger V_{FB} value was observed for $Cu/HfO_2/Si$ capacitor, the corresponding work function (4.9 eV) still fell into the required window for p-channel devices. Figure 5.12(a) shows the *I-V* curves of $Cu/HfO_2/Si$ capacitors before and after BTS at 150°C for 1000 sec. The current levels are basically unchanged for the $Cu/HfO_2/Si$ capacitor after BTS. Figure 5.12(b) shows the gate current and substrate current variation curves during the bias-temperature stressing. Figure 5.13 depicts the typical *C-V* curves of $Cu/HfO_2/Si$ capacitors at frequencies varies from 1 kHz to 1 MHz. Similar to the previous work, significant degradation in the capacitance at accumulation was found at the frequency of 1 MHz. And the hump that occurred for the lower frequencies suggests the interface state exists in the $Cu/HfO_2/Si$ capacitor measured. Nevertheless, this result indicates that HfO_2 is electrically stable with Cu gate electrode. It is speculated that the stability is due to the considerably high density of HfO_2 (9.68 g/cm^3) [128], which is more than two times that of Al_2O_3 (3.97 g/cm^3). As a result, HfO_2 serves not only as a promising gate dielectric but also an excellent barrier against Cu diffusion, even though the density data quoted above are for bulk materials rather than thin films. Figure 5.14 depicts V_{FB} shifts of $Cu/HfO_2/Si$, $Al/HfO_2/Si$, $Cu/SiO_2/Si$, and $Al/SiO_2/Si$ capacitors as a function of temperature ranging from 100 to 200°C after BTS test. The BTS stress was performed at +1 MV/cm for 1000 sec. Clearly, V_{FB} shifts are negligible except for the $Cu/SiO_2/Si$ capacitors. These results imply that HfO_2 can effectively block Cu ion drift at least up to 200°C.

5.5.4 Constant Current Stress and Charge-to-Breakdown

Figure 5.15 shows the typical *I-V* curves of HfO_2 and SiO_2 MIS capacitors. Obviously, the breakdown voltage for the SiO_2 capacitor is nearly three times larger than that of the HfO_2 capacitor. Figure 5.16 shows the gate voltage variation as a function of time for the SiO_2 and HfO_2 capacitors with different gate electrodes, when subjected to CCS. The stressing current used was -1 mA/cm^2. The reason why we used such low current density for stressing is owing to the fact that the Q_{BD} is extremely hard to be monitored under the condition of -100 mA/cm^2 for the Cu/SiO_2/Si capacitors when Cu was incorporated. In the case of SiO_2 capacitors, a larger voltage shift observed in the Cu-gate capacitor, compared to the Al-gate counterpart, implies the incorporation of Cu ions into SiO_2 dielectric during BTS test does result in higher electron trapping rate. By contrast, different metal gates (i.e., Al and Cu) only lead to indiscernible change in gate voltage shift during CCS for the HfO_2-based capacitors. These results suggest that the SiO_2 dielectric is more vulnerable than HfO_2 to Cu diffusion. As a result, the SiO_2 capacitors will breakdown more easily when Cu is employed as the gate electrode. Noticeably, the gate voltage variation curve for the HfO_2 capacitor as a function of stressing time is very rough in nature, as shown in Figure 5.17(a). This behaves totally different from the smooth curve for the SiO_2 capacitor, as shown in Figure 5.17(b). The charging-discharging effect is implied to take place anytime for the HfO_2 capacitors, even when the initial stage of the CCS. Figure 5.18 shows the Weibull distributions of the charge-to-breakdown (Q_{BD}) for all four capacitor configurations. Consistent with the results in Figure 5.16, the value of 63% Q_{BD} for the Cu-gate SiO_2 capacitors is more than one order of magnitude lower than that for the Al-gate SiO_2 capacitors. This severe reliability degradation is the main reason why Cu is excluded from the conventional FEOL processes of silicon-based ULSI manufacturing. However, our finding strongly indicates that this is no longer an issue for the HfO_2 dielectric. From the cumulative Q_{BD} plots of HfO_2 capacitors with the Cu and Al gate electrodes, no significant difference is observed between the two groups, indicating that Cu diffusion has only negligible effects on the reliability of

HfO_2-based capacitors. No degradation was observed even though 4-nm-thick HfO_2 was used in Cu/HfO_2/Si capacitor, as shown in Figure 5.18 [129]. Moreover, the mechanism is mainly soft breakdown in such HfO_2 film. It is notable here that flatband voltage shifts were taken place for some of the samples using n-type Si. The reason is unknown so far.

5.6 Conclusions

Hafnium oxide film was evaluated as possible candidate material to replace SiO_2 for gate dielectric in complementary metal-oxide-semiconductor technology. Both sputtering and MOCVD methods can be used as the tool of thin-film HfO_2 deposition. In view of the film uniformity and interfacial layer growth, however, sputtering maybe not sufficient to be a production tool in the future.

AVD-deposited HfO_2 capacitors using Cu and Al as the gate electrode have been fabricated and investigated for the first time. The counterparts with thermally grown SiO_2 dielectric were also constructed for comparison. Our results clearly show that HfO_2 dielectric depicts superior resistance against Cu diffusion after BTS test, compared to SiO_2. Moreover, the presence of Cu metal in direct contact with HfO_2 has negligible impact on the reliability of the HfO_2 capacitor. The fact that HfO_2 can behave as a good barrier against Cu diffusion is attributed to its considerably high density. This finding is important as it suggests the feasibility of a Cu integration process from the p-channel gate electrode to BEOL interconnect, which will allow the use of the gate electrode as the first-level metal simultaneously, resulting in a simplified process.

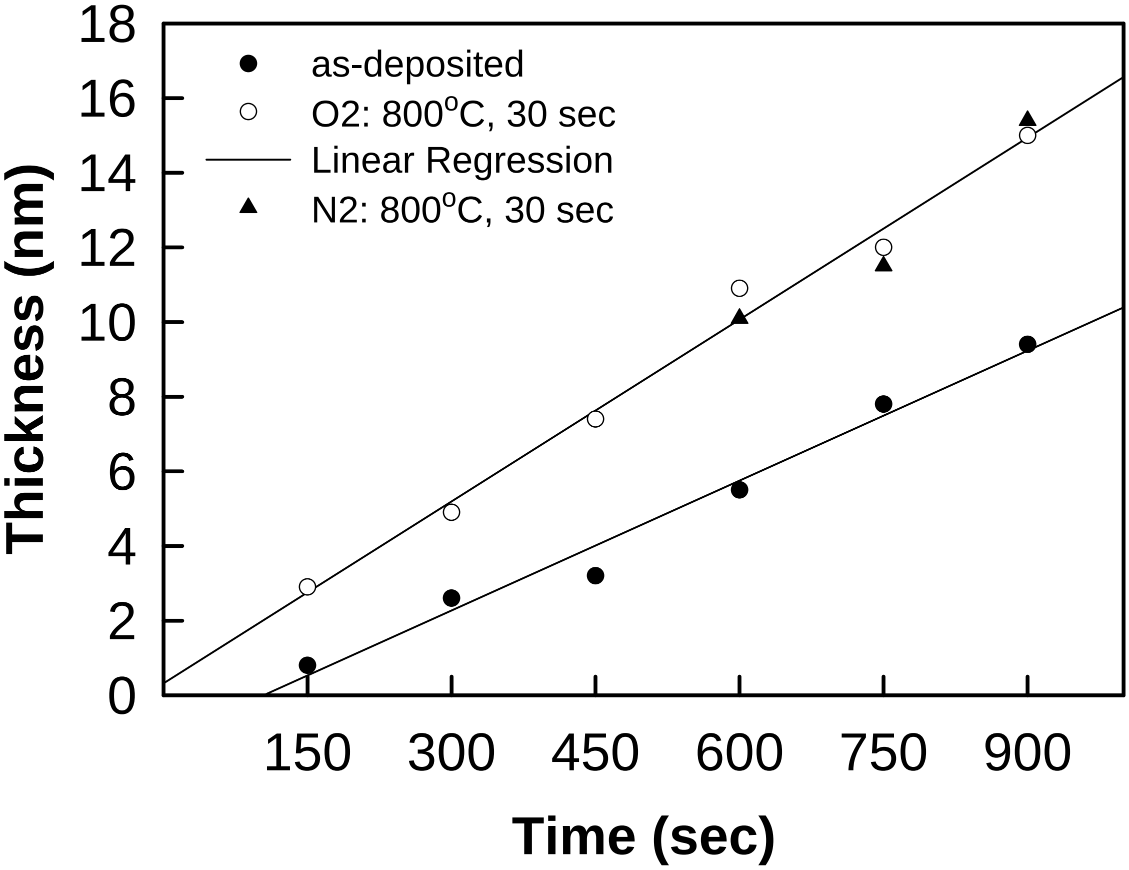
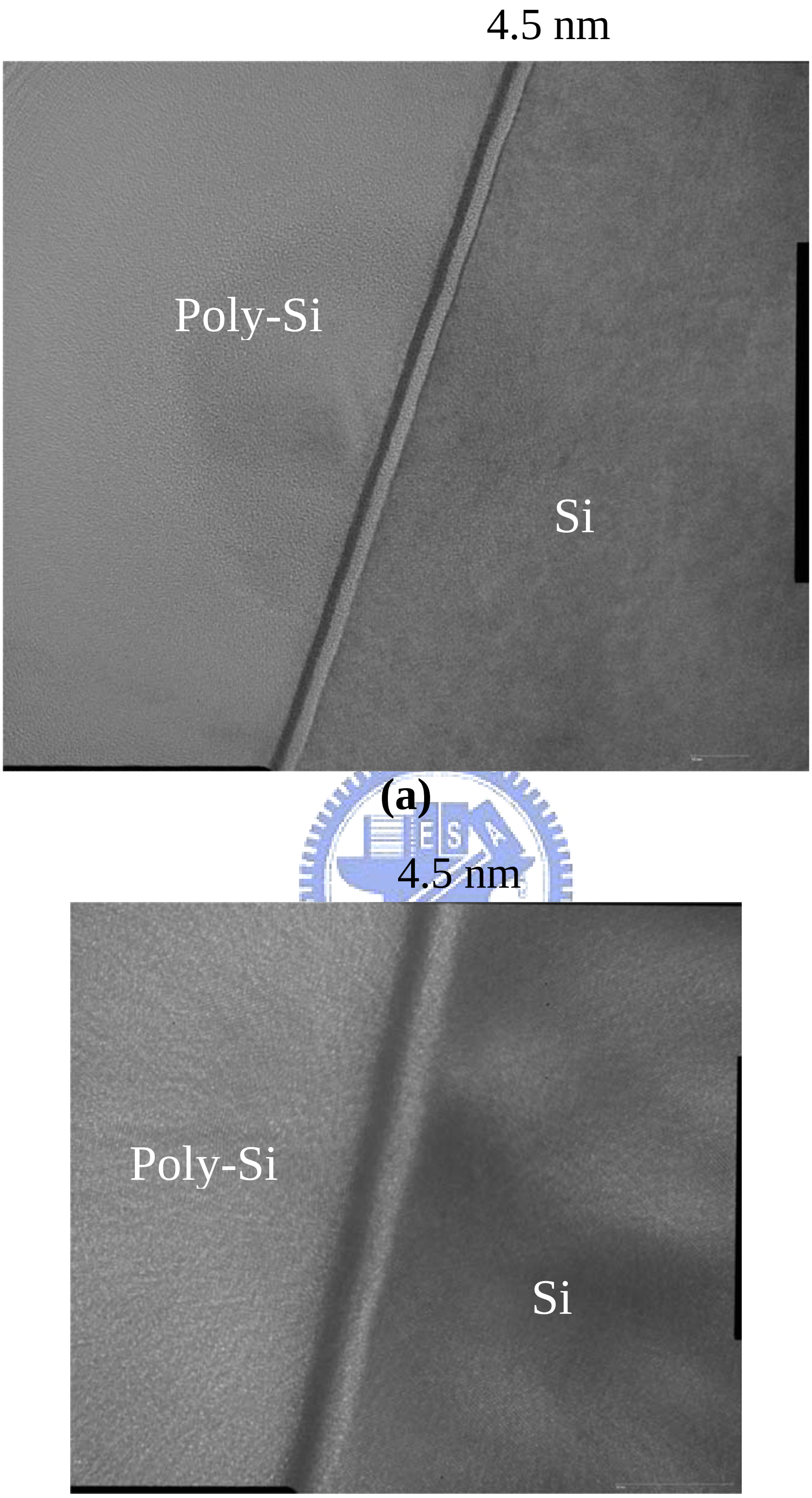


Fig. 5.1 Thickness of HfO_2 film as a function of deposition time before and after O_2 and N_2 ambient annealing.



(b)

Fig. 5.2 TEM picture of HfO_2 film deposited by PVD (a) with the power of 100 W for 300 sec, (b) with higher resolution. The PDA condition is 800°C in O_2 ambient for 30 sec.

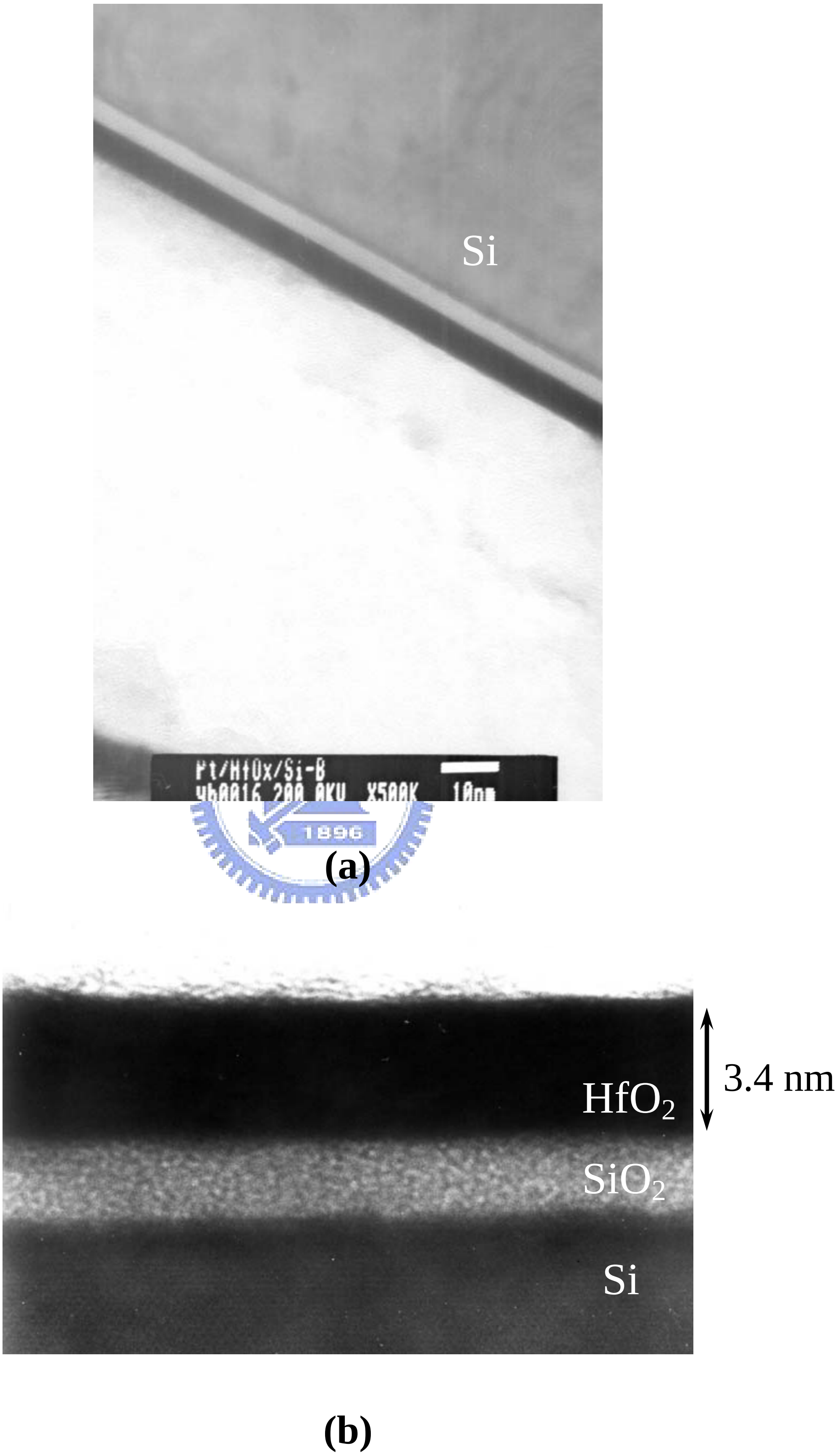


Fig. 5.3 (a) TEM picture of Pt/HfO_2/Si deposited by PVD. (b) TEM picture of Pt/HfO_2/Si deposited by PVD with higher resolution.

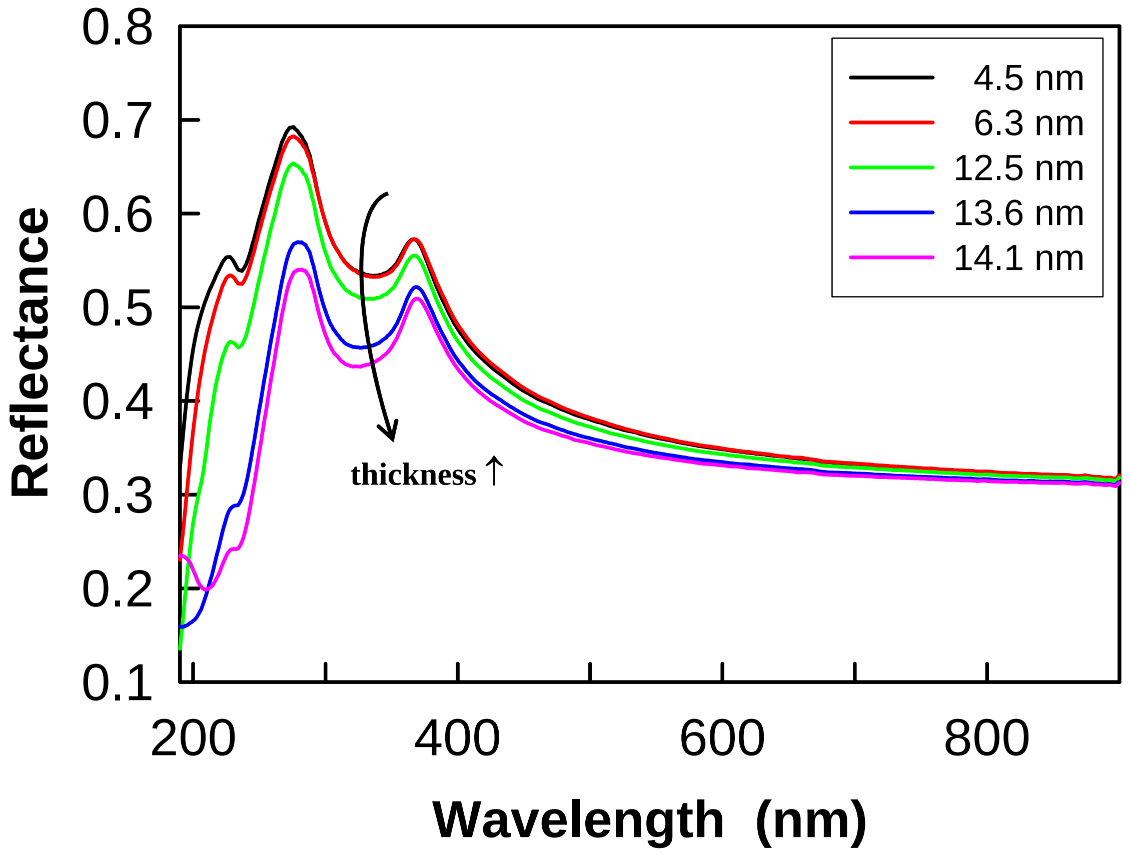


Fig. 5.4 Reflectance spectra of thin HfO_2 films on Si.

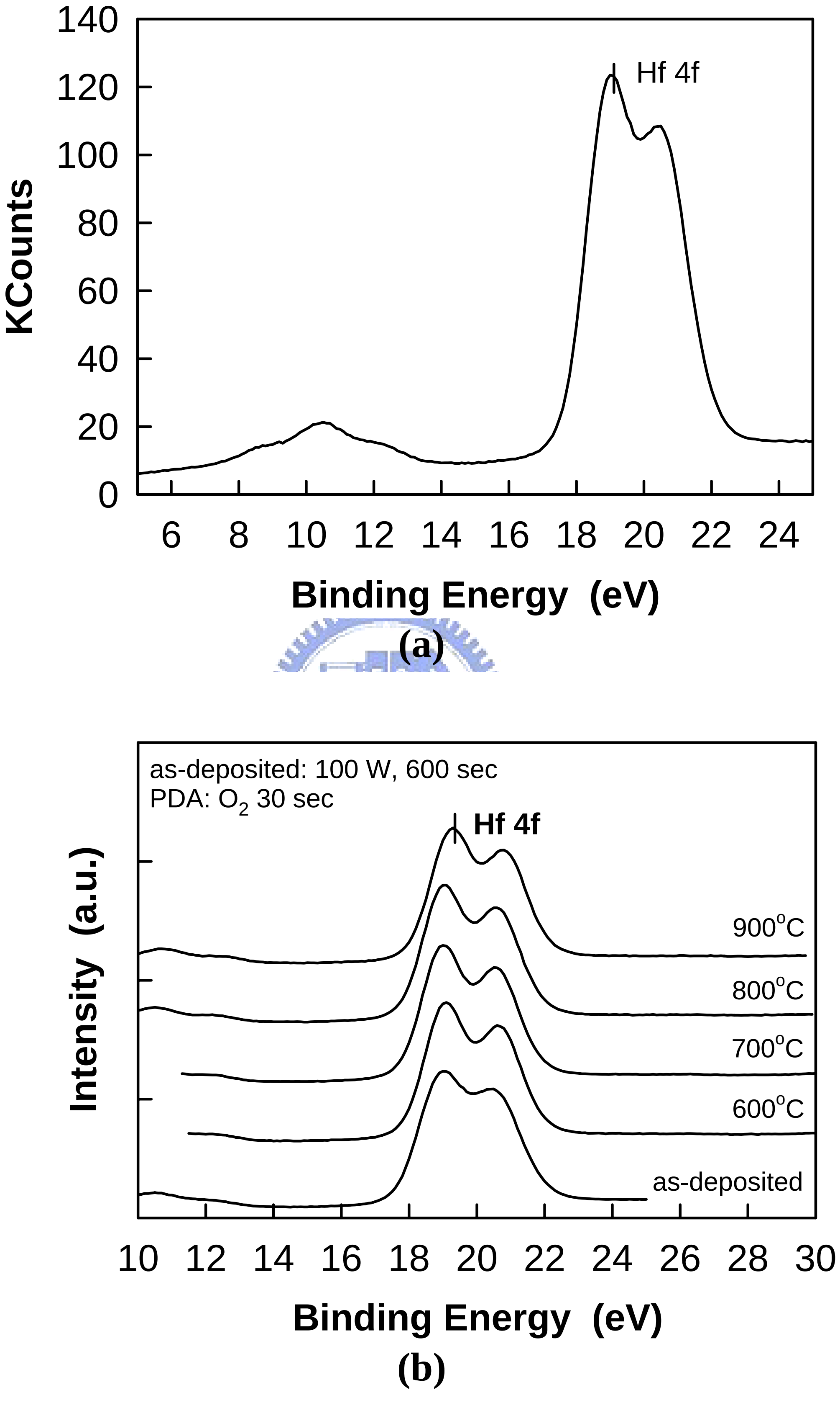


Fig. 5.5 (a) XPS spectrum shows a typical HfO_2 chemical bonding. (b) XPS spectra show HfO_2 chemical bonding after elevated temperature annealing.

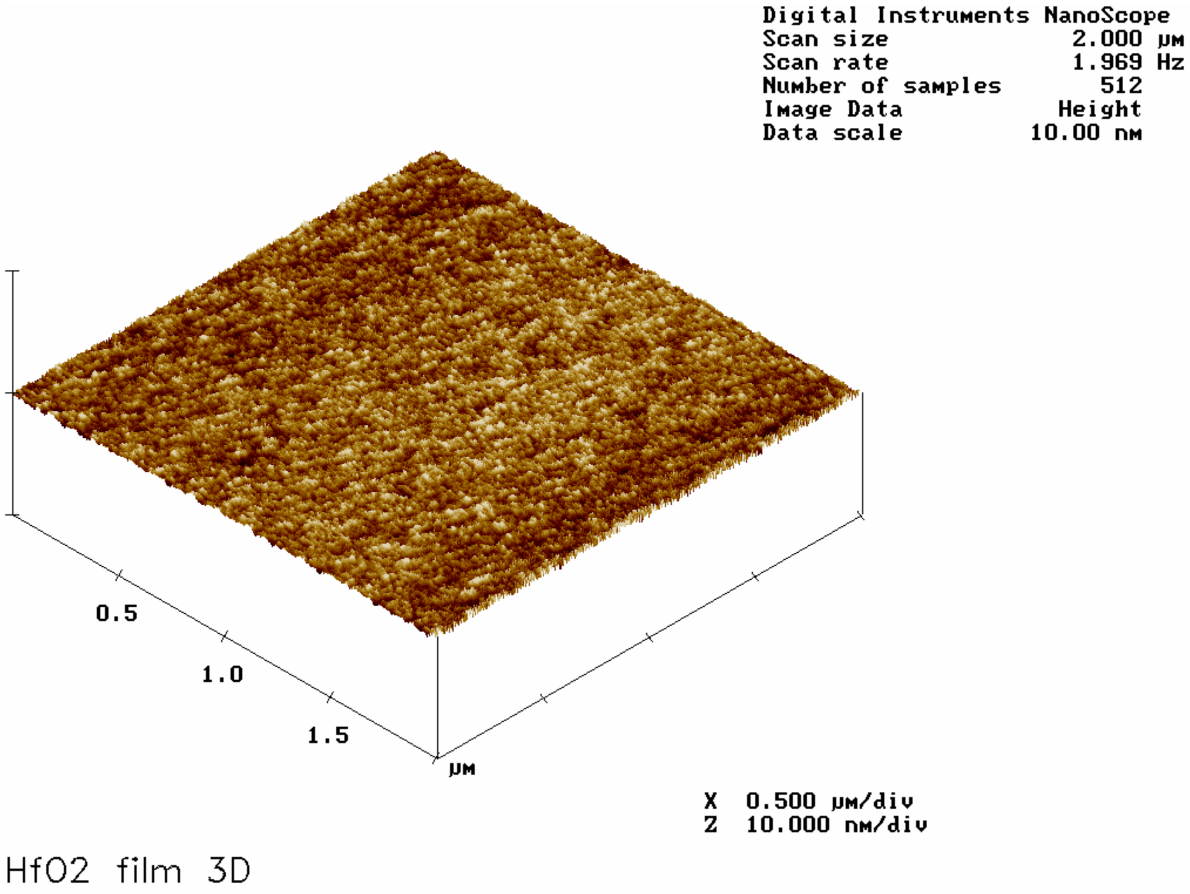


Fig. 5.6 AFM image of HfO_2 on p-Si, the RMS roughness is about 0.14 nm.

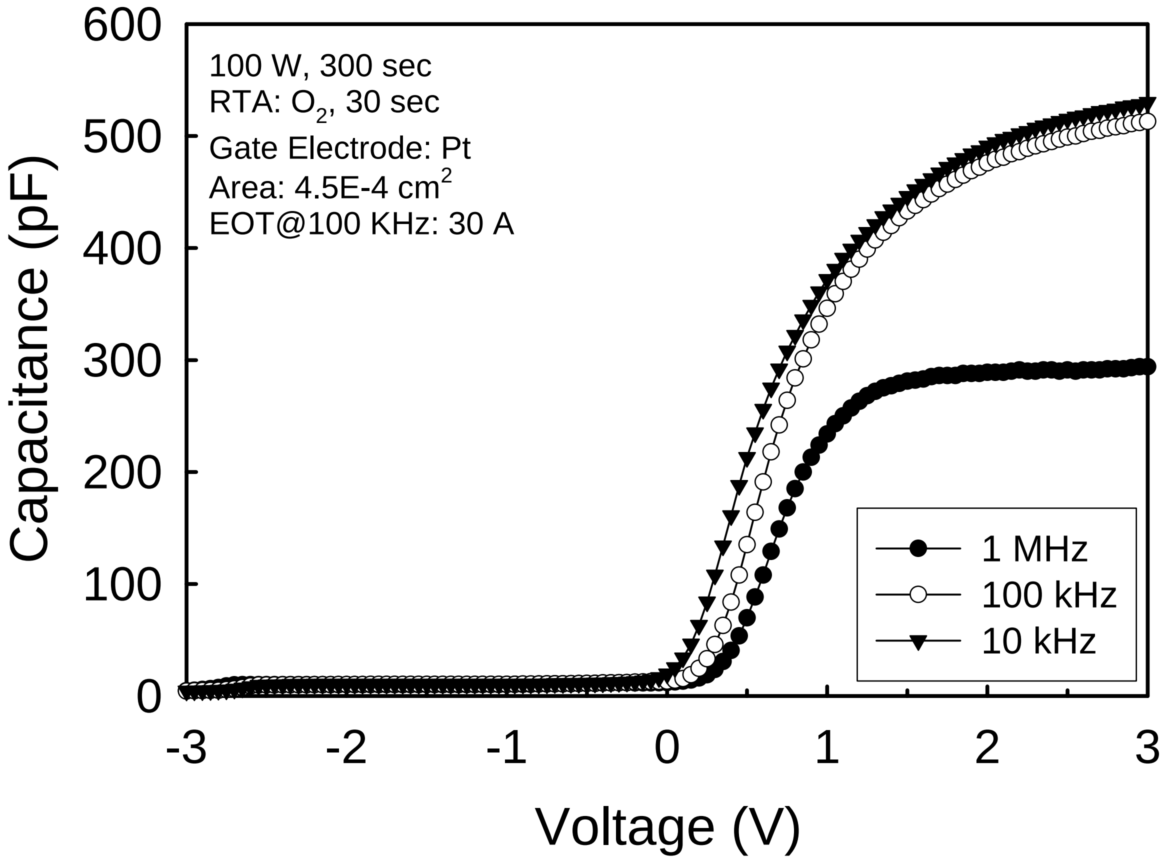


Fig. 5.7 *C-V* curves of a thin-film HfO_2 capacitor with Pt electrode on n-Si substrate.

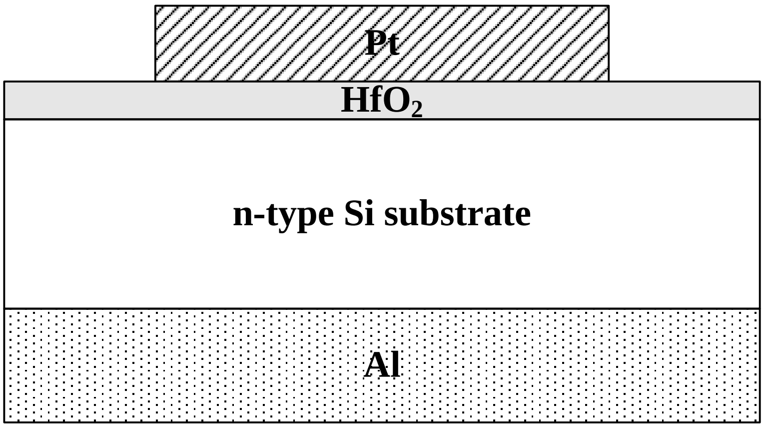


Fig. 5.8 Schematic representation of an HfO_2 capacitor with Pt electrode on n-Si substrate.

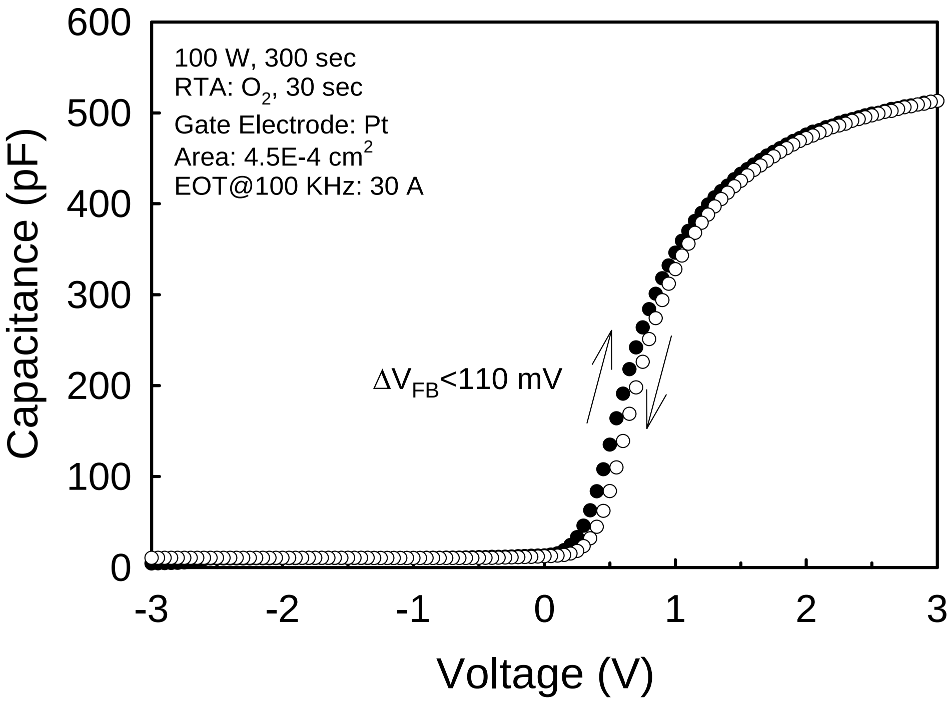


Fig. 5.9 100 kHz curves of both positive and negative *C*-*V* sweeps. The hysteresis is less than 110 mV.

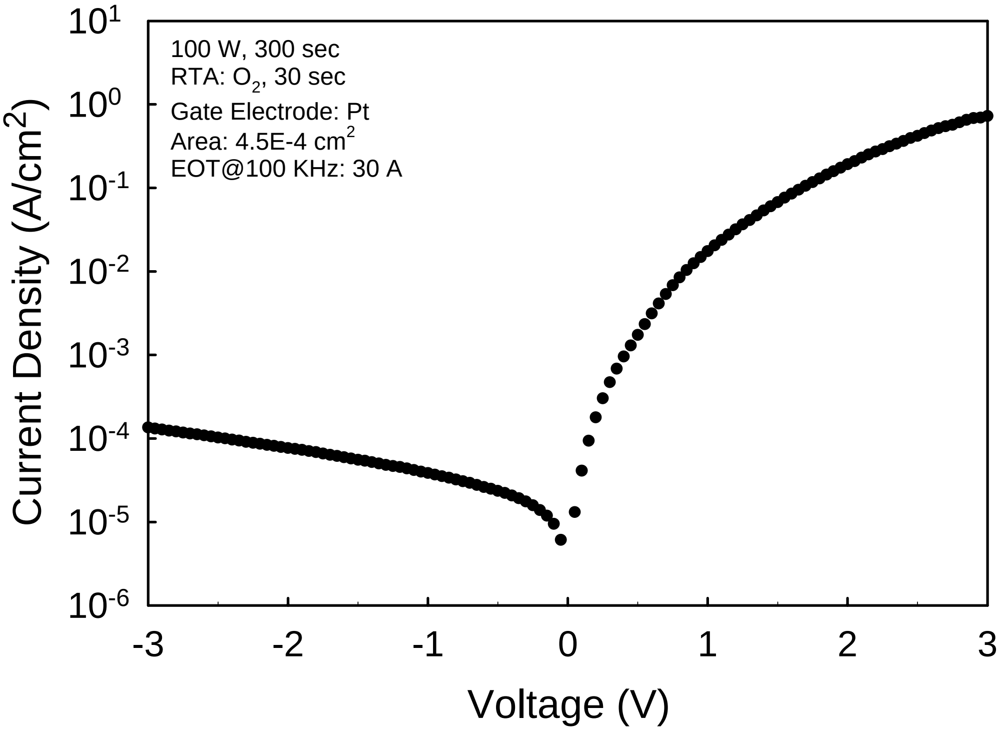


Fig. 5.10 *I*-*V* curves for the film shown in Fig. 5.9.

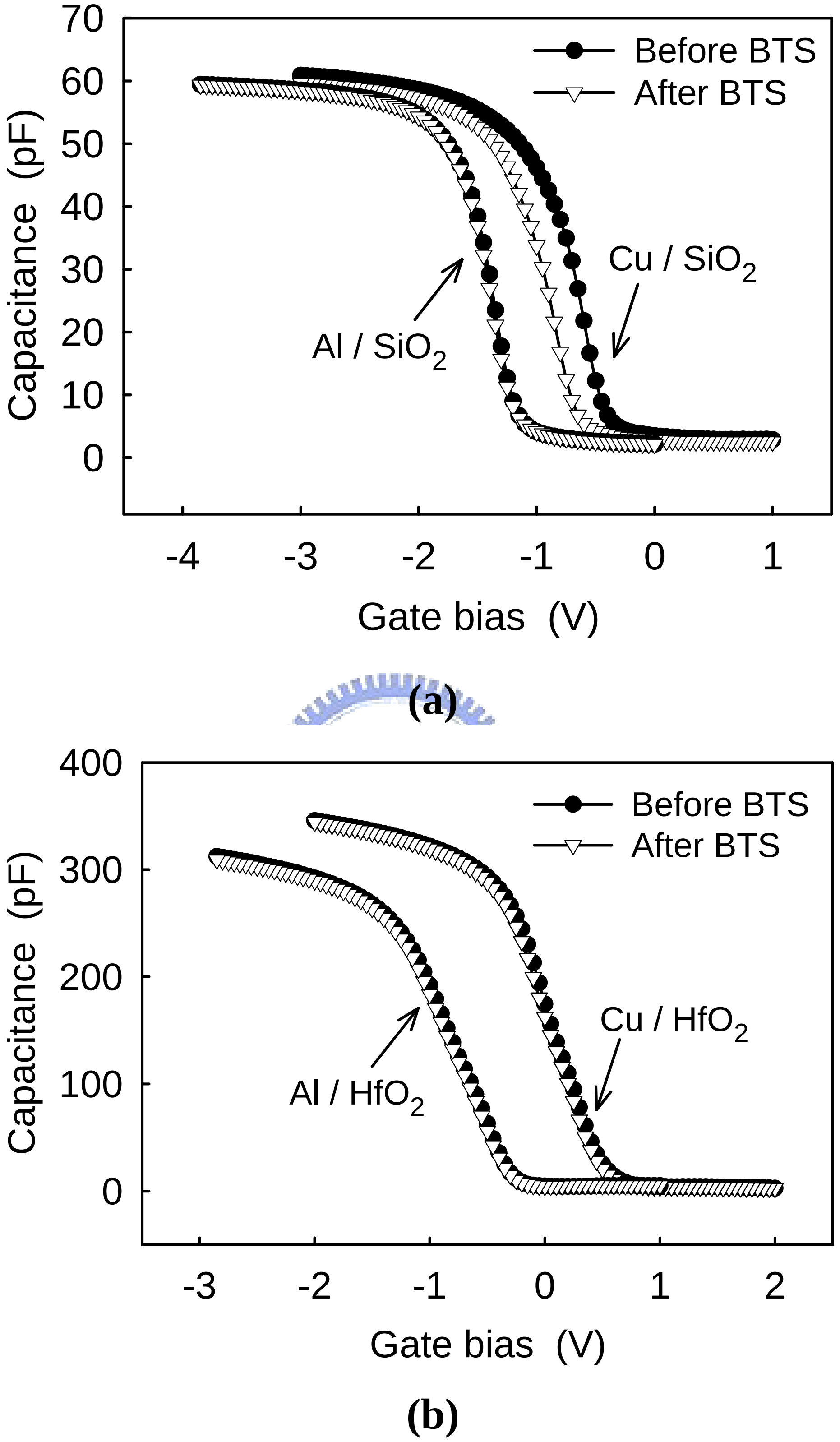
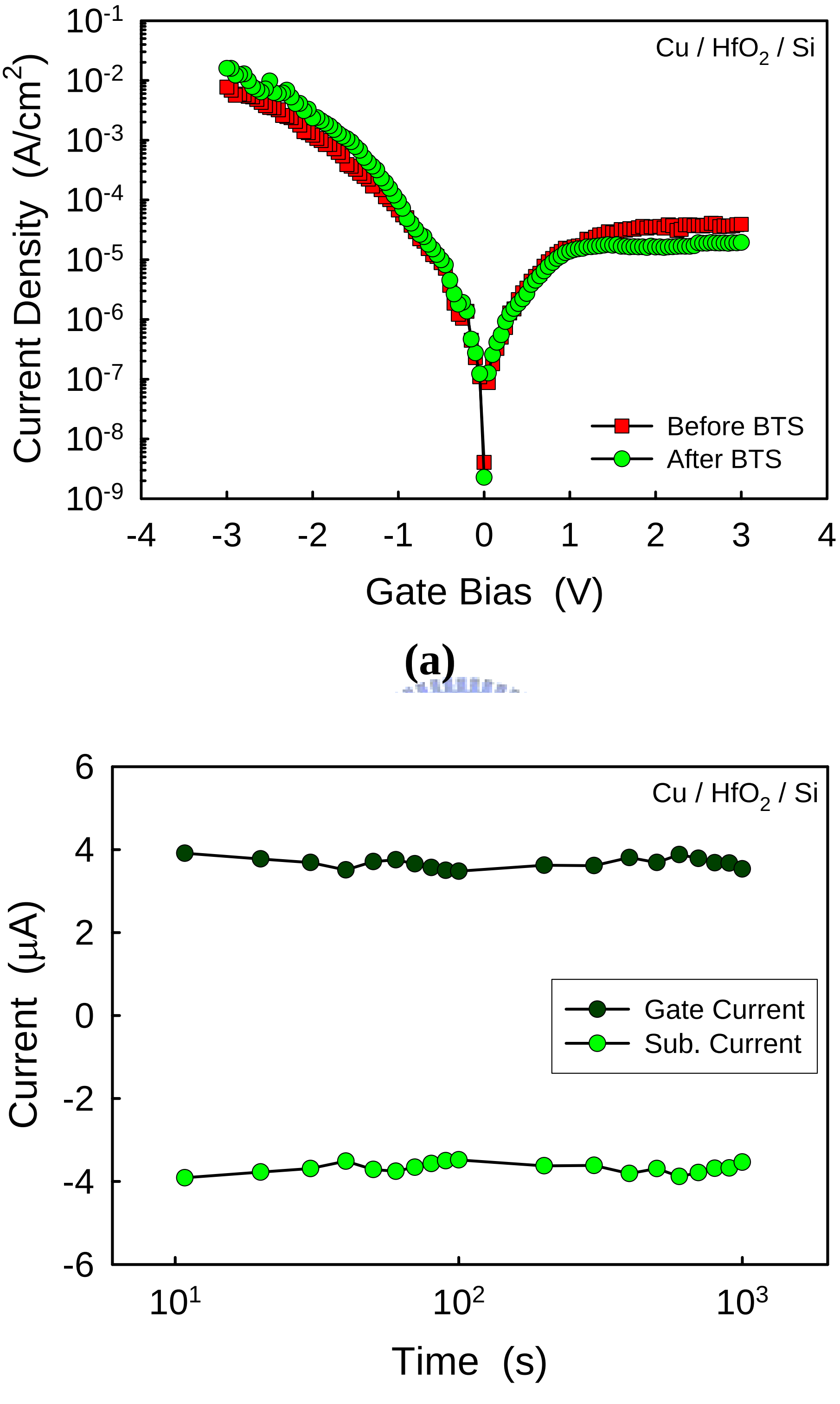


Fig. 5.11 *C-V* curves of (a) Cu/SiO$_2$/Si and Al/SiO$_2$/Si capacitors, (b) Cu/HfO$_2$/Si and Al/HfO$_2$/Si capacitors before and after BTS at 150°C for 1000 sec. The applied field was +1 MV/cm.



(a)

(b)

Fig. 5.12 (a) Typical *I*-*V* curves of Cu/HfO$_2$/Si capacitors before and after BTS at 150°C for 1000 sec. (b) Typical gate current and substrate current variation curves of Cu/HfO$_2$/Si capacitors during BTS. The applied field was +1 MV/cm.

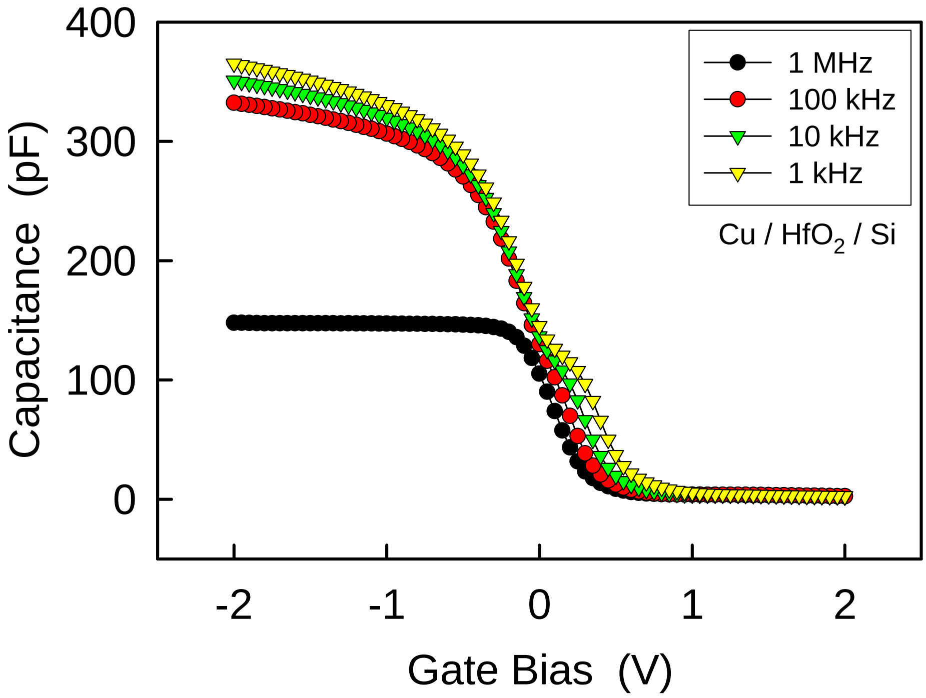


Fig. 5.13 Typical *C-V* curves of Cu/HfO$_2$/Si capacitors at frequencies varies from 1 kHz to 1 MHz.

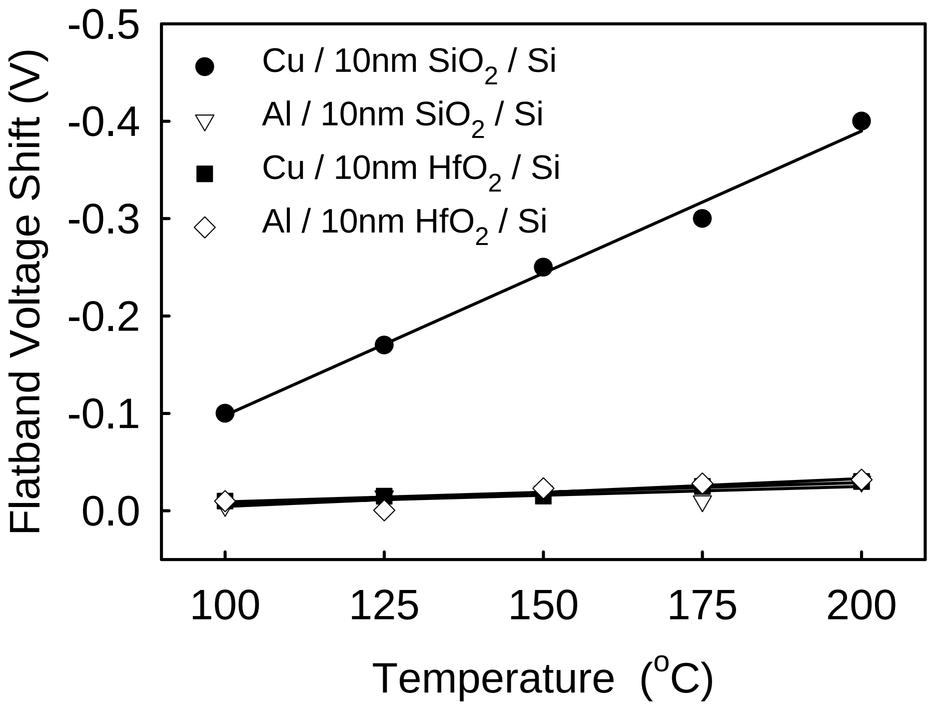


Fig. 5.14 V_{FB} shifts of Cu/SiO$_2$/Si, Al/SiO$_2$/Si, Cu/HfO$_2$/Si, and Al/HfO$_2$/Si capacitors after BTS test at +1 MV/cm for 1000 sec. The temperatures were varied from 100 to 200°C.

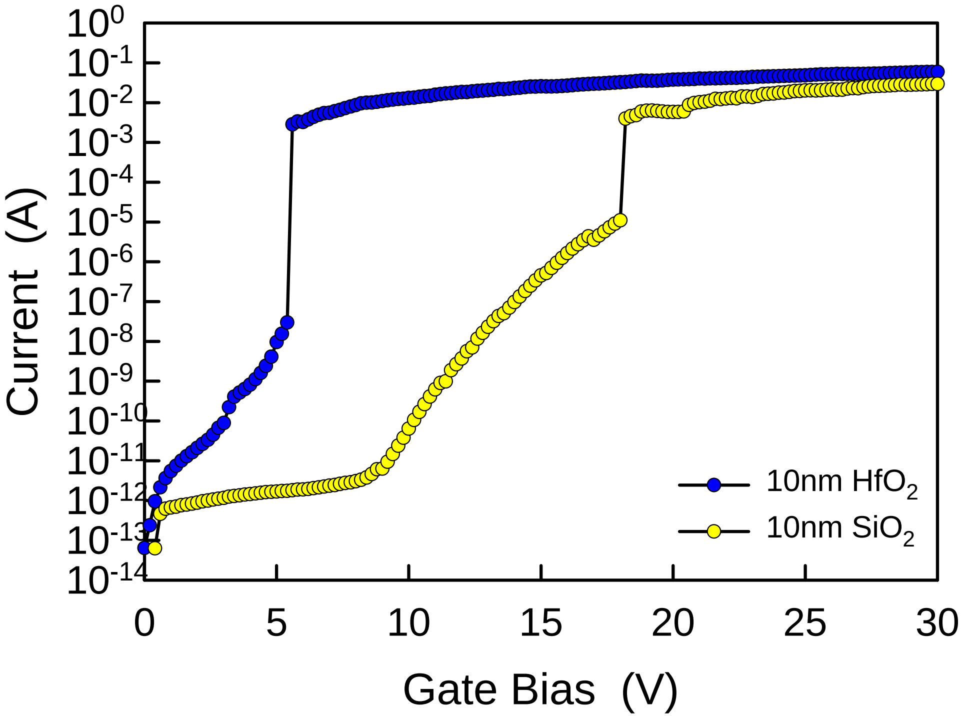


Fig. 5.15 Typical *I-V* curves of HfO_2 and SiO_2 MIS capacitors.

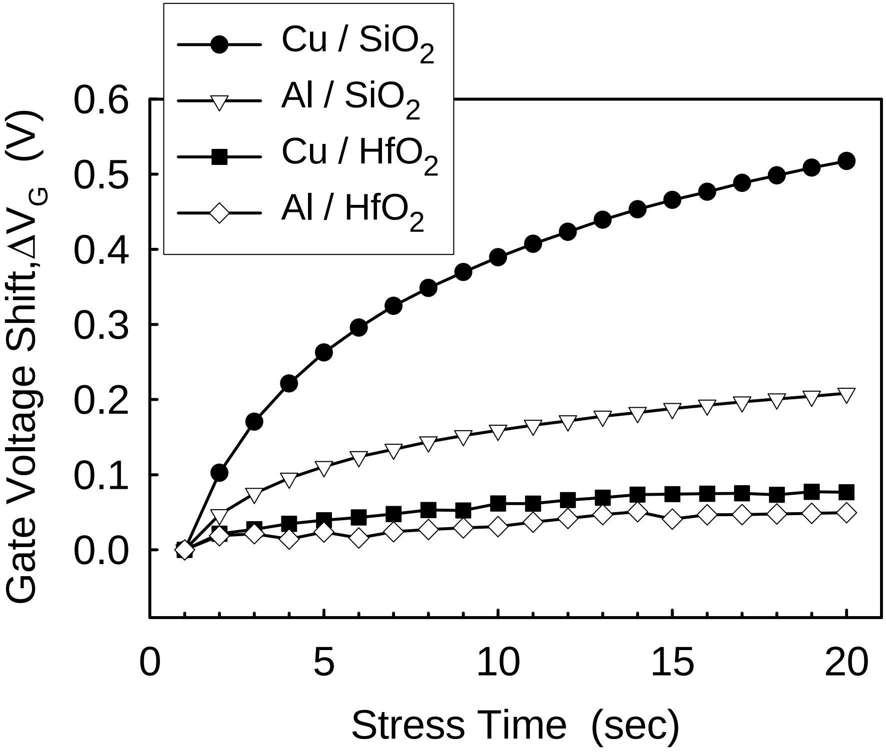
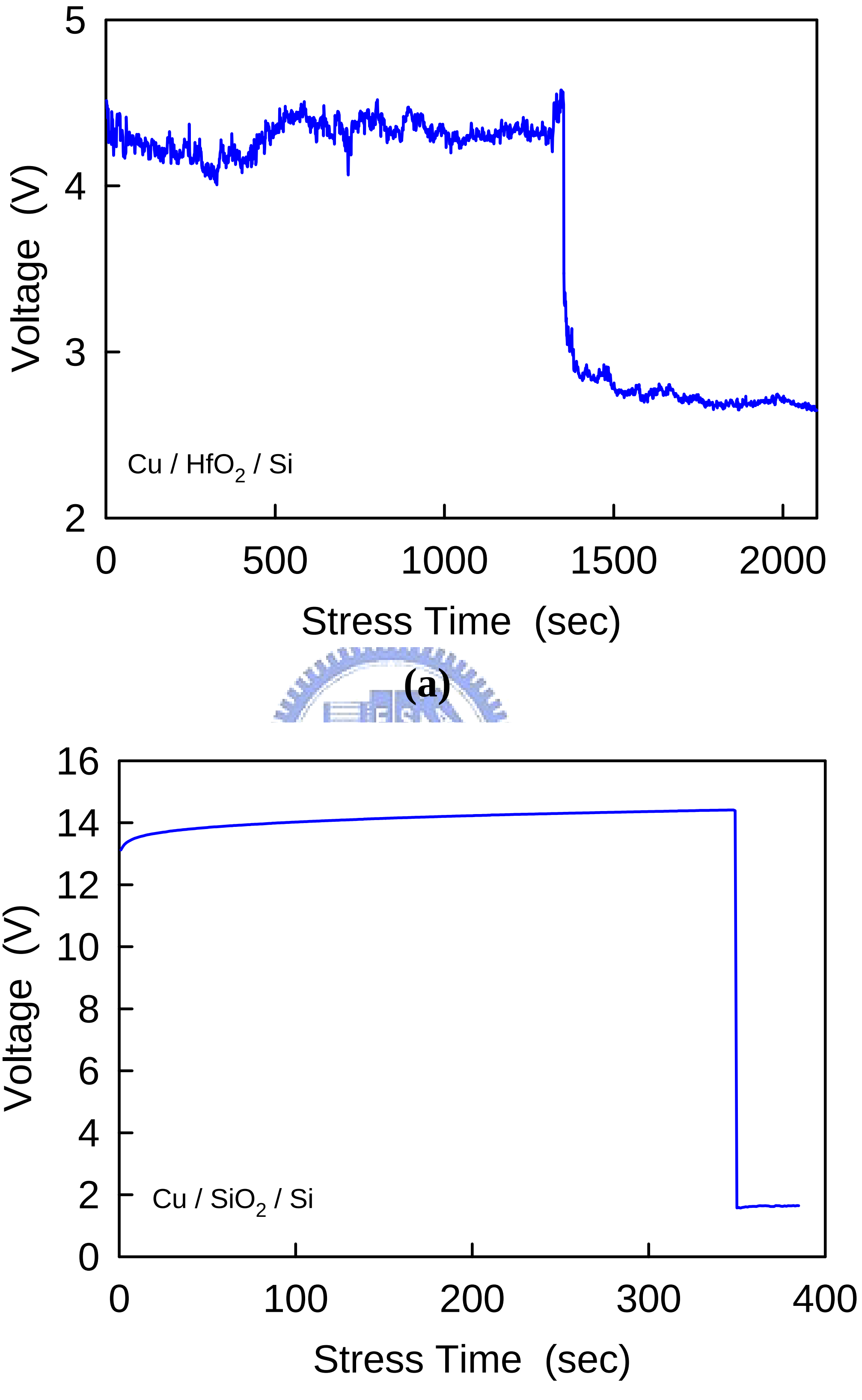


Fig. 5.16 Gate voltage variation of SiO_2 and HfO_2 capacitors with Cu and Al gate electrodes subjected to CCS as a function of time.



(a)

(b)

Fig. 5.17 Gate voltage variation of (a) HfO_2 and (b) SiO_2 capacitors with Cu gate electrodes subjected to CCS as a function of time.

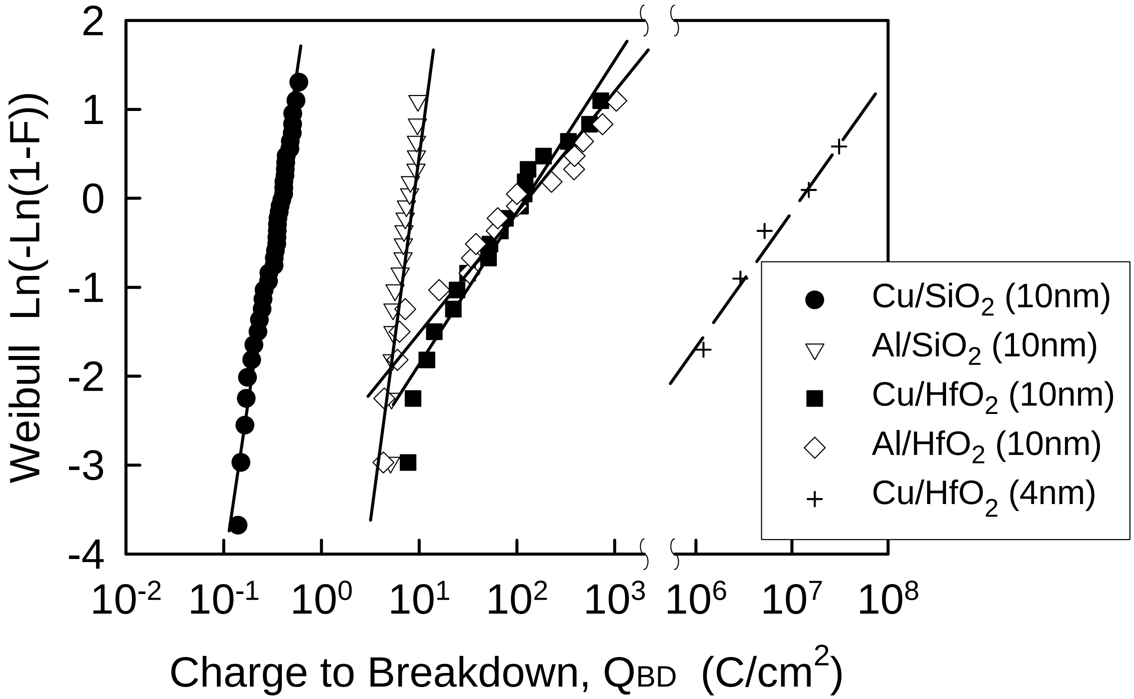


Fig. 5.18 Cumulative Q_{BD} plots of Cu/HfO_2/Si, Al/HfO_2/Si, Cu/SiO_2/Si, and Al/SiO_2/Si capacitors.

Chapter 6

Investigation of HfO_2 Dielectrics for Inter-Poly Dielectrics and Metal-Insulator-Metal Capacitors

6.1 Introduction

It is well known that the capacitance of a parallel-plate capacitor is normally a function of the area of the electrode, the dielectric constant of the dielectric, and the thickness of the dielectric. Both top electrode and bottom electrode of the capacitor under consideration are assumed to be metallic conductors with high conductance. However, if one of the electrodes is n^+/p^+ polysilicon, a depletion region extending into the polysilicon is formed at the polysilicon/dielectric interface, thereby rendering the capacitance of such a structure somewhat lower than that if both electrodes had been metallic. In recent years, the inter-poly dielectrics (IPDs) and metal-insulator-metal (MIM) capacitors in next-generation nonvolatile memories (NVMs) and silicon radio-frequency (RF) applications have attracted great attention. The scaling down of IPDs is important with a large gate coupling coefficient, small cell size, and low programming voltage [130]. For MIM capacitors, the advantages are high conductive electrodes and low parasitic capacitance compared to IPDs [131].

In recent years, the dramatic increase in wired and wireless communications has demanded the need for high quality passives for analog and mixed signal applications. MIM capacitors using one of the standard back-end metal layers as bottom electrode have emerged as key passive components for microprocessors, high frequency circuits, and mixed-signal integrated circuits applications [132], [133]. Compared with double poly linear capacitors, they offer the advantages of reduced series resistance and lower parasitic capacitance [134]. A high capacitance density is important for a MIM capacitor to increase the circuit density and reduce the cell area and cost. Therefore, adoption of high-k material like Al_2O_3 or HfO_2 is a very efficient way to increase the capacitance density [135]. Silicon oxide and silicon nitride are dielectrics that are commonly used in conventional capacitors, but their capacitance densities are limited due to low dielectric constants. It is expected to be one solution to enhance the capacitance density by using higher dielectric constant materials. Among various high-*k* dielectric candidates, HfO_2 has been investigated as a promising material in gate dielectric of MOSFETs due to its high dielectric constant, excellent thermal stability, and high band gap. [136]. In addition, excellent MOS capacitors with HfO_2 have also been demonstrated [137]. Therefore, it seems that HfO_2 is a promising candidate for the above applications. In this work, MIM capacitors with HfO_2 dielectrics have been fabricated and investigated. Experimental results show low leakage current of ~5×10^{-9} A/cm^2 and high capacitance density of ~3.4 fF/μm^2 at 100 kHz in the MIM capacitors. The temperature coefficient and frequency dispersion effect for these MIM capacitors were very small. Different metal electrodes like tantalum, aluminum, and copper were also investigated and compared. Finally, the mechanism of electrical transport was extracted for the HfO_2 MIM capacitors.

6.2 Experimental Procedure

Standard 6-in (150-mm) Si wafers, with a resistivity of 15-25 Ω-cm, were used in this study. An additional 500-nm thermal SiO_2 was grown on the Si substrate to increase the substrate isolation. The IPDs and MIM capacitors with HfO_2 films were subsequently formed on the 500-nm SiO_2. Before high-*k* dielectrics deposition, a layer of 200-nm-thick low-pressure-chemical-vapor-deposition (LPCVD) polysilicon was deposited and doped as the bottom electrode of the IPDs. HfO_2 films (20-nm) were then prepared by metal-organic-chemical-vapor-deposition (MOCVD) at 345°C. After that, a layer of 200-nm-thick LPCVD polysilicon was deposited and doped as the top electrode. A photolithography step and dry etching were subsequently conducted to define the IPDs. Finally, rapid thermal annealing (RTA) was performed at 600°C in N_2 ambient for 30 sec. For the case of MIM capacitors fabrication, a layer of 100-nm-thick HfN film was deposited on SiO_2 as the bottom electrode. Following that, HfO_2 film (20-nm) and TiN film were deposited and patterned in sequence. All these processes are performed at room temperature.

In the second part of this work, on the other hand, the procedure was described as follow. After an additional 500-nm thermal SiO_2 was grown on the Si substrate to increase the substrate isolation. The MIM capacitors with HfO_2 films were subsequently formed on the 500-nm SiO_2. Before high-*k* dielectrics deposition, a layer of Ta film was deposited by sputtering on SiO_2 as the bottom electrode. HfO_2 films (50-nm) were then prepared by sputtering in O_2 ambient. After that, a layer of Ta film was deposited as the top electrode. The pattern of the MIM capacitors was defined using a metal mask. The counterparts of the MIM capacitors with Al and Cu metals as the top electrodes were also fabricated for comparison. Finally, furnace annealing was conducted at 400°C in N_2 ambient for 30 min.

The leakage current was measured using a Keithley Model 4200-SCS Semiconductor Characterization System, and the capacitance was measured using an Agilent 4284A precision LCR meter at frequencies varied from 1 kHz to 1 MHz. In order to investigate the thermal stability of the high-k dielectric film, thermal stresses were performed with measurement temperatures varied from 25°C to 125°C.

6.3 Comparison of Inter-Poly Dielectrics and Metal-Insulator-Metal Capacitors

Figure 6.1 shows the current density-voltage (*J*-*V*) characteristics of the HfO_2 IPD and MIM capacitors. The leakage current densities are around 10^{-9} A/cm^2. From Figure 6.1, the HfO_2 IPD and MIM capacitors show leakage 5.68×10^{-9}A/cm^2 and 2.27×10^{-9}A/cm^2 at 2V, respectively. The IPD leakage is slightly larger than the MIM capacitor because of the interface roughness between polySi/HfO_2.

Figure 6.2 shows the capacitance density as a function of temperature of the HfO_2 MIM capacitor at frequencies from 100 Hz to 1 MHz. The measurement temperatures are varied from 25°C to 150°C. The results show that the capacitance density decreases with the temperature. The MIM capacitor shows smaller capacitance density at higher measurement frequency. This is because the resistivities of the fabricated metal electrodes (HfN and TiN) are larger compared with the traditional metal electrode (Al). Therefore, the series resistance between the top electrode and the bottom electrode of the measured MIM capacitor is larger and the measured capacitance density at higher frequency is reduced. To verify the effect of electrode resistivity, we also fabricated a MIM capacitor with aluminum as the top electrode and obtained smaller frequency dispersion result (not shown here). However, the capacitance densities are higher than the other reports [138]-[139].

The capacitance density of the HfO_2 IPD is shown in Figure 6.3. The data are similar to the MIM capacitor case depicted in Figure 6.2. The measured temperatures are extended to 200°C. However, more serious frequency dispersion effect is shown in the IPD data. The capacitance density decreases to about 0.2 fF/μm^2 at 1 MHz compared to 6.6 fF/μm^2 at 100 kHz. This is because the even larger resistivity of polysilicon electrode used in the IPD structure. The capacitance density of the IPD as a function of frequency is shown in Figure 6.4 to clarify the frequency dispersion effect associated with the polysilicon electrode.

K. J. Yang *et al.* proposed a technique utilizing two different frequencies to extracting the frequency-independent capacitance from high-frequency *C-V* measurements [140]. For the MIM capacitor cases depicted above, however, the variation of the capacitance was still observed after calculation. This technique seems not suitable for our cases here.

6.4 Metal-Insulator-Metal Capacitors with HfO_2 Dielectric

6.4.1 High-Density MIM Capacitors with HfO_2 Dielectric

Figure 6.5 depicts the capacitance density as a function of applied voltage for HfO_2 at frequencies ranging from 1 kHz to 1 MHz. Both the top and bottom electrodes using here are Ta. The capacitor area in this measurement is 2×10^{-4} cm^2. The capacitance densities decrease with frequency and are almost constant from –5 V to 5 V. High capacitance value of 3.3 $fF/\mu m^2$ was measured at 100 kHz. The MIM capacitors using different top electrodes of Al, Ta, and Cu are compared in Figure 6.6. The capacitance densities depicted in Figure 6.6 were measured at frequency of 100 kHz. The capacitor with Al top electrode shows smaller capacitance density of 2.9 $fF/\mu m^2$. This is reasonable because of the interfacial layer of Al_2O_3 formed between HfO_2 and Al film during sample preparation. The overall capacitance was reduced by the lower dielectric constant of Al_2O_3. On the other hand, the capacitance density of the capacitor with Cu top electrode exhibits record high value of 3.4 $fF/\mu m^2$ in such thickness regime. The average voltage dependence of the MIM capacitor from 1 kHz to 1

MHz follows the voltage dependence of C_o ($\alpha \times V^2 + \beta \times V + 1$), where the voltage coefficients of capacitance (VCC) values of α and β are listed in Table 6.1. The requirement of the quadratic coefficient of capacitance α is smaller than 100 ppm/V^2, and the requirement of the linear coefficient of capacitance β is below 1000 ppm/V according to the ITRS roadmap [141].

Figure 6.7 shows the leakage current density-voltage (*J*-*V*) characteristics of HfO_2 MIM capacitors with different top electrodes of Al, Ta, and Cu. The measured area is 2×10^{-4} cm^2 for all of the samples. The leakage current densities of the MIM capacitors exhibit nearly the same order of magnitude at low field region. However, the current densities of the MIM capacitors with Ta and Cu top electrode show a little larger than that of the capacitor with Al top electrode after 2 V. Beyond 3 V, the current densities of the MIM capacitor with Cu top electrode increases obviously, while that of the capacitors with Al top electrode keeps the lowest current level until 5 V. The leakage current densities for the MIM capacitors with Al, Ta, and Cu top electrodes are 5.0×10^{-9}, 7.8×10^{-9}, and 9.0×10^{-8} A/cm^2 at 5 V, respectively.

The loss tangent values as a function of frequency for the HfO_2 dielectric MIM capacitors with three different top electrodes are shown in Figure 6.8. Similar trend in loss tangent values (1/*Q* factor) are observed for all of the samples. The lowest loss tangent value was measured at frequencies of 100 kHz and 10 kHz. At frequencies of 1 MHz and 1 kHz, the loss tangent values increase to a value around 0.05.

6.4.2 Thermal Stress on the MIM Capacitors

Figure 6.9 depicts the capacitance density of the MIM capacitor with Ta top electrode as a function of frequency after thermal stress from 25°C to 125°C. At lower temperature, the capacitance density decreases with frequency. However, this is not the case at elevated temperature. The capacitance density does not decrease monotonically with frequency but has a minimum at the frequency of 100 kHz. The same thermal stress measurement was conducted for the capacitor with Al and Cu top electrode and the results are shown in Figure 6.10. The tendency of the capacitance density for Al top electrode is similar to that for Ta top electrode. The capacitance density decreases initially and then increases with frequency for the case of Al top electrode. The poorer frequency dispersion for Al top electrode compared with that for Ta top electrode is probably the increased interface defect density around the interfacial layer formed at the less stable Al/HfO_2 interface under the elevated temperature measurements. On the other hand, the capacitance density for Cu top electrode is obviously lowered at elevated temperatures. In addition, the capacitance density decreases with frequency at all thermal stress conditions. The major reason is considered to be the interface defect density increasing during the thermal stress process.

6.4.3 Leakage Mechanism of the MIM Capacitors

In order to elucidate the leakage mechanism, a plot of the leakage current density versus the square root of the applied electric field in the high electric field regime was sketched, as shown in Figure 6.11. To make the plots concise and clear, only high field region is shown. Figure 6.11(a), (b), and (c) show ln (J/E) and $E^{1/2}$ characteristics of the Ta/HfO_2/Ta, Al/HfO_2/Ta, and Cu/HfO_2/Ta MIM capacitors, respectively. We found that all leakage current densities of Ta, Al, and Cu top electrode capacitors are increased with temperature, revealing a temperature dependence on the leakage behavior. In addition, all leakage current densities are linearly related to square root of the applied electric field. These linear variations of current densities, after careful calculation, correspond to Frenkel-Poole (FP) type conduction mechanism [142],

$$\boldsymbol{J} = \boldsymbol{J}_0 \exp\left(\frac{\beta_{\mathrm{FP}} \boldsymbol{E}^{1/2} - \phi_{\mathrm{FP}}}{\boldsymbol{k}_{\mathrm{B}} \boldsymbol{T}}\right) \tag{6.1}$$

where $J_0 = \sigma_0 E$ is the low field current density, σ_0 the low field conductivity, $\beta_{\mathrm{FP}} = (e^3/\pi\varepsilon_0\varepsilon)^{1/2}$, ϕ_{FP} the height of trap potential well. Rearrangement of Equation (6.1) yields a linear relationship between ln J and $1/T$, capable of calculating the height of trapping potential well ϕ_{FP}

$$\ln \boldsymbol{J} = \ln(\boldsymbol{J}_0) - \frac{1}{\boldsymbol{T}}\left(\frac{\phi_{\mathrm{FP}}}{\boldsymbol{k}_{\mathrm{B}}} - \frac{\beta_{\mathrm{FP}} \sqrt{\boldsymbol{E}}}{\boldsymbol{k}_{\mathrm{B}}}\right) \tag{6.2}$$

The values of $e\phi_{\mathrm{FP}}$ extracted from the slope of the equation are 0.95, 1.01, 0.90 eV for Ta, Al, Cu top electrode, respectively. The calculated conduction mechanism of Frenkel-Poole type for all samples indicates that the current conduction is essentially via the trap state. However, some variation still exists in the extracted height of trap potential with respect to different top electrodes. This implies that the traps at and around the interface rather than the traps at deep level play the major role to the conduction mechanism.

6.5 Conclusions

The IPD and MIM capacitors have been successfully fabricated with HfO_2 as the dielectric layer. The measurement results show high capacitance density compared to the data shown in previous literatures. The leakage currents of the IPD and MIM capacitors are very small. Although the resistivity of the electrodes are larger because of the nitrogen incorporated. The frequency dispersion effect is still not very serious for the MIM capacitors. For the IPD, the thermal stability is very good and the temperature coefficient is very small. These show that the HfO_2 dielectric is very suitable for IPD and MIM applications.

HfO_2 MIM capacitors with different metal top electrodes have been investigated in the second part. The MIM capacitor with Al top electrode exhibits the lowest capacitance density, while that with Cu top electrode exhibits the highest capacitance value of 3.4 $fF/\mu m^2$. Due to the Al_2O_3 layer formed between Al and HfO_2, the capacitance density and the leakage current density were reduced to 2.9 $fF/\mu m^2$ and 5.0×10^{-9} A/cm^2 (at 5 V), respectively. On the other hand, although the MIM capacitor with Cu top electrode shows larger leakage current density at higher electric field, the successful fabrication of the Cu top electrode capacitor implies the possibility of integrating Cu with HfO_2 dielectrics. Thus indicates that it is very suitable for HfO_2 dielectric to use in silicon IC applications.

Table 6.1 Voltage linearity coefficients α (ppm/V^2) and β (ppm/V) as a function of frequency for the HfO_2 MIM capacitors with Ta, Al, and Cu top electrode.

Frequency	Tantalum (Ta)		Aluminum (Al)		Copper (Cu)	
	α (ppm/V^2)	β (ppm/V)	α (ppm/V^2)	β (ppm/V)	α (ppm/V^2)	β (ppm/V)
1 MHz	65.1	150.3	35.5	83.3	55.4	47.7
100 kHz	70.2	181.0	36.0	105.2	53.6	79.1
10 kHz	74.4	125.8	41.2	93.7	230.1	84.5
1 kHz	87.0	130.1	161.5	200.6	153.4	–33.7

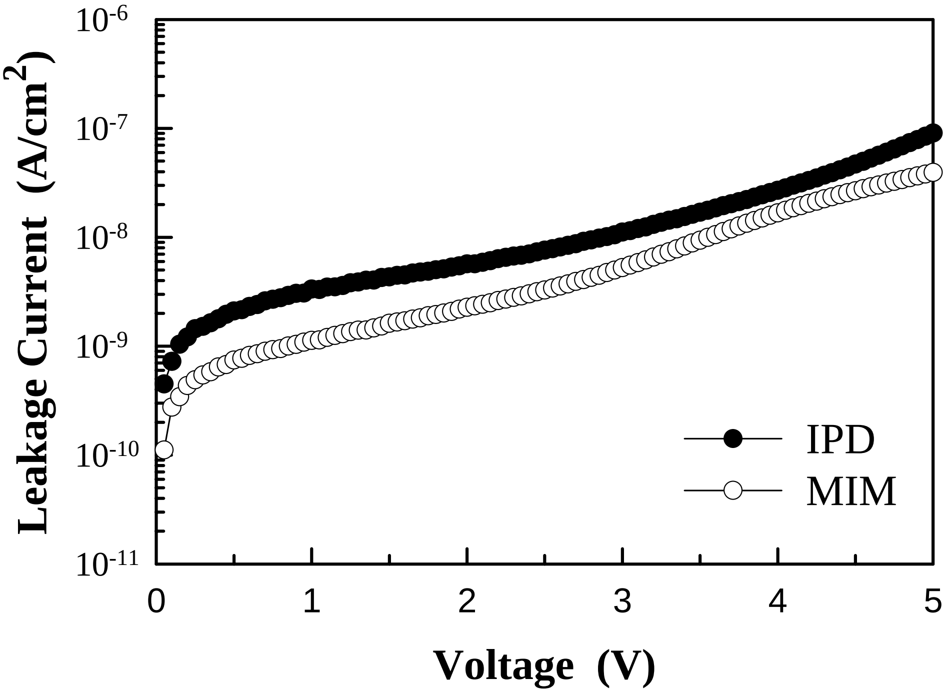


Fig. 6.1 Current-voltage (*J-V*) characteristics of the IPD and MIM capacitors.

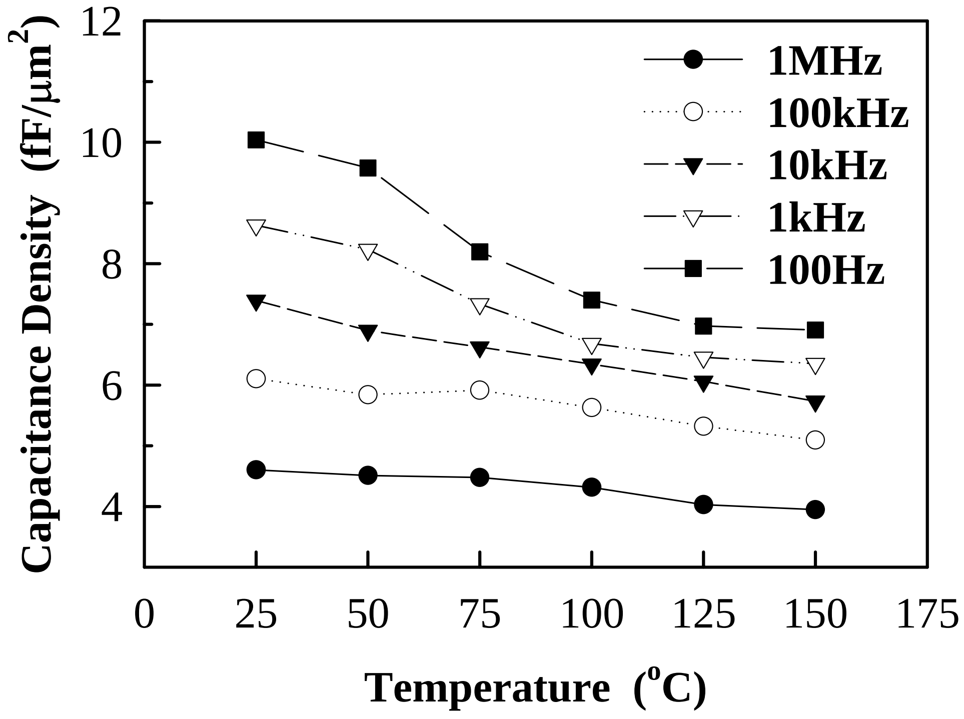


Fig. 6.2 Capacitance density of the MIM capacitor as a function of temperature at frequencies varied from 100Hz to 1MHz.

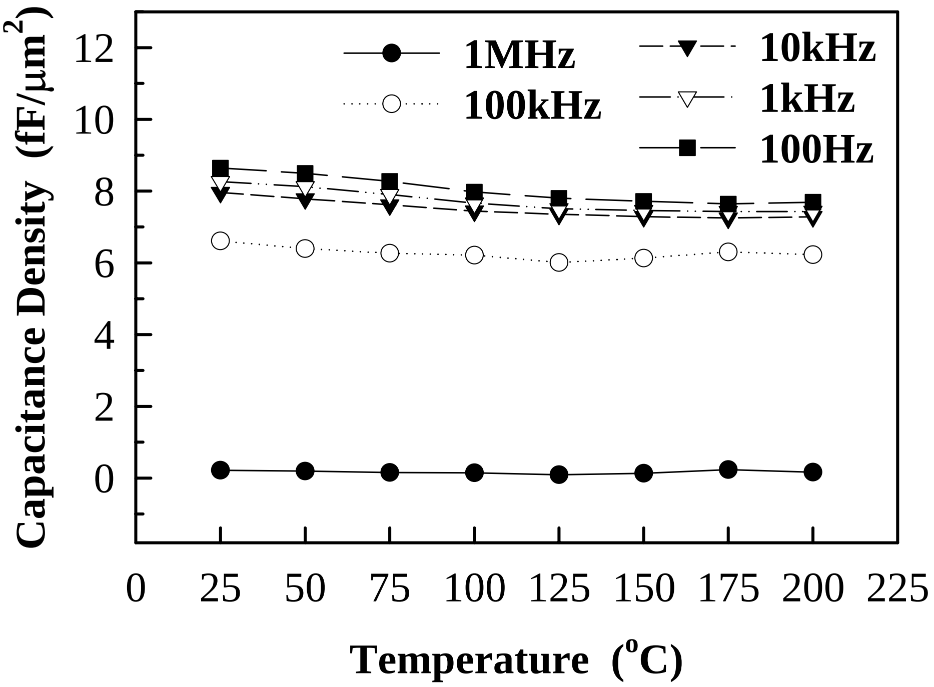


Fig. 6.3 Capacitance density of the IPD as a function of temperature at frequencies varied from 100Hz to 1MHz.

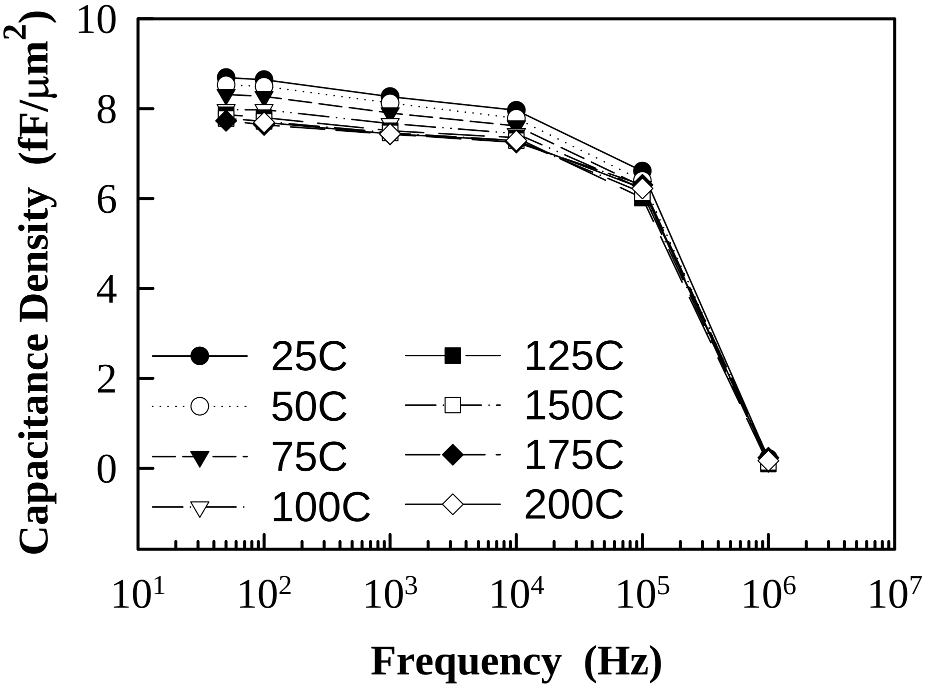


Fig. 6.4 Capacitance density of the IPD as a function of frequency at temperatures varied from 25°C to 200°C.

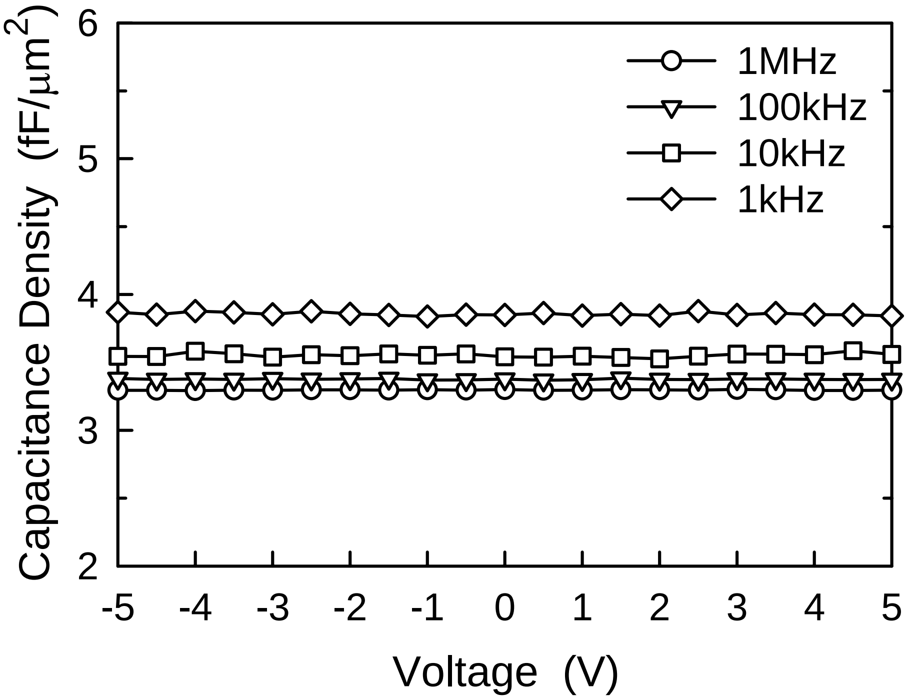


Fig. 6.5 Capacitance-voltage (*C*-*V*) characteristics of HfO_2 MIM capacitors with Ta electrodes at the frequencies from 1 kHz to 1 MHz.

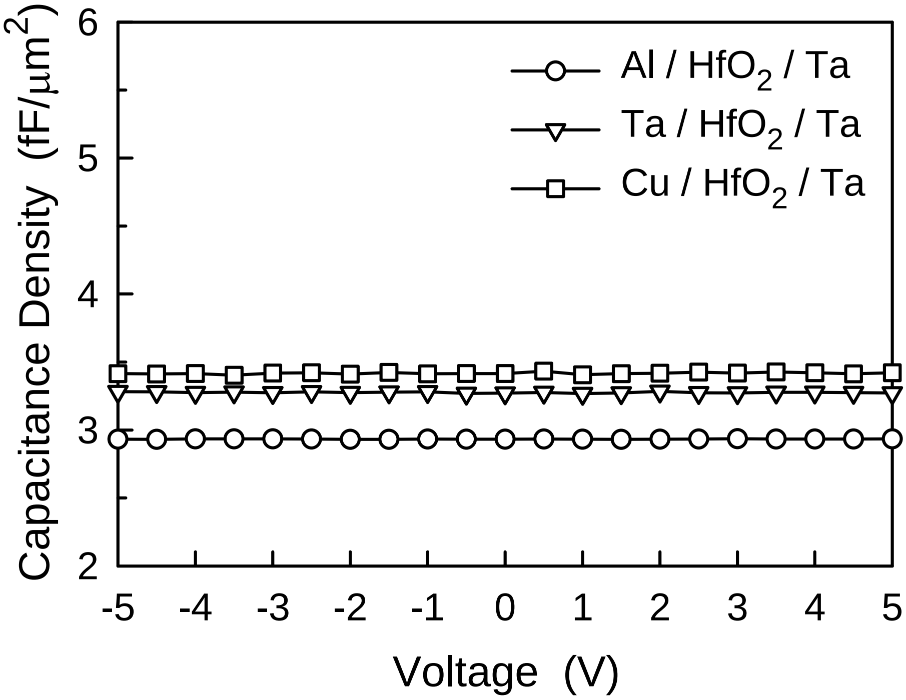


Fig. 6.6 Capacitance-voltage (*C*-*V*) characteristics of HfO_2 MIM capacitors with Al, Ta, and Cu top electrodes at the frequency of 100 kHz.

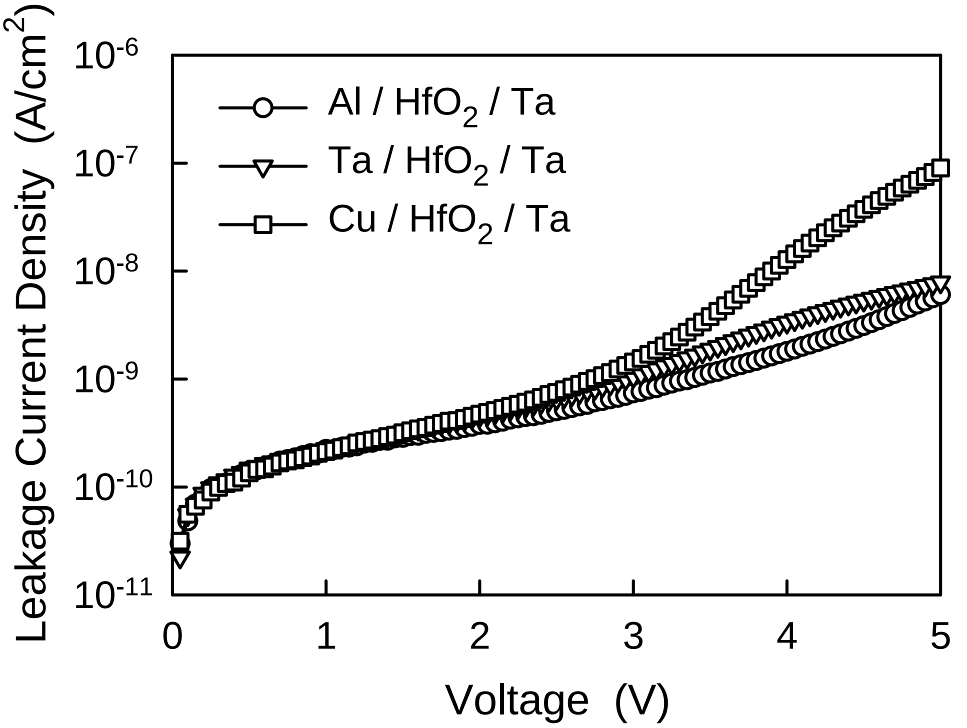


Fig. 6.7 Current density-voltage (*J*-*V*) characteristics of the HfO$_2$ MIM capacitors with the top electrodes of Al, Ta, and Cu.

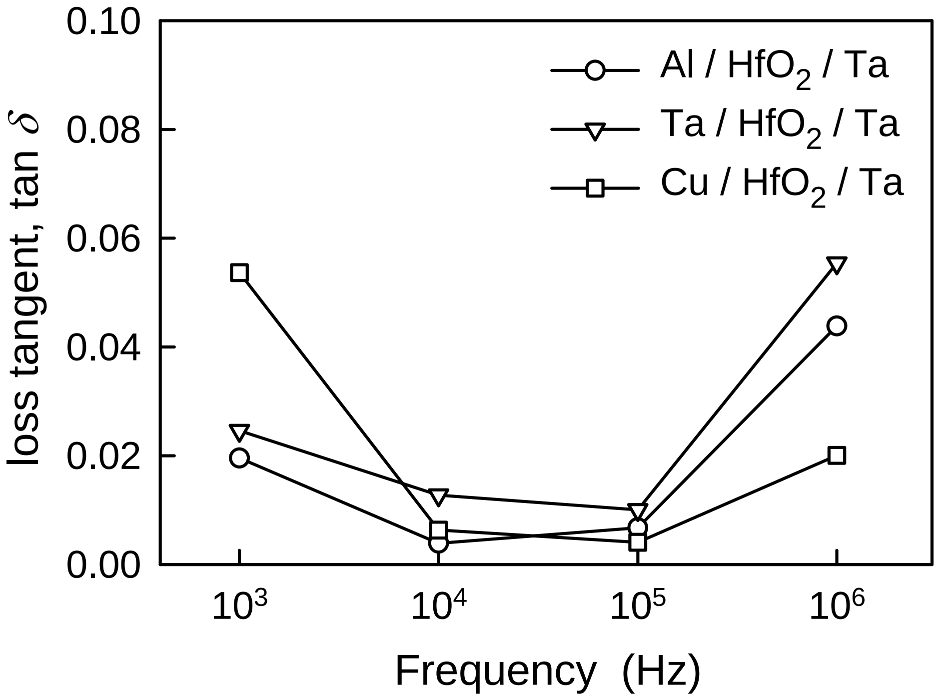


Fig. 6.8 Loss tangent as a function of frequency for the MIM capacitors with Al, Ta, and Cu top electrodes.

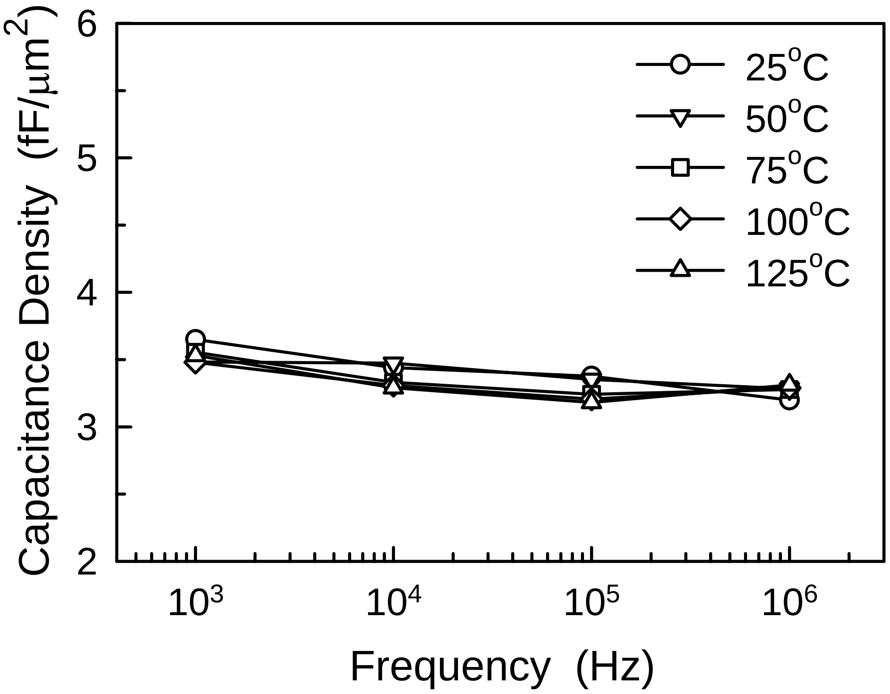


Fig. 6.9 Capacitance density of the MIM capacitor with Ta top electrode as a function of frequency after thermal stress from 25°C to 125°C.

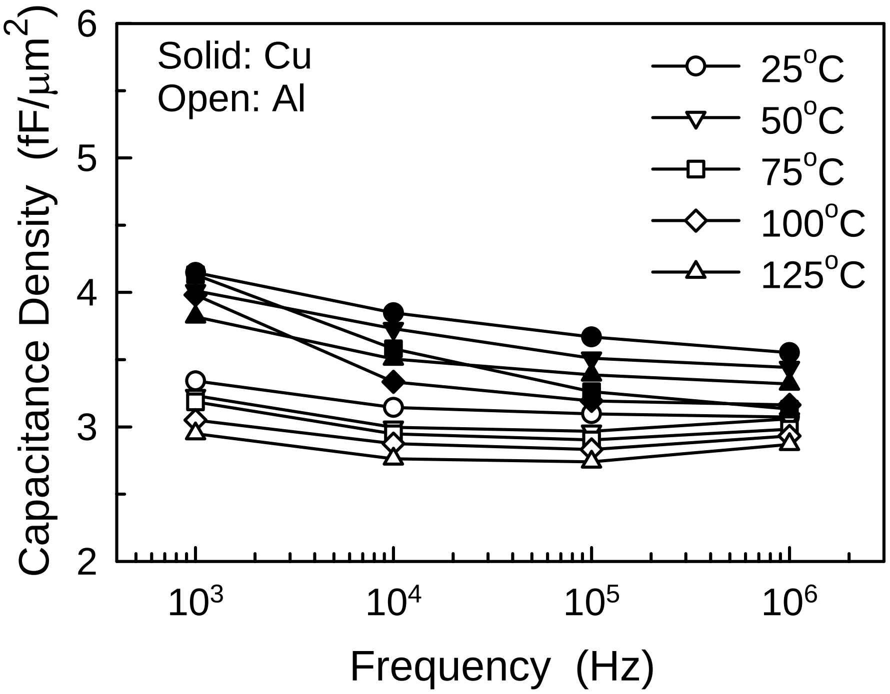
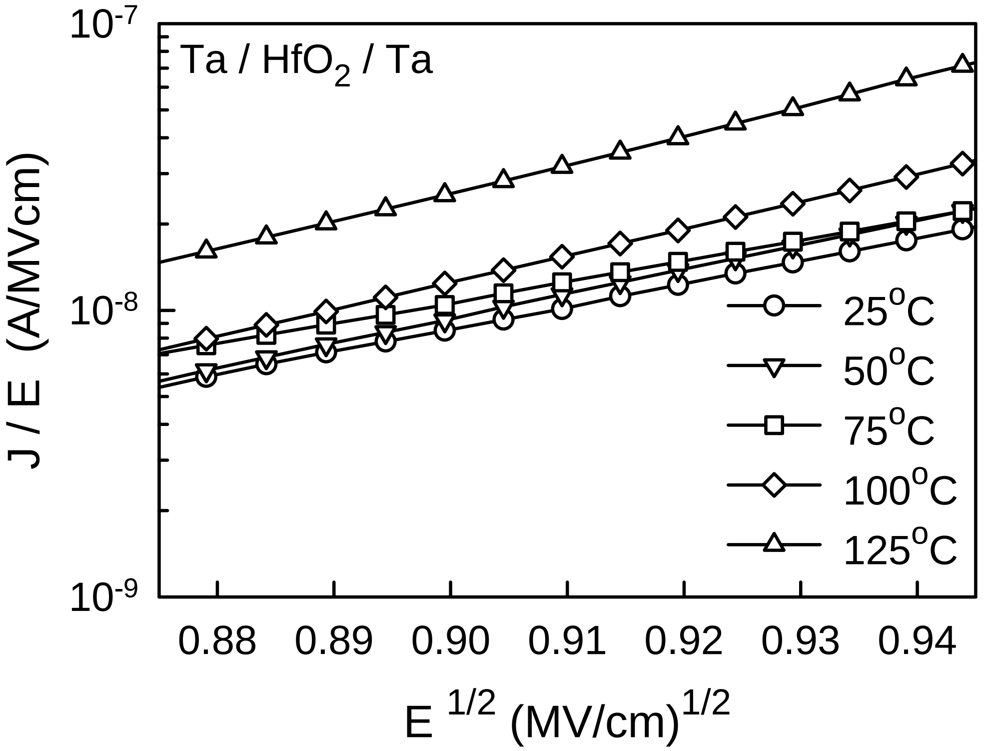
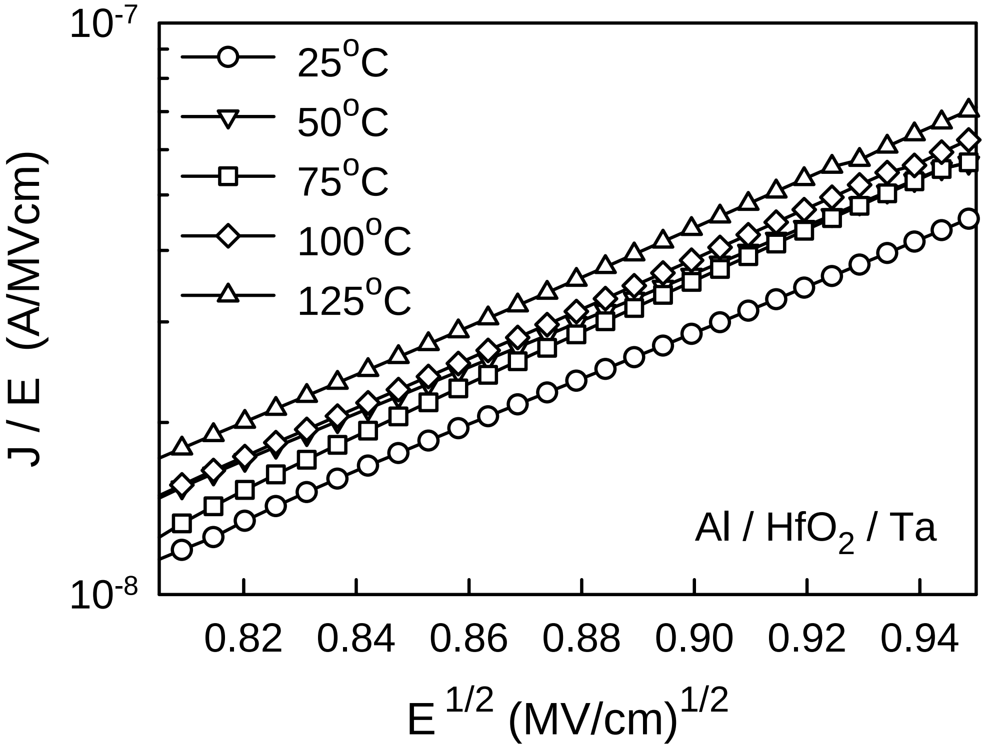


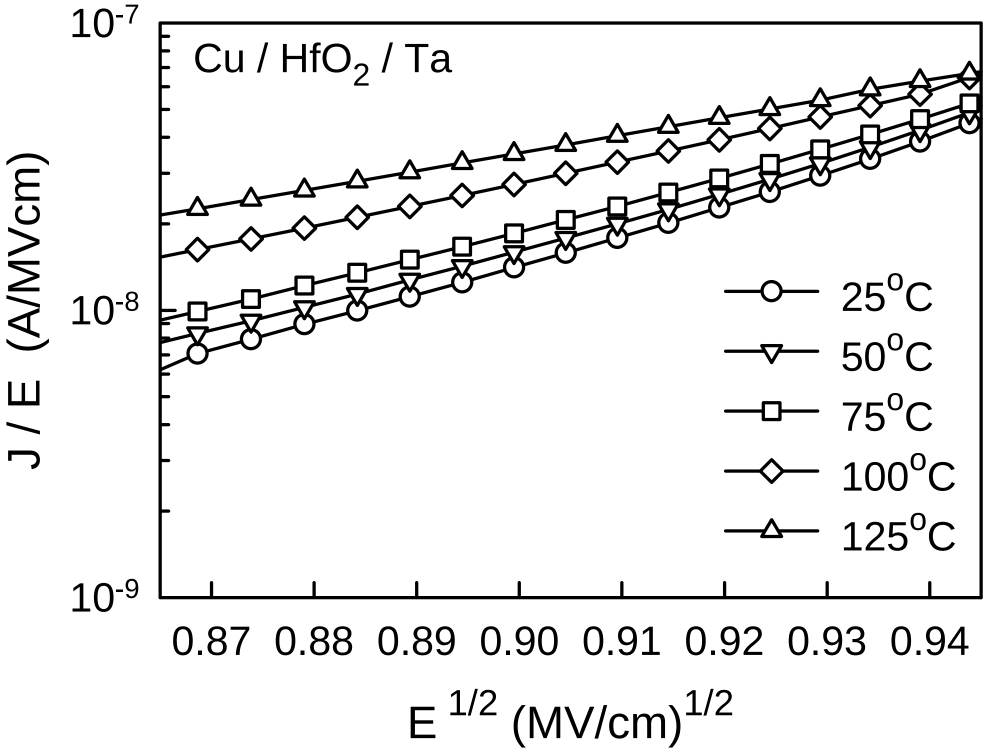
Fig. 6.10 Capacitance density of the MIM capacitor with Al and Cu top electrode as a function of frequency after thermal stress from 25°C to 125°C.


Ta / HfO$_2$ / Ta
J / E (A/MVcm)
E $^{1/2}$ (MV/cm)$^{1/2}$
10^{-7}
10^{-8}
10^{-9}
0.88
0.89
0.90
0.91
0.92
0.93
0.94
25^{o}C
50^{o}C
75^{o}C
100^{o}C
125^{o}C

(a)


Al / HfO$_2$ / Ta
J / E (A/MVcm)
E $^{1/2}$ (MV/cm)$^{1/2}$
10^{-7}
10^{-8}
0.82
0.84
0.86
0.88
0.90
0.92
0.94
25^{o}C
50^{o}C
75^{o}C
100^{o}C
125^{o}C

(b)



(c)

Fig. 6.11 Poole-Frenkel plot showing the current density versus electric field characteristics at five measurement temperatures from 25°C to 125°C for HfO_2 MIM capacitor with (a) Ta, (b) Al, and (c) Cu top electrode.

Chapter 7

Conclusions and Suggestions for Future Work

7.1 Conclusions of This Study

The hot carrier injection reliability of nMOSFET's with ultrathin plasma nitrided gate oxide is investigated in this thesis. The devices with plasma nitrided oxide suffer more transconductance reduction and threshold voltage shift. The degradation is direct proportional to the plasma nitridation time. For channel hot-carrier stressing, the most efficient stressing condition is located at $V_g = V_d$, rather than maximum substrate current or $V_g = V_d / 2$ which is often utilized for traditional nMOSFETs. For substrate hot-carrier stressing, the raising of substrate voltage can enhance the device degradation considerably. We report, for the first time, an enhanced degradation under negative substrate bias in nMOSFETs with ultrathin plasma nitrided gate dielectric. The enhanced degradation is attributed to the introduction of paramagnetic electron trap precursors during plasma nitridation. Similar to NBTI in pMOSFETs, our findings are important for nMOSFETs from the reliability point of view. For channel hot-carrier stressing of pMOSFET's, the most efficient stressing condition is located at $V_g = V_d$, which is corresponding to the region of maximum gate current. The negative threshold voltage shift indicates a positive charge build-up in the gate dielectric. The positive charge can result from either hole trapping in the dielectric or the creation of positively charged interface states at the dielectric interface. For negative bias temperature stressing, appreciable enhancement of the threshold voltage shift can be observed through the raising of temperature. The enhanced device degradation is attributed to the H-related species and the interface trap generated during NBT stressing. Even though the incorporation of nitrogen into thermal oxide is advantageous in many respects, our findings suggest that careful attentions need to be paid to ensure that plasma-nitrided gate dielectric meets the reliability requirements for the sub-100nm device technology node.

The second part in this thesis is high-*k* gate dielectrics related to hafnium oxide. Hafnium oxide film was evaluated as possible candidate material to replace SiO_2 for gate dielectric in complementary metal-oxide-semiconductor technology. Both sputtering and MOCVD methods were used as the tool of thin-film HfO_2 deposition. In view of the film uniformity and interfacial layer growth, however, sputtering maybe not sufficient to be a production tool in the future. AVD-deposited HfO_2 capacitors using Cu and Al as the gate electrode have been fabricated and investigated for the first time. The counterparts with thermally grown SiO_2 dielectric were also constructed for comparison. Our results clearly show that HfO_2 dielectric depicts superior resistance against Cu diffusion after BTS test, compared to SiO_2. Moreover, the presence of Cu metal in direct contact with HfO_2 has negligible impact on the reliability of the HfO_2 capacitor. The fact that HfO_2 can behave as a good barrier against Cu diffusion is attributed to its considerably high density. This finding is important as it suggests the feasibility of a Cu integration process from the gate electrode to BEOL interconnect, which will allow the use of the gate electrode as the first-level metal simultaneously, resulting in a simplified process.

HfO_2 MIM capacitors with different metal top electrodes have also been investigated. The MIM capacitor with Al top electrode exhibits the lowest capacitance density, while that with Cu top electrode exhibits the highest capacitance value of 3.4 $fF/\mu m^2$. Due to the Al_2O_3 layer formed between Al and HfO_2, the capacitance density and the leakage current density were reduced to 2.9 $fF/\mu m^2$ and 5.0×10^{-9} A/cm^2 (at 5 V), respectively. On the other hand, although the MIM capacitor with Cu top electrode shows larger leakage current density at higher electric field, the successful fabrication of the Cu top electrode capacitor implies the possibility of integrating Cu with HfO_2 dielectrics. Thus indicates that it is very suitable for HfO_2 dielectric to use in silicon IC applications.

7.2 Suggestions for Future Work

In the study of high-*k* gate dielectrics related to hafnium oxide, the superior resistance against Cu diffusion after BTS test is observed. The presence of Cu metal in direct contact with HfO_2 has negligible impact on the reliability of the HfO_2 capacitor. However, the transistor has not been processed yet. The next step of this study is the achievement of the MOSFET fabrication, followed with the device characterization and verification of the findings in previous work.

The MIM capacitors with HfO_2 gate dielectric have been studied. The behavior of the capacitors related to different metal electrodes exhibits somehow slightly variations. Although such difference can be roughly imagined from the interface formed on the dielectric, the mechanism behind is still not understood. Further experiments and analyses are required to clarify the interaction between the metal electrode and the dielectric, especially for the Cu metal that connecting to the MIM capacitors in the BEOL.

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超薄電漿氮化氧化層與高介電常數氧化鉿於閘極介電層之研究

Study on Ultrathin Plasma Nitrided Oxide and HfO_2 High-κ Gate Dielectrics

Publication List

International Journals:

[1] **Tsu-Hsiu Perng**, Chao-Hsin Chien, Ching-Wei Chen, Horng-Chih Lin, Chun-Yen Chang, and Tiao-Yuan Huang, “Enhanced Negative Substrate Bias Degradation in nMOSFETs With Ultrathin Plasma Nitrided Oxide,” *IEEE Electron Device Letters*, vol. 24, pp. 333-335, May 2003.

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