Circuit and Layout Co-Design for ESD Protection in Bipolar-CMOS-DMOS (BCD) High-Voltage Process

Wen-Yi Chen, *Student Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—The n-channel lateral double-diffused metal–oxide–semiconductor (nLDMOS) devices in high-voltage (HV) technologies are known to have poor electrostatic discharge (ESD) robustness. To improve the ESD robustness of nLDMOS, a co-design method combining a new waffle layout structure and a trigger circuit is proposed to fulfill the body current injection technique in this work. The proposed layout and circuit co-design method on HV nLDMOS has successfully been verified in a 0.5-μm 16-V bipolar-CMOS-DMOS (BCD) process and a 0.35-μm 24-V BCD process without using additional process modification. Experimental results through transmission line pulse measurement and failure analyses have shown that the proposed body current injection technique can significantly improve the ESD robustness of HV nLDMOS.**

***Index Terms*—Bipolar-CMOS-DMOS (BCD) process, body current injection, electrostatic discharge (ESD), lateral double-diffused metal–oxide–semiconductor (LDMOS).**

I. Introduction

WITH the thriving applications on automotive electronics, liquid-crystal display, and light-emitting-diode driver ICs, the demands of high-voltage (HV) ICs are rapidly increasing [1]. In HV ICs, the power supply voltage $V_{\rm CC}$ is often over 10 V or even higher. To fabricate devices to sustain such a high operating voltage, not only the process complexity but also the difficulty to guarantee the reliability of HV devices is increased. Among the reliability issues of ICs, electrostatic discharge (ESD) is an important and inevitable event to the circuits and systems of microelectronics products during fabrication, packaging, and assembling processes [2]–[5]. ESD protection in HV technology is challenging and has recently received much attention [6]–[9].

To improve the ESD robustness of HV n-channel metal–oxide–semiconductors (NMOSs), several techniques related to process modifications have been reported [9]–[13]. The method of inserting N+ buried layer has been used to enhance the ESD robustness of n-channel lateral double-diffused metal–oxide–semiconductor (nLDMOS) [9]. However, additional process steps and mask layers are needed. In addition, a heavily doped P-type adaptive implantation at the source side of HV NMOS has been used to avoid the nonuniform triggering of a parasitic n-p-n bipolar junction transistor (BJT) when the HV NMOS is drawn with a large array, i.e., large device dimensions (W/L) [13].

In this paper, the influence of a highly doped P-type boron implantation (PBI) layer on the ESD robustness of HV n-channel lateral DMOS (nLDMOS) is first investigated. The nLDMOS was designed to discharge the ESD current through the parasitic BJT inherent in the nLDMOS. A circuit and layout co-design method is then proposed to improve the ESD robustness of the nLDMOS [14], [15]. The proposed method exploits the body current injection to improve the turn-on uniformity of nLDMOS devices during ESD stresses. Therefore, it does not require process modifications or additional mask layers, and has been verified in a 0.5-μm 16-V bipolar-CMOS-DMOS (BCD) process and a 0.35-μm 24-V BCD process.

II. Effect of PBI on the ESD Performance of HV nLDMOS

Fig. 1(a) shows the traditional (stripe) layout diagram of an nLDMOS in the 0.5-μm 16-V BCD process. The nLDMOS in the 0.5-μm 16-V BCD process is defined within one single oxide diffusion (OD) region, so that the gap between the N+ drain and the polygate is the active area. Device cross-sectional view of the 16-V nLDMOS along the $\rm A-A'$ line in Fig. 1(a) is shown in Fig. 1(b). A PBI was optionally implanted underneath the source N+ and P+ regions in the 16-V nLDMOS to investigate its effectiveness on ESD robustness.

For the nLDMOS in the 0.35-μm 24-V BCD process, the drain and source/body regions are defined in different active areas, as shown in Fig. 2(a). The gap between the N+ drain and the polygate of the nLDMOS device is thereby a field oxide (FOX) region. A device cross-sectional view along the $\rm A-A'$ line of the 24-V nLDMOS in Fig. 2(a) is shown in Fig. 2(b). The FOX gap of the 24-V nLDMOS can avoid the field crowding near the drain of nLDMOS, which, in turn, helps the nLDMOS to sustain the high operating voltage of 24 V. In both HV technologies, because the nLDMOS devices are surrounded by HV n-well [16], the p-type body (p-body) of nLDMOS devices are fully separated from the common p-type substrate (P-sub). Additional P+ body pick up at every source region is required to provide the potential of the p-body. Channel lengths are defined by the overlapped distance of the p-body and the polygate.

To analyze the characteristics of devices under human body model (HBM) ESD stresses, a transmission line pulse (TLP) system with 100-ns pulsewidth is commonly adopted [17]. Fig. 3 shows the TLP-measured $I-V$ characteristics of the 16-V nLDMOS with traditional (stripe) layout style. Both 16-V

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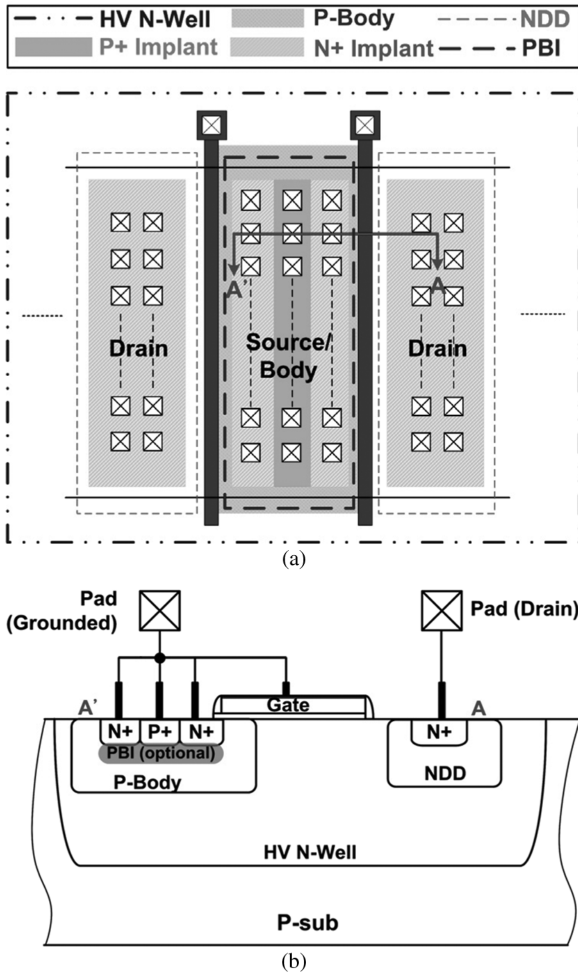


Fig. 1. (a) Layout diagram and (b) device cross-sectional view along the $\mathrm{A}-\mathrm{A}'$ line of the nLDMOS in a 0.5-μm 16-V BCD process with optional PBI implantation.

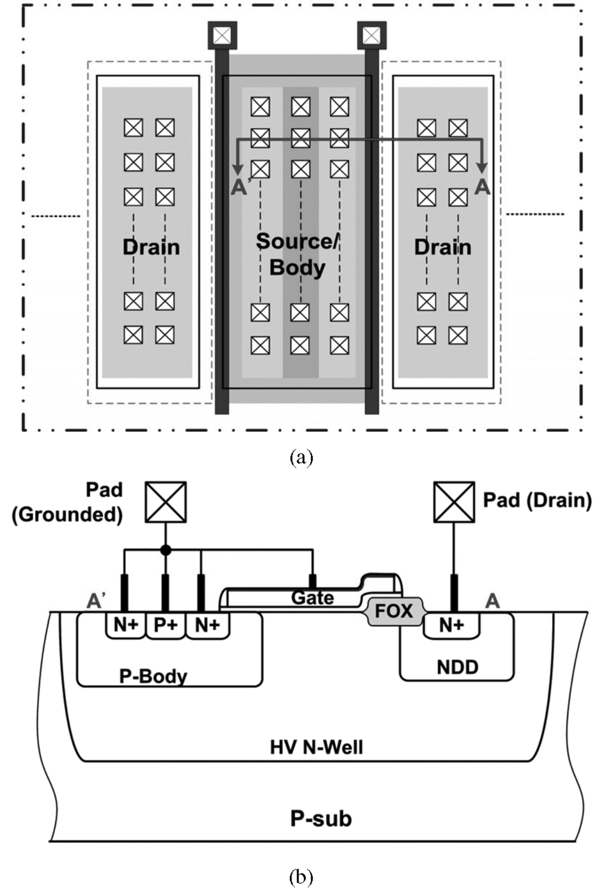


Fig. 2. (a) Layout diagram and (b) device cross-sectional view along the $\mathrm{A}-\mathrm{A}'$ line of the nLDMOS in a 0.35-μm 24-V BCD process.

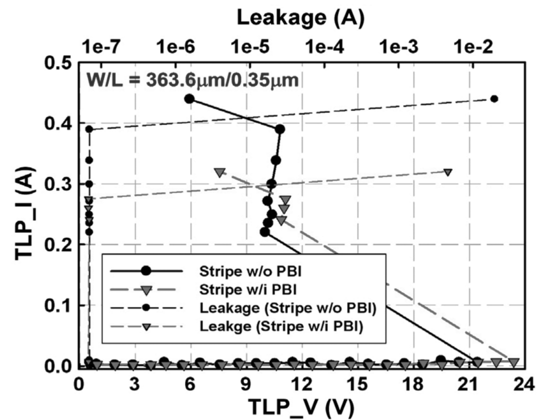


Fig. 3. TLP-measured $I-V$ characteristics of the gate-grounded 16-V nLDMOS devices with or without the PBI implantation in the source region.

nLDMOSs with and without PBI layer in Fig. 3 have the same device dimension (W/L) of 363.6 μm/0.35 μm, with each finger having a width of 45.45 μm. From the TLP measurement results, the bipolar trigger voltage V_{t1} of the gate-grounded 16-V nLDMOS without PBI implantation is 21.4 V. With the heavily doped PBI implantation to reduce the parasitic p-body resistance at the source side of nLDMOS, the V_{t1} of the gate-grounded 16-V nLDMOS is increased to 23.4 V. Because the bipolar beta gain of parasitic BJT in nLDMOS is also suppressed by the PBI implantation, the holding voltage of the first snapback is slightly increased from 10 to 10.86 V by the insertion of the PBI layer. However, the secondary breakdown current I_{t2} of the 16-V nLDMOS was found to be degraded from 0.39 to 0.28 A due to the insertion of the PBI layer.

To explain the degradation on the ESD robustness of nLDMOS with PBI implantation, the typical $I-V$ characteristic of a gate-grounded NMOS (ggNMOS) during ESD stresses is depicted in Fig. 4. When the voltage across the ggNMOS is higher than the reverse drain/body junction breakdown voltage of the ggNMOS, the HV n-well/p-body in Fig. 2(b), e.g., the drain current of the ggNMOS, starts to increase due to the avalanche generation. The junction breakdown V_{av} is typically defined as the voltage corresponding to a 1-μA current level in the ggNMOS. Before the avalanche generation current is large enough to forward bias the parasitic body/source junction diode, the ggNMOS acts as a reverse-biased diode [HV n-well/p-body in Fig. 2(b)]. Therefore, the voltage keeps increasing without snapback. When the avalanche-generated hole current forward biases the parasitic body/source junction diode, parasitic n-p-n BJT is turned on, and the snapback happens. Due to the turn-on operation of the BJT inherent in the ggNMOS, the voltage across the ggNMOS is clamped down to the holding region.

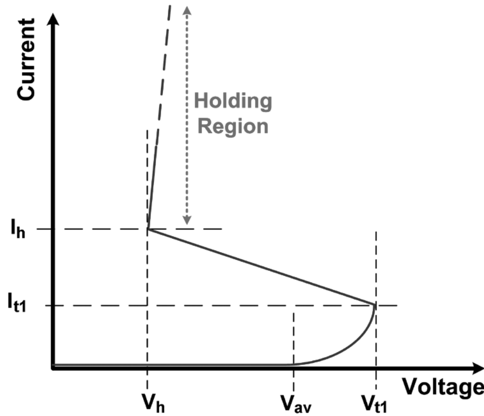


Fig. 4. Typical $I - V$ characteristic of a ggNMOS under ESD stresses.

The maximum reverse diode current before the snapback of the ggNMOS is defined as I_{t1} in this work. For devices with large-array design, the effective device width W is usually higher than several thousands of micrometers in order to have high driving capability or low turn-on resistance in specified applications. With a large effective device width, considerable I_{t1} can flow through large-array devices before the triggering of parasitic BJT. Due to the consideration of silicon area, large-array devices are not drawn with the foundry-provided ESD design rules in IC products. Therefore, nonuniform triggering among BJT inherent in the large-array device is serious. Consequently, triggering of BJT induces devastating results to the large-array devices [13]. Triggering of BJT has also been reported to cause ESD failures of HV power-rail ESD clamp circuits with big field-effect transistor (BigFET) [18].

For the 16-V nLDMOS studied in this work, the heavily doped PBI layer reduces the effective resistance of p-body (R_{body}). With the reduced R_{body}, the I_{t1} of nLDMOS is increased, because the turn-on operation of the BJT requires $(I_{t1} \times R_{\text{body}}) \geq V_{\text{tdiode}}$, where V_{tdiode} is the voltage to forward bias the p-body/N+ junction diode. Due to the fact that the considerable I_{t1} can flow through large-array nLDMOS, where BJT triggering is devastating, the additional P-type implantation at the source side of nLDMOS is beneficial to the ESD robustness of stand-alone large-array nLDMOS. ESD energy is mainly discharged through the reverse diode current I_{t1} of the large-array nLDMOS. However, for lack of snapback to clamp down the ESD discharging voltage, large-array nLDMOS is not suitable to protect internal circuits.

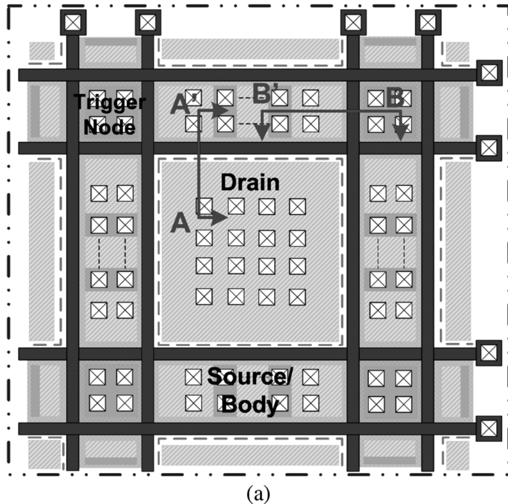
For ESD protection nLDMOS devices that are not large-array devices, they usually rely on the turn-on operation of BJT to clamp down ESD voltages to their holding regions and to protect the gate oxide of internal circuits from being damaged by the high ESD stressing voltages. They are therefore drawn with ESD design rules, and the overall effective gate widths are much smaller, compared with those of large-array nLDMOS devices. These devices exhibit low I_{t1}, because the high current density of (I_{t1}/W) makes the p-body/N+ diode easily forward biased under ESD stresses. As a result, the effect of PBI on increasing I_{t1} is negligible. As shown in Fig. 3, both 16-V nLDMOSs with and without PBI implantation exhibit low I_{t1} current. Furthermore, the magnitude of I_{t1} is not critical for nonlarge-array ESD protection nLDMOS, because the ESD current is mainly discharged through the holding region of the nLDMOS. With the bipolar beta gain being suppressed by the PBI implantation, the measured I_{t2} of nLDMOS was found to be degraded by the insertion of PBI implantation.

III. New Layout Structure With Circuit Co-Design to Improve the ESD Robustness of nLDMOS

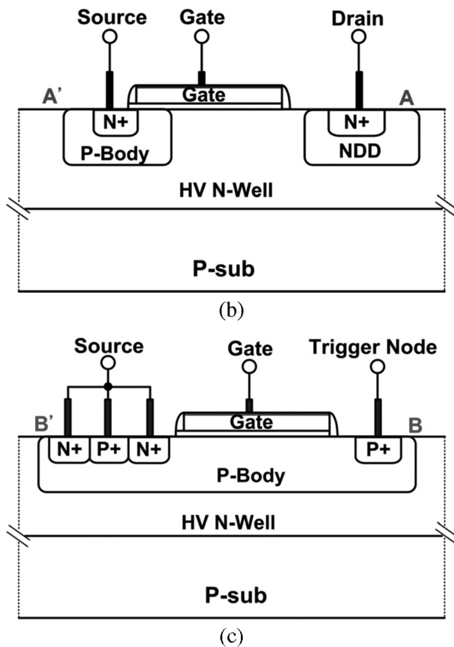
From the measurement results shown in Fig. 3, it is known that the PBI layer degrades the ESD robustness of nLDMOS when the nLDMOS device relies on the parasitic BJT to discharge ESD energies, i.e., snapback-based nLDMOS. Because the available process modification from foundry is not effective in improving the ESD robustness of snapback-based nLDMOS, a layout technique without additional mask or process step is proposed in this work.

In low-voltage (LV) CMOS technologies, one of the most effective methods to increase the ESD robustness of ESD protection devices is the substrate-triggered/substrate-pump technique [19]–[24]. To inject the substrate-triggered current into the base of the parasitic n-p-n BJT inherent in LV NMOS, a P+ trigger node was placed at the drain and connected to the trigger circuit [20]. However, in HV nLDMOS, the base of its parasitic n-p-n BJT is the p-body region, which is surrounded by the HV n-well. As a result, the traditional layout method in LV technologies to inject the substrate-triggered current by placing the P+ trigger node at the drain side cannot be implemented in the HV BCD processes.

In order to effectively inject the trigger current into the p-body of nLDMOS (the base of n-p-n BJT), nLDMOS realized in waffle layout style is proposed in this work. Fig. 5(a) shows the layout diagram of nLDMOS with the waffle layout style (waffle nLDMOS). In the waffle layout style, the drain of nLDMOS is drawn in a square. The source and body of the waffle nLDMOS are laid out at the four sides of the drain square. Such a waffle layout style leads to four squares (trigger nodes) at the diagonal corner of a drain square. Both the p-body regions in the two studied BCD processes are implanted before the formation of gate oxide; therefore, the four squares at the diagonal corner of drain are shorted to the body pick up at the source/body region. Device cross-sectional views along the $\mathrm{A}-\mathrm{A}'$ and $\mathrm{B}-\mathrm{B}'$ lines of Fig. 5(a) are shown in Fig. 5(b) and (c), respectively. By using the waffle layout structure, the body current can be injected from trigger nodes and be collected by the grounded P+ pick up at the source/body. The injected body current at the trigger node acts as the base current to turn on the parasitic n-p-n BJT inherent in nLDMOS. With such a new waffle layout arrangement, the P+ contacts at the source/body side can ensure the body potential of the waffle nLDMOS at ground during normal circuit operation. The potential of the trigger nodes of the waffle nLDMOS is dynamically controlled through the circuit co-design method. A trigger circuit is designed to distinguish normal circuit operating conditions and ESD stress conditions [25]. Under normal circuit operating conditions, the trigger circuit biases the trigger nodes of the waffle nLDMOS at ground potential. Under ESD stress conditions, the trigger circuit provides the required body injection current to enhance the turn-on uniformity of the waffle



(a)



(b)

(c)

Fig. 5. (a) Layout top view, (b) device cross-sectional view along the $\mathrm{A}-\mathrm{A}'$ line, and (c) device cross-sectional view along the $\mathrm{B}-\mathrm{B}'$ line of the nLDMOS with the new proposed waffle layout style in a 0.5-μm 16-V BCD process.

nLDMOS. Effectiveness of the newly proposed layout and circuit co-design method has been verified in a 0.5-μm 16-V BCD process and a 0.35-μm 24-V BCD process.

A. In 0.5-μm 16-V BCD Process

To verify the turn-on ability of the parasitic n-p-n BJT in the waffle nLDMOS through the body current injection, a stand-alone waffle nLDMOS with its trigger nodes connected to a bonding pad was fabricated in the 0.5-μm 16-V BCD process. Different levels of body current I_B were injected into the stand-alone waffle nLDMOS through its trigger nodes. Measurement setup is shown in the inset of Fig. 6, where $R_{\rm Body}$ denotes the equivalent resistance of the p-body from the trigger nodes to the P+ body pick up. With the larger injected I_B current, the nLDMOS exhibited the higher collector current I_C. This result has verified that the parasitic n-p-n BJT inherent in the waffle nLDMOS can successfully be triggered on through the body current injection.

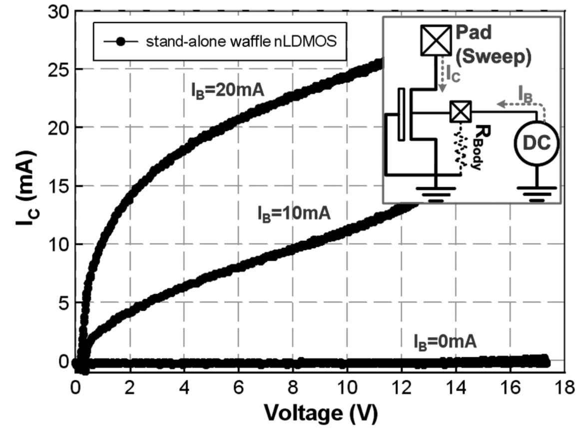


Fig. 6. Turn-on verification of the stand-alone 16-V nLDMOS drawn in waffle style with the additional body current (I_B) injection.

To provide the body current during ESD stresses, a trigger circuit composed of an RC distinguisher and an HV inverter was fabricated on chip. Because the ESD voltage transition is on the order of nanoseconds but normal circuit power-on transition is on the order of milliseconds, they can be distinguished through the time delay of the RC distinguisher. Corresponding measurement setup to verify the stand-alone trigger circuit and the device dimensions of the HV inverter used in the 0.5-μm process is shown in the inset of Fig. 7. During the verification measurement, the output of the stand-alone trigger circuit was externally shorted to the trigger nodes of a stand-alone 16-V waffle nLDMOS. Measurement result showed that the trigger circuit can provide a peak trigger current $I_{\rm Trigger}$ of 25 mA to the trigger nodes of the stand-alone waffle nLDMOS when a 20-V voltage pulse with 10-ns rise time t_r and 1-μs pulsewidth $t_{\rm pw}$ was applied, as shown in Fig. 7. After 200 ns, $I_{\rm Trigger}$ fades to 0 mA, because the input voltage of the inverter has followed up the input voltage transition through the RC distinguisher. The trigger circuit can therefore effectively distinguish ESD transition from the normal circuit power-on transition, because the normal circuit power-on transition has a rise time on the order of milliseconds.

The 100-ns TLP-measured $I-V$ curves among the stand-alone stripe, stand-alone waffle, and body-injected waffle nLDMOS devices are shown in Fig. 8. The stripe nLDMOS in Fig. 8 has a layout style as that shown in Fig. 1(a). The waffle nLDMOS in Fig. 8 has a layout style as that shown in Fig. 5(a), and the trigger nodes of the waffle nLDMOS are internally shorted to source. The body-injected waffle nLDMOS in Fig. 8 has a layout style as that shown in Fig. 5(a), and the trigger nodes in the body-injected waffle nLDMOS were internally connected to the trigger circuit through metal directly wiring in the chip. The trigger circuit has the same design parameters to the one verified in Fig. 7. These three nLDMOS have the same device dimension of 363.6 μm/0.35 μm in layout. Failure criterion (1-μA leakage current under 16-V drain bias voltage) is the same to all devices to judge their ESD robustness. The measured results show that the stripe nLDMOS and waffle nLDMOS have roughly the same secondary breakdown current

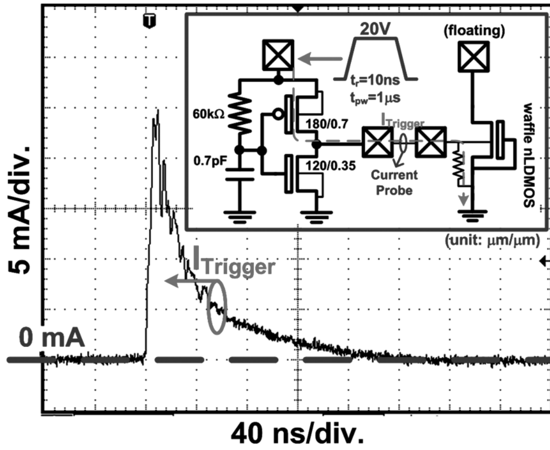


Fig. 7. Turn-on verification of the stand-alone trigger circuit in the 0.5-μm 16-V BCD process. The measurement setup is shown in the inset of this figure.

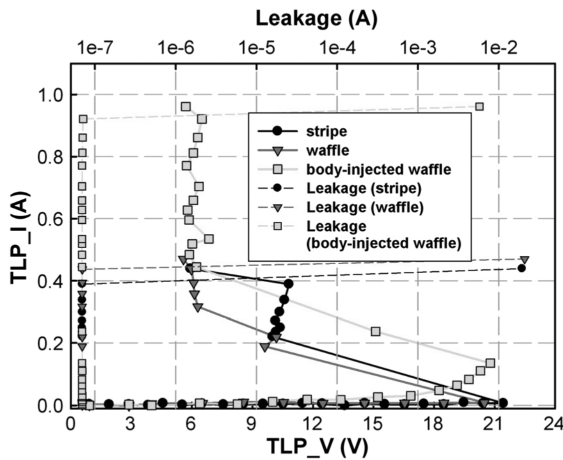


Fig. 8. 100-ns TLP-measured $I - V$ curves of 16-V nLDMOS with stripe, waffle, and body-injected waffle layout style.

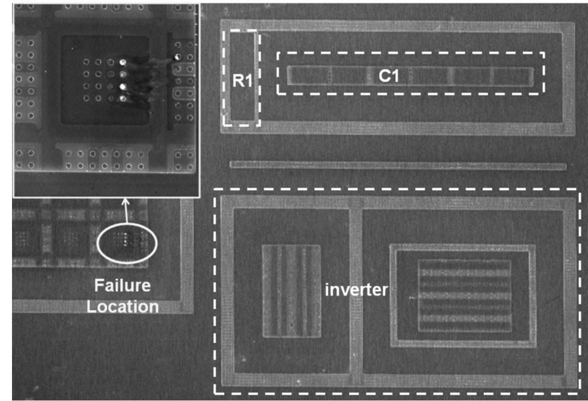


Fig. 9. SEM image of the body-injected waffle nLDMOS after 100-ns TLP measurement.

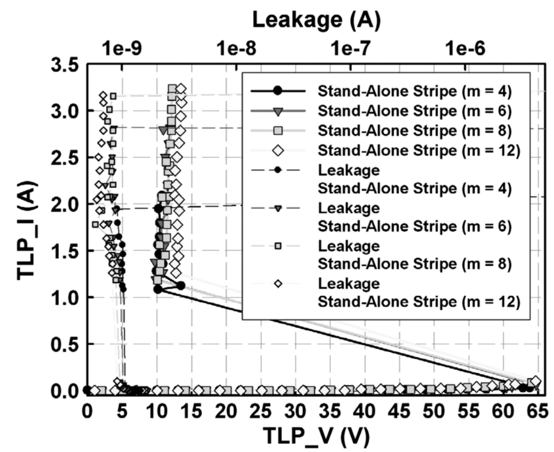


Fig. 10. TLP-measured $I - V$ characteristics of stand-alone 24-V nLDMOS in stripe layout style. The dimension for each finger of the stripe nLDMOS is $73.2\ \mu\text{m}/0.75\ \mu\text{m}$.

I_{t2} of 0.39 A and 0.41 A, respectively, if the body current injection was not applied. By applying the body current injection, the I_{t2} of the waffle nLDMOS can significantly be increased from 0.41 to 0.95 A. From the 100-ns TLP measurement, a more-than-twice increase on I_{t2} has been achieved through the waffle layout style and the body current injection technique. The measured HBM ESD robustness for stand-alone stripe, stand-alone waffle, and body-injected waffle nLDMOS devices is 0.75, 0.75, and 1.25 kV, respectively.

A scanning electron microscope (SEM) image of the body-injected waffle nLDMOS after 100-ns TLP measurement is shown in Fig. 9. The failure location of the body-injected waffle nLDMOS was found on the drain of the nLDMOS. This result shows that the ESD current is mainly discharged by the nLDMOS, instead of the trigger circuit, which, in turn, confirms the effectiveness of body current injection to improve the ESD robustness of the waffle nLDMOS.

B. In 0.35-μm 24-V BCD Process

In the 0.5-μm 16-V BCD process, substantial improvement on the ESD robustness of the nLDMOS has been achieved by using the waffle layout style along with the trigger circuit to provide body current injection. To study the width scaling to the ESD protection level of the nLDMOS, the circuit and layout co-design technique was fulfilled in a 0.35-μm 24-V BCD process.

The TLP-measured $I - V$ characteristics of stand-alone stripe nLDMOS and stand-alone waffle nLDMOS in the 0.35-μm 24-V BCD process are shown in Figs. 10 and 11, respectively. The measured I_{t2} for stand-alone stripe nLDMOS with a finger number of 4, 6, 8, and 12 is 1.94, 2.81, 3.15, and 3.16 A, respectively. Each finger of the 24-V stripe nLDMOS is $73.2\ \mu$m/$0.75\ \mu$m. For stand-alone waffle nLDMOS with 2 × 2, 3 × 3, and 4 × 4 drain squares, the measured I_{t2} is 1.8, 2.78, and 3.49 A, respectively. Each drain square of the 24-V waffle nLDMOS is $73.2\ \mu$m/$0.75\ \mu$m. From the TLP measurement results, nonlinear scaling of ESD robustness to the device width was observed on both stand-alone waffle and stand-alone stripe nLDMOS. A SEM image of the stand-alone 2 × 2 waffle nLDMOS after TLP measurement is shown in Fig. 12(a). ESD failures were found only on two drain squares of the 2 × 2 stand-alone waffle nLDMOS. Furthermore, the enlarged image of the ESD failure locations in Fig. 12(a) is shown in Fig. 12(b). Surface current filamentation traces are observed in Fig. 12(b), which implies a superficial current

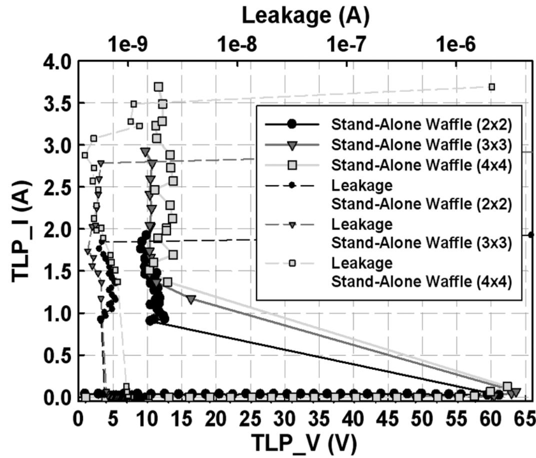
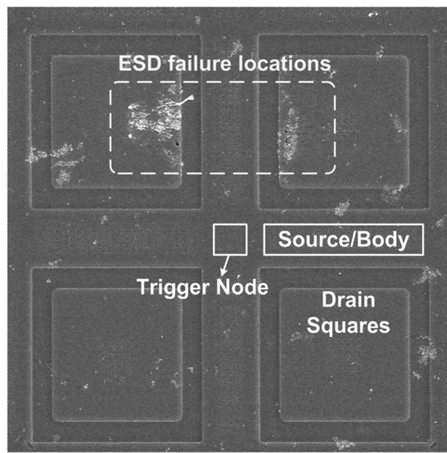
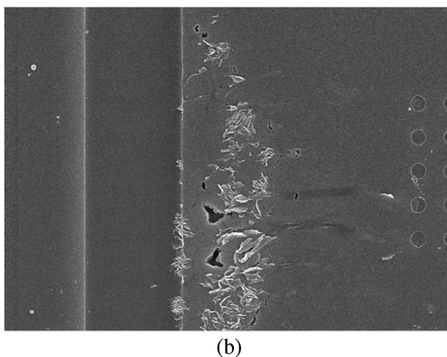


Fig. 11. TLP-measured $I-V$ characteristics of stand-alone 24-V nLDMOS in waffle layout style. The dimension for each drain square of the waffle nLDMOS is $73.2\ \mu\text{m}/0.75\ \mu\text{m}$.



(a)



(b)

Fig. 12. (a) SEM image of the stand-alone 24-V waffle nLDMOS with 2 × 2 drain squares after 100-ns TLP measurement and (b) enlarged image of ESD failure locations.

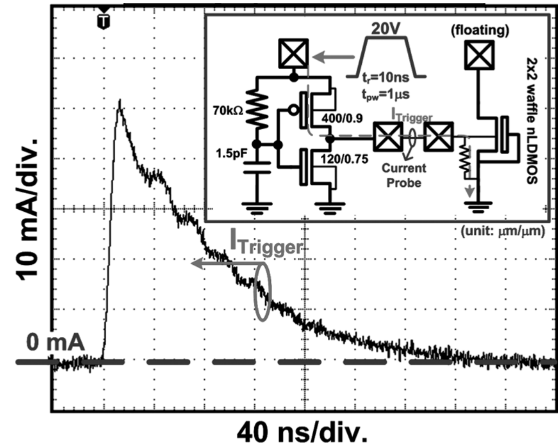


Fig. 13. Turn-on verification of the stand-alone trigger circuit in the 0.35-μm 24-V BCD process. The measurement setup is shown in the inset of this figure.

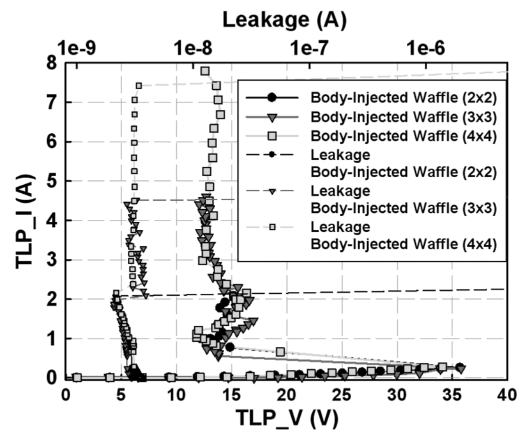


Fig. 14. TLP-measured $I-V$ characteristics of body-injected 24-V nLDMOS with waffle layout style.

discharging path of the stand-alone nLDMOS devices during ESD stresses.

In the 0.35-μm 24-V BCD process, the ESD detection circuit was also composed of an RC distinguisher and an HV inverter. A stand-alone trigger circuit was fabricated on-chip to verify the driving capability of the trigger circuit, as shown in Fig. 13. The corresponding measurement setup and device dimensions of the HV inverter used in the 0.35-μm process are shown in the inset of Fig. 13.

The output of the stand-alone trigger circuit was externally shorted to the trigger nodes of a stand-alone 24-V nLDMOS with waffle layout style. A voltage pulse with 10-ns rise time t_r and 1-μs pulsewidth t_{pw} was given into the stand-alone trigger circuit. Measurement result showed that the trigger circuit can provide a peak I_{Trigger} of 50 mA into the trigger nodes of the waffle nLDMOS.

With the body current injection, TLP-measured $I-V$ characteristics for body-injected waffle nLDMOS are shown in Fig. 14. TLP-measured I_{t2} for body-injected waffle nLDMOS with 2 × 2, 3 × 3, and 4 × 4 drain squares are 2.07, 4.41, and 7.42 A, respectively.

In addition to the body-injected waffle nLDMOS, the body current injection method was managed to be implemented on the nLDMOS with stripe layout style. As the layout diagram shown in Fig. 15, two P+ trigger bars were drawn at the two sides of the 24-V nLDMOS with the stripe layout style. The output of the trigger circuit was internally connected to these two P+ trigger bars, and these two P+ trigger bars were electrically shorted to the grounded P+ at the source side through the p-body of

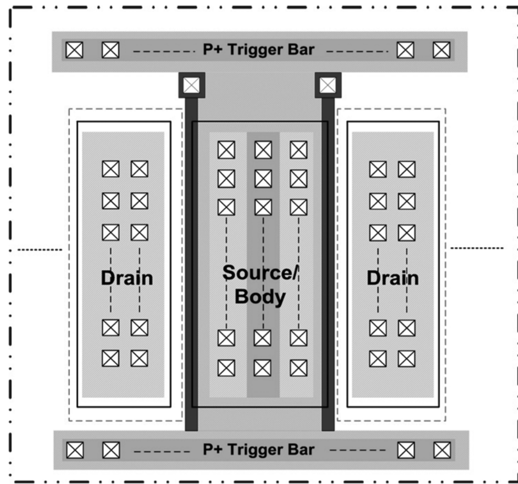


Fig. 15. Layout diagram of the 24-V stripe nLDMOS with two P+ trigger bars at two sides of the device for body current injection.

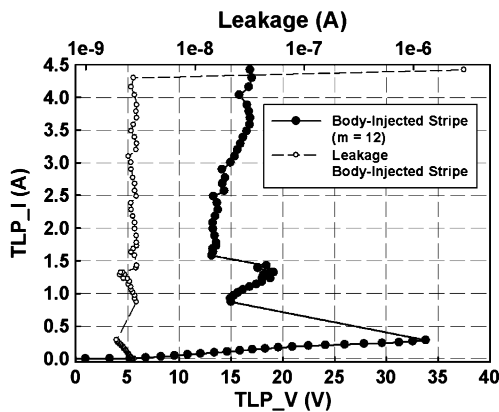


Fig. 16. TLP-measured $I-V$ characteristics of body-injected 24-V nLDMOS in stripe layout style.

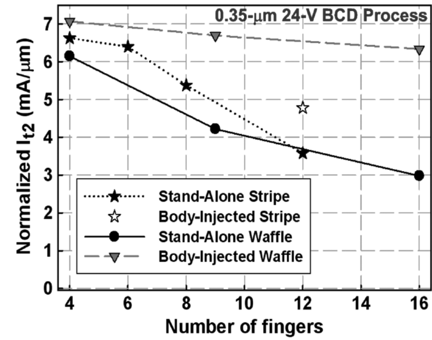


Fig. 17. Normalized I_{t2} current among different types and fingers of 24-V nLDMOS.

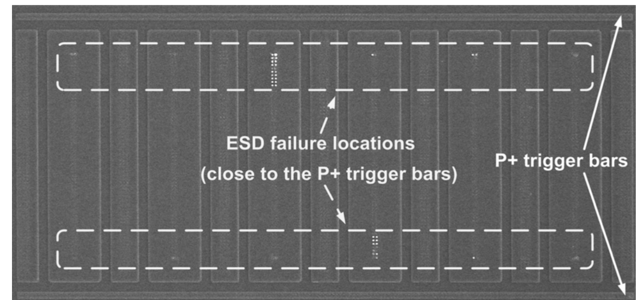


Fig. 18. SEM image of the body-injected 24-V nLDMOS with stripe layout style after 100-ns TLP measurement.

the nLDMOS. The 24-V stripe nLDMOS can therefore be body injected during ESD stresses through the two P+ trigger bars.

For the body-injected stripe nLDMOS, the studied device has 12 fingers, each having a width of 73.2 μm/0.75 μm. The TLP-measured $I-V$ characteristic for the body-injected stripe nLDMOS is shown in Fig. 16. Compared to the stand-alone stripe nLDMOS with 12 fingers, the measured I_{t2} is increased from 3.16 to 4.2 A by using the body current injection.

To compare the ESD performances between different types of nLDMOS, TLP-measured I_{t2} values are normalized to corresponding effective device widths (W), as shown in Fig. 17. For stand-alone nLDMOS devices, a slightly higher normalized I_{t2} is found on the stripe nLDMOS when the number of fingers is 4. With the increasing number of fingers, normalized I_{t2} for stand-alone stripe nLDMOS is found to more rapidly degrade than that for stand-alone waffle nLDMOS. For the stripe nLDMOS devices studied in this work, fingers were drawn in parallel. For the waffle nLDMOS devices, drain squares were both horizontally and vertically expanded. As a result, the horizontal layout width of the stripe nLDMOS is larger than that of the waffle nLDMOS. For example, the layout width for the stripe nLDMOS with 12 fingers is 180.2 μm, whereas the layout width for the waffle nLDMOS with 4 × 4 drain squares is 136.5 μm. Because bonding pads were placed at the middle of the testing devices, the stripe nLDMOS has the higher mismatch of parasitic metal resistance from the bonding pad to each finger of the nLDMOS. Accordingly, the stand-alone stripe structure shown in Fig. 17 shows a severer degradation rate on the normalized I_{t2} values, compared with the stand-alone waffle structure [13].

With the body current injection, the stripe nLDMOS with P+ trigger bars was found to have normalized I_{t2} lie in between stand-alone nLDMOS devices and body-injected waffle nLDMOS. A SEM image of the body-injected stripe nLDMOS with P+ trigger bars after TLP measurement is shown in Fig. 18. From the SEM image, contact spiking was observed in every finger of the body-injected stripe nLDMOS. However, contact spiking was found only on the drain regions near the two P+ trigger bars. No ESD failure was observed at the center portion of the stripe nLDMOS with body current injection. Because the body current was injected from the two P+ trigger bars, which was grounded by the P+ body contacts at the source side, parasitic BJTs closer to the P+ trigger bars have smaller parasitic p-body resistance from the P+ trigger bars to the grounded P+ body contacts. As a result, parasitic BJTs closer to the P+ trigger bars receive higher body injection current during ESD stresses. This inhomogeneous body current distribution leads to the result that ESD failures were found to localize on the drain contacts close to the two P+ trigger bars. For nLDMOS devices in waffle layout style, because the side width of each drain square is 18.3 μm (which is much shorter than the 73.2-μm finger width of the body-injected stripe nLDMOS), they were less impacted by the inhomogeneous body current distribution.

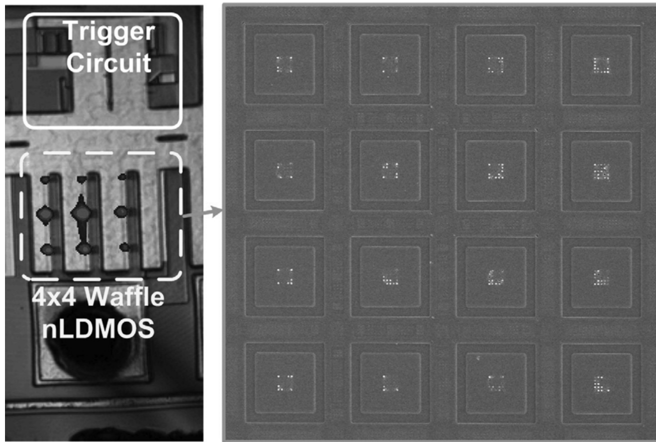


Fig. 19. OBIRCH and SEM images of the body-injected 24-V nLDMOS with waffle layout style after 100-ns TLP measurement.

TABLE I
ESD ROBUSTNESS OF NLDMOS DEVICES STUDIED IN THIS WORK

		W/L (μm/μm)	I_{t2} (A)	HBM (kV)
16-V nLDMOS	Stand-Alone Stripe	(45.45/0.35) x 8	0.39	0.75
	Stand-Alone Waffle	(40.4/0.35) x 9	0.41	0.75
	Body-Injected Waffle		0.95	1.25
24-V nLDMOS	Stand-Alone Stripe	(73.2/0.75) x 4	1.94	3.5
		(73.2/0.75) x 6	2.81	4
		(73.2/0.75) x 8	3.15	5
		(73.2/0.75) x 12	3.16	5.5
	Body-Injected Stripe	(73.2/0.75) x 12	4.2	7
	Stand-Alone Waffle	(73.2/0.75) x 4	1.8	3
		(73.2/0.75) x 9	2.78	4.5
		(73.2/0.75) x 16	3.49	6.5
	Body-Injected Waffle	(73.2/0.75) x 4	2.07	4
		(73.2/0.75) x 9	4.41	7
		(73.2/0.75) x 16	7.42	>8

Body-injected waffle nLDMOS thereby performed higher normalized I_{t2} than that of body-injected stripe nLDMOS.

From the normalized I_{t2} among different types of nLDMOS devices shown in Fig. 17, nonuniform triggering was found to be substantially alleviated by using the waffle layout style and the body current injection. Body-injected waffle nLDMOS therefore exhibits the highest normalized I_{t2} among different types of nLDMOS shown in Fig. 17. Optical-beam-induced resistance change (OBIRCH) and SEM images of the body-injected waffle nLDMOS with 4×4 drain squares after TLP measurement are shown in Fig. 19. OBIRCH analysis in Fig. 19 shows uniform ESD failure locations on the waffle nLDMOS, instead of the trigger circuit, which implies that the ESD current is properly discharged through the ESD protection nLDMOS. With ESD failures spreading on every drain square of the 4×4 waffle nLDMOS, the SEM image further confirms that uniform triggering of nLDMOS is successfully achieved by using the body current injection. From the TLP measurement results and failure analyses, the effectiveness of body current injection on improving the ESD robustness of HV nLDMOS has been verified. The ESD robustness of nLDMOS devices studied in this work is summarized in Table I. Six samples were tested for the HBM ESD protection levels shown in Table I, and the levels reported in Table I are the lowest ESD-sustained levels among the six tested samples.

IV. CONCLUSION

nLDMOS in high-voltage technologies has been known to have poor ESD robustness. Additional PBI on the source side of nLDMOS has been found to degrade the ESD robustness of snapback-based nLDMOS. Through the collaboration of the newly proposed waffle layout style and the ESD trigger circuit, the body-injected technique has been fulfilled in a 0.5-μm 16-V BCD process and a 0.35-μm 24-V BCD process. The 100-ns TLP measurement results have shown that, by using the body current injection, the I_{t2} of the waffle nLDMOS can substantially be increased. Failure analyses have further revealed the improved turn-on uniformity of nLDMOS devices by the body current injection. From these experimental results, the body-injected technique has been verified as an effective method to increase the ESD robustness of nLDMOS in HV ICs without modifying process steps nor increasing mask layers.

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