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Variation of Electrostatic Discharge Robustness Induced by the Surface Morphology of High Power Light-Emitting Diodes

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The capability of high-power nitride-based light-emitting diodes (HPLED) to withstand electrostatic discharge (ESD) is very important key index due to the horizontal structure of the insulating property of the sapphire substrate. Accordingly, the investigation of ESD failure mechanisms is a beneficial topic. However, it is difficult to real-time monitor the damage caused by the ESD stress because it occurred in a very short period. Before the series ESD stress, atomic force microcopy (AFM) and conductive AFM (C-AFM) were applied to explore the correlation between surface morphology and electrical properties of LED chips. Furthermore, after the series ESD stress, transmission electron microscopy (TEM) was used to investigate the failure modes and compare to the distribution of the surface current observed by C-AFM. These findings suggest that the V-shaped defect and surface morphology are strong correlate to the endurance of ESD stress.
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1. Introduction

High bright blue and green light-emitting diodes (LEDs) have been successfully commercialized using GaN-based LEDs and applied widely in many fields.[1–4] Such applications are available in traffic light, full color display, backlight of mobile phone, and white light source with phosphors for general illumination. The rapid developments of the solid state light (SSL) of LEDs are due to several advantages comparing to conventional lights, such as longer lifetime, higher efficiency, lower pollution, and so on. In recent years, many applications of LEDs become more and more popular. Therefore, we require more stable LEDs. Due to the insulating feature of sapphire substrates, it is very important to improve electrostatic discharge (ESD) reliability of nitride-based devices. In the investigation of ESD endurance, there are many methods to combine a GaN-based LED with a device such as a metal oxide semiconductor (MOS) capacitor,[5] an inverse-parallel protection diode,[6] complementary metal–oxide–silicon (CMOS) protection circuits,[7] a GaN Schottky diode,[8] a Si-based Zener diode[9] and so on. Although these methods can effectively improve the ESD characteristic of GaN-based LEDs, it takes more complex processing steps which may result in lower production yields and higher production coasts.

In the present day, the LED chips have to do a sampling inspection of ESD stress before the shipment. The ESD simulating test is a part of reliability of LED chips and can check the early failure stresses of LED chips. To understand the role of ESD stress and the physical environments, it is important to quantify the characteristic times of an ESD stress. There are three fundamental models to simulate ESD stress in the nature. The first model used in the ESD industry is known as the human body model (HBM) pulse which is intended to represent the interaction the electrical discharge from a human being, who is charged, with a component, or object. Another model is known as the machine model (MM) pulse which is intended to represent the interaction the electrical discharge from a conductive source, which is charged, with a component, or object. At last, the charged device model (CDM) represents an electrostatic discharge interaction between a chip and a discharging means where the chip is pre-charged.[10]

The total failure periods can be expressed as a bathtub curve which is widely used in reliability engineering. It describes a particular form of the hazard function which comprises three parts: The first part is a decreasing failure rate, known as early failure periods. The second part is a constant failure rate, known as random failure periods. The third part is an increasing failure rate, known as wear-out failure periods.[11] In this study, we demonstrate the damage in detail using the high resolution examination instruments to investigate the failure of LED chips due to ESD simulation.

2. Experiment

The available 1 W blue high-brightness LED (HBLED) chips in this investigation were growth on the substrate of (0001) sapphire with standard size of $1 \times 1\,\mathrm{mm}^2$. A schematic diagram of a GaN-based multiple quantum well (MQW) LED was shown in Fig. 1. LED structure (dominant wavelength at 447 nm) consisted of a low-temperature thick GaN buffer layer, an undoped GaN layer, a highly conductive n-type GaN layer, an InGaN/GaN MQW active layer, and a p-type GaN layer. A mesa was performed for the current isolation and silicon dioxide film was deposited to preserve the sidewall of the LED device. A thin layer of indium tin oxide (ITO) around 300 nm thicknesses was deposited on the p-GaN layer and was used as the transparent contact layer (TCL). ESD stress occurred in a very short period and the accumulation of heat would be negligible during the experiment. Thus, LED chips were only soldered on TO-46 metallic package without any extra heatsink. At first, the electroluminescence (EL) spectrum and the current–voltage (I–V) characteristics were cataloged before the ESD stresses. The ESD stresses were simulated using a Model Ecdm-400E of ESD/CDM simulator from Tokyo Electronics Trading, which meets all of the testing requirements specified in MIL-STD-883 Method 3015, MIL-STD-750 Method 1020, ESD STM5.1, and EIA/JEDEC JESD22-A114-B for HBM model. After the increasing voltages of 500 V, 1 kV, 2 kV, 4 kV, and 99 times of 4 kV, both of EL spectrum and I–V characteristics were examined

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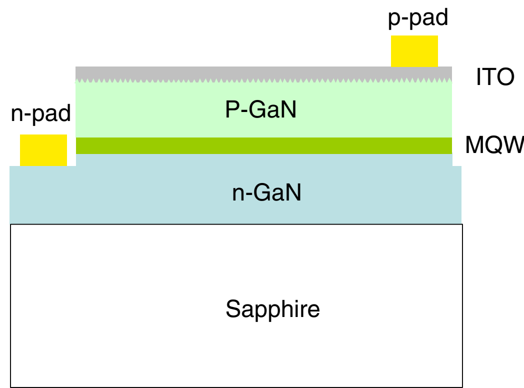

Fig. 1. (Color online) Schematic diagram of GaN-based LED structure.

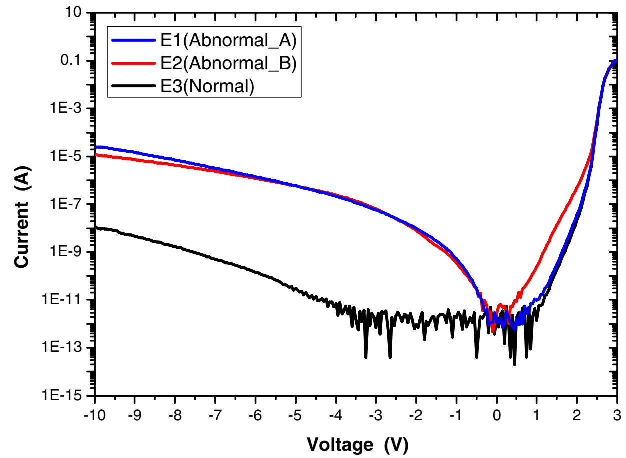

Fig. 2. (Color online) *I*–*V* characteristics of three specific LED chips were measured from −10 to 3 V.

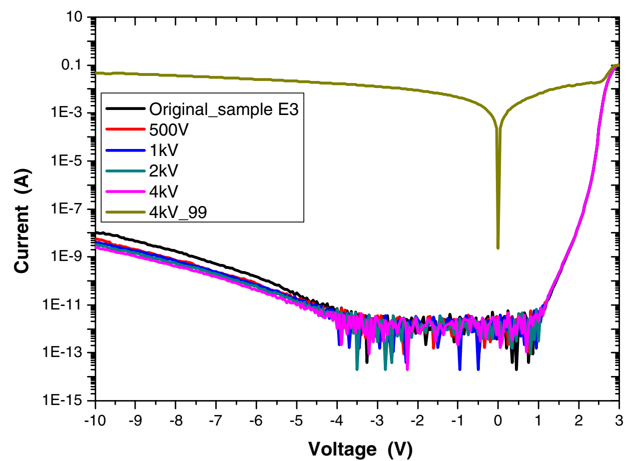

Fig. 3. (Color online) The semi-log plot of *I*–*V* curves shows the representative electrical properties of sample E3.

to chose specific damaged chips to do further examinations for investigating ESD failure mechanisms of LED chips.

The following is our technique to investigate the failure characterization of ESD stresses and evaluate the ESD endurance of LED chips. The electroluminescent (EL) mapping images are measured by ProMetric Color Model 14011 of Radiant Imaging. with Olympus BH2-UMA optical microscope. *I*–*V* characteristics were examined by Keithley 2430 sourcemeter and Veeco INNOVA conductive atomic force microscopes (C-AFM). In specifically destructive failure analysis, the infra-red optical beam induced resistance change (IR-OBIRCH) images localizes the defective point precisely and rapidly, which are taken by Hamamatsu μAMOS-200. Then, the abnormal micro-slices of chip are taken by FEI Nova-600 of focus ion beam (FIB). The global and local images of are captured by a Hitachi S-4800 scanning electron microscope (SEM). The precise cross-section images of transmission electron microscope (TEM) are taken by FET Tecnai G2F-20.

3. Results and Discussion

In the investigation, a complete wafer including over two thousands chips was measured their electrical properties. Three specific and representative LED chips were selected to label from E1 to E3 as shown in Fig. 2. The reverse leakage current of majority LED chips kept the baseline around 10^{-8} A under −10 V, such as sample E1. It was noting that the reverse leakage currents of sample E2 and sample E3 were close to the maximum specification 2 μA under −5 V and 3 orders of magnitude higher than the baseline (sample E3) of the reverse leakage current under −10 V.

All of the samples were under the increasing series of ESD stresses of 500 V, 1 kV, 2 kV, 4 kV, and 99 times of 4 kV. For each ESD stress, the electrical properties were immediately measured. After the series of ESD stresses, most of *I*–*V* curves presented that the reverse leakage currents improved slightly. Figure 3 displayed the effect of gradually increasing ESD stresses on the *I*–*V* characteristics of sample E3. After ESD stress of 500 V, 1 kV, 2 kV and 4 kV, the reverse leakage current was smaller than that without ESD stress, implying that ESD stress confined or improved some leakage paths. The reverse leakage currents in GaN-based LED chips that were heteroepitaxially grown on sapphire substrate are mostly associated with the tunneling of carriers through the dislocations, and the dislocation density was determined by the crystal growth.[12,13] LED undergoes both high-level injection and self-heating during ESD stress. This causes the temperature to increase, modulating the diode response. By modification of the diode high-level injection equation during an ESD event, we can calculate the current. In this development, it is assumed that the heating is expressed as the change of the junction temperature. The increase of junction temperature (T_J) is equal to the product of the thermal impedance (θ_{TH}) and the input power (P_D) as

$$T_J = \theta_{TH} P_D.$$

The power consumption can be evaluated as the power consumption in the diode region,

$$P_D = I_D V_D,$$
$$T_J = \theta_{TH}(I_D V_D).$$

The approach for the diode equation due to high-level injection and self-heating is solved for by correcting the temperature term by the temperature increase.[10] The increase of junction temperature and the extra electrical fields induced by ESD stress become the driving force to patch the chip defect, and thus the ESD stress reduced the conductivity of the dislocations for leakage currents. As the

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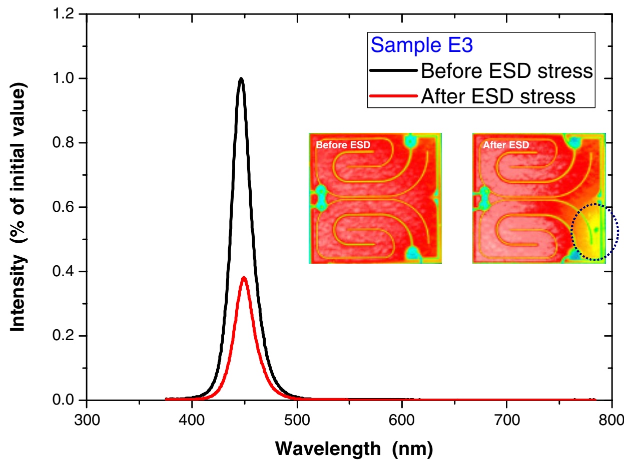

Fig. 4. (Color online) The spectrum distribution and EL mapping of sample E3 before and after the series ESD stresses.

ESD voltage was increased to 4 kV, the leakage current of sample E3 still kept stability around 10^{-8} A. However, the leakage current dramatically increased by 6 to 7 orders of magnitude after 99 times of 4 kV ESD stress. This implies that the continuous ESD stress would induce the accumulation effect in damaging the crystal and causing the defects.

Figure 4 presents the emission spectrum and EL mapping of sample E3 before and after the series ESD stress. The red-shift of the peak wavelength was minor under the ESD stress — only approximately 2.2 nm, but the intensity decayed around 61.75%. The damage caused by the ESD stress seriously affected the luminescence efficiency. Thus, as shown in the inset of Fig. 4, the EL mapping image of sample E3 after ESD stress exhibited that the intensity distribution of light was obvious decreased near the damage point at the right bottom corner of the chip.

For further investigating the failure mechanisms, the optical beam induced resistance change (OBIRCH) was used to locate the failure point and the OBIRCH image was consistent with the EL mapping image. According to OBIRCH defect image, the failure location was defined precisely and the melting damage caused by ESD stress was located on rough surface of the chip through SEM review. FIB was applied to drill a little piece of defect point and investigated the failure interfaces between different layers and dislocations.

After the series of ESD stress, three distinct damage characteristics were observed from the treated LED chips. The first damage characteristic was found between the p-pad metal line and mesa of LED chips labeled E1 which the defect was obviously caused in the chip processes. According to the EL mapping and OBIRCH image of sample E1, the impact area was not just a spot but an area. Furthermore, the ESD endurance of sample E1 was lower than other samples and it could not pass the most basic ESD stress of 500 V. As displayed in Figs. 5(a) and 5(b), the cleavage of ring-shape was on the top surface of LED chip, and a big V-shape crack at the bottom. In this case, the big crack and cleavage created a major short circuit through the MQW and caused the failure of LED chips. The second damage characteristic was found near the metal line of LED chips label E2 which the ITO film melted and threading

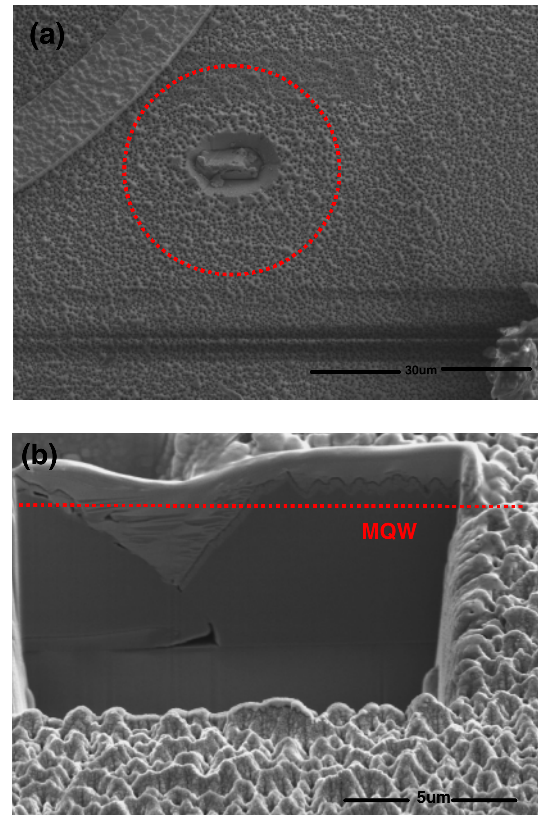

Fig. 5. (Color online) The characterization of sample E1 LED chip. (a) Top view of SEM image in the failure place. (b) The cross-section of local LED chip after FIB drilling.

dislocations occurred after the ESD stress of 2 kV. From SEM images of Figs. 6(a) and 6(b), there were large melting areas on the chip surface and a lot of voids were found in the image of SEM cross-section between ITO film and sapphire substrate. The third damage characteristic was found on the edge of the mesa of LED chip labeled E3 that presented the majority of the normal LED chips. The failure phenomena of sample E3 were the same as sample E2. The boiling area was discovered on rough ITO surface and many voids were found between ITO layer and p-GaN layer. However, the ESD endurance of sample E3 was better than some abnormal samples (such as sample E1 and E2) and it passed the series ESD stress till 99 times of 4 kV.

There were three possible failure mechanisms to explain the break down and weak ESD endurance between ITO and p-GaN. (1) In the process of roughing the surface of p-GaN layer in order to improve the light extraction efficiency, either the wet etching or low temperature growth of p-GaN layer was always forming the V-shaped pits which also appear as a result of surface termination of threading dislocations.[14] (2) Considering ITO as metal, V-shaped pits was filled with ITO like conductive needle-points. According to electromagnetics of the general physics, the needle-points endured the highest electric field and easily to cause the failure of break down. (3) Occasionally, the controls of the processes or parameters were not well enough and easily to form leakage paths. Thus, the LEDs with high reverse leakage currents have poor ESD endurance because the ESD stress would destroy the obvious leakage paths, such as sample E1.

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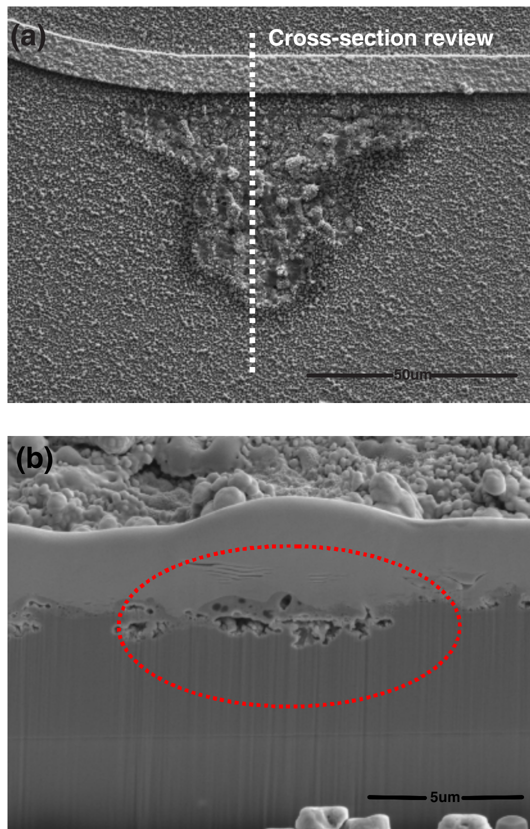

Fig. 6. (Color online) The characterization of sample E2 LED chip. (a) Top view of SEM image in the failure place. (b) The cross-section of local LED chip after FIB drilling.

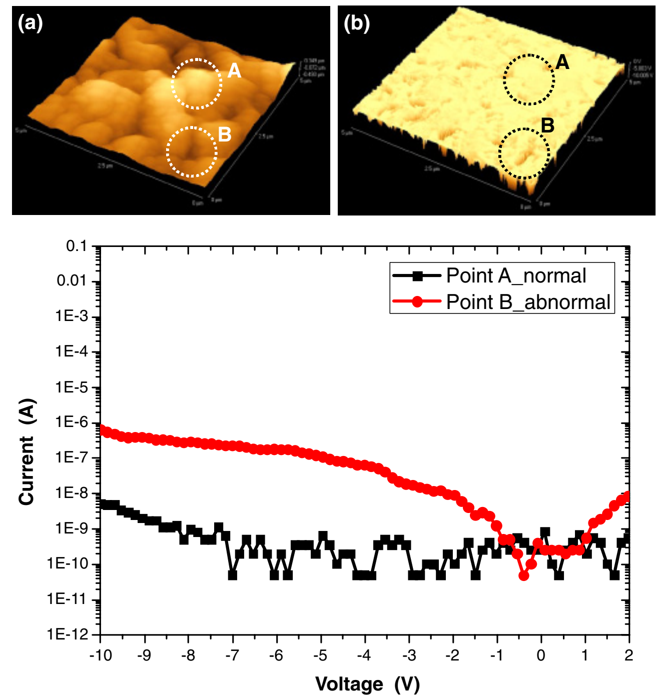

Fig. 7. (Color online) (a) AFM topography of sample E3. (b) C-AFM current image of sample E3 under −3 V reverse bias. (c) Nano-scale local *I*–*V* characteristics of sample E3 recorded at a defect-free region (point A_normal) and at a V-shaped defect (point B_abnormal).

In order to confirm our explanation as mentioned above, the AFM detection was employed to sample E3 before the ESD stress, then, to further compare with the TEM review. Figure 7(a) showed the $5 \times 5\,\mu m^2$ AFM image of sample E3 surface scanned in tapping mode and the root-mean square (RMS) surface roughness was around $0.7\,\mu m$. Figure 7(b) presented the $5 \times 5\,\mu m^2$ C-AFM current image recorded under -3 V reverse bias in the same area. No significant surface current was detected in the V-shaped defect-free area, such as point A. In contrast, it was obvious that most of the detectable currents were localized at the edge of the V-shaped defect, such as point B. According to the Figs. 7(a) and 7(b), strong correlation between the topography and the current image was obtained at a reverse bias of -3 V. Figure 7(c) presented the *I*–*V* characteristics recorded by placing the nano-scale diamond tip at the defect-free region (point A) and at the V-shaped defect (point B) as ramping the bias from $+2$ to -10 V. The reverse current at point A was greater than point B around two orders of magnitude under -10 V reverse bias. Therefore, LED still demonstrates the significantly different characteristics, even within a single chip, which leads to the specific distribution of the ESD stresses.

After the series ESD stress of sample E3, FIB was applied to drill a little piece of defect point precisely and explored the failure interface by TEM review as shown in Fig. 8. A TEM cross-section image of sample E3 showed the direct evidence of threading dislocations occurred in the location of V-shaped pits. Under high ESD stresses, the rough

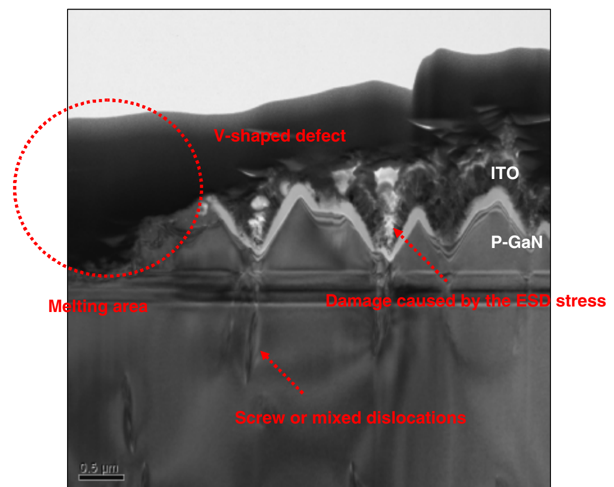

Fig. 8. (Color online) A cross-section image of bright-field TEM showing that V-shaped pits appear as a result of surface termination of threading dislocations under melting areas.

topography caused high electric field to induce corona discharge and then the discharge and self-heating caused the serious dislocations. V-shaped dislocation caused by the ESD stress was obviously generated from ITO film to p-GaN layer, and even broke through the MQW to cause short circuits parallel to the diode. Therefore the current might pass through the short circuits, and the LED chip produced heat instead of light. The dislocation density would not be the only key index to evaluate the ESD endurance. The performances of surface profile and leakage current of LED chip are also the main assessment factors.

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4. Conclusions

In the experiments, three distinct ESD damage characteristics in the specific high power LED chips are found: (1) The chip with the process defect cannot endure ESD stress of 250 V. (2) The chip with improper process parameters only endures ESD stress of 1 kV. (3) The chip with the optimum process can endure ESD stresses of 4 kV for few times. According to the trend of *I–V* characteristics, the endurance of ESD is better as the reverse leakage current of LED chip is smaller. Although the failure mechanisms of ESD damages are complicate, we could do a simple conclusion from our study. Without considering the quality of the chip or in-line process issue, the correlation between the AFM topography image and the C-AFM current image confirms that surface morphology is responsible for the ESD endurance. The area with high electrical field, such as V-shaped pits, is the major factor to enhance ESD damages during the ESD stress. Our results suggest that suppression of the V-shaped defect and the modification of surface morphology are essential for increasing the ESD endurance.

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