Impact of Process-Induced Uniaxial Strain on the Temperature Dependence of Carrier Mobility in Nanoscale pMOSFETs

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***Abstract*—This letter provides an experimental assessment of temperature dependence of mobility for advanced short-channel strained devices. By accurate split C–V mobility extraction under various temperatures, we examine the impact of process-induced uniaxial strain on the temperature dependence of mobility and mobility enhancement in nanoscale pMOSFETs. Our study indicates that the strain sensitivity of hole mobility becomes less with increasing temperature, and it is consistent with previous mechanical-bending result. Furthermore, the carrier-scattering mechanism for the pMOSFET under uniaxial compressive strain tends to be more phonon limited at a given vertical electric field, which explains the larger drain current sensitivity to temperature present in the compressively strained PFET.**

***Index Terms*—Mobility, MOSFET, strain silicon, temperature dependence.**

I. Introduction

UNIAXIAL strained-Si technology is crucial to transistor performance in state-of-the-art CMOS development [1]–[3]. The temperature effect on strain-enhanced mobility is of special importance because it may provide insights for the underlying mechanisms responsible for the performance enhancement. Several studies have investigated the temperature effect on strain-enhanced mobility in the past [4]–[7]. For NMOS, the temperature effect of process-induced biaxial strain [4], [5], uniaxial strain [4], and mechanical uniaxial strain [6] applied on devices has been experimentally studied. The results all indicated less strain sensitivity in carrier mobility with decreasing temperature. For PMOS, the temperature effect of process-induced biaxial strain [5] and mechanical uniaxial strain [7] has also been investigated. The results showed higher strain sensitivity in carrier mobility with decreasing temperature, i.e., an opposite trend with NMOS. However, the temperature effect of process-induced uniaxial strain in nanoscale PMOS devices is still not reported and merits investigation.

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In this letter, we conduct an experimental assessment for the impact of the process-induced uniaxial strain on the temperature dependence of carrier mobility in nanoscale pMOSFETs.

II. Experimental Setup

pMOSFETs with channel direction $\langle 110 \rangle$ with neutral, tensile, and compressive uniaxial contact Etch-Stop Layer (CESL) were manufactured based on the state-of-the-art CMOS technology on a 300-mm (100) silicon substrate [8], [9]. Shallow Trench Isolation (STI) was patterned to define the active region. A uniform channel doping was implanted to define the PMOS devices and maintain reasonable threshold voltage. Then an ultrathin nitride oxide was grown on the surface of the wafer. The polygate was implanted with heavily doped P$+$ species and postannealed to increase the gate activation rates. Then the ultrashallow Highly Doped Drain (HDD) implant, oxide/nitride spacer formation, source and drain implant, postimplantation annealing, and back-end process were implemented sequentially. The effective channel doping is around 2×10^{18} cm^{-3} for short-channel devices based on TCAD simulation. The equivalent oxide thickness is about 17 Å. For comparison purposes, nitride films with neutral, -2.8-GPa compressive strain, and 1.6-GPa tensile stress were deposited on pMOSFETs at the CESL deposition stage. The details about our TCAD simulation are in [15].

Since the external resistance $(R_{\rm sd})$ is crucial to the short-channel mobility extraction [10], [11], the intrinsic drain current (I_D) was calibrated by considering the series-resistance effect [8]. The physical polygate length $(L_{\rm phy})$ was obtained using inline SEM measurement. The LDD overlap region under the gate $(L_{\rm ov})$ was extracted by the split C–V method [14]. The effective channel length $(L_{\rm EFF})$ can then be derived by subtracting $L_{\rm ov}$ from $L_{\rm phy}$. Finally, the mobility for short-channel devices can be determined [8]. In this letter, PMOS devices with effective channel length $L_{\rm EFF} = 95$ nm were measured with temperature ranging from 100 to 300 K.

III. Results and Discussion

Fig. 1 shows the drain current (I_D) versus gate voltage characteristics at various temperatures for the PMOS devices under test. The drain current shows strong correlation with stressor types and can be explained by the extracted carrier mobility, as shown in Fig. 2. It can be seen from Fig. 2 that the short-channel mobility in PMOS $(L_{\rm EFF} = 95$ nm$)$ shows significant dependence on the uniaxial strain. The PMOS mobility prefers

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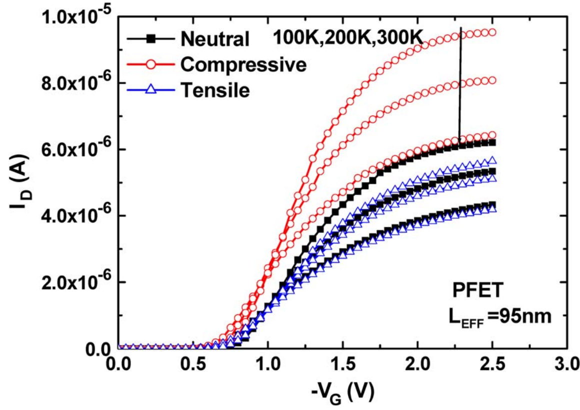

Fig. 1. Drain current versus gate voltage at various temperatures for PFETs with various stressors. The drain bias (V_{DS}) is -5 mV. The temperature dependence of the drain current shows strong correlation with stressor types. The length of diffusion is 0.29 μm.

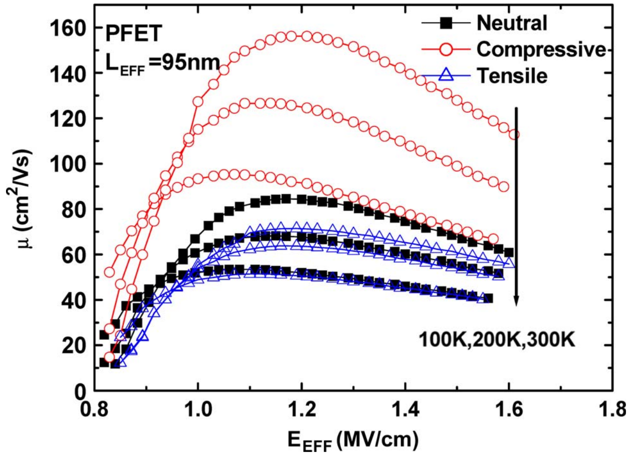

Fig. 2. Extracted carrier mobility shows significant dependence on the uniaxial stressor.

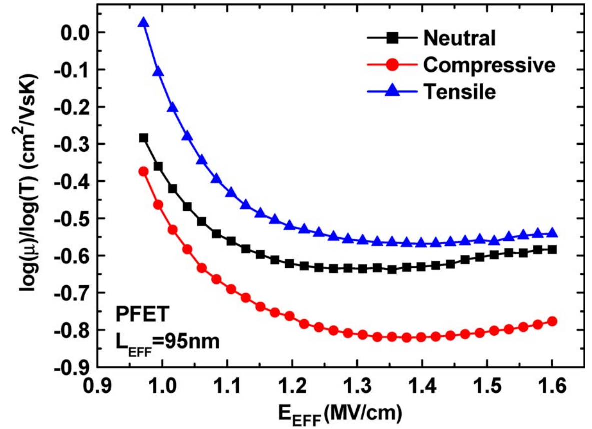

Fig. 3. Temperature sensitivity of hole mobility versus the vertical field for various uniaxial stressors.

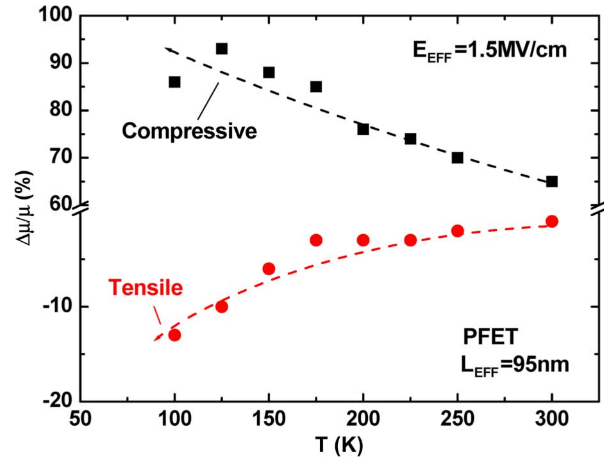

Fig. 4. Hole-mobility enhancement versus temperature at $E_{\mathrm{EFF}} =$ 1.5 MV/cm for PMOS devices with various stressors.

compressive stress because of the strain-reduced conductivity effective mass [9].

In addition, Fig. 2 shows that the mobility is degraded when temperature increases in the high vertical-field region, where phonon scattering is important [12], [13]. Moreover, the temperature dependence of mobility shows strong sensitivity to strain. In other words, as the mobility is enhanced by compressive strain, its temperature dependence also increases.

Fig. 3 shows the temperature sensitivity $(\log \mu / \log T)$ of the hole mobility versus the vertical effective electric field (E_{EFF}). For a given stressor, it can be seen that the temperature sensitivity increases (i.e., more negative) and then saturates as E_{EFF} increases. More importantly, the $\log \mu / \log T$ for the PFET under compressive strain is the highest in absolute value among the three stressors. In other words, the scattering mechanism of the PMOS device becomes more phonon limited [12], [13] under compressive strain. This also explains why the temperature sensitivity of drain current for the compressively strained PFET is the largest among the three stressors, as shown in Fig. 1.

Fig. 4 shows the hole-mobility enhancement $(\Delta\mu/\mu)$ versus temperature at $E_{\mathrm{EFF}} = 1.5$ MV/cm. It shows that for both compressive and tensile stressors, the magnitude of $\Delta\mu/\mu$ decreases as temperature increases. Our result from the process-induced uniaxial stressors is consistent with the study in [7], in which an external compressive uniaxial mechanical stress was applied.

Based on the model proposed in [7], it is plausible that as temperature increases, the compressively strained PFET has less holes to populate states near the band edge where the conductivity effective mass along the channel direction is smaller. Therefore, the observed mobility enhancement decreases with increasing temperature.

IV. Conclusion

We have investigated the temperature dependence of mobility for advanced short-channel strained PMOS devices. By accurate split C–V mobility extraction under various temperatures, we examine the impact of process-induced uniaxial strain on the temperature dependence of mobility and mobility enhancement in nanoscale pMOSFETs. Our study indicates that the strain sensitivity of hole mobility becomes less with increasing temperature, and it is consistent with previous uniaxial mechanical-bending result. Furthermore, the carrier-scattering mechanism for the pMOSFET under uniaxial compressive strain tends to be more phonon limited at a given vertical electric field, which explains the larger drain current sensitivity to temperature present in the compressively strained PFET.

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