Nanoscale p-MOS Thin-Film Transistor With TiN Gate Electrode Fabricated by Low-Temperature Microwave Dopant Activation

Yu-Lun Lu, *Student Member, IEEE*, Fu-Kuo Hsueh, Kuo-Ching Huang, Tz-Yen Cheng, Jeff M. Kowalski, Jeff E. Kowalski, Yao-Jen Lee, *Member, IEEE*, Tien-Sheng Chao, *Senior Member, IEEE*, and Ching-Yi Wu

***Abstract*—In this letter, nanoscale p-MOS TFTs with a TiN gate electrode were realized using a novel microwave (MW) dopant-activation technique. We compared both low-temperature MW annealing and rapid thermal annealing. We successfully activated the source/drain region and suppressed the short-channel effects using low-temperature MW annealing. This technique is promising from the viewpoint of realizing high-performance and low-cost upper layer nanoscale transistors required for low-temperature 3-D integrated circuit fabrication.**

***Index Terms*—Low temperature, metal gate, microwave (MW) anneal, rapid thermal annealing (RTA).**

I. Introduction

THE 3-D DESIGN of integrated circuits (ICs) is considered to be a promising solution to increase the device packing density and to reduce the interconnection delay, power consumption, and cost [1], [2]. However, dopant activation using a high thermal budget process may cause diffusion and redistribution of dopants in the 3-D structure, in turn affecting the underlying interconnects and device layers [3], [4]. In addition, one of the main challenges in fabricating a nanometer-scale transistor is the accurate control of the active doping regions. However, applying any high-temperature process after implantation causes dopant diffusion and redistribution. High diffusion rates make it difficult to realize a shallow junction depth. Rapid thermal annealing (RTA) has an emissivity-related pattern effect, where the photon adsorption strongly depends on the material and temperature. Therefore, it relies on heat transfer at the cost of undesired diffusion. In addition, the pattern effect or shadow from an upper stack is expected to be more significant and degrades the uniformity of the dopant activation of devices in the different levels of a 3-D structure.

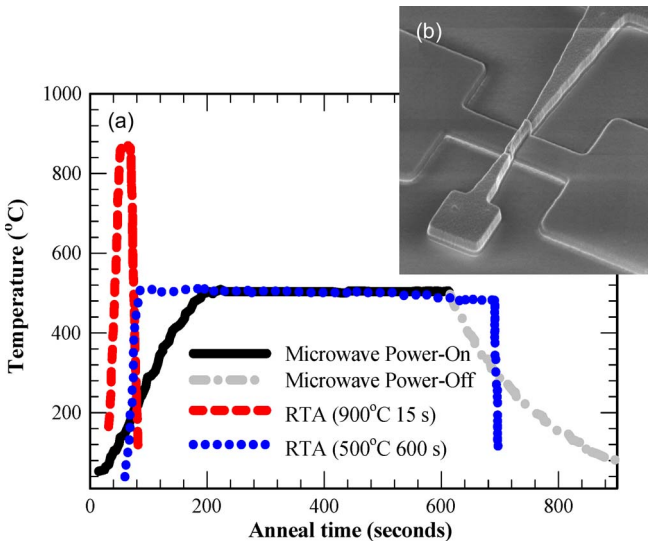

Fig. 1. (a) Comparison of temperature profiles of different dopant-activation methods. The MW anneal time is defined as the period when the MW power is turned on. (b) Side-view SEM image of the device.

Microwave (MW) annealing is a potential solution for the issues of 3-D fabrication because it may provide a lower temperature process that restrains diffusion and results in good activation [5]. For example, a 3-nm-thick Ge epilayer on a Si substrate was preserved with boron activation, illustrating a low-temperature MW annealing process application [6].

The mechanisms of MW energy absorption in semiconductors includes ohmic heating and dielectric relaxation [7]–[10]. In particular, at lower frequencies (<10 GHz) ohmic heating will dominate [8].

Furthermore, metal and metal alloys are more attractive as alternative gate-electrode materials than a doped poly-Si gate because the use of the latter involves many constraints such as high resistivity, poly depletion, and instability in high-k

Manuscript received January 15, 2010; revised January 26, 2010. Date of publication March 8, 2010; date of current version April 23, 2010. This work was supported in part by the National Science Council, Taiwan, under Contracts NSC-98-2221-E-492-019, NSC-98-2221-E-212-033-MY3, and NSC-98-2120-M-006-003. The review of this letter was arranged by Editor J. K. O. Sin.

Y.-L. Lu, T.-Y. Cheng, and T.-S. Chao are with the Department of Electrophysics, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: yulun.ep96g@g2.nctu.edu.tw; alexcheng@frontiersemi.com; tschao@mail.nctu.edu.tw).

F.-K. Hsueh is with the National Nano Device Laboratories, Hsinchu 30078, Taiwan (e-mail: fkhsuech@ndl.org.tw).

K.-C. Huang is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 30010, Taiwan (e-mail: evol6381@hotmail.com).

J. M. Kowalski and J. E. Kowalski are with DSG Technologies, Inc., Morgan Hill, CA 95037-7522 USA (e-mail: jeff.edward@dsgtek.com; jeff.kowalski@dsgtek.com).

Y.-J. Lee is with the National Nano Device Laboratories, Hsinchu 30010, Taiwan, and also with the Department of Physics, National Chung Hsing University, Taichung 402, Taiwan (e-mail: yjlee@ndl.org.tw).

C.-Y. Wu is with the Department of Electrical Engineering, Dayeh University, Changhua 51591, Taiwan (e-mail: jameswu@mail.dyu.edu.tw).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2010.2042924

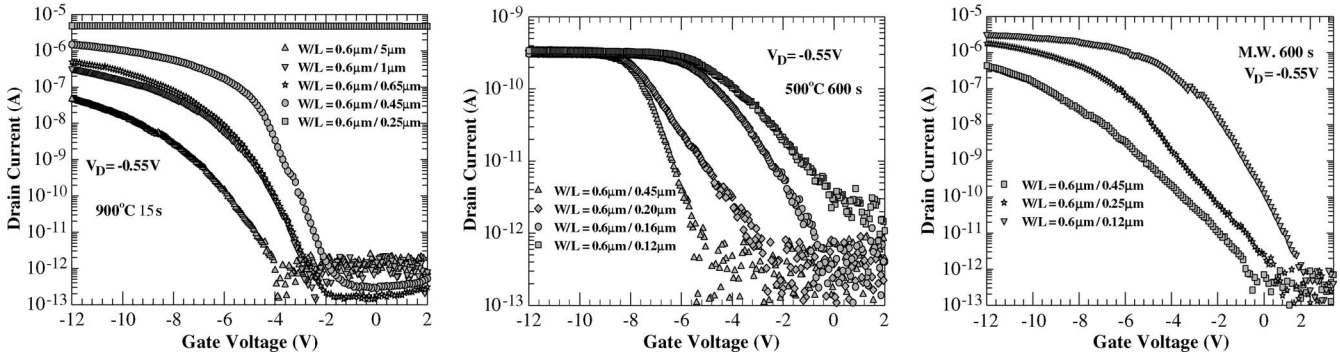

Fig. 2. Discussion of the characteristics (I_D–V_G) of p-MOS TFTs annealed by RTA and MW annealing. (a) RTA at 900 °C for 15 s and (b) furnace at 500 °C for 500 s. (c) MW annealing for 600 s. In (a), as the gate length is below 0.2 μm, the punchthrough effect dominates the transfer characteristics, and in (c), the $I_{\rm on}/I_{\rm off}$ ratios are about 10^8 for p-MOS using MW anneal for 600 s with $W/L = 60$ nm/120 nm.

materials. Recently, TiN has been investigated as a potential gate-electrode material because of the work function near the midgap in Si, and it is frequently used as a diffusion barrier.

In this letter, we demonstrate p-type metal–oxide–semiconductor thin-film transistors (p-MOS TFTs) with a TiN gate electrode in which the short-channel effects were suppressed.

II. Experiments

A 6-in (100) bulk silicon wafer was used as the starting material. After a 1-μm-thick silicon dioxide (SiO_2) layer was thermally grown as a buried oxide, a 50-nm-thick undoped amorphous Si film was deposited using low-pressure chemical vapor deposition (LPCVD), followed by solid-phase crystallization for recrystallization to improve the channel mobility. The active region was defined by electron-beam lithography. Then, a 45-nm-thick tetraethoxysilane oxide layer was deposited by LPCVD as a gate dielectric, and a 150-nm-thick TiN layer was deposited by PVD. After the gate was patterned by anisotropic etching, the source (S) and drain (D) were implanted with BF_2 (15 keV at 5×10^{15} cm^{-2}) for p-MOS TFTs followed by different dopant-activation conditions. The MW heating was performed in an AXOM-300 highly multimoded chamber, manufactured by DSG Technologies, Inc.[11].

Fig. 1(a) shows a comparison of the temperature profiles of different dopant-activation methods. Annealing was carried out using a 5.8-GHz MW for 600 s, and the maximum temperature was 500 °C. A N_2 purge was performed before the MW was started, and the N_2 flow was maintained until the process was completed. The MW annealing process time was defined as the duration for which the MW was turned on. In addition, the splits of RTA at 900 °C for 15 s and 500 °C for 600 s were used as the control splits, and they were in the N_2 flow environment during all annealing processes. The temperature profiles were measured from the wafer backside by an infrared detector during the RTA and MW anneal. Fig. 1(b) shows the top-view scanning electron microscopy (SEM) image, and the L_G/W is 0.12 μm/0.6 μm, where the gate oxide thickness is 45 nm and the channel thickness is 45 nm. The electrical characterizations were carried out using a Keithley 4200 system at room temperature.

III. Results and Discussions

Fig. 2 shows the transfer characteristics of p-MOS TFTs with different gate lengths annealed by (a) RTA at 900 °C for 15 s, (b) RTA at 500 °C for 600 s, and (c) MW for 600 s. From Fig. 2(a), the $I_{\rm on}/I_{\rm off}$ ratio is approximately 10^6 ($I_{\rm on}$ at $V_G = -12$ V and $I_{\rm off}$ at $V_G = 2$ V) with $L_G = 0.45$ μm. In addition, as the gate length is less than 0.45 μm, the off-current increases and the S/D punchthrough behavior, for which the $I_{\rm on}/I_{\rm off}$ ratio is approximately 10^0 with $L_G = 0.25$ μm, is observed. Therefore, with a 45-nm-thick gate oxide, it is difficult to fabricate nanometer-scale TFTs by the high-temperature RTA process. In the case of annealing by RTA at 500 °C for 600 s, as shown in Fig. 2(b), under the same annealing temperature and time as that for MW annealing, the magnitudes of all the on-currents are limited to approximately 10^{-9} A regardless of the transistor dimensions. The $I_{\rm on}/I_{\rm off}$ ratio is approximately 10^3 as L_G varies from 0.45 to 0.12 μm, indicating that the efficiency of boron activation in the S/D region by RTA at 500 °C for 600 s is too low to drive the D current.

However, it is interesting to note that the minimum gate lengths, as shown in Fig. 2(c), yielded by MW annealing for 600 s are 0.12 μm with $W = 0.6$ μm. The punchthrough effect is suppressed due to the low-temperature annealing process. In addition, the $I_{\rm on}/I_{\rm off}$ ratios are approximately 10^8 ($I_{\rm on}$ at $V_G = -12$ V and $I_{\rm off}$ at $V_G = 2$ V) for the p-MOS TFT fabricated using MW annealing for 600 s with $W/L = 0.6$ μm/120 nm. It appears that the low-temperature MW annealing process could suppress the short-channel effects. Furthermore, as compared with MW annealing using conventional RTA, the efficiency of boron activation in the S/D region is high in the case of nanoscale p-MOS TFT fabrication.

Fig. 3 shows the resistivity of a poly-Si film in the S/D region under different annealing conditions. In the case of annealing by RTA at 500 °C for 600 s under the same annealing temperature as that for MW annealing, the resistivity is the highest among all splits, indicating that the dopant could not be activated effectively.

The large resistivity of the S/D region after annealing by RTA at 500 °C for 600 s demonstrated the limit of the magnitude of the on-current, as shown in Fig. 2(b). In addition, under MW annealing for 600 s, the resistivity could be suppressed by around four orders, indicating that the dopant could be activated

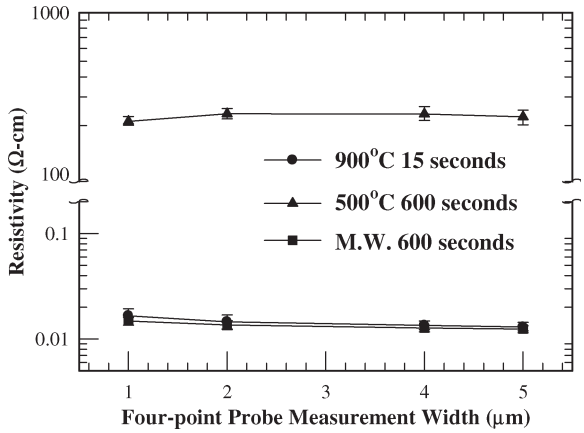

Fig. 3. Resistivity (ρ) of all splits as a function of the four-point probe measurement width. Resistivity (ρ) = Resistance (R) $\times$ A/L.

effectively by MW annealing. These phenomena indicate that, in addition to the temperature, the MW energy absorbed by a dopant is an important factor for dopant activation. Therefore, from the resistivity of the poly-Si film and the transfer characteristics, the dopant activation, punchthrough, and short-channel effect might be improved using MW annealing relative to RTA. It is also possible that residual PO_2 differences between the MW and RTA systems could account for some of the different results between the MW and RTA anneals [12]. The precise measurement of low PO_2 (at ppm levels) is beyond the scope and ability of this letter and remains a topic for future investigation.

IV. Conclusion

Different dopant-activation conditions are compared for various annealing techniques. The punchthrough characteristics and short-channel effect were suppressed by using a low-temperature MW dopant-activation technique, as demonstrated for nanoscale gate p-MOS TFTs. In addition, the results of the resistivity in the S/D region suggested that the boron dopant could be activated effectively with suitable short-channel-effect behavior by MW annealing for 600 s. Finally, this technique is promising from the viewpoint of realizing high-performance and low-cost upper layer nanoscale transistors required for 3-D ICs due to its low-temperature annealing process.

References

[1] S. Wong, A. El-Gamal, P. Griffin, Y. Nishi, F. Pease, and J. Plummer, "Monolithic 3D integrated circuits," in *Proc. Int. VLSI-TSA*, 2007, pp. 1–4.

[2] E.-K. Lai, H.-T. Lue, Y.-H. Hsiao, J.-Y. Hsieh, C.-P. Lu, S.-Y. Wang, L.-W. Yang, T. Yang, K.-C. Chen, J. Gong, K.-Y. Hsieh, R. Liu, and C.-Y. Lu, "A multi-layer stackable thin-film transistor (TFT) NAND-type flash memory," in *IEDM Tech. Dig.*, 2006, pp. 11–15.

[3] J.-H. Park, M. Tada, D. Kuzum, P. Kapur, H.-Y. Yu, H.-S. P. Wong, and K. C. Saraswat, "Low temperature ($\leq$ 380 °C) and high performance Ge CMOS technology with novel source/drain by metal-induced dopants activation and high-k/metal gate stack for monolithic 3D integration," in *IEDM Tech. Dig.*, 2008, pp. 389–392.

[4] K. C. Saraswat, S. J. Souri, V. Subramanian, A. R. Joshi, and A. W. Wang, "Novel 3-D structures," in *Proc. SOI Conf.*, 1999, pp. 54–55.

[5] Y.-J. Lee, Y.-L. Lu, F.-K. Hsueh, K.-C. Huang, C.-C. Wan, T.-Y. Cheng, M.-H. Han, J. M. Kowalski, J. E. Kowalski, D. Heh, H.-T. Chuang, Y. Li, T.-S. Chao, C.-Y. Wu, and F.-L. Yang, "3D 65 nm CMOS with 320 °C microwave dopant activation," in *IEDM Tech. Dig.*, 2009, pp. 31–34.

[6] Y.-J. Lee, F.-K. Hsueh, S.-C. Huang, J. M. Kowalski, J. E. Kowalski, A. T. Y. Cheng, A. Koo, G.-L. Luo, and C.-Y. Wu, "A low-temperature microwave anneal process for boron-doped ultrathin Ge epilayer on Si substrate," *IEEE Electron Device Lett.*, vol. 30, no. 2, pp. 123–125, Feb. 2009.

[7] H. Bosman, W. Tang, Y. Y. Lau, and R. M. Gilgenbach, "Heating of a particulate by radio-frequency electric and magnetic fields," *Appl. Phys. Lett.*, vol. 85, no. 15, pp. 3319–3321, Oct. 2004.

[8] K. Thompson, Y. B. Gianchandani, J. Booske, and R. F. Cooper, "Direct Si–Si bonding by electromagnetic induction heating," *J. Microelectromech. Syst.*, vol. 11, no. 4, pp. 285–292, Aug. 2002.

[9] K. Thompson, J. H. Booske, Y. B. Gianchandani, and R. F. Cooper, "Electromagnetic annealing for the 100 nm technology node," *IEEE Electron Device Lett.*, vol. 23, no. 3, pp. 127–129, Mar. 2002.

[10] K. Thompson, J. H. Booske, R. F. Cooper, and Y. B. Gianchandani, "Electromagnetic fast firing for ultrashallow junction formation," *IEEE Trans. Semicond. Manuf.*, vol. 16, no. 3, pp. 460–468, Aug. 2003.

[11] [Online]. Available: http://www.dsgtek.com/

[12] D. F. Downey, J. W. Chow, W. Lerch, J. Niess, and S. D. Marcus, "The effects of small concentrations of oxygen in RTP annealing of low energy boron, BF2 and arsenic ion implants," in *Proc. Mater. Res. Soc.*, Apr. 1999, pp. 263–272.