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博 士 論 文

矽鍺與矽碳薄膜應用於金氧半場效電晶體和

複晶矽鍺與多通道薄膜電晶體之研究

Study on SiGe and SiC Films in MOSFETs and

Poly-SiGe and Multi-Channel Poly-Si in TFTs

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矽鍺與矽碳薄膜應用於金氧半場效電晶體和複晶矽鍺與多通道薄膜電晶體之研究

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摘　要

本論文提出兩種元件，金氧半場效電晶體和複晶矽薄膜電晶體的製備來驗證薄膜的效應和應用於元件上面的整合度。

首先，我們提出在矽鍺($Si_{0.8}Ge_{0.2}$)磊晶薄膜中使用化學機械研磨方式來降低晶格不匹配所造成粗糙的表面，我們將全面的研究研磨墊和研磨液對平坦度的影響，接著使用一種新穎的研磨後清洗液應用於表面的清潔，經由加入表面清潔劑(surfactant, TMAH)和螯合劑(chelating agent, EDTA)可以有效的去除表面的微粒子和金屬殘留，表面的粗糙度也可有效的改善至 0.6 奈米。在電性方面，電容的量測可以得到高的崩潰電壓、低的漏電流和較佳的累積崩潰電荷密度；在電晶體的驗證上，可以得到十個百分比的電流增加。

接著，探討使用矽碳($Si_{1-y}C_y$, y=0.005)薄膜於動態臨限電壓電晶體(DTMOS)的應用，經由此介面層引入通道可有效抑制硼原子的擴散，達成高的基底摻雜和低的表面濃度分布。所形成的超陡峭(super-steep-retrograde)通道可使的表面散射(surface scattering)現象降至最低，對於動態臨限電壓電晶體元件有較好轉導(1.2倍)、高的導通電流(1.8 倍)和較低的臨限電壓(threshold voltage)表現，可以應用於低電壓操作元件。

第二部分我們研究 n 型複晶矽薄膜電晶體在多重通道(multi-channel)的表現。藉由增加通道的數目以提高閘極的控制能力，可以改善元件的電特性；包括提高導通電流，降低臨界電壓及次臨限擺幅(subthreshold swing)。然而，元件的可靠度卻會因此而變差。我們推測是由於在多重通道的結構中，靠近汲極端的電場強度會增加，而導致更嚴重的碰撞游離(impact ionization)所造成。

在論文的最後，我們開發出一種改善複晶矽鍺薄膜電晶體(poly-SiGe TFTs)的製程，經由氨氣的被覆(passivation)可以有效降低溫下矽鍺薄膜通道的缺陷；而經過化學機械研磨對於表面平坦化處理可以有效減低表面的粗糙度，所形成複晶矽鍺薄膜電晶體在結合此兩種處理的最佳化製程，可以得到很好的電性和可靠度表現，達成應用在低溫製程薄膜電晶體的應用。

Study on SiGe and SiC Films in MOSFETs and Poly-SiGe and Multi-Channel Poly-Si in TFTs

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ABSTRACT

In this thesis, two kinds of devices (MOSFETs and TFTs) have been fabricated to examine the films effect and integration of device characteristics.

First, the effects of polish pad conditions and slurry solid contents on SiGe chemical mechanical polishing (CMP) process were investigated. The novel cleaning solutions with various surfactants and chelating agents for post-CMP SiGe were studied. By adding the surfactant (TMAH) and chelating agent (EDTA) into the diluted ammonium solution, removal efficiency of particles and metallic impurities is increased. The smooth strained-Si surface on flatten $Si_{0.8}Ge_{0.2}$ buffer layer of 0.6 nm can be achieved. The electrical performances of capacitors such as breakdown voltage, leakage current and Q_{bd} are significantly improved for post-CMP cleaning.

Furthermore, the optimal condition of SC1+TE sample has increased about 10 % in drive current. This post-CMP cleaning process is useful for planarization of strain-relaxed SiGe virtual substrates in MOSFET application.

Next, we have demonstrated the fabrication of Dynamic Threshold voltage MOSFET (DTMOS) using the $Si_{1-y}C_y$ (y=0.005) incorporation inerlayer channel. Compare to conventional Si-DTMOS, the introduction of the $Si_{1-y}C_y$ interlayer for this device is realized by super-steep-retrograde (SSR) channel profiles due to the retardation of boron diffusion. The excellent performances obtained in the $Si_{1-y}C_y$ interlayer DTMOS are due to both the same substrate doping concentration and lower channel surface impurity concentration. So the surface impurity scattering could be reduces. We have successfully achieved the low threshold voltage and heavily doped substrate DTMOS with superior characteristics in terms of the higher transconductance ($1.2\times G_m$) and saturation current ($1.8\times I_D$). It appears to be a very promising technology for nano-scale device and ultra-low voltage application.

Then, we demonstrate the fabrication process and the electrical characteristics of n-channel polycrystalline silicon Thin-Film Transistors (poly-Si TFTs) with different numbers of channel stripes. The device's electrical characteristics, such as on-current,

threshold voltage, and subthreshold swing, were improved by increasing the number of channel stripes due to the enhancement of gate control. However, the electric field strength near the drain side was enlarged in multi-channel structures, causing severe impact ionization. Therefore, for the fabrication of highly reliable devices and to improve the yield of multi-channel TFTs, the channel structures must be carefully designed.

Finally, the improvement of polycrystalline silicon germanium thin-film transistors (poly-SiGe TFTs) using NH_3 passivation and CMP process was examined. Experimental results indicated that NH_3 passivation could effectively improve the turn on characteristics. Moreover, the TFTs fabricated on polished poly-SiGe film exhibit higher carrier mobility, better subthreshold swing, lower threshold voltage, and higher on/off current ratio due to the smooth poly-SiGe interface. The results clearly show that by employing the plasma and CMP steps, significant improvement in the poly-SiGe TFTs with low thermal budget can be achieved.

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Chapter 1

Introduction

1.1 Background

The past several years have witnessed rapid growth in the study of strained silicon due to its potential ability to improve the performance of very large scale integrated (VLSI) circuits independent of geometric scaling. Historically, performance improvements in metal-oxide semiconductor field-effect transistors (MOSFETs) have been attained by shrinking device dimensions such as the gate length and gate oxide thickness. However, the practical benefit of scaling is declining as physical and economic limits are approached, and novel solutions are increasingly being sought. The incorporation of new materials, from the interconnect level (Cu, low-k), to the gate stack (high-k dielectrics, metal gate electrodes), and even the substrate [strained-Si, silicon-on-insulator (SOI) wafers] is emerging as an important way to continue to improve circuit performance. Strain improves MOSFET drive currents by fundamentally altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths. There has been significant interest in SiGe heteroepitaxial growth on silicon substrates, because Si/ SiGe hetero-structures allow band-gap engineering to be used in conjunction with silicon technology. Of particular interest are the pseudomorphic p-type $Si_{1-x}Ge_x$ channel (x =10-20%) modulation doped field effect transistor (MODFET), the n-type strained Si channel MODFET and the p-type strained $Si_{1-x}Ge_x$ channel MODFET (x > 70%). Excellent review articles on these high mobility devices can be found in [1]-[5].

Strained silicon on relaxed silicon-germanium (SiGe) substrates is a promising candidate for transistor performance enhancement [6]. Strain splits the degeneracy in the conduction and valence bands of Si, enhances the transport properties of electrons and holes, and provides transistor speed enhancement. High quality strained-relaxed buffer layers are required for the high performance devices. But the relaxed SiGe layers tend to have the threading dislocation and rough surface. Several methods such as the graded buffer layers [7] and low temperature buffer [8] methods have been studies. The relaxation during the growth of the visual substrate results in a cross-hatch (misfit dislocations) which increases the surface roughness.

Next, we introduce the overview of poly-Si thin-film transistor. The TFTs have been widely investigated in industrial applications, such as active-matrix liquid-crystal displays (AMLCDs), high density static random access memories (SRAMs), electrical erasable programming read only memories (EEPROM) and candidate for 3-D ICs' applications, etc. Within those applications, the application of AMLCDs is the major driving force to promote the developments of poly-Si TFT technology [9]-[17]. It has been reported that the α-Si films can be crystallized by several techniques, such as SPC (solid-phase crystallization) [18], [19]; ELA (excimer laser annealing) [20], [21] and MILC (metal-induced lateral crystallization) [22] to obtain a large grain size of poly-Si to raise the field effect mobility. Additionally, there were other methods such as plasma treatments to passivate the defects in the channel or narrowing the channel width to reduce the trap state density. The electrical characteristics of poly-Si TFT is mainly influenced by the defects in the grain boundaries and within the grain [23]. Trap states resulted from those defects within the channel lead to poor device performance, such as low field effect mobility, large leakage current [24], bad subthreshold slope and high threshold voltage. It is

necessary to recover the trap states in the poly-Si channel to enhance the device performance. For this purpose, hydrogenation has been suggested to be an effective method [25]-[27]. The atomic hydrogen can recover interface states between poly-Si and SiO_2 and passivate defects in the grain boundaries to improve the device characteristics. Furthermore, other different treatments have been demonstrated to further enhance the device performance, for instance, H_2/N_2 mixture plasma [28], nitrogen implantation with H_2 plasma [29], pre-oxidation NH_3 annealing with H_2 plasma [30], NH_3 plasma [31], O_2 plasma [32], and H_2/O_2 plasma [33]. The atomic nitrogen and oxygen also have passivation effect by themselves and moreover the hydrogen passivation effects are greatly enhanced with their incorporation, leading to the observed great improvement in the device performance. Nevertheless, poly-Si TFTs with hydrogenation treatment have a troublesome problem in the performance degradation for the devices under electrical stress. It have been reported that the reliability of hydrogen-passivated TFTs was considerably poor because weak Si-H bonds or Si-Si bonds might be broken to cause the creation of trap states in the poly-Si channel [34].

1.2 Motivation

The epitaxy films used in chapter 3 and 4 were prepared by the UHVCVD system. First, the chemical mechanical polishing (CMP) process has become the mainstream of globe planarization technique in fabrication of deep submicron integrated circuit. To reduce this surface roughness, the CMP process is applied to the grown layers to reduce the surface roughness. Some previous works have been introduced it into polishing SiGe buffer layers [35]-[41]. The high crystalline quality of the re-growth layer with smooth interface makes it possible to fabricate high

performance SiGe device with low surface roughness scattering. However, the wafer surface after CMP process is seriously contaminated with particles and metallic impurities form polishing slurry. In addition, the metallic impurities will induce many crystal defects in Si wafer during thermal process [42]. And the planarized SiGe buffer layer roughness will be increased due to the etching effect [43]. Our previous studies have found that the novel post-CMP cleaning solution can significantly reduce the contamination retention [44]-[46]. We applied it to the post-CMP cleaning on SiGe buffer layer. Furthermore, the capacitor and MOSFET electrical characteristics of strained-Si re-growth on various solutions process were also evaluated.

Next, the epitaxy $Si_{1-y}C_y$ films also applied to the novel device application. A n-channel DTMOS with boron implantation was studied [47], [48]. The Dynamic Threshold MOSFET (DTMOS) structure offers a promising technology to achieve both high speed and low power performance. In order to take full advantage of the high current drive inherent in DTMOS, Chang *et al.* proposed the use of super-steep-retrograde (SSR) indium-channel profile [49], [50]. On the other hand, Takagi *et al.* also proposed a novel SiGe channel heterostructure DTMOS for reducing the threshold voltage in spite of keeping impurity doping level at the body region [51]. Transient enhanced diffusion (TED) of boron and phosphorus during annealing of implantation damage can be suppressed by incorporation of substitutional carbon. $Si_{1-y}C_y$ layer have been applied to suppress boron diffusion in hetero-junction bipolar transistors (HBT). The incorporation of substitutional carbon in silicon can reduce fast diffusion spices of boron diffusion in silicon [52]-[57]. An explanation for this behavior has been provided that the substitutional carbon present in the silicon substrate acts as the sink for silicon self-interstitial and the carbon spices are displaced by the silicon self-interstitial during thermal treatment processes. We

will examine the DTMOS device with the interlayer SiC films.

Moreover, the gate electrode across the channel may induce side-channels in both sides of the channel region, and these side-channels may increase the effective channel width. Especially when the channel width is scaled down, the side-channel effect is more distinct. The average carrier concentration in the channel region of the corner of the poly-Si gate electrode is increased by electrostatic focusing from the top gate and both side gates of the stripes [58]. It is believed that the gate control capability was obviously improved in narrow width devices. Accordingly, poly-Si TFTs with narrow and multiple channels have been proposed to enhance electrical characteristics [59]-[61]. However, no complete reliability analysis has been carried out in the poly-Si TFTs with narrow and multiple channels. We will demonstrate the fabrication process and the electrical reliability of n-channel poly-Si TFTs with different channel stripes.

Finally, silicon germanium (SiGe) is a promising candidate for use as the TFTs channel film, as it requires lower processing temperature than Si. Since the melting point of SiGe is lower than that of Si, the lower process temperature can be used for TFTs fabrication [62]-[65]. For low-temperature solid phase crystallization (LT-SPC) applications, SiGe is particularly advantageous, as it requires substantially shorter annealing cycles than required for the crystallization of Si. To date, using conventional SPC processing with no pre-amorphization implant, SiGe TFTs performance has generally been worse than poly-Si TFT performance. The SiGe TFTs performance has been improved substantially through the use of thin Si interlayer to improve the gate oxide interface [66]. However, little has been done to improve the intrinsic quality of the SiGe channel film itself; the binary nature of the SiGe system

complicates optimization and modeling substantially. In previously described preliminary optimization of SiGe TFTs through the use of multi-factorial design of experiment techniques [67], [68]. However, the rough surface of channel causes the poor performance and the low reliability of the device. It is shown that a planarized polysilicon surface will yield TFTs with improved performance and reliability. The CMP process has been used extensively for smoothing surface of polysilicon films [69]-[74]. Thus it is possible to be applied to smooth the poly-SiGe films. In this study, we develop optimization strategies for fabrication of high-performance SiGe TFTs.

1.3 Thesis Organization

There are six chapters in this dissertation. This thesis is organized as follow:

In chapter 1, the overview of our study and motivations of this thesis are described.

In chapter 2, the introduction of the UHVCVD system instrument used in our experiments. We have fabricated high-quality relaxed SiGe films using an intermediate Si interlayer within the channel region and SiC films.

In chapter 3, we have investigated planarization of rough surfaces of strain-relaxed $Si_{0.8}Ge_{0.2}$ buffer layer by CMP and post-CMP cleaning. The effects of polish pad conditions and slurry solid contents on SiGe CMP process were investigated. By optimizing the polishing conditions, the smooth strained-Si surface on flatten $Si_{0.8}Ge_{0.2}$ buffer layer of 0.6 nm can be achieved. The novel cleaning solutions with various surfactants and chelating agents for post-CMP SiGe were studied. The surfactant (TMAH) and chelating agent (EDTA) into the diluted ammonium solution, removal efficiency of particles and metallic impurities is increased.

In chapter 4, we have demonstrated the fabrication of Dynamic Threshold voltage MOSFET (DTMOS) using the Si1-yCy (y=0.005) incorporation interlayer channel. Compare to conventional Si-DTMOS, the introduction of the Si1-yCy interlayer for this device is realized by super-steep-retrograde (SSR) channel profiles due to the retardation of boron diffusion. A low surface channel impurity with heavily doped substrate can be achieved simultaneously. We have developed a novel n-channel Si1-yCy interlayer heterostructure DTMOS structure.

In chapter 5, we demonstrate the fabrication process and the electrical characteristics of n-channel polycrystalline silicon Thin-Film Transistors with different numbers of channel stripes. Poly-Si TFTs with multiple channels have better performance than conventional TFTs. Then, we fully discuss about the reliability of poly-Si TFTs with multiple channels. The effects of the number of channel stripes in multi-channel TFTs on performance and reliability have been investigated. For the fabrication of highly reliable devices and to improve the yield of multi-channel TFTs, the channel structures must be carefully designed.

In chapter 6, the improvement of polycrystalline silicon germanium thin-film transistors (poly-SiGe TFTs) using NH_3 passivation and chemical mechanical polishing (CMP) process was examined. Experimental results indicated that NH_3 passivation could effectively improve the turn on characteristics.

Finally, conclusions of this dissertation and recommendation for further research are presented in chapter 7. The compatibility of the propose technology can meet the trend of process requirement. It is expected that the processes in this thesis can be good choices in the future deep-submicron generation.

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Chapter 2

Deposition of SiGe and SiC Epitaxy Films by Ultra-High Vacuum Chemical Vapor Deposition (UHVCVD) System

2.1 Introduction

In the last few years, there has been significant interest in SiGe heteroepitaxial growth on silicon substrates, because Si/ SiGe hetero-structures allow band-gap engineering to be used in conjunction with silicon technology. Of particular interest are the pseudomorphic p-type $Si_{1-x}Ge_x$ channel (x =10-20%) modulation doped field effect transistor (MODFET), the n-type strained Si channel MODFET and the p-type strained $Si_{1-x}Ge_x$ channel MODFET (x > 70%). Excellent review articles on these high mobility devices can be found in [1]-[5]. To minimize the number of threading dislocations inside the relaxed $Si_{1-x}Ge_x$ buffer layer, it is customary to grow initially a rather thick linearly graded or step-graded SiGe layer (with a Ge composition close to zero at the beginning of the ramp and equal to x at the end of it), whose function is to accommodate gradually the lattice mismatch between Si and $Si_{1-x}Ge_x$, and thus confine the misfit dislocations inside the graded layer. The combination of a $Si_{1-x}Ge_x$ graded layer followed by a relaxed constant composition $Si_{1-x}Ge_x$ buffer layer is called a virtual substrate.

Strain improves MOSFET drive currents by fundamentally altering the band structure of the channel and can therefore enhance performance even at aggressively scaled channel lengths. A relaxed $Si_{1-x}Ge_x$ graded buffer creates a larger lattice constant on a Si substrate (i.e., “virtual substrates”) and can be used as an epitaxial

template for depositing Si-rich layers in a state of biaxial tension or Ge-rich layers in a state of biaxial compression. While uniaxial strain in the channel region of bulk Si MOSFETs can be intentionally induced during device processing, $Si_{1-x}Ge_x$ virtual substrates allow for the fabrication of wafer-scale strained layers that can confine holes or electrons. Such band-engineered heterostructures can be optimized to allow mobility enhancement factors over bulk Si of 2 for electrons and as high as 10 for holes.

The 4.2% difference in the lattice constants of Si and Ge atoms can be used to create high-mobility strain-engineered devices. Electron mobility is enhanced in strained-Si compared with bulk-Si due to tensile strain splitting the six-fold degenerate conduction band valleys and causing the resulting two-fold band with lower energy and reduced in-plane effective mass to be preferentially filled [6]. A four-fold band with increased energy is also created, which additionally contributes to the higher electron mobility through a reduction in intervalley scattering. Tensile strained-Si layers are, thus, useful for electron channels of high mobility n-MOSFETs. Epitaxial growth of Si on relaxed SiGe alloys creates such strained-Si layers due to the larger atomic spacing of Ge, and consequently relaxed SiGe alloys [7], compared with Si. Hole transport is improved in both tensile strained-Si and compressively strained-SiGe compared with bulk-Si. Modifications to the electronic band structure and a reduction of the hole effective mass have been found to increase mobility in strained-SiGe by five times [8]. Epitaxial growth of SiGe on either bulk-Si or relaxed SiGe alloys with a lower Ge content than the growing film can produce compressively strained-SiGe. There are some challenges in using strain to enhance the performance of CMOS devices and many of these are related to the critical thickness of a strained-layer [9]. If a strained-layer is grown above the critical thickness, strain

relaxes with the introduction of misfit defects at the strained-Si-SiGe hetero-interface and the enhanced transport properties arising from the strain are lost. Minimizing the exposure of the strained-material to high thermal budgets during processing reduces the probability of material degradation, since high temperatures cause strain to relax. However, non-optimized processing conditions may lead to degraded extrinsic performance [10]-[12]. Reducing the thickness of the strained-layer may protect the material against strain relaxation, but very thin channel layers compromise the performance gains achievable [13]. Dual-channel structures [14] minimize the cumulative strain within the devices by the sequential growth of tensile and compressively strained-layers, thereby allowing higher thermal budgets to be used before the onset of strain relaxation. The strain-compensation within the dual channel structure can alternatively be traded off against thicker strained-channel layers. By growing a compressive strained-SiGe layer followed by a tensile strained-Si layer on a single-relaxed SiGe "virtual substrate," the band offsets between the oppositely strained-materials can be used to create high mobility surface n- and buried p-channel MOSFETs. This dual-channel CMOS architecture has been shown theoretically to maximize the transconductance of both n- and p-channel devices for a range of achievable mobilities [15]. The benefits of using dual-channel device architectures have recently received attention [14]-[18]. Rim et al. have investigated p-channel performance in dual-channel architectures using a compressively strained-SiGe layer below a tensile strained-Si layer [16], but have only provided a limited assessment of electron mobility in such structures. Researchers at the Massachusetts Institute of Technology (MIT) have considered dual-channel structures with a view to optimizing buried p-MOS devices using relaxed Si Ge virtual substrates (VS), with [8], [17], [18], concluding that surface electron mobility is not influenced by the presence of a compressive SiGe buried p-channel layer. However, the devices had long channel

lengths and were fabricated using a low thermal budget process, unlike conventional CMOS. Optimizing the VS for n-channel performance is paramount, since n-MOSFETs often dominate circuit speed. Previously reported strained-Si n-channel MOSFETs fabricated using a high thermal budget on a dual-channel architecture, which was designed for obtaining high n-channel performance [14]. The devices were fabricated on ultrahigh vacuum chemical vapor deposition (CVD) virtual substrate material and demonstrated some of the highest performance gains reported to date compared with unstrained-Si control devices over a wide range of gate lengths. However, the primary aim of incorporating the buried strained-SiGe layer is to improve p-channel devices; in order for the increased complexity of dual-channel designs to be worthwhile, n-channel performance must not be compromised compared with devices having single-strained-Si surface channels, which benefit from having less complicated layer structures and processing requirements. At present, there are a number of uncertainties in understanding the advantages to strained-Si n-channel devices by using a dual-channel structure, and thus far, an experimental investigation has not been undertaken. Improved performance may be anticipated due to the increased confinement of electrons in the high mobility strained-Si surface channel compared with single-channel strained-Si MOSFETs. However, increased Ge diffusion into the tensile strained-Si channel from the high Ge-content strained-SiGe layer during processing, and additional complexity in the material growth, may offset any advantages offered by the double quantum well structure.

Due to the carrier mobility enhancement in the channel, strained Si complementary metal oxide semiconductor field effect transistors (CMOSFETs) have been reported to have a great improvement on dc and RF characteristics [20], [21]. In order to introduce tensile stress into Si, strain-relaxed SiGe layers grown on a Si

substrate are required to serve as virtual substrates [22], [23]. The conventional method for achieving fully relaxed SiGe epi-layers with low threading dislocations (TDs) densities is to grow 1–2 μm thick SiGe layers, in which mismatch strain is gradually released by a modified Frank–Reed (MFR) mechanism [24], [25].

We have fabricated high-quality relaxed SiGe films using an intermediate Si or $Si_{1-y}C_y$ layer [26, 27]. The misfit dislocations induced by the SiGe overlayers were formed or confirmed at the interface of SiGe overlayers and the intermediate $Si_{1-y}C_y$ layers.

2.2 UHV-CVD System Features

A photograph and the configuration of the SiGe epitaxial growth system are shown in Fig. 2.1 (a) and (b). The Unaxis SIRIUS UHV-CVD tool is built as customized unit. The system differs with regard to the arrangement of the pumps, the external appearance and other details. The reactor and load lock chamber has been improved to realize ultra-clean ambient for low temperature epitaxial growth. Fig. 2.2 shows an overview picture of how the system can be laid out. The sectional view shown in Fig. 2.3 is the inside layout of the SIRIUS schematically. The process chamber (D) from a cylindrical spaces, is connected to the UHV pump (A) via the vacuum duct (B) and can be evacuated to ultra high vacuum. The duct can be disconnected from the UHV pump with a gate valve directly before the UHV pump. The reactor tube is sealed off from the atmosphere with two sealing flanges (C). The furnace (E) is laid around the process chamber. It can be electrically heated and produces an exactly specified thermal flat zone of approx. ± 0.5℃ in the process chamber with an electric controller. The process chamber is separated from the load lock chamber (H) by the gate valve (G).

2.3 Epitaxy film growth

2.3.1 SiGe film

The starting materials adopted were 4 inch diameter, 15–25 Ω cm, p-type (001) -oriented Si wafers. All the epitaxial films investigated in this work were grown at 600℃ in a commercially available multi-wafer UHV/CVD system (Unaxis Sirrus 400). The base pressure of the reactor is typically below 8×10^{-9} mbar. High purity SiH_4, 5% GeH_4 diluted in He, were used as Si, Ge and B sources, respectively. Prior to the epitaxial growth, the p-Si wafers were dipped in a 10% HF solution to maintain the H-termination on the surface of the substrate before transferred to the UHV/CVD reactor in a quartz wafer boat through a load lock which is pumped down to a base pressure of 1×10^{-6} mbar within 10 min. A 60 nm thick Si buffer layer was first grown to cover the wafer surface. Then a 700-nm-thick $Si_{0.8}Ge_{0.2}$ film (the Ge concentration linearly graded from 0 to 20% were prepared) with a 50-nmthick intermediate Si layer was grown on the Si buffer, Finally, a 20-nm thick Si strained layer was deposited [27].

2.3.2 SiC film

Four-inch diameter, 10-25Ω cm, p-type (001)-oriented Si wafers were used as starting substrates. All structures investigated in this work were grown at 600 °C in a commercially available ultrahigh vacuum chemical vapor deposition (UHV/CVD) system. Pure SiH_4, $SiCH_6$, and 5% GeH_4 diluted in He were used as precursors. Before epitaxial growth, the Si wafers were dipped in a 10% HF solution to achieve the H passivation. A 60 nm thick Si buffer layer was first grown to cover the wafer surface. A 5 nm thick intermediate $Si_{1-y}C_y$ (y= 0.5%) layer was then grown on the Si

buffer. Finally, a 30 nm thick strained Si cap layer was deposited.

2.4 CMP System Features

Chemical mechanical planarization (CMP) is a process of smoothing and planed surfaces with the combination of chemical and mechanical forces, a hybrid of chemical etching and free abrasive polishing. Mechanical grinding alone causes too much surface damage, while wet etching alone cannot attain good planarization. Most chemical reactions are isotropic and etch different crystal planes with different speed. CMP involves both effects at the same time. A typical CMP tool consists of a rotating platen that is covered by a pad. The wafer is mounted upside down in a carrier on a backing film. The retaining ring keeps the wafer in the correct horizontal position. Both, the platen and the carrier are rotating. Good speed control is important. The carrier is also oscillating. For loading and unloading a robot system is installed. During loading and unloading the wafer is kept in the carrier by vacuum. During chemical mechanical polishing, pressure is applied by down force on the carrier, transferred to the carrier through the carrier axis. Beside that also gas pressure or back pressure is loaded on the wafer. The fact that high points on the wafer are subjected to higher pressures compared to lower points, hence, the removal rates there are enhanced and planarization is achieved. The slurry is supplied from above on the platen. Process relevant are the grain size and material of the abrasive component and the pH control of the slurry. We applied it to the post-CMP cleaning on SiGe buffer layer. Furthermore, the capacitor and MOSFET electrical characteristics of strained-Si re-growth on various solutions process were evaluated. Also, the CMP process was examined on the poly-SiGe TFTs.

2.5 Summary

This chapter introduces the instrument used in our experiment. The epitaxy films used in chapter 3 and 4 were prepared by the UHVCVD system in ERSO/ ITRI (Division of Semiconductor Device Technology, Electronics Research and Service Organization, Industrial Technology Research Institute).

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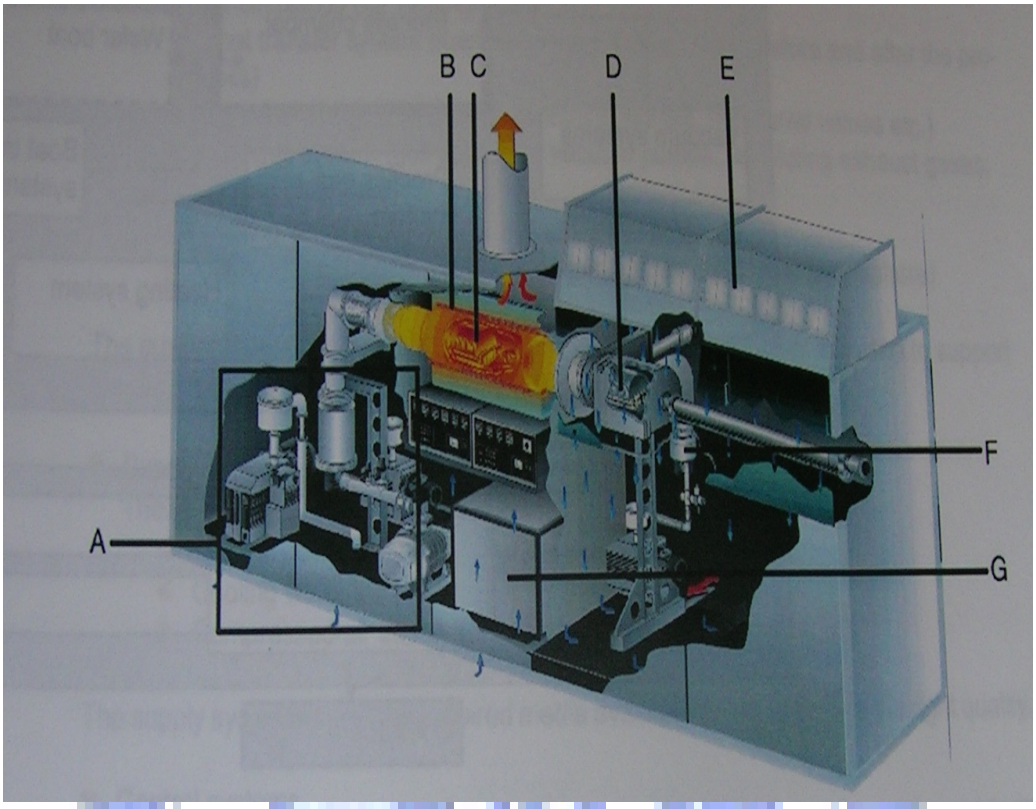
(a)

(b)

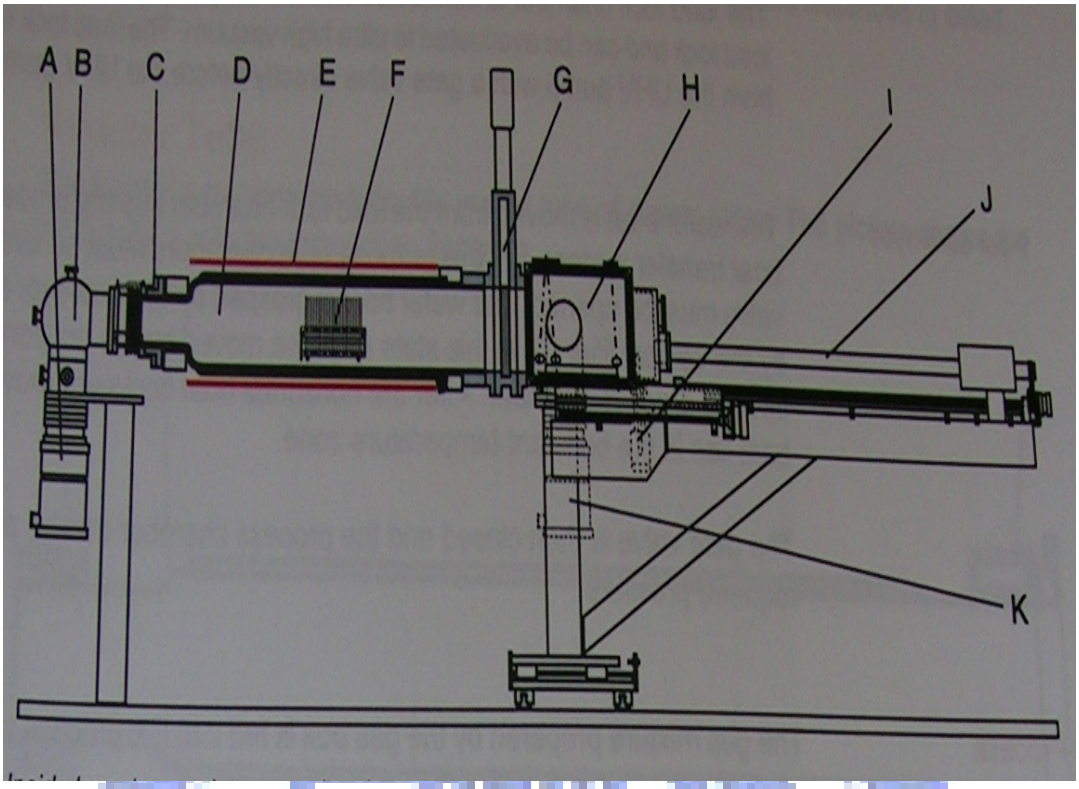
Fig. 2.1 Epitaxial films growth system SIRIUS (a) facade of the system and (b) process chamber.



Overview picture

A. Pumping station
B. Furnace
C. Reactor tube
D. Load lock
E. Clean air module (flow box)
F. Pumping system for load lock
G. Gas box

Fig. 2.2 Configurations of vertical SiGe epitaxial growth system.



Inside layout around process chamber

A. UHV pump of process chamber
B. Vacuum duct
C. Sealing flange
D. Process chamber
E. Furnace
F. Wafer boat with substrates
G. Gate valve between process chamber and load lock chamber
H. Load lock chamber
I. Boat conveyor vertical lifter
J. Horizontal boat conveyor
K. UHV pump for load lock chamber

Fig. 2.3 Configurations of film growth system inside layout around process chamber.

Chapter 3

The CMP Process and Cleaning Solution for Planarization of Strain-Relaxed SiGe Virtual Substrates in MOSFET Application

3.1 Introduction

Strained silicon on relaxed silicon-germanium (SiGe) substrates is a promising candidate for transistor performance enhancement [1]. Strain splits the degeneracy in the conduction and valence bands of Si, enhances the transport properties of electrons and holes, and provides transistor speed enhancement. High quality strained-relaxed buffer layers are required for the high performance devices. But the relaxed SiGe layers tend to have the threading dislocation and rough surface. Several methods such as the graded buffer layers [2] and low temperature buffer [3] methods have been studies. The relaxation during the growth of the visual substrate results in a cross-hatch (misfit dislocations) which increases the surface roughness. The chemical mechanical polishing (CMP) process has become the mainstream of globe planarization technique in fabrication of deep submicron integrated circuit. To reduce this surface roughness, the CMP process is applied to the grown layers to reduce the surface roughness. Some previous works have been introduced it into polishing SiGe buffer layers [4]-[10]. The high crystalline quality of the re-growth layer with smooth interface makes it possible to fabricate high performance SiGe device with low surface roughness scattering. However, the wafer surface after CMP process is seriously contaminated with particles and metallic impurities form polishing slurry. In addition, the metallic impurities will induce many crystal defects in Si wafer during

thermal process [11]. And the planarized SiGe buffer layer roughness will be increased due to the etching effect [12]. Our previous studies have found that the novel post-CMP cleaning solution can significantly reduce the contamination retention [13]-[15]. The surfactant Tetra Methyl Ammonium Hydroxide (TMAH) and the chelating agent Ethylene Diamine Tetra Acetic acid (EDTA) were used to enhance the removal efficiency of particle and metal. We found that removal efficiency of particle and metallic impurity for the post-poly-Si CMP cleaning. The electrical characteristics can be also improved by the novel post-CMP solution. In this chapter, we applied it to the post-CMP cleaning on SiGe buffer layer. Furthermore, the capacitor and MOSFET electrical characteristics of strained-Si re-growth on various solutions process were also evaluated.

3.2 Experimental

3.2.1 CMP procedure

The SiGe epitaxy layers on Si (100) substrate were prepared by ultra high vacuum chemical vapor deposition (UHVCVD) system. The novel relaxed 700-nm-thick SiGe buffer with a 50-nm-thick Si inserted layer was used in this work [16]. For measuring the SiGe layer thickness, we used the Electron Cyclotron Resonance (ECR) etcher to form the trench on the SiGe buffer layer and surface profiler to measure the height of the trench in order to monitor the thickness. The CMP experiment was carried out on a Westech model 372M CMP processor consisting of a Rodel IC 1400 pad and Politex buffering pad with diluted CABOT SS-25 slurry. The solid content of the experimental slurry was diluted by deionized (DI) water at volume ratios of 1/9and 1/18. The downforce pressure was fixed at 3 psi for studying the time effects. In the following, it was varied from 3 to 7 psi for 1

minute to investigate the effects of the down force pressure and removal rate. Surface morphologies were characterized by atomic force microscope (AFM).

3.2.2 Post CMP cleaning process

In the post-CMP cleaning experiment, wafers were sprayed with diluted NH_4OH solution with mega-sonic, followed by dispensing the cleaning solution with PVA brush after CMP process. There were four kinds of cleaning solution separated as following: (SC1) diluted 29% NH_4OH, (SC1+T) 29% NH_4OH+2.38% TMAH (volume ratio to NH_4OH is 1%), (SC1+E) 29% NH_4OH+EDTA (100 ppm), and (SC1+TE) 29% NH_4OH+2.38%+ TMAH (1%) + EDTA (100 ppm). Particle number was counted by the TENCOR surface scan model 4500 system. The total refection x-ray fluorescence spectrometry (TXRF) ATOMIKA model 8030W can be used to determine the metallic impurity. After the post-CMP cleaning process, 20 nm strained-Si film was form on the CMP SiGe buffer layer. For verifying the clean solution effect, a 20 nm TEOS oxide was formed a capacitor and MOSFET structures. The electrical properties of the capacitor of the current-voltage and time dependent dielectric breakdown (TDDB) characteristics were measured by using the Hewlett-Packard (HP) 4156 semiconductor parameter analyzer.

3.3 Results and Discussion

3.3.1 Material analysis

Figure 3.1 and 3.2 show the SiGe AFM image of the as-grown buffer layer before and after planarization. Various slurry solid contain and different pad properties shown in Table 3.1. There are four kinks of conditions. The effects of polishing pad properties on the process characteristics have been performed. The IC

1400 pad was compared with Politex polishing pad regard to the surface roughness. Polishing with the Politex pad, a better uniformity were achieved. As shown in Fig. 3.2, Ge01 and Ge03 samples almost have no cross-hatch pattern. The soften Politex pad is composite by the porous polymer and it could be uniformly distributed the polish particles. No differences in the pad influence on the geometry effects which can be explained with the same near-surface layer affecting the interaction between pad and wafer. The hardness of the IC 1400 allows the material to planarize across wide areas with minimal dishing and good planarity, but Politex polishing pad improves the resilience and compressibility of the pad and enhances the global uniformity in the polish removal. For the different solid content, the volume ratios of 1/9 shows better surface morphology at AFM root mean square (RMS) results in Table I. In order to have the controllable removal rate, different period of time from 1 to 3 minutes in 3 psi shown in Fig. 3.3 (a). The removal rate is a linear distribution amount the time scale, but the time extrapolation is not zero. As we started to polish the surface, it could be a thin oxide covered the SiGe buffer layer and slowed the polish rate. In fig. 3.3 (b) the pressure dependent removal rate will be saturated at a higher pressure. The conditions of stable removal rate and smooth surface interface are polished by Politex pad and 1/9 solid content ratio in 1minute and 3 psi. As Fig. 3.4 illustrates, the samples with and without CMP process was following by strained-Si re-growth. The RMS values of with and without CMP are 0.6 and 1.8 nm respectively. The Surface roughness and cross-hatch pattern were eliminated by CMP. Fig. 3.5 shows residual particles on the post-CMP cleaning surface with different solution. It is found that SC1+TE sample exhibits the highest efficiency. The slight surface etching of the wafer and electrical repulsion between wafer surface and particle can enhance removal of particles. It has been shown that hydrophobic surface resides more heavily particles on the wafer surface than hydrophilic surface [17]. Fig.

3.6 shows the metallic impurity concentration measured by TXRF. The metallic contaminants are significantly removed by the SC1+E and SC1+TE solution. The chelating agent reacts with metal ion as in the forms of metal-chelating complex.

3.3.2 Device characteristics

In Fig. 3.7, the current *vs.* electric voltage of the MOS capacitor cleaned by four solutions are shown. The MOS capacitor using SC1+TE solution depicts the lowest leakage current and highest breakdown voltage among these four samples. It is obviously seen that SC1 and SC1+T samples exhibits the second breakdown effect and it could be due to the metallic and particle containment shown in Fig. 3.5 and 3.6. Figure 3.8 shows the Weibull plot of leakage current measured at 3 Volts. The breakdown voltage distribution is shown in Fig. 3.9. A constant current stressing is used to investigate the gate oxide integrate. The charge to breakdown (Q_{bd}) measurements were performed on the post-CMP cleaning samples. The distribution for solution SC1+TE shows high Q_{bd} that can be attributes to efficient removal the particle and metal contaminations on strained-Si MOS capacitors. And we also applied it in MOSFET fabrications. The output characteristics of devices with channel length of 5 μm are shown in Fig. 3.11, the drain current increased about 10 % between SC1 and SC1+TE samples. The novel cleaning solutions with TMAH and EDTA showed the improvements which indicated that this solution for post-CMP on SiGe virtual substrates is a critical technique for developing high performance strained-Si MOSFET.

3.4 Summary

We have investigated planarization of rough surfaces of strain-relaxed $Si_{0.8}Ge_{0.2}$ buffer layer by CMP and post-CMP cleaning. It was found that soften polish pad can be eliminated SiGe surface roughness. The optimum conditions can achieve the strained-Si surface roughness of 0.6 nm. For the post-CMP cleaning process, various cleaning solutions have been applied to the SiGe buffer layer. By adding the surfactant (TMAH) and chelating agent (EDTA) into the diluted ammonium solution, removal efficiency of particles and metallic impurities is increased. The electrical performances of capacitors such as breakdown voltage, leakage current and Q_{bd} are significantly improved for post-CMP cleaning. Furthermore, the optimal condition of SC1+TE sample has increased about 10 % in drive current. This post-CMP cleaning process is useful for planarization of strain-relaxed SiGe virtual substrates in MOSFET application.

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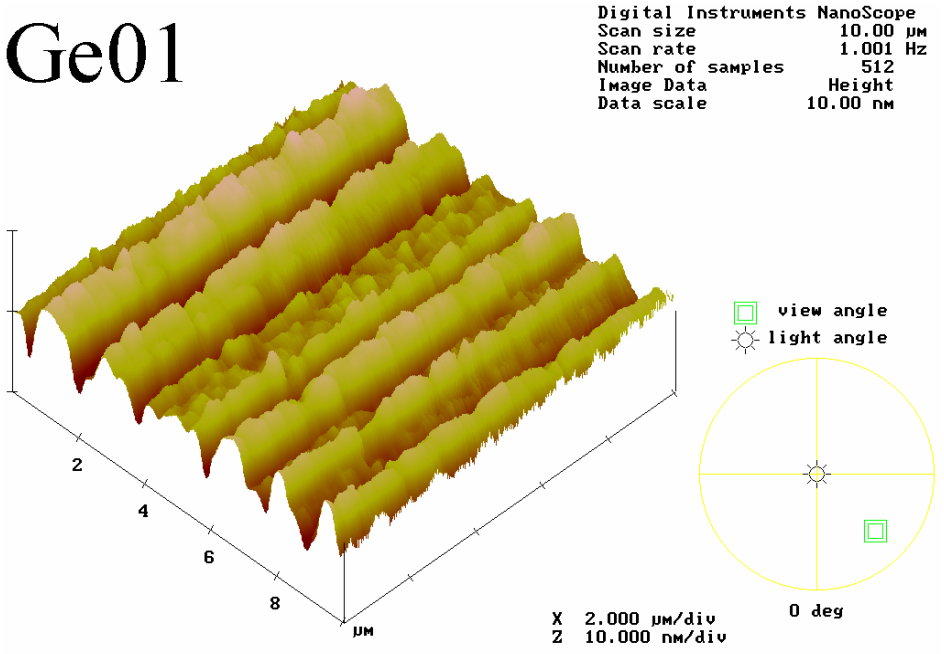
Table 3.1 Different slurry and pad conditions for Ge01, Ge02, Ge03 and Ge04 samples.

Slurry condition / Pad condition	Slurry : H_2O 1 : 9	Slurry : H_2O 1 : 18
Politex pad	**Ge01** (AFM R.M.S.) 20.6 Å → 2.52 Å	**Ge03** (AFM R.M.S.) 25.3 Å → 3.39 Å
IC1400 pad	**Ge02** (AFM R.M.S.) 22.1 Å → 2.69 Å	**Ge04** (AFM R.M.S.) 22.3 Å → 3.59 Å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light angle
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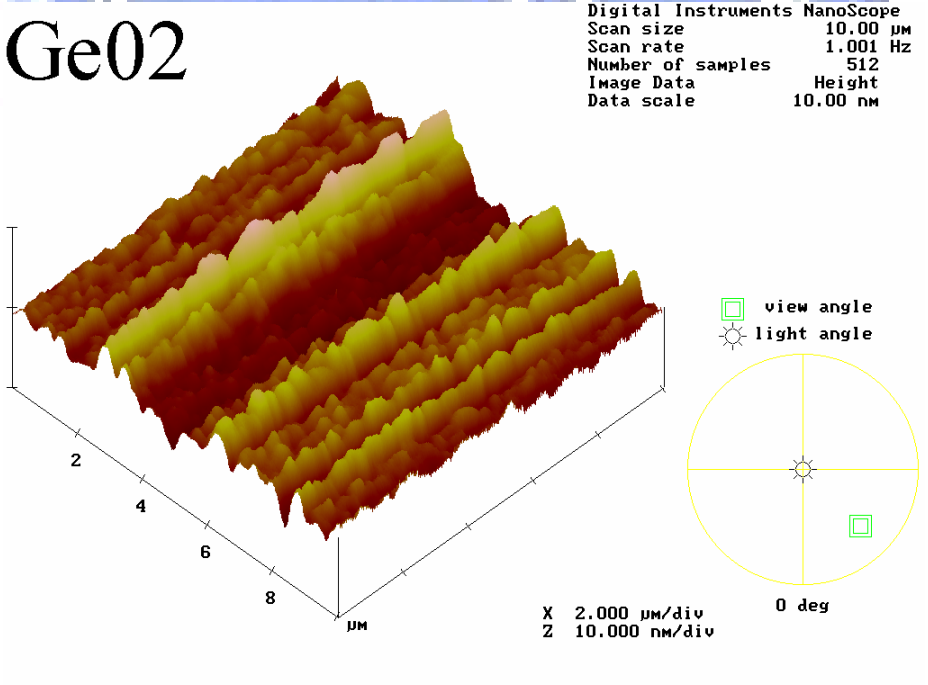
X 2.000 µm/div
Z 10.000 nm/div
0 deg

(a)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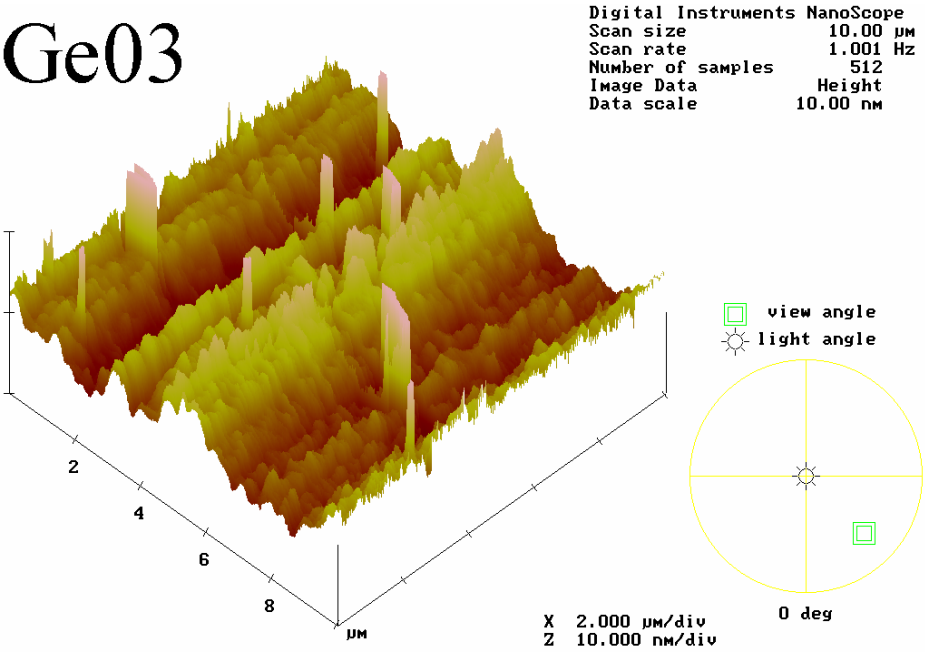
(b)



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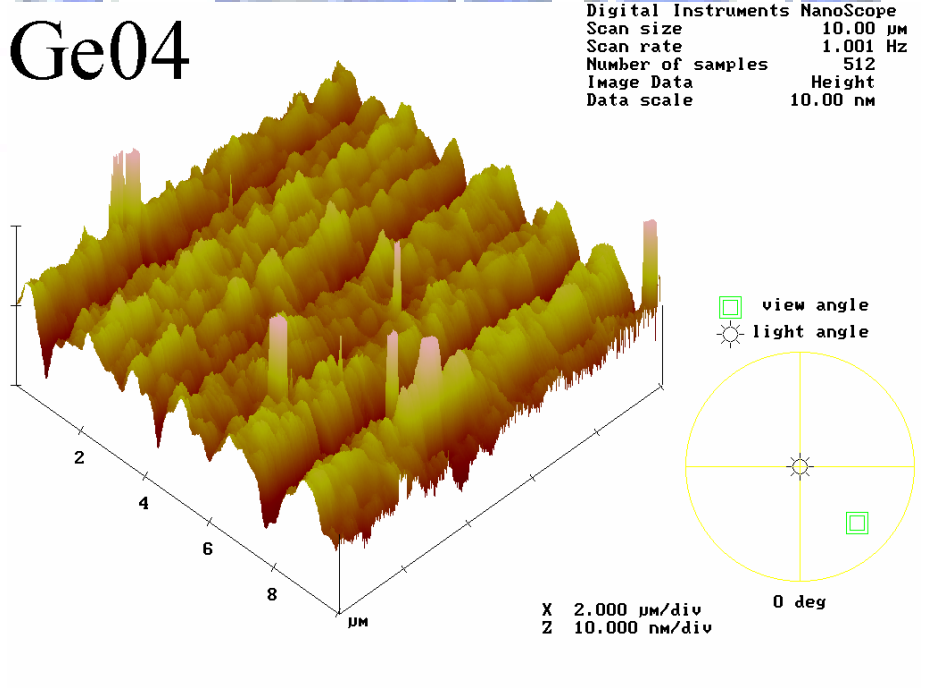
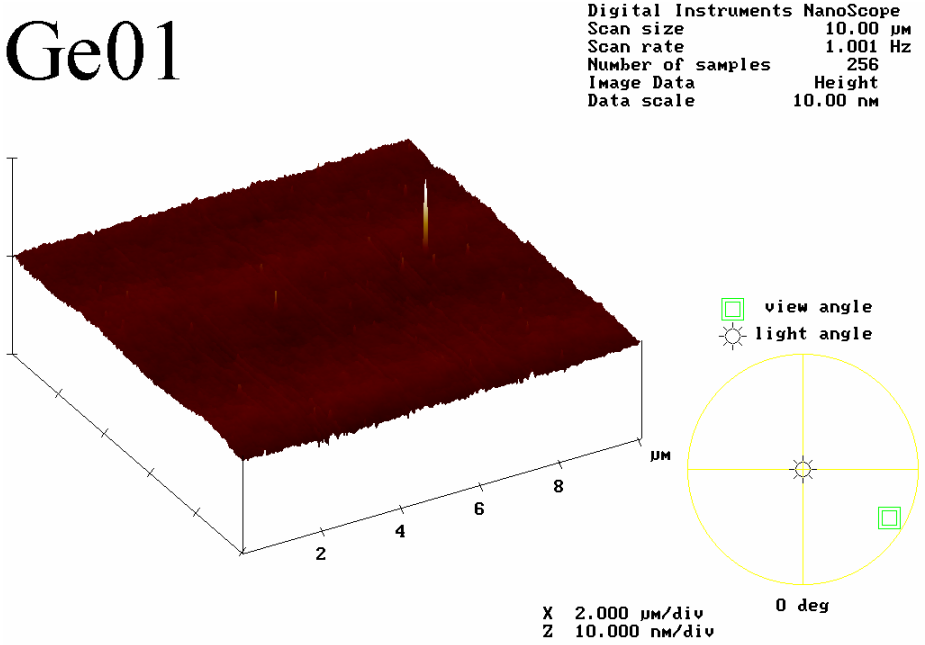


(d)

Fig. 3.1 AFM images of strained-relaxed SiGe buffer layers before CMP process. Different slurry and pad conditions for (a)Ge01, (b)Ge02, (c)Ge03 and (d)Ge04 samples.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Digital Instruments NanoScope
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light angle
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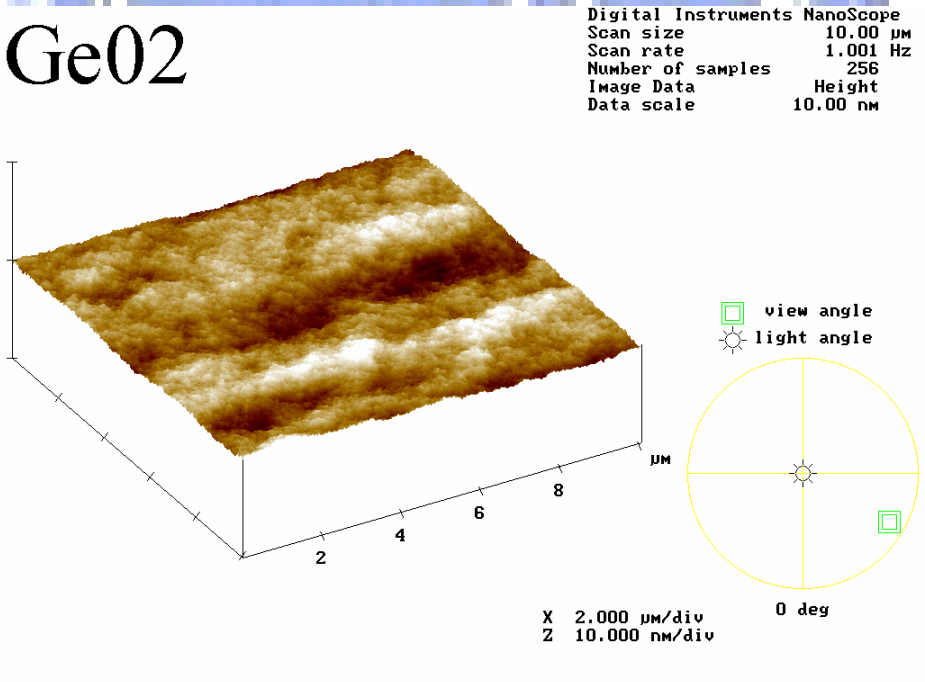
(a)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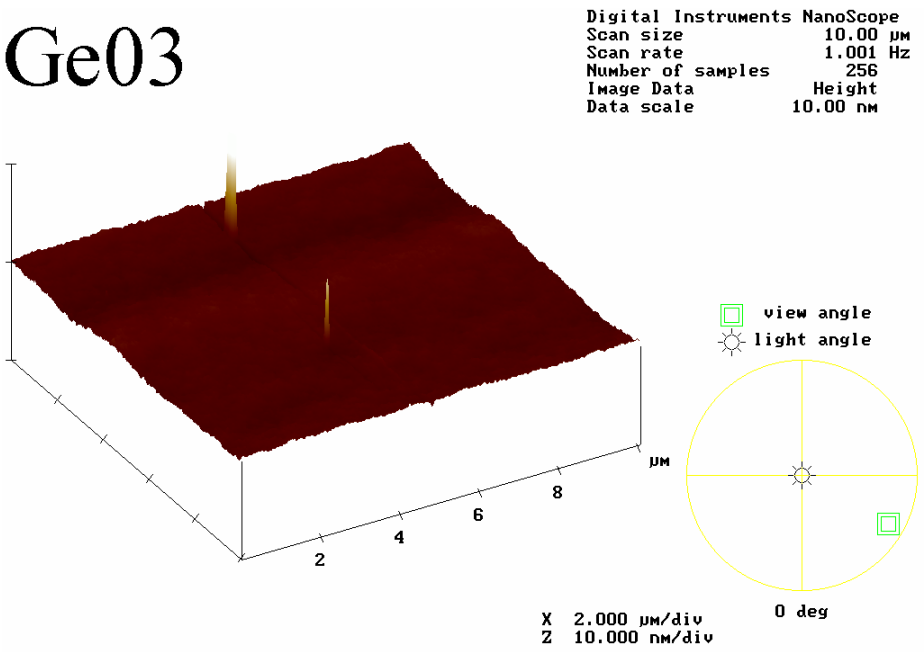
(b)



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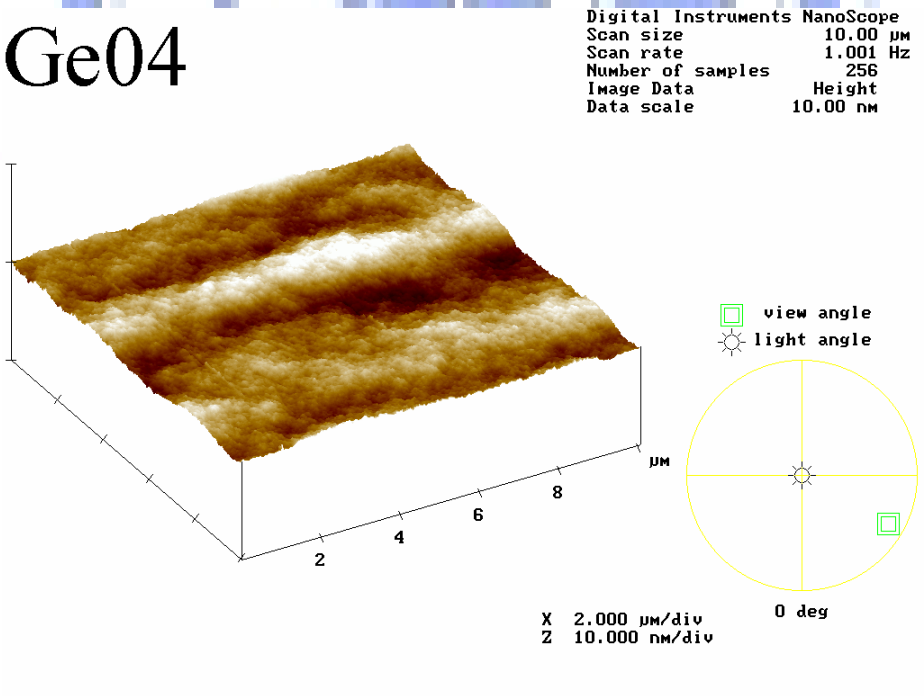


(d)

Fig. 3.2 AFM images of strained-relaxed SiGe buffer layers after CMP process. Different slurry and pad conditions for (a)Ge01, (b)Ge02, (c)Ge03 and (d)Ge04 samples.

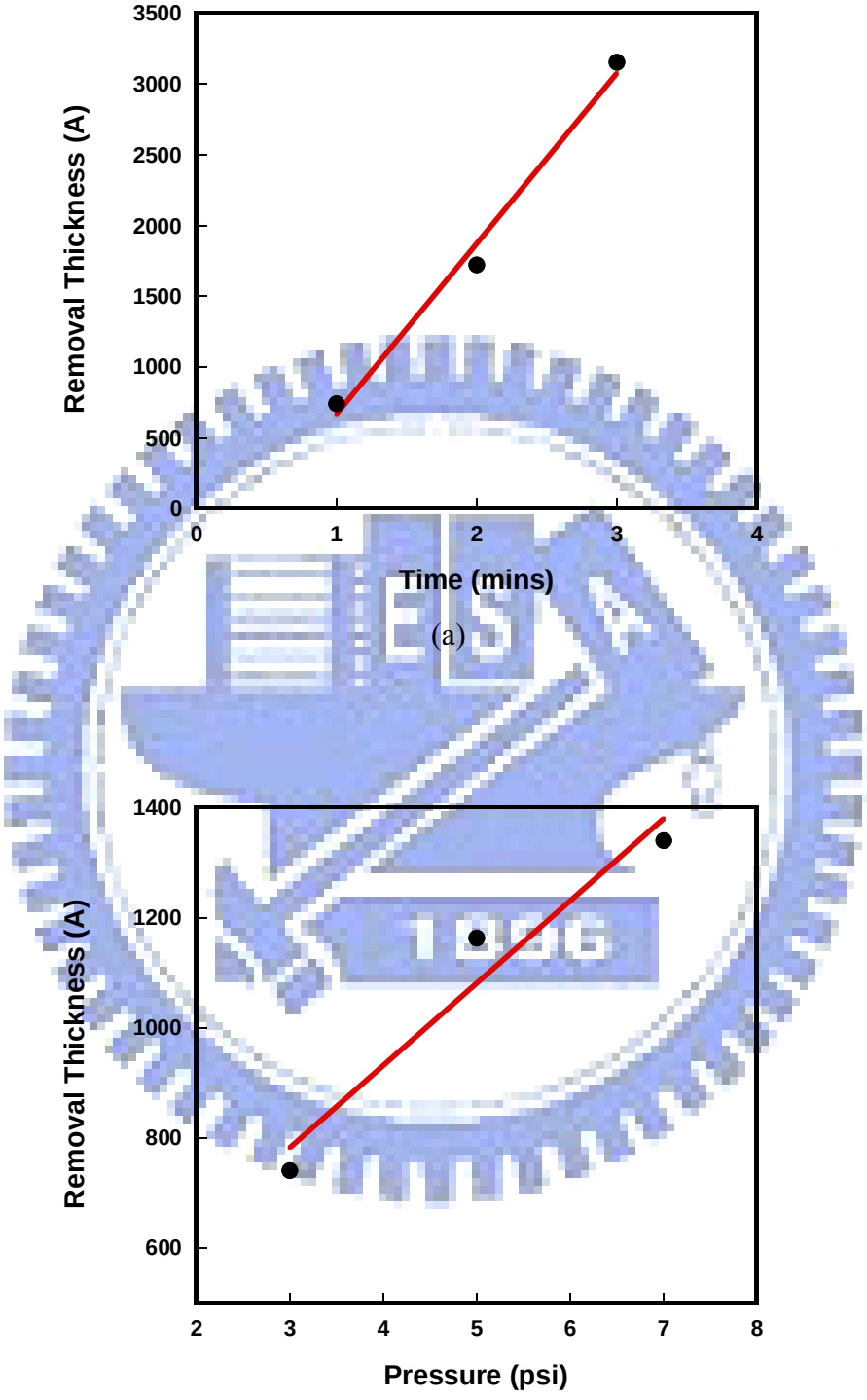
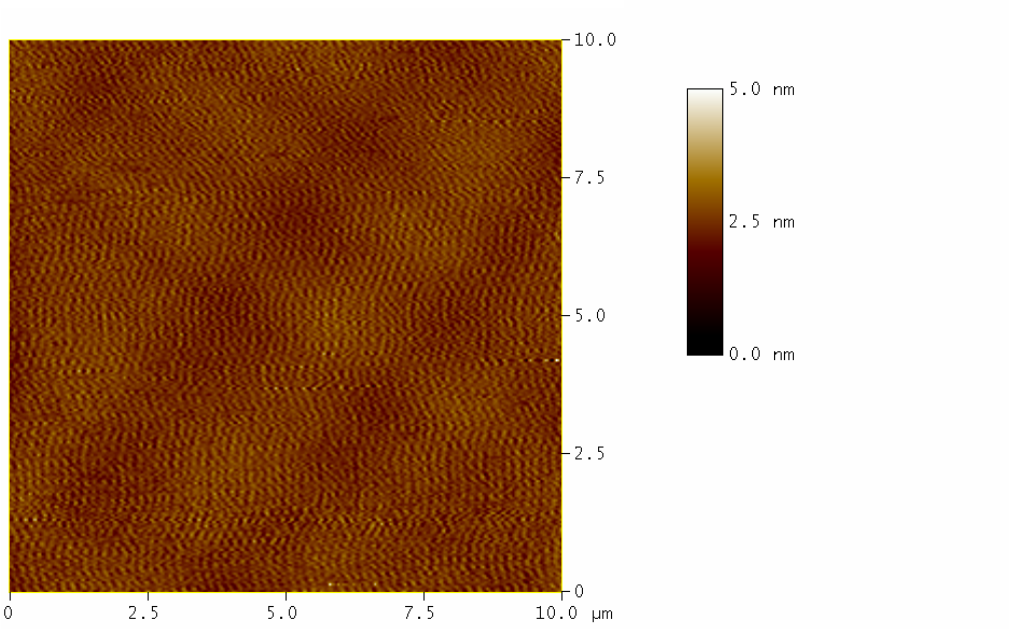
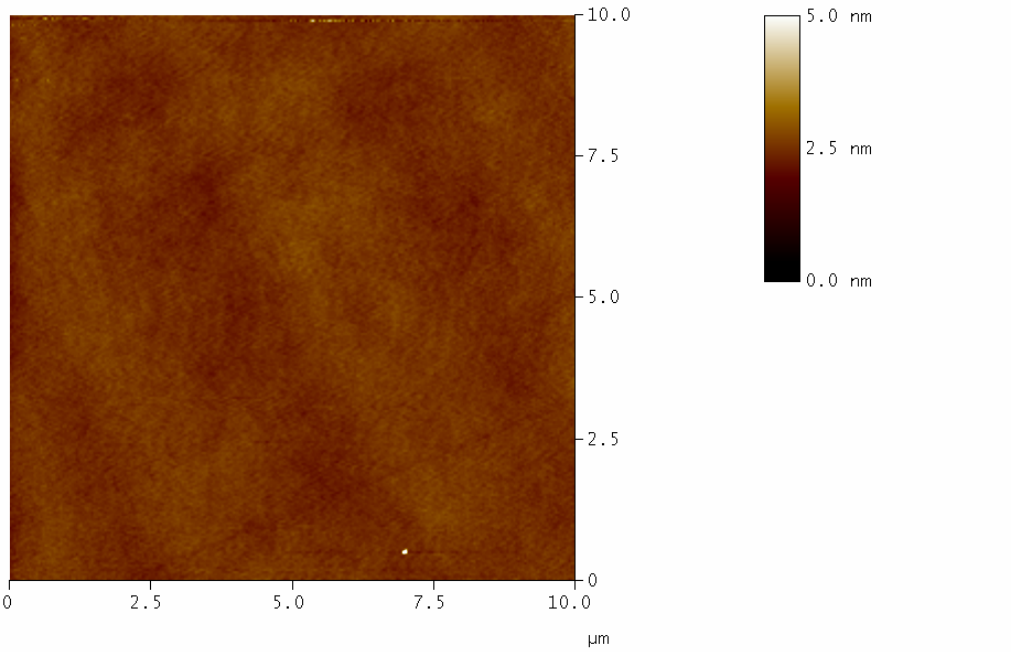


Fig. 3.3 Removal rate of (a) time dependent and (b) pressure dependent in SiGe layers.



(a)



(b)

Fig. 3.4 AFM images of strained-Si surfaces without and with CMP process. The RMS values are (a) without CMP 1.8 nm and (b) with CMP process 0.6 nm respectively.

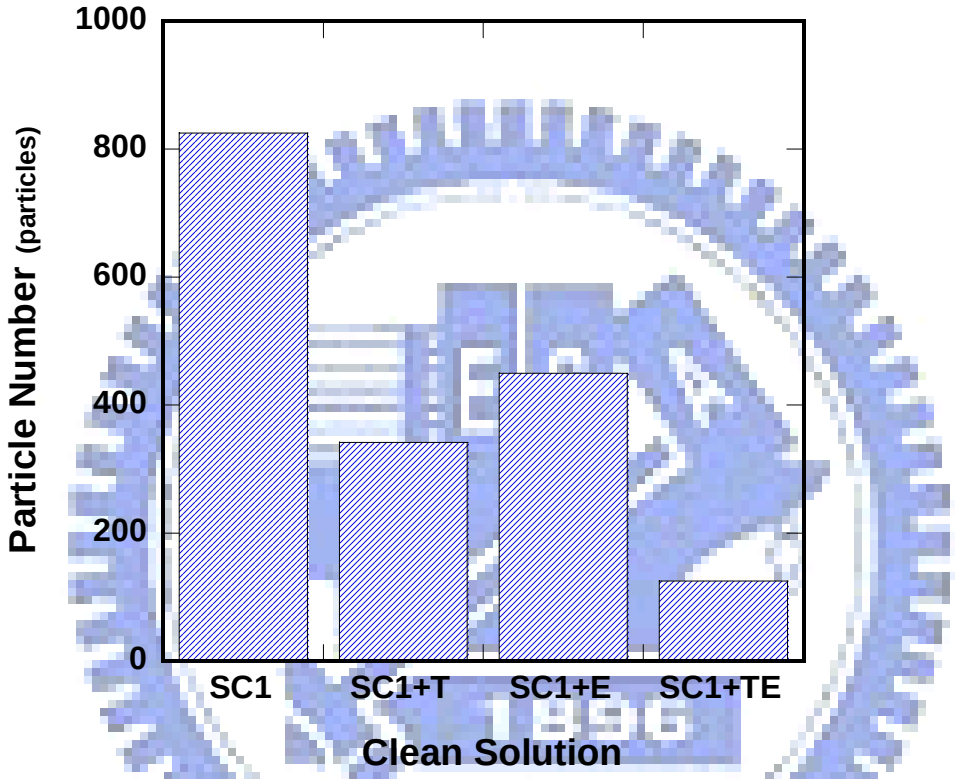


Fig. 3.5 Particle residual number on post-CMP cleaning surface of SiGe buffer layers in different solutions.

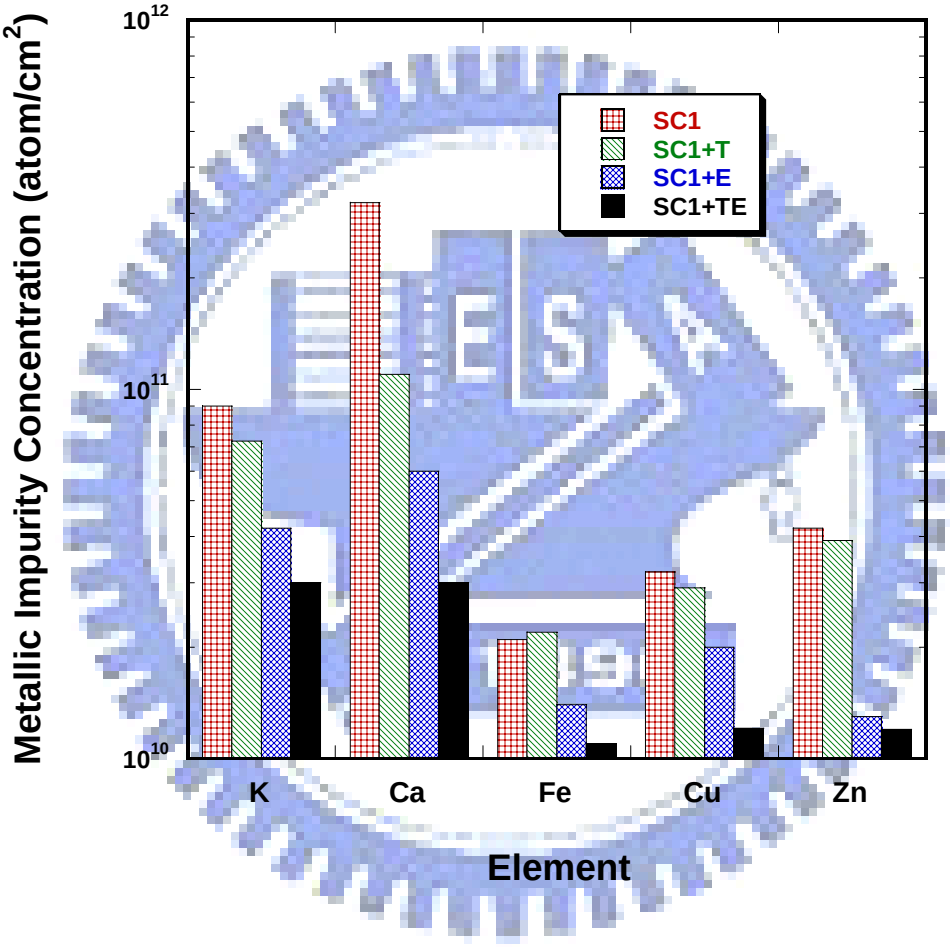


Fig. 3.6 The metallic contaminant concentration on SiGe buffer layer by TXRF.

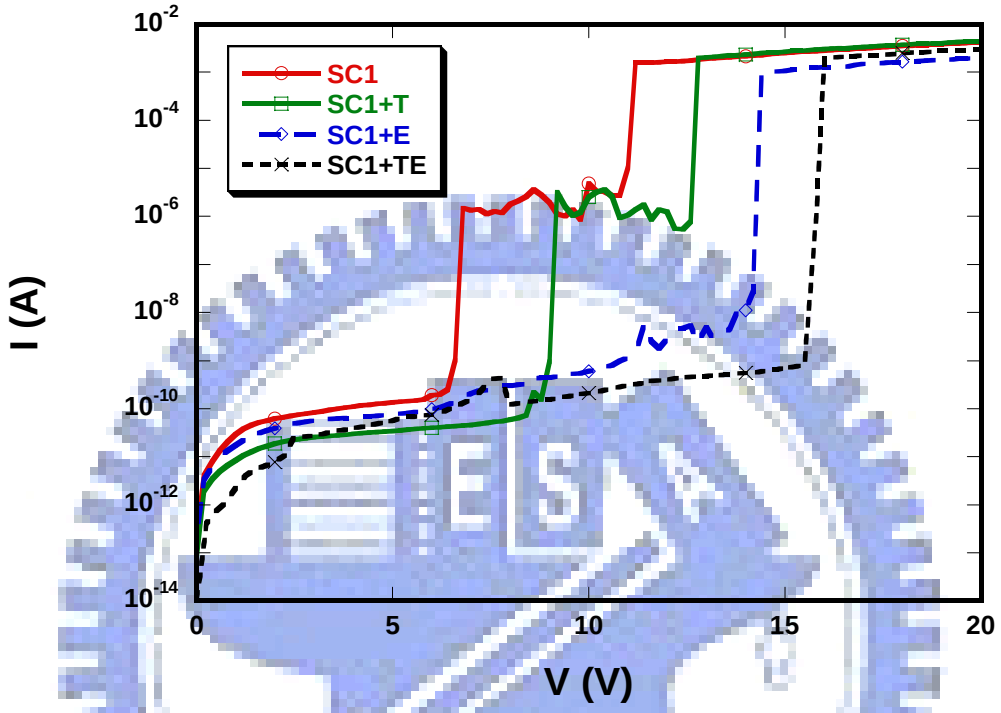


Fig. 3.7 The current *vs.* voltage characteristic of MOS capacitors with 20 nm TEOS oxide on the strained-Si with different cleaning method.

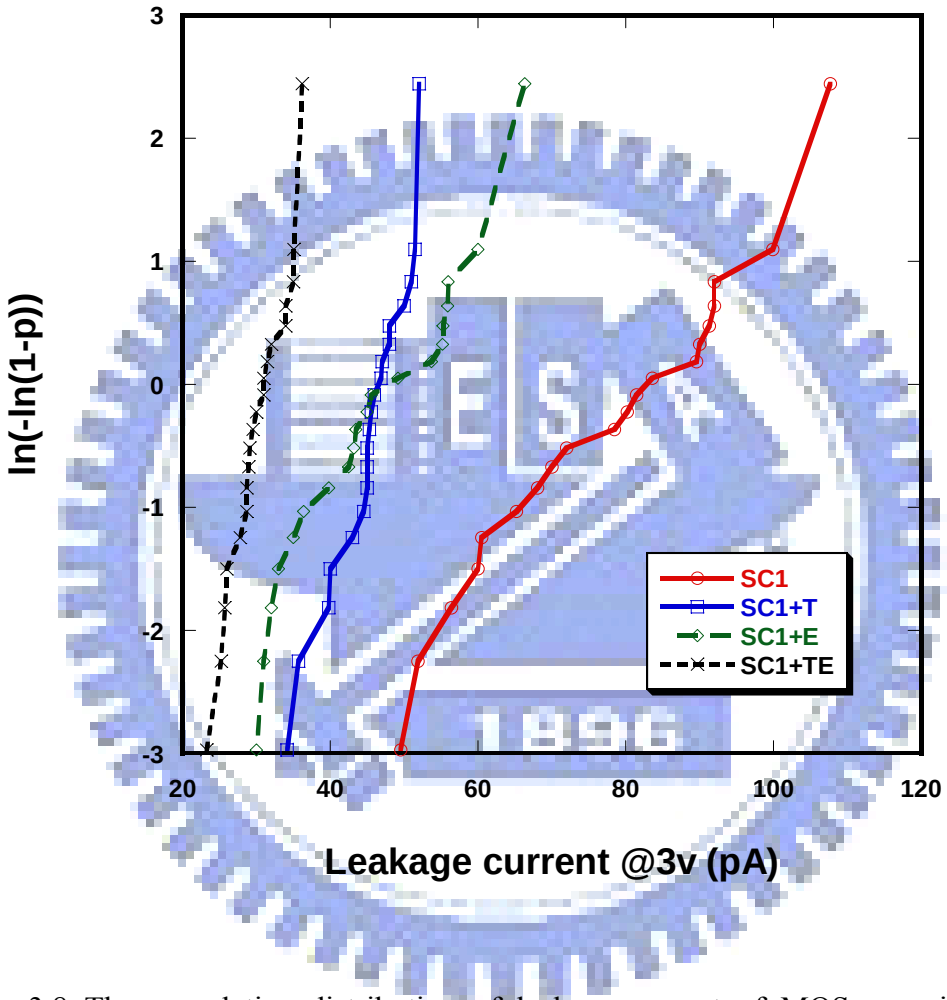


Fig. 3.8 The cumulative distribution of leakage current of MOS capacitors with different cleaning method.

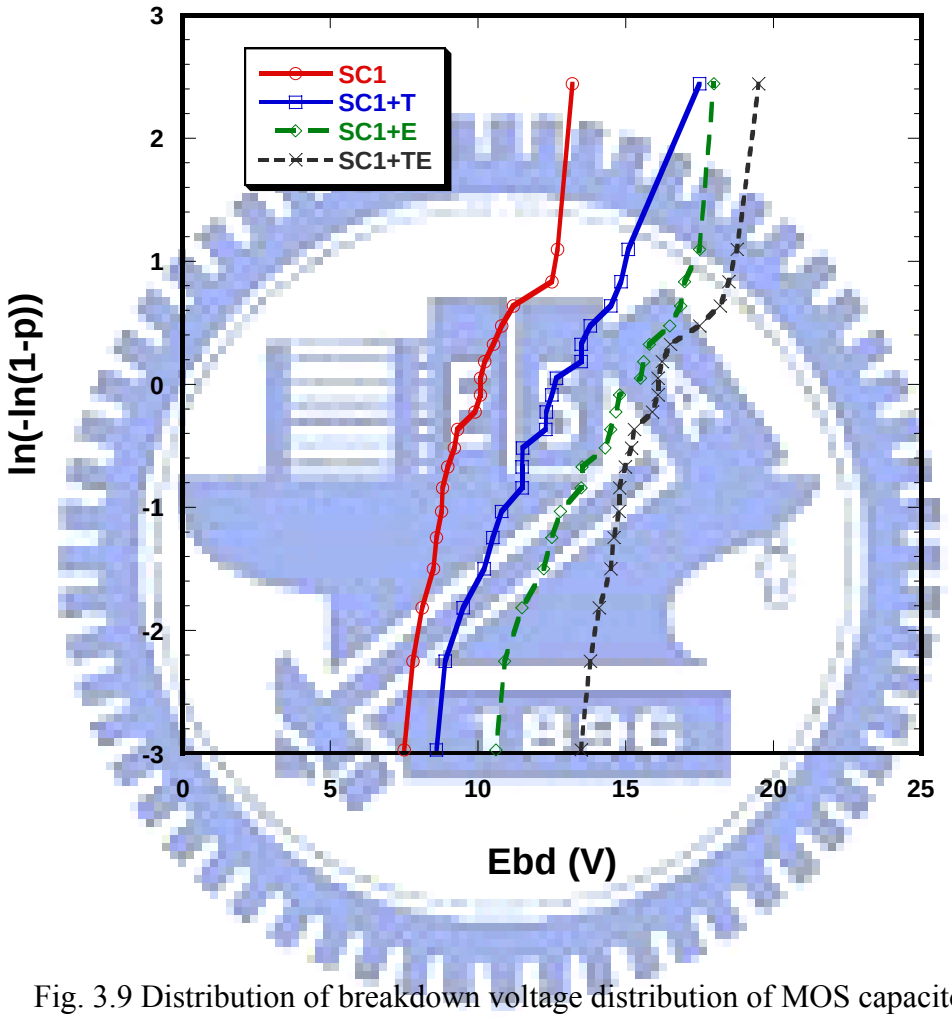


Fig. 3.9 Distribution of breakdown voltage distribution of MOS capacitors.

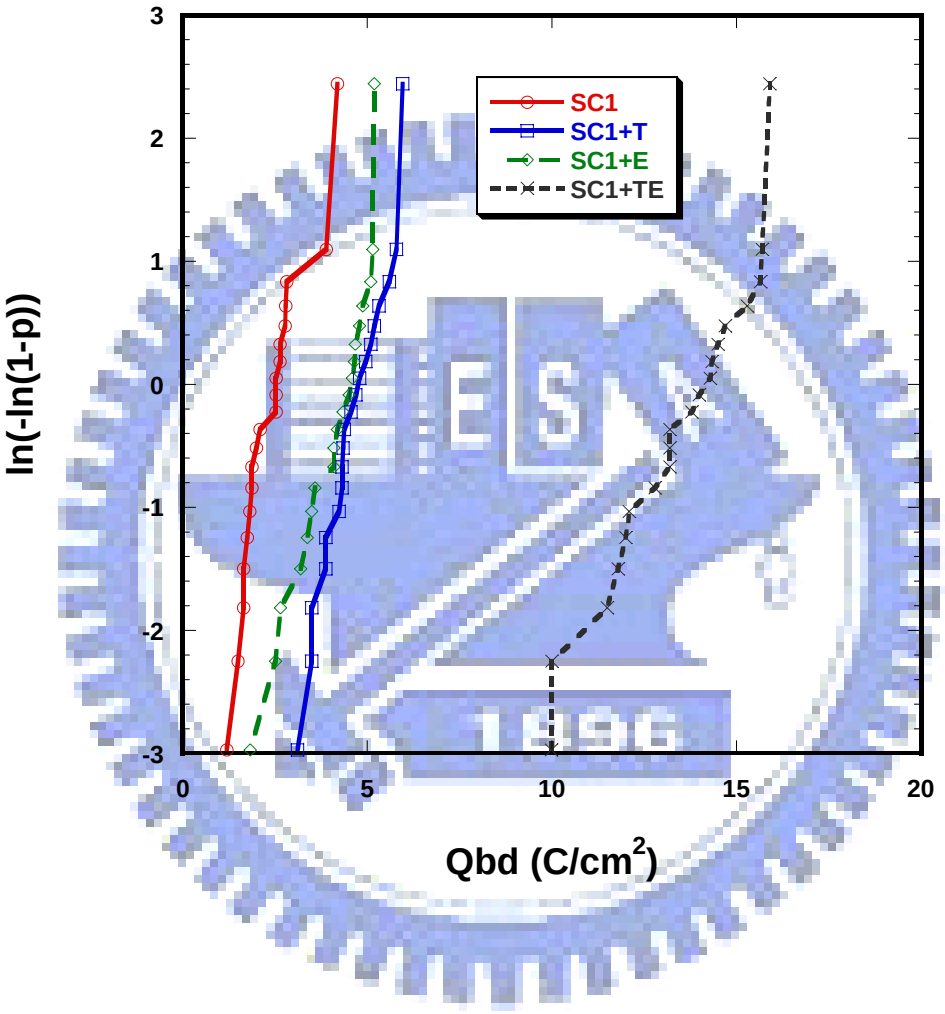


Fig. 3.10 The charge-to-breakdown of MOS capacitors under constant current stress in four kinds of different solutions.

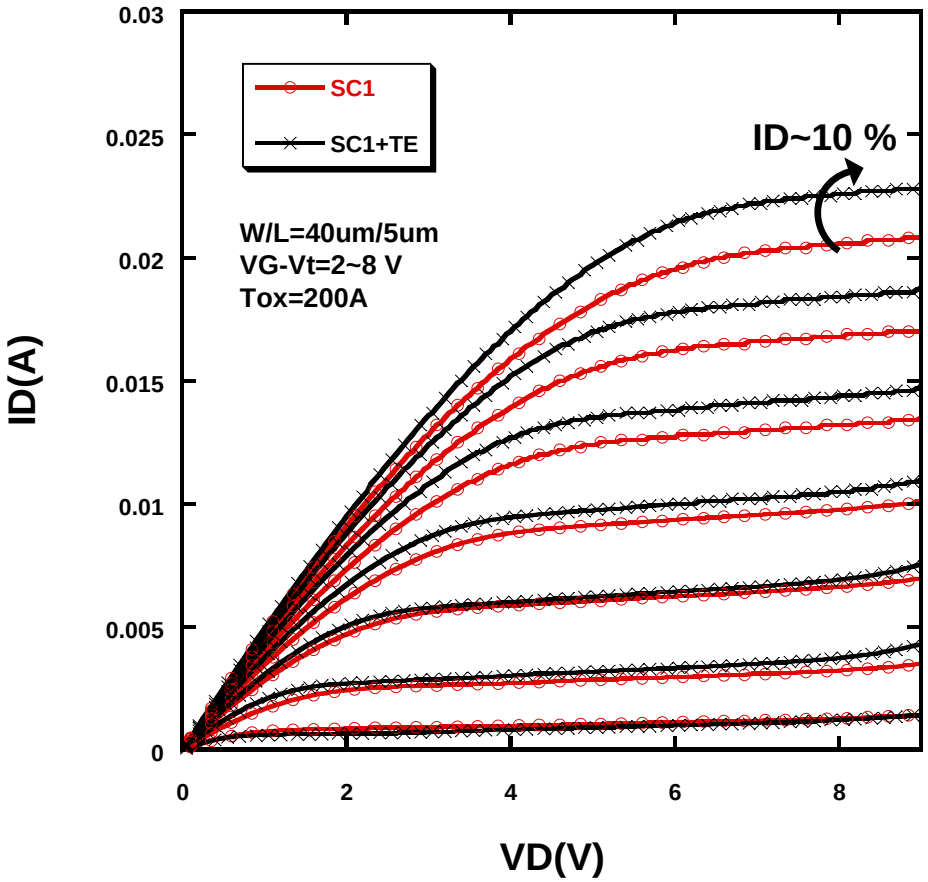


Fig. 3.11 The current enhancement of 10 % between SC1 and SC1+TE samples.

Chapter 4

A Novel Dynamic Threshold Voltage MOSFET (DTMOS) Using Heterostructure Channel of $Si_{1-y}C_y$ Interlayer

4.1 Introduction

As MOS devices continue to be scaled down, the low supply voltage is desirable to minimize the power consumption. The Dynamic Threshold MOSFET (DTMOS) structure offers a promising technology to achieve both high speed and low power performance [1], [2]. By shorting the gate to the body, the threshold voltage operating under the DT-mode is reduced by forward biasing of the body, so its current drive can be significantly enhanced in the on state. In addition, the subthreshold swing could be attaining to the ideal value (~60 mV/dec.). To enhance the driver current under DT-mode, large body factor, γ, is necessary to increase the threshold voltage reduction. The γ factor was strongly depended on the substrate impurity doping concentration. In order to take full advantage of the high current drive inherent in DTMOS, Chang *et al.* proposed the use of super-steep-retrograde (SSR) indium-channel profile [3], [4]. On the other hand, Takagi *et al*. also proposed a novel SiGe channel heterostructure DTMOS for reducing the threshold voltage in spite of keeping impurity doping level at the body region [5].

Transient enhanced diffusion (TED) of boron and phosphorus during annealing of implantation damage can be suppressed by incorporation of substitutional carbon [6]-[9]. $Si_{1-y}C_y$ layer have been applied to suppress boron diffusion in hetero-junction

bipolar transistors (HBT) [10], [11]. The incorporation of substitutional carbon in silicon can reduce fast diffusion spices of boron diffusion in silicon. An explanation for this behavior has been provided that the substitutional carbon present in the silicon substrate acts as the sink for silicon self-interstitial and the carbon spices are displaced by the silicon self-interstitial during thermal treatment processes. In this paper, a novel $Si_{1-y}C_y$ heterostructure n-channel DTMOS with boron implantation was studied. Compare to those two samples, with and without $Si_{1-y}C_y$ interlayer, it shows superiority over conventional DTMOS. We have successfully achieved the low threshold voltage and heavily doped substrate DTMOS with superior characteristics in terms of the higher transconductance and saturation current.

4.2 Experimental

Two samples, with and without (w/o) carbon incorporation, were prepared. Samples in this study were grown epitaxially on (100) silicon wafer in ultra high vacuum chemical vapor deposition (UHVCVD) system with a thin 5 nm $Si_{1-y}C_y$ (y=0.005) layer and 30 nm silicon cap layer. The substrates were implanted with 2×10^{13} cm^{-2} BF_2 at 75 keV and annealed at 950℃ for 30 s. The 6 nm gate oxide was grown, followed by the deposition of a 200 nm polysilicon gate. After gate patterning, a self-aligned n+ poly Si gate and source/drain ion implantation with P of 1E15 cm^{-2} was formed at 40 keV. The body contact junction was implanted and annealed by BF_2 in the rapid thermal process (RTP) system at the same substrate annealing conditions. Afterwards, a passivation layer was deposited and patterned to complete contact metallization. The gate and body contacts were provided separately. Electrical characteristics were performed using a HP4156 system.

4.3 Results and Discussion

The channel profiles were measured by the secondary ion mass spectroscopy (SIMS) for with and without $Si_{1-y}C_y$ layer shown in Fig. 4.1 This profiles were measured after all thermal cycles. Compare to control sample, the samples with the $Si_{1-y}C_y$ layer exhibit a super-steep-retrograde channel profile. In the presence of carbon, the boron concentration was dropped from $1.8\times10^{18}cm^{-3}$ to $\sim10^{17}cm^{-3}$ over a distance of 30 nm. By introducing carbon atom, the carbon significantly reduces TED of boron atom. The substitutional carbon provides a sink for excess interstitials in crystalline Si which suppressing interstitial-enhanced boron diffusion. The efficacy of incorporation carbon has been attributed to its ability to locally suppress the silicon self-interstitial concentration [6]-[9].

From SIMS analyses (shown previously in Fig. 4.1), the sample with $Si_{1-y}C_y$ layer has lower surface dopant concentration than the control sample while they have the same substrate doping concentration. It can therefore have a higher bulk impurity and does not increase the threshold voltage (V_{th}). Fig. 4.2 shows the body effects of n-channel MOSFET with and without $Si_{1-y}C_y$ interlayer samples. A separate terminal was used to control the body voltage. The threshold voltage at zero body bias is denoted for its initial threshold voltage. They have almost the same slope because of its similar substrate concentration. However, the surface concentration for the $Si_{1-y}C_y$ sample is lower than that of w/o $Si_{1-y}C_y$ interlayer samples. We found the $Si_{1-y}C_y$ sample indeed depicts a lower threshold voltage for lightly doped channel surface.

Fig. 4.3 shows the drain current versus gate voltage in subthreshold region which the device size is W/L=10 μm/5 μm. The drain voltage was 0.1 V. In the DT-mode operation, the gate and body contacts are tied to together (i.e., $V_G=V_{sub}$) and standard

mode operation (i.e., V_{sub}=0 V). The subthreshold swing for both samples show nearly ideal value (about 60 mV/dec.) which has been explained by Assaderaghi *et al.*[2]. Corresponding transconductance (G_m) is also shown in Fig. 4.3, it shows 1.2 times higher G_m between with and w/o $Si_{1-y}C_y$ samples. We believe this is due to the lower surface doping concentration and the larger body factor of $Si_{1-y}C_y$ sample. A low impurity surface channel and the heavily doped body enhances the body bias effect, and devices show the combination of low V_{th} and high body factor, simultaneously. In addition, in both operation modes, the G_m shows it superiority over the sample w/o $Si_{1-y}C_y$ interlayer. From Fig. 4.1 and 4.2, the channel surface impurity doping concentration determines the impurity scattering phenomenon. The output characteristics of with and w/o $Si_{1-y}C_y$ layer under standard and DT-mode operation varies from 0.2 V to 0.7 V with a 0.1 V step. The current drives of those two samples in the standard and DT-mode for the device size of W/L=10 μm/5 μm were shown in Fig. 4.4 (a) and (b), respectively. The drain current for the sample with $Si_{1-y}C_y$ layer is 1.8 times larger than that of Si DTMOS. In addition, the saturation current under DT-mode was larger than that under standard mode. It is worthy to note here that the disaster under DT-mode in V_G=0.7 V was due to the leakage current between the substrate and source terminals diode, which limit the operation voltage of DT-mode to V_G < 0.7 V.

4.4 Summary

We have developed a novel n-channel $Si_{1-y}C_y$ interlayer heterostructure DTMOS structure. This layer could effectively reduce the diffusion of boron beneath the channel region. A low surface channel impurity with heavily doped substrate can be achieved simultaneously. The excellent performances obtained in the $Si_{1-y}C_y$ interlayer

DTMOS are due to both the same substrate doping concentration and lower channel surface impurity concentration. So its surface impurity scattering could be reduces and it can offer a superior performance in future scaled devices. This device achieves 1.2 times higher G_m and 1.8 times larger drain current. It appears to be a very promising technology for nano-scale device and ultra-low voltage application.

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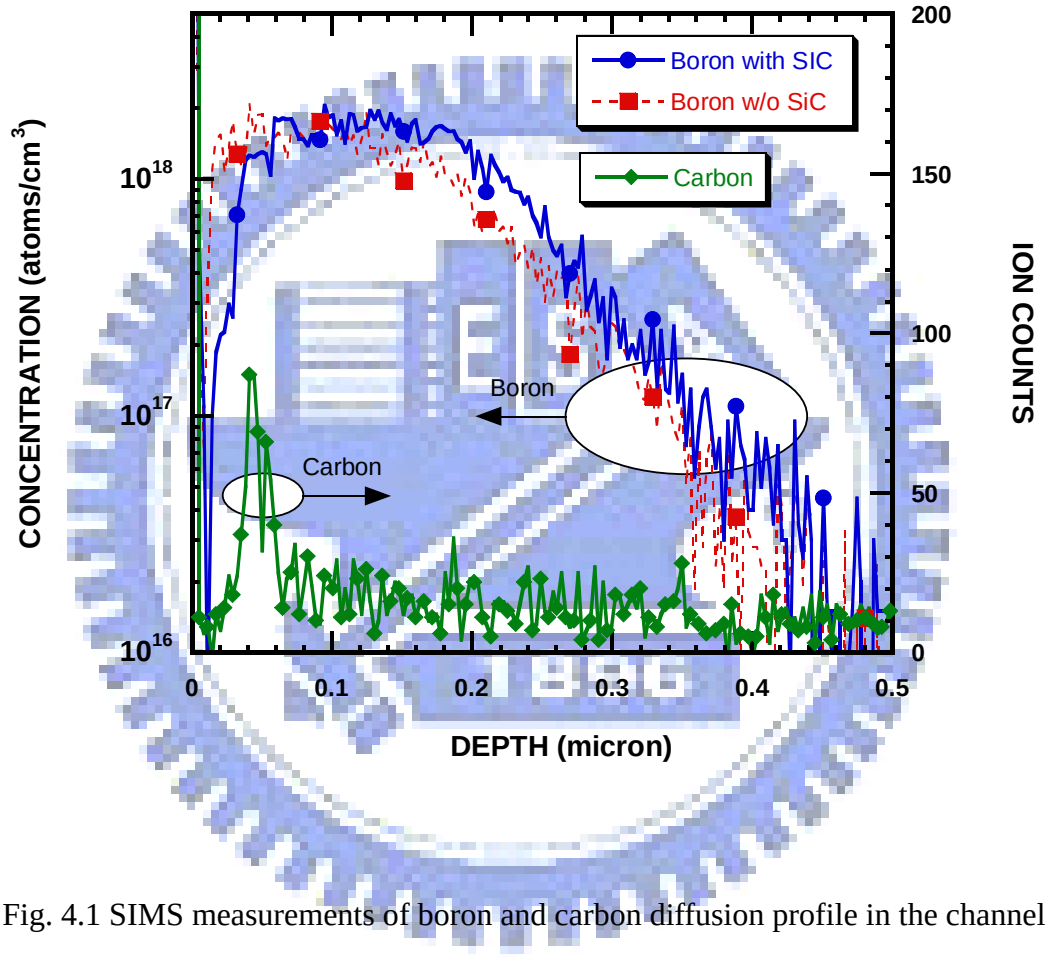

Fig. 4.1 SIMS measurements of boron and carbon diffusion profile in the channel region.

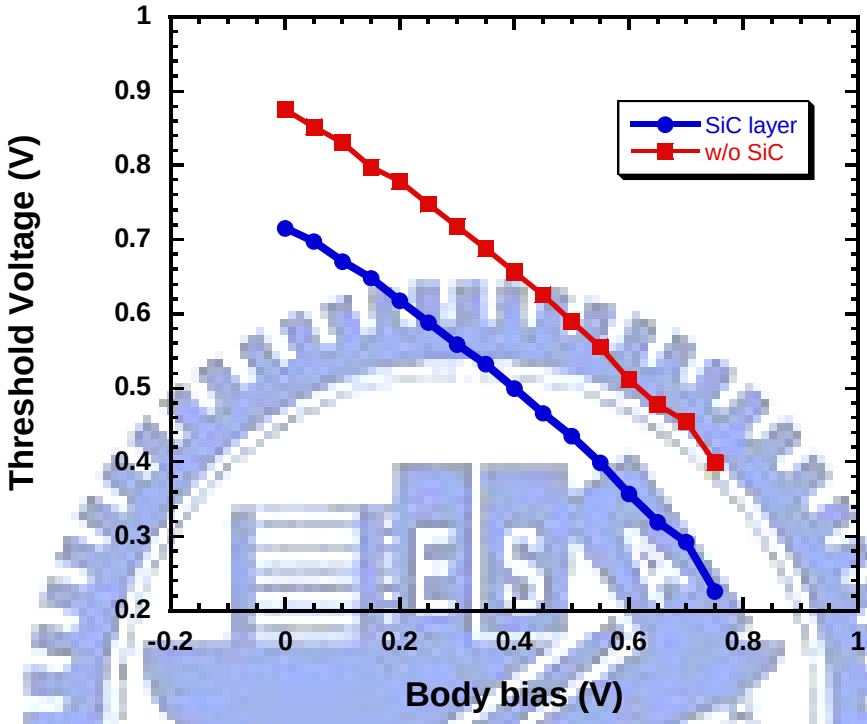

Fig. 4.2 Threshold voltage versus different body bias for a W/L=10 μm/5 μm NMOSFET.

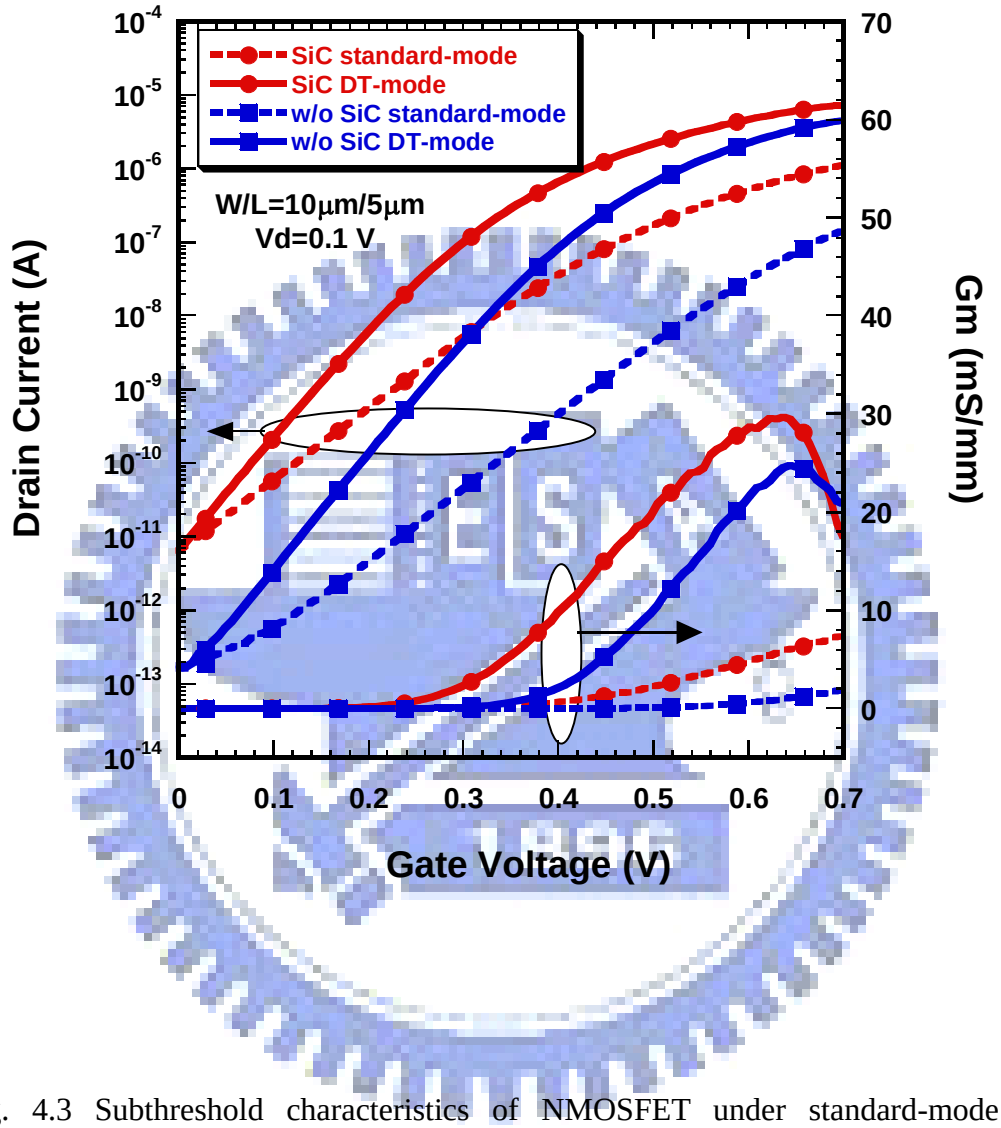

Fig. 4.3 Subthreshold characteristics of NMOSFET under standard-mode and DT-mode. Drain current and transconductance (G_m) for the samples with and without $Si_{1-y}C_y$ layer.

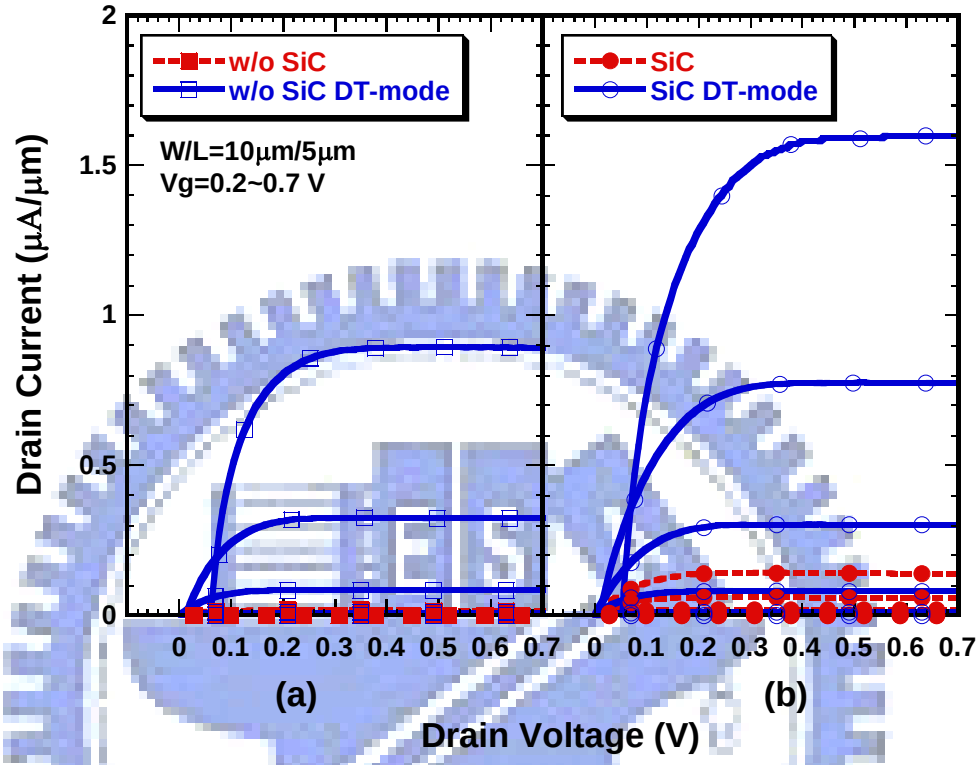

Fig. 4.4 Drain current of (a) without $Si_{1-y}C_y$, and (b) with $Si_{1-y}C_y$ devices in standard-mode and DT-mode. Gate voltage varies from 0.2 to 0.7 V in 0.1 V step.

Chapter 5

Electrical Characteristics and Reliability of Multi-channel Polycrystalline Silicon Thin-Film Transistors

5.1 Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much interest because of the possibility of integrating driving circuits and pixel elements. Poly-Si TFTs have many advantages compared with conventional amorphous-Si TFTs, including a higher driving current and greater carrier mobility. It is known that the existence of grain boundaries within the poly-Si channel region has great influence on the electrical characteristics of poly-Si TFTs [1], [2]. Some previous research reports have discussed the large number of grain boundary trap states in the poly-Si channels, and localized potential barriers are produced for the transportation of carriers from grain to grain [3]-[5]. Many suggestions have been proposed, and it have been revealed that poly-Si TFTs with narrow channels have better performance in terms of lower threshold voltage [6], smaller subthreshold swing [7], and effective kink effect suppression due to the reduction of grain boundary trap states. It has been concluded that the density of grain boundary trap states existing in the channel near the pattern edge is much lower than elsewhere. As the channel width is scaled down, the effect of the poly-Si pattern edge becomes dominant. Additionally, it has also been reported that the kink effect can be enhanced by the existence of grain boundary trap states [8], [9]. A larger number of grain boundary trap states causes a more severe impact ionization and results in a pronounced kink effect.

Moreover, the gate electrode across the channel may induce side-channels in both sides of the channel region, and these side-channels may increase the effective channel width. Especially when the channel width is scaled down, the side-channel effect is more distinct. The average carrier concentration in the channel region of the corner of the poly-Si gate electrode is increased by electrostatic focusing from the top gate and both side gates of the stripes [10]. It is believed that the gate control capability was obviously improved in narrow width devices. Accordingly, poly-Si TFTs with narrow and multiple channels have been proposed to enhance electrical characteristics [11]-[13]. However, no complete reliability analysis has been carried out in the poly-Si TFTs with narrow and multiple channels.

In this study, we demonstrate the fabrication process and the electrical characteristics of n-channel poly-Si TFTs with different channel stripes. Poly-Si TFTs with multiple channels have better performance than conventional TFTs. Finally, we fully discuss about the reliability of poly-Si TFTs with multiple channels.

5.2 Experimental

Figure 5.1 shows the process flow of the proposed poly-Si TFTs. First, 500-nm-thick thermal oxide was grown on the Si wafer using a furnace system. All experimentals devices in this study were fabricated on thermally oxidized Si wafers. Then, 100-nm-thick amorphous silicon layers were deposited on the thermal oxide layer using low-pressure chemical vapor deposition (LPCVD) at 550°C. Then, amorphous silicon films were recrystallized by solid phase crystallization (SPC) at 600°C for 24 h in an N_2 ambient to form poly-Si films. Poly-Si films were patterned into active regions by transformer coupled plasma (TCP) etching using a gas mixture of Cl_2 and HBr.

After RCA cleaning, a 100-nm-thick tetraethylorthosilicate (TEOS) oxide was deposited by LPCVD with TEOS and O_2 gases at 695°C to form the gate insulator. A 200-nm-thick poly-Si was deposited to serve as the gate electrode by LPCVD at 595°C. Then, the poly-Si film was patterned and etched by TCP etching to form the gate electrode, and the gate oxide on the source/drain was removed using dilute HF solution. The regions of source, drain, and gate were doped by self-aligned phosphorous ion implantation at a dosage and energy of 5×10^{15} cm^{-2} and 40 keV, respectively. Dopant activation was performed by rapid thermal annealing (RTA) at 700°C for 20 s, followed by the deposition of a 400-nm-thick passivation oxide using PECVD at 350°C and the definition of contact holes. Finally, a 500-nm-thick Al was deposited by sputtering and patterned for metal pads, and devices were passivated by NH_3 plasma treatment for 2 h at 300°C. Electrical characteristics were determined using a HP4156 system.

5.3 Results and Discussion

5.3.1 Device characteristics

A cross-sectional view of conventional and multi-channel poly-Si TFTs, which is parallel to the direction of the source and drain electrodes, is shown in Fig. 5.2. Figure 5.3 depicts the cross-section perpendicular to the direction of the source and drain electrodes. We discuss the transfer characteristics of the conventional and proposed TFTs with single, 8, 20, and 40 stripes having the same total channel width as shown in Fig. 5.4. We also discuss the reliability of conventional and proposed TFTs with different numbers of stripes in the channel. Figures 5.5 and 5.6 show the transfer characteristics (I_{DS}-V_{GS}) and field effect mobility for the conventional and proposed TFTs with different numbers of stripes in the channel. Table 5.1 summarizes

the measured and extracted parameters from the devices. The threshold voltage, subthreshold swing, on-state current (V_{GS}=20V), and off-state current (V_{GS}=-5V) were measured at V_{DS}=1V. As can be seen, the electrical characteristics of the poly-Si TFTs with multiple channels are significantly improved. The threshold voltage and subthreshold swing is degraded with the decreasing of stripes number in the channel. It has been reported that the grain boundary trap state density in the channel regions near the pattern edge is much lower than elsewhere in the poly-Si channel [6]-[7].

5.3.2 Extraction of trap state density

In order to verify if the trap state density is reduced, the effective trap state density (N_t) was calculated. Figure 5.7 shows the effective trap state density of poly-Si TFTs with various numbers of stripes in the channel. The effective trap state densities for S1, M8, M20, and M40 are 5.80×10^{12}, 5.71×10^{12}, 5.40×10^{12}, and 5.06×10^{12} cm^{-2}, respectively. The N_t is calculated from the transfer characteristics by Levinson's method and Proano's method [14], [15]. The plots of the ln $[I_D/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at low V_{DS} and high V_{GS}. The N_t was extracted from the slopes of these curves. Therefore, we deduce that the improved N_t, threshold voltage, and the subthreshold swing arose because of the improvement in the gate control capability in the TFT with various number of stripes, because better gate control capability causes a lower potential barrier located at the grain boundary.

Furthermore, as shown in Figures 5.5 and 5.6, the on-state current and field effect mobility are also improved as the number of stripes in the poly-Si channel increase. Generally, the increase in effective channel width due to additional sidewall results in the enhancement of on-state current. However, from Fig. 5.8, we can see that the increased ratios for the on-state current for M8, M20, and M40 are 7.45, 24.9, and 36.3%, respectively, and they are much larger than the increased ratio of the

effective channel width. Therefore, it can be concluded that the channel sidewall effect is not the dominant factor to improve the electrical characteristics of multiple channel poly-Si TFTs. The improvements of the on-state current and field effect mobility were contributed to the increasing average carrier concentration due to the enhancement of gate control [10], because the electrostatic focusing from the top gate and both side gates of the stripes caused the average carrier concentration in the channel region of the poly-Si gate electrode corner to increase.

Figure 5.9 shows the output characteristics of conventional and proposed poly-Si TFTs with different number of stripes in the channel when $V_G - V_{th}$=0.5, 2, and 3.5 V. It can be seen that the kink effect was suppressed with the increase in the stripes in the poly-Si channels. The better the gate control, the larger the depletion region existing in the channel, and therefore the fewer holes accumulated within the channel region. It can be concluded that the kink effect suppression is due to the improvement in gate control.

Figure 5.10 presents the on-state current, field effect mobility, and threshold voltage as a function of different gate lengths with numbers of channel stripes. The threshold voltage, field effect mobility, and on-state current were improved as the number of channel stripes increased. This result can be found for every channel length. However, it can also be seen that the field effect mobility decreased with the channel length. We attribute this phenomenon to the increase in series resistance.

5.3.3 Device Reliability

Finally, the reliability of conventional and proposed poly-Si TFTs with single, 2, 4, 10, and 20 stripes in the same total channel width is discussed. The hot-carrier stress test was performed at $V_{D,stress}$=15 V, $V_{G,stress}$=10 V, with the source electrode

grounded for 200 s to investigate the device reliability. Figure 5.11 shows the variations in the on-state current (I_{on}) and threshold voltage (V_{th}) as a function of hot carrier stress time. The variations in I_{on} and V_{th}, were defined as $(I_{on,stressed} - I_{on,initial})/I_{on,initial} \times 100\%$ and $(V_{th,stressed} - V_{th,initial})/V_{th,initial} \times 100\%$, respectively, where $I_{on,stressed}$, $V_{th,stressed}$, $I_{on,initial}$, and $V_{th,initial}$ represent the measured values before and after electrical stress. Generally, lower grain boundary trap state density causes slighter impact ionization under hot carrier stress, and hence the reliability of a device is improved. However, in Fig. 5.11, the degradation rate of the on-state current and threshold voltage deteriorated as the number of stripes in the poly-Si channel increased. Therefore, we discuss this phenomenon.

Figure 5.12 presents the trap state density in the poly-Si channel before and after 4 s, 10 s, and 100 s of hot carrier stress with conditions of V_{DS}=15 V, V_{GS}=10 V, and with the source electrode grounded. Figure 5.13 shows the increasing ratio of trap state density within the channel after 4 s, 10 s, and 100 s of electrical stress. It was clearly demonstrated that the trap state density after hot carrier stress increased as the number of poly-Si channel stripes increased. The electric field strength at the drain side of dual-gate poly-Si TFTs is larger than that of the single-gate poly-Si TFTs under the same bias conditions (V_{DS}=15 V, V_{GS}=10 V). This phenomenon will be more significant in the tri-gate poly-Si TFTs. Besides electric field strength near the drain, corner effect and sidewall roughness will also enhance the device's degradation rate. Therefore, the electric field at the drain side was enlarged as the numbers of stripes in the poly-Si channel increased under hot carrier stress to cause severe impact ionization and hence to generate more trap states.

5.4 Summary

The effects of the number of channel stripes in multi-channel TFTs performance and reliability have been investigated. As the number of stripes increased, the electrical characteristics of devices were improved significantly due to the enhancement of gate control. However, a severe reliability was found which can be attributed to the enlargement of the electric field at drain side. Therefore, for the fabrication of highly reliable devices and to improve the yield of multi-channel TFTs, the channel structures must be carefully designed.

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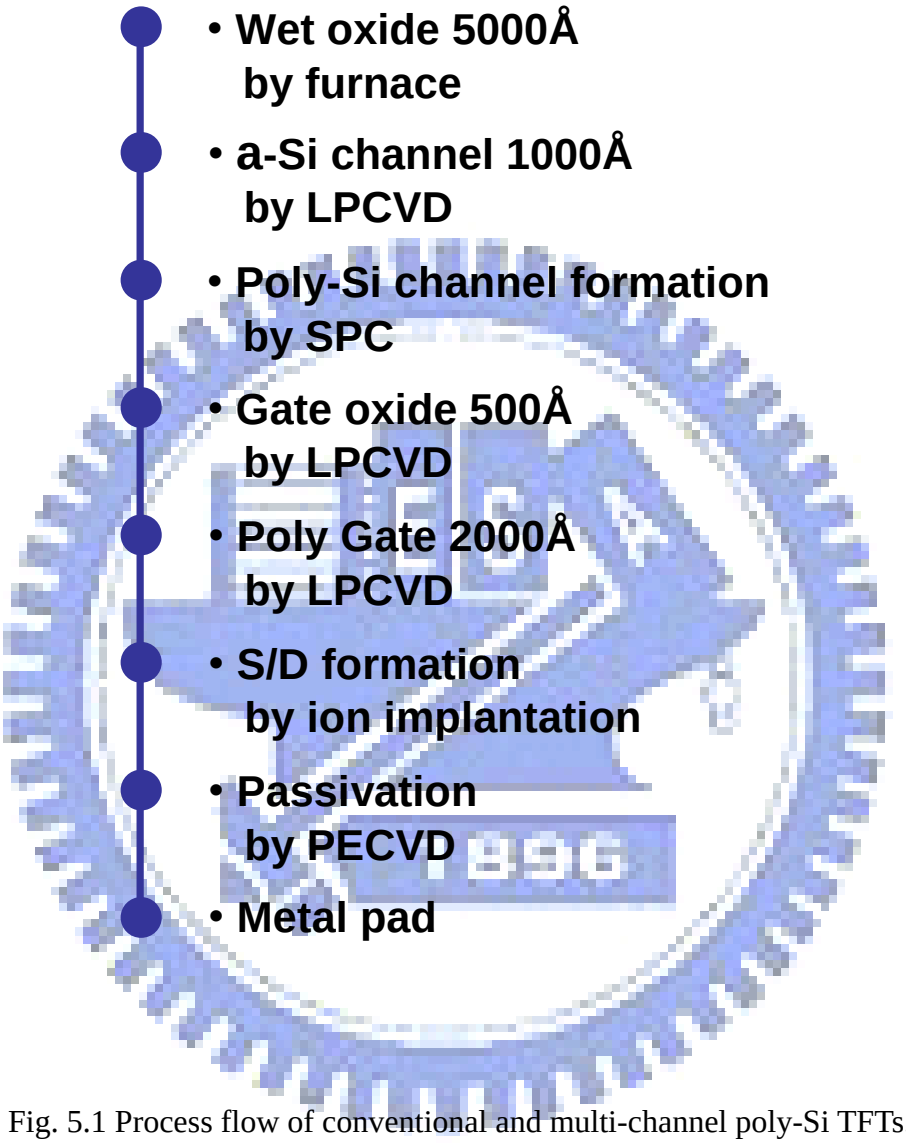


Fig. 5.1 Process flow of conventional and multi-channel poly-Si TFTs.

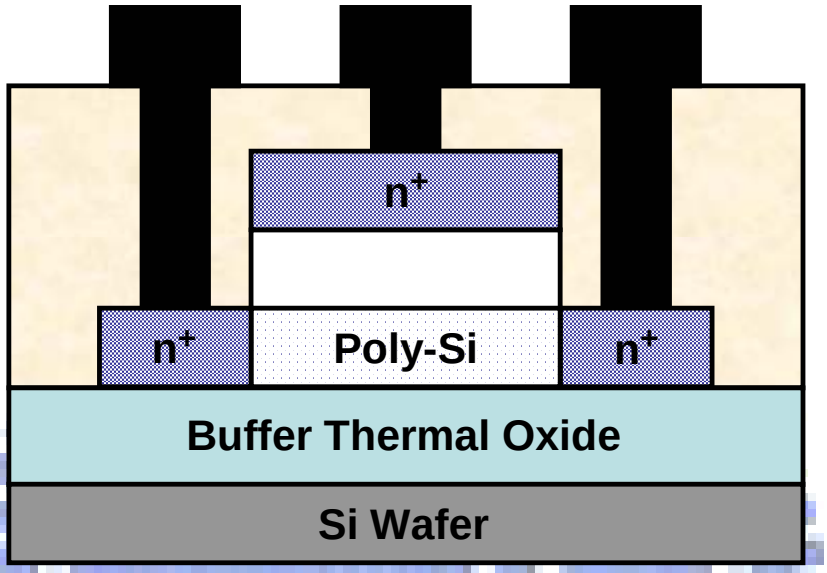


Fig. 5.2 The cross-section of conventional and multi-channel poly-Si TFTs is parallel to the direction of the source and drain electrodes.

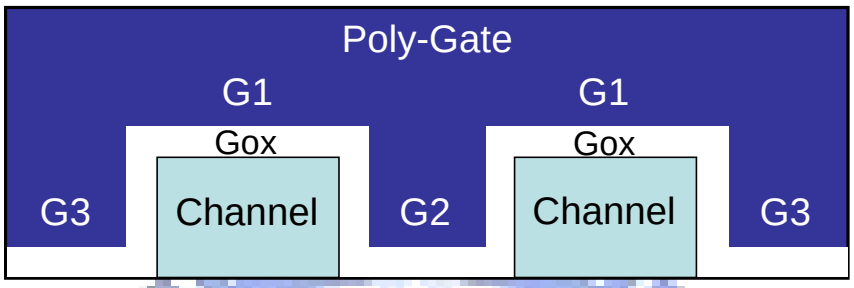


Fig. 5.3 The cross-section of conventional and multi-channel poly-Si TFTs is perpendicular to the direction of the source and drain electrode.

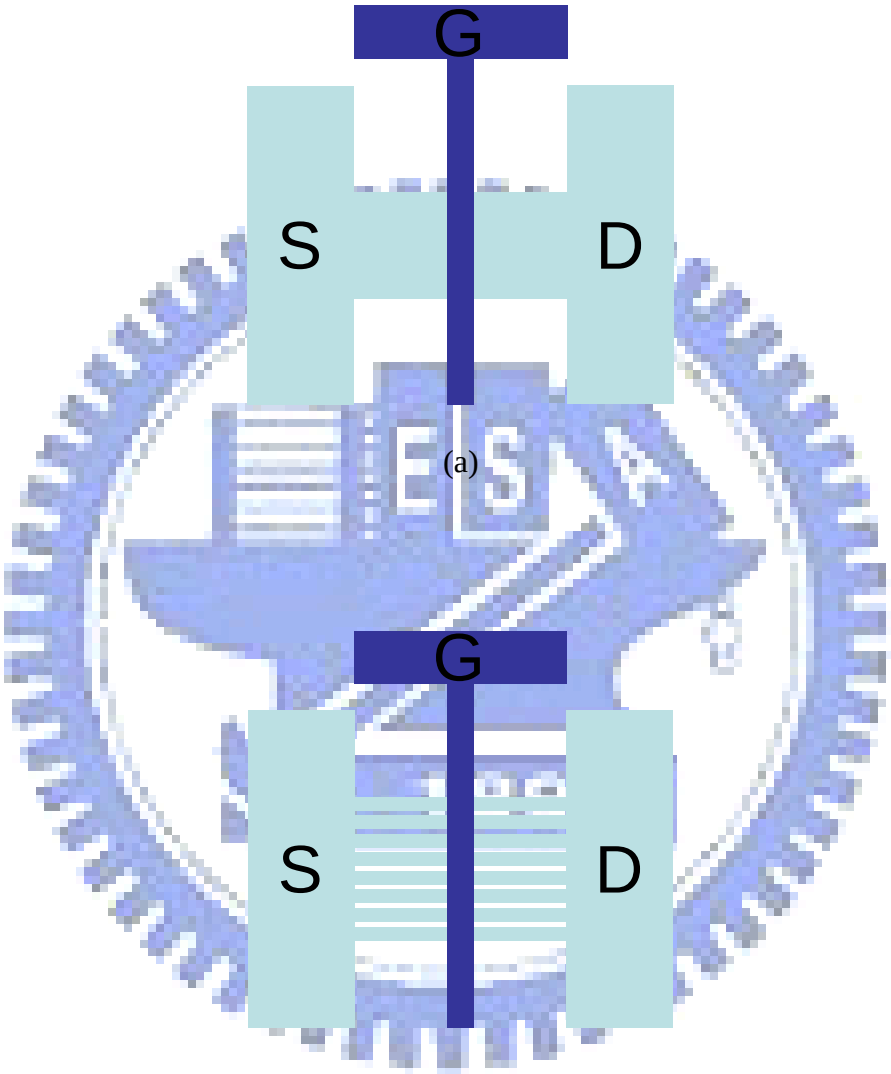


Fig. 5.4 Top view of (a) the conventional and (b) multi-channel poly-Si TFTs. The effective channel width W_{eff} = 40 μm ; channel length L = 2 μm.

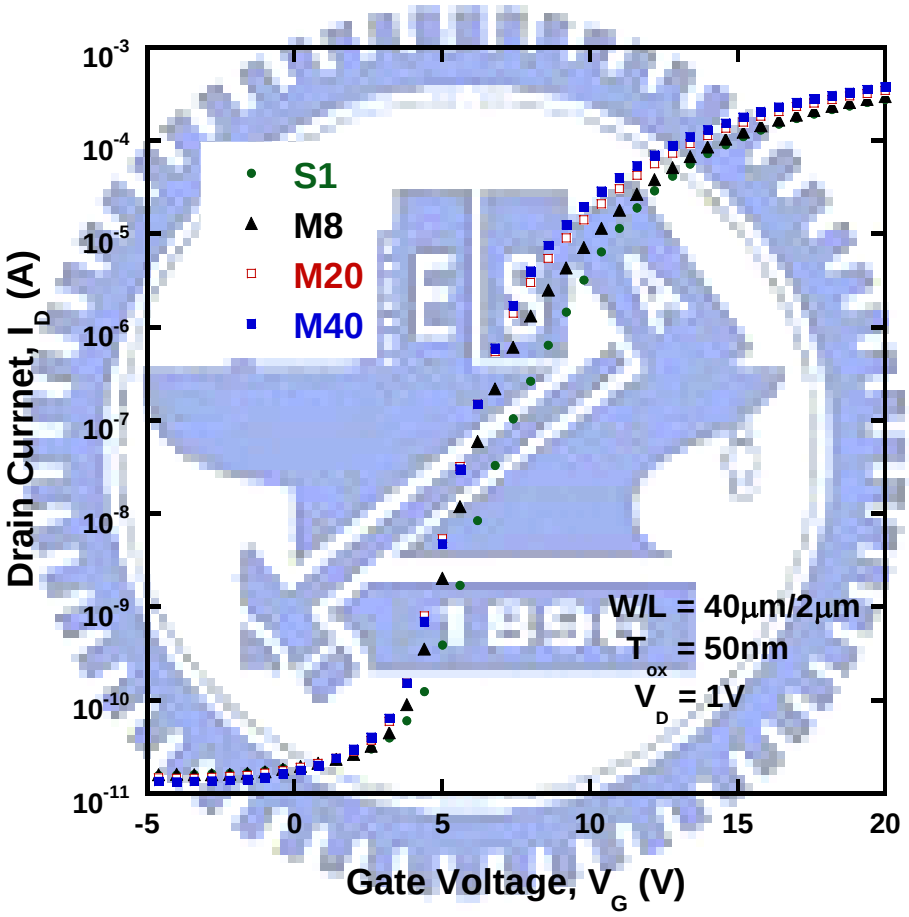


Fig. 5.5 Transfer characteristics of the conventional and the proposed multi-channel poly-Si TFTs with different stripes of channel.

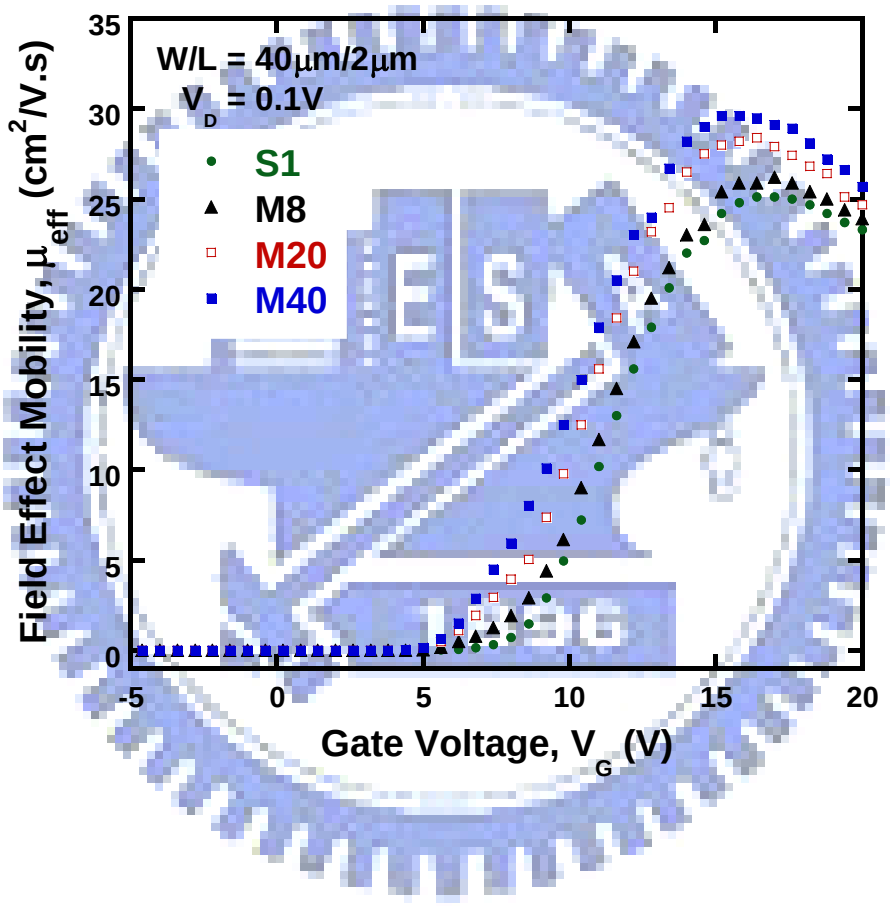


Fig. 5.6 Field effect mobility of conventional and proposed multi-channel poly-Si TFTs with different number of stripes in the channel.

Table 5.1 Summary of device parameters of conventional and proposed multi-channel poly-Si TFTs (W/L = 40 μm/2 μm) with different numbers of stripes in the channel.

	S1	M8	M20	M40
V_{th} (V)	9.65	9.33	8.97	8.67
S. S. (V/dec.)	1.257	1.230	0.987	0.923
μ_{eff} ($cm^2V^{-1}s^{-1}$)	25.3	26.1	28.5	29.6
I_{on} at VG=20V (A)	2.76×10^{-4}	2.96×10^{-4}	3.44×10^{-4}	3.76×10^{-4}
I_{off} at VG=-5V (A)	1.56×10^{-11}	1.56×10^{-11}	1.51×10^{-11}	1.43×10^{-11}
ON/OFF Ratio	1.79×10^{7}	1.91×10^{7}	2.37×10^{7}	2.89×10^{7}
N_t (cm^{-2})	5.80×10^{12}	5.71×10^{12}	5.40×10^{12}	5.06×10^{12}

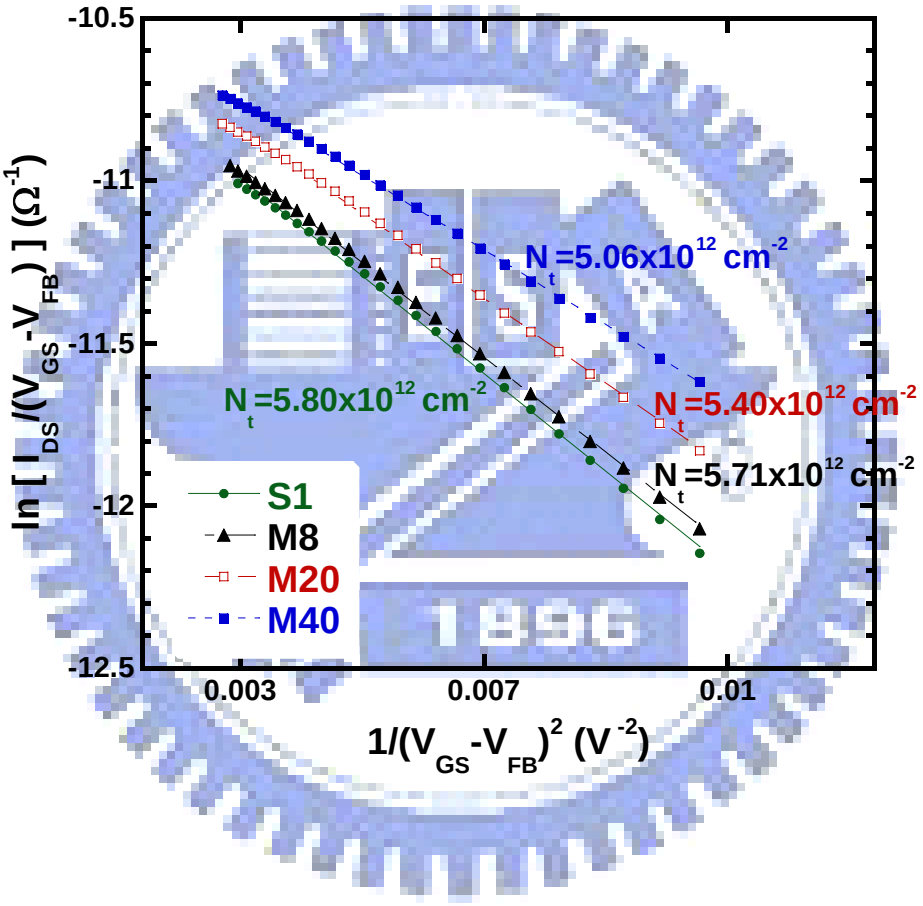


Fig. 5.7 Trap state density of conventional and proposed multi-channel poly-Si TFTs with different number of stripes in the channel.

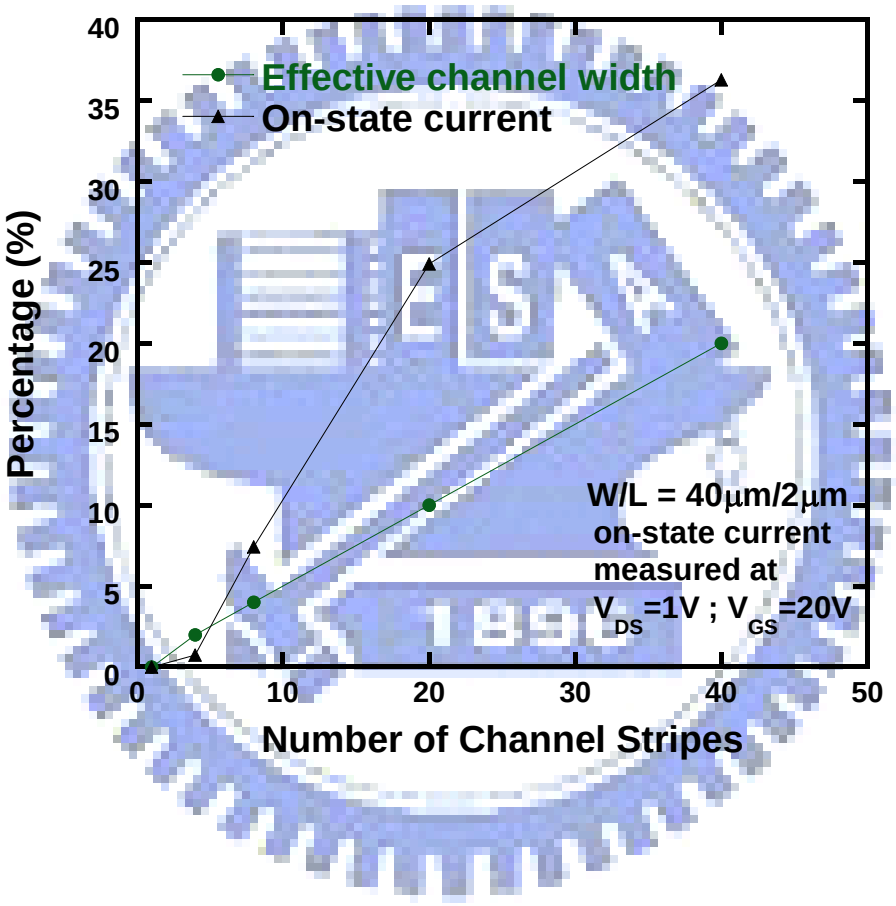


Fig. 5.8 Increasing ratio of the effective channel width and the on-state current as a function of number of channel stripes.

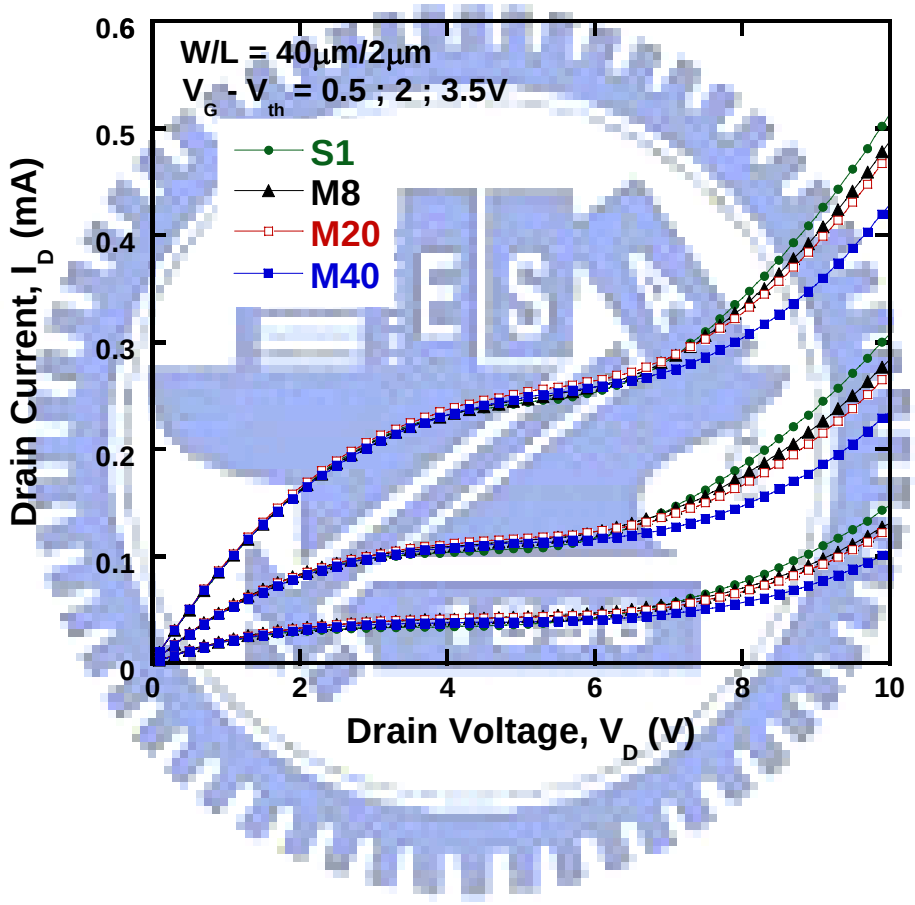
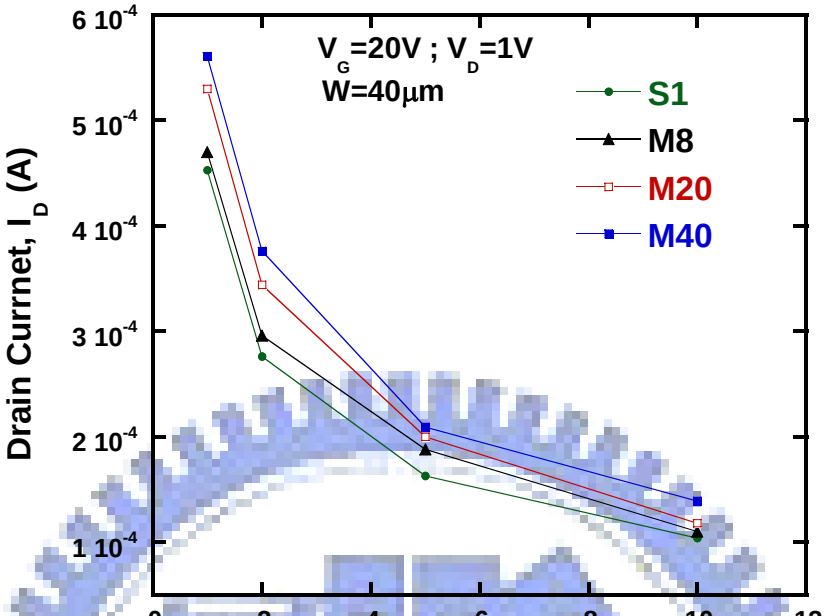
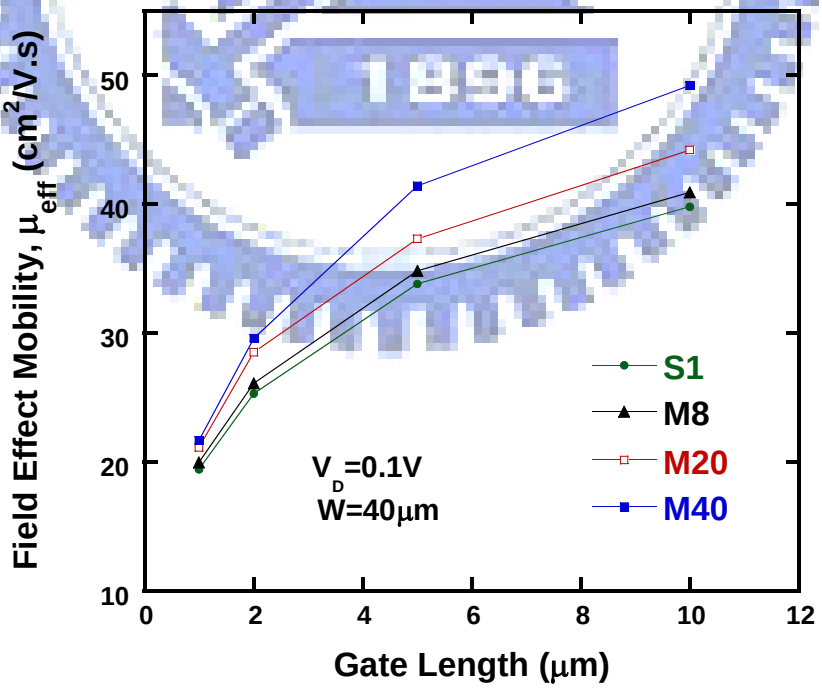


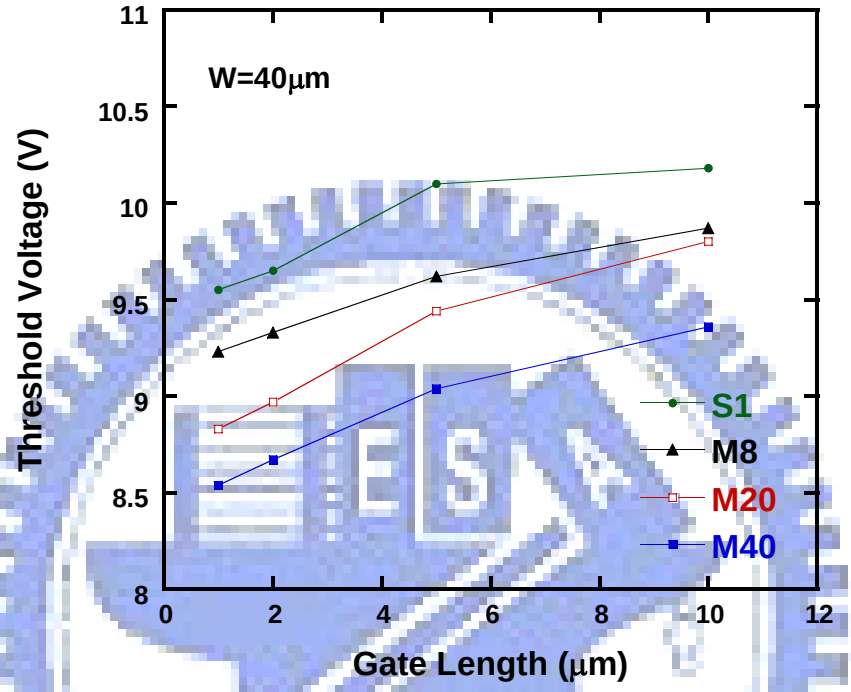
Fig. 5.9 Output characteristics of conventional and proposed poly-Si TFTs with different numbers of stripes in the channel. ($V_G - V_{th}$ = 0.5; 2; 3.5V).


V_G=20V ; V_D=1V
W=40μm
S1
M8
M20
M40
Drain Currnet, I_D (A)
6 10^-4
5 10^-4
4 10^-4
3 10^-4
2 10^-4
1 10^-4
0
2
4
6
8
10
12
Gate Length (μm)

(a)


Field Effect Mobility, μ_eff (cm²/V.s)
50
40
30
20
10
V_D=0.1V
W=40μm
S1
M8
M20
M40
0
2
4
6
8
10
12
Gate Length (μm)

(b)



(c)

Fig. 5.10 (a) On-state current, (b) field effect mobility, and (c) threshold voltage as a function of different gate lengths with the number of channel stripes.

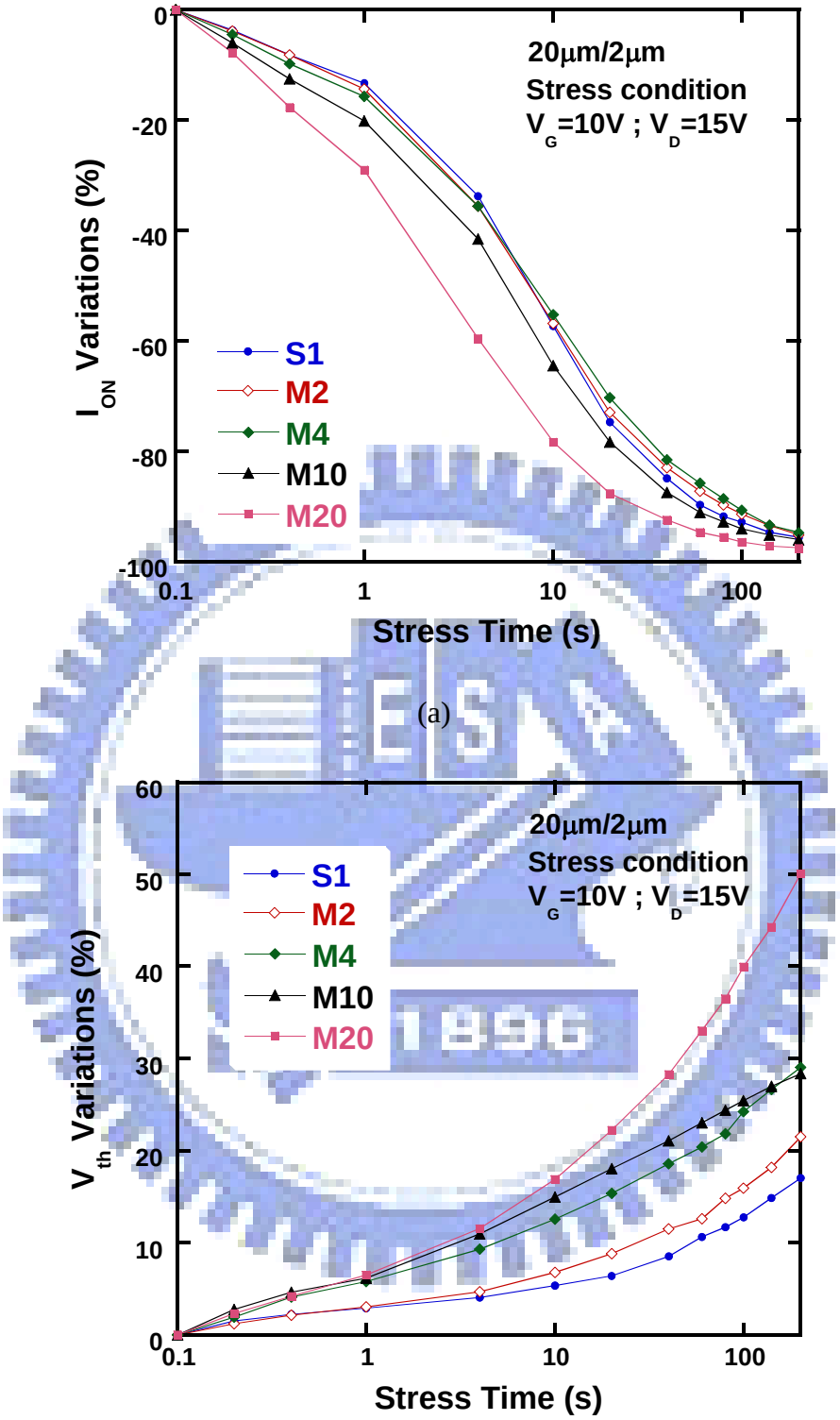


Fig. 5.11 (a) On-current, and (b) threshold voltage degradation as a function of time under hot-carrier stress.

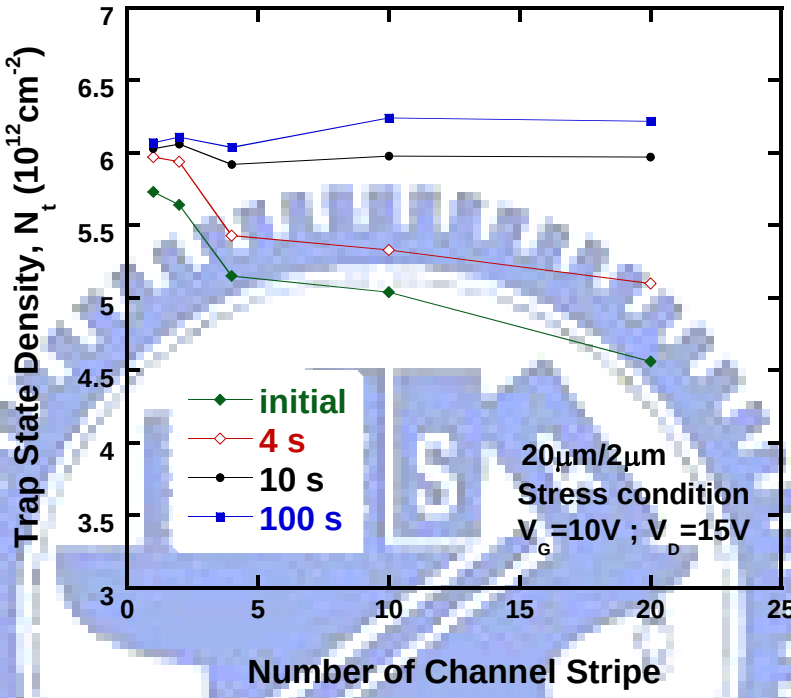


Fig. 5.12 Trap state density (N_t), before and after 4 s, 10 s, and 100 s stress with different numbers of channel stripes.

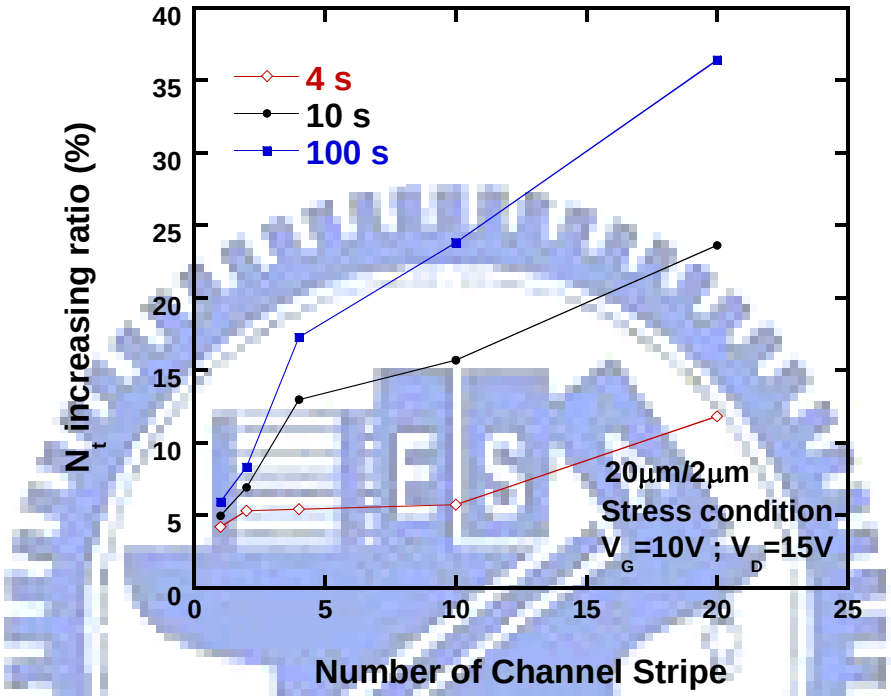


Fig. 5.13 Increasing ratio of trap state density after 4 s, 10 s, and 100 s stress with different numbers of channel stripes.

Chapter 6

Effect of Chemical Mechanical Polish Process on Low-Temperature Poly-SiGe Thin-Film Transistors

6.1 Introduction

Thin-film transistors (TFTs) have been widely used in various applications, such as static random access memories (SRAMs) [1], electrical erasable programming read only memories (EEPROMs) [2], linear image sensors [3], thermal printer heads [4], photodetector amplifier [5], scanner [6], and integrated driver transistors for active matrix liquid crystal displays (AMLCDs) [7]-[9].

Silicon germanium (SiGe) is a promising candidate for use as the TFT channel film, as it requires lower processing temperature than Si. Since the melting point of SiGe is lower than that of Si, the lower process temperature can be used for TFTs fabrication [10]-[13]. For low-temperature solid phase crystallization (LT-SPC) applications, SiGe is particularly advantageous, as it requires substantially shorter annealing cycles than required for the crystallization of Si. SiGe TFTs fabricated using scanned rapid thermal annealing (RTA) have also been demonstrated [14]. SiGe is advantageous for scanned RTA processes, as it requires lower crystallization temperatures, reducing glass warpage. To date, using conventional SPC processing with no pre-amorphization implant, SiGe TFT performance has generally been worse than poly-Si TFT performance [13]. SiGe TFT performance has been improved substantially through the use of thin Si interlayer to improve the gate oxide interface [15]. However, little has been done to improve the intrinsic quality of the SiGe

channel film itself; the binary nature of the SiGe system complicates optimization and modeling substantially. In previously described preliminary optimization of SiGe TFT's through the use of multifactorial design of experiment techniques [16], [17].

However, the rough surface of channel causes the poor performance and the low reliability of the device. It is shown that a planarized polysilicon surface will yield TFTs with improved performance and reliability. The CMP process has been used extensively for smoothing surface of polysilicon films [18]-[23]. Thus it is possible to be applied to smooth the poly-SiGe films. In this study, we develop optimization strategies for fabrication of high-performance SiGe TFTs.

6.2 Experimental

The main process sequence for fabricating the poly-SiGe TFTs is illustrated in Fig. 6.1 The starting materials were 6-inch dummy wafers capped with a 500-nm-thick thermal oxide. Un-doped 100-nm- thick amorphous silicon germanium ($Si_{1-x}Ge_x$,x =0.18) films were deposited by low-pressure chemical vapor deposition (LPCVD). Then the a-SiGe films were transformed into polysilicon phase by a solid-phase re-crystallization (SPC) treatment at 550 ℃ for 12hr. The films were then polished by CMP process. The parameters of CMP process condition were shown in Table 6.1. After definition of the active channel regions, a 50-nm-thick CVD oxide layer was deposited to form the gate oxide. Subsequently, the SiGe films were deposited and patterned to form the gate electrode. For n-channel transistors, P+ implant with a dosage of 5×10^{15} cm^{-2} at 25 KeV was performed. The implanted dopants were activated in N_2 ambient at 550 ℃. Next, a 300-nm-thick passivation oxide was deposited, followed by contact hole and aluminum pad formation. The samples were then subjected to the NH_3 plasma treatment in various time periods.

Electrical characteristics were performed using a HP4156 system.

6.3 Results and Discussion

6.3.1 Device Characteristics

The surface roughness of the poly-SiGe films were examined by atomic force microscope (AFM). Fig. 6.2 shows the surface image of this film before and after CMP. It can be seen that CMP is very effective in smoothing the surface. The roughness of SiGe films are 4.75nm, 1.2nm and 0.35nm for unpolished and polished in 10 and 20 seconds, respectively.

Fig. 6.3 illustrates the I-V characteristics of unpolished TFTs with various NH_3 plasma treatment times. The treatment results in superior electrical characteristics because of the grain boundaries passivation. The transfer curves of samples with and without CMP process are shown in Fig. 6.4. The observable improvements were not only due to the mobility enhancement, but also due to the significantly reduced leakage current with the reduction of surface roughness. The characteristics of with and without CMP process are shown in Table 6.2. The TFTs fabricated on polished poly-SiGe film exhibits higher carrier mobility, better subthreshold swing, lower threshold voltage, higher on/off current ratio and reduction of trap state density.

6.3.2 Extraction of density of state and reliability issues

To clarify how the nitrogen passivate the trap states of poly-Si TFTs, Fig.6.5 shows the density of states (*DOS*) in the band gap by field-effect conductance method [24] in different NH_3 treated time. As shown this Figure, both deep states and tail

states are significantly reduced in the NH_3 treated TFT. SiGe-TFTs is required lower processing temperature than Si. It exists many dangling bonds and strain bonds at the SiO_2/poly-Si interface, resulting in high deep states and tail states [25], [26]. However, for the NH_3 plasma treated TFT, nitrogen atoms were introduced into the SiO_2/poly-Si network to terminate the dangling bonds, release the strain bonds and form the S-N or Si-H bonds. For the long time NH_3 treated TFTs, nitrogen atoms were introduced into the interface reducing the trap state and resulting in a great improvement of device characteristics.

The hot-carrier stress test was performed at V_D=15V, V_G=10V, and source electrode grounded for 200 sec to investigate the device reliability. The variation in threshold voltage (V_{th})is defined as ($V_{th,stressed}$–$V_{th,initial}$)/ $V_{th,initial}$×100%, where the $V_{th,initial}$ and $V_{th,stressed}$ are the measured V_{th} prior to and after the electrical stress. As can be seen, the fluorination process can greatly alleviate the On-current degradation under a hot carrier stress.Fig. 6.6 shows the variations of the threshold voltage over hot carrier stress time. The improvement of the surface roughness at the oxide/poly SiGe interface is found to be critical to reduce the hot carrier generation rate and eliminate damage.

6.4 Summary

We have fabricated poly-SiGe TFTs using CMP process. This work examines the study of the poly-SiGe TFTs using NH_3 passivation and CMP process. Experimental results indicate that NH_3 passivation could effectively improve the turn on characteristics. Moreover, the TFTs fabricated on polished poly-SiGe film exhibits higher carrier mobility, better subthreshold swing, lower threshold voltage, and higher on/off current ratio. The results clearly show that by employing the plasma and CMP

steps, significant improvement in the poly-SiGe TFTs with low thermal budget and reduction of the hot carrier generation rate can be achieved. By NH_3 treated poly SiGe TFTs which could reduce the trap state and resulting in a great improvement of device characteristics.

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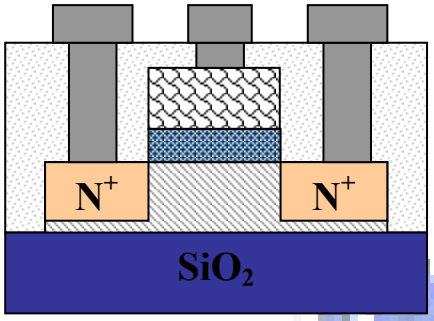
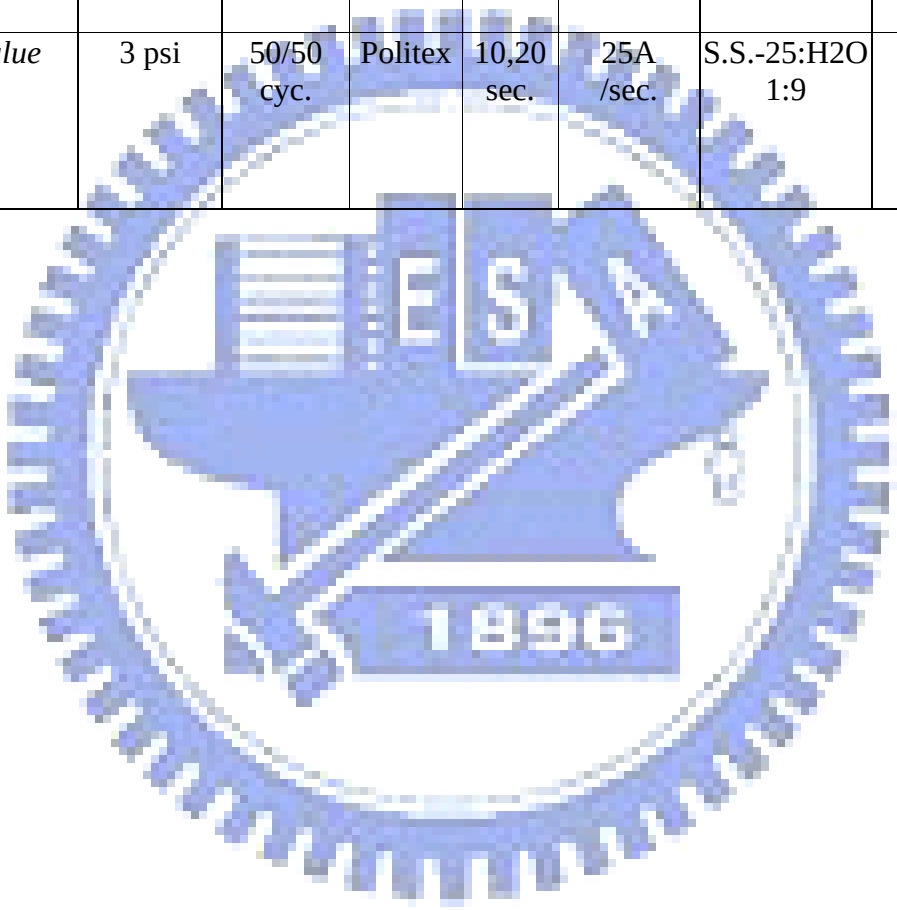


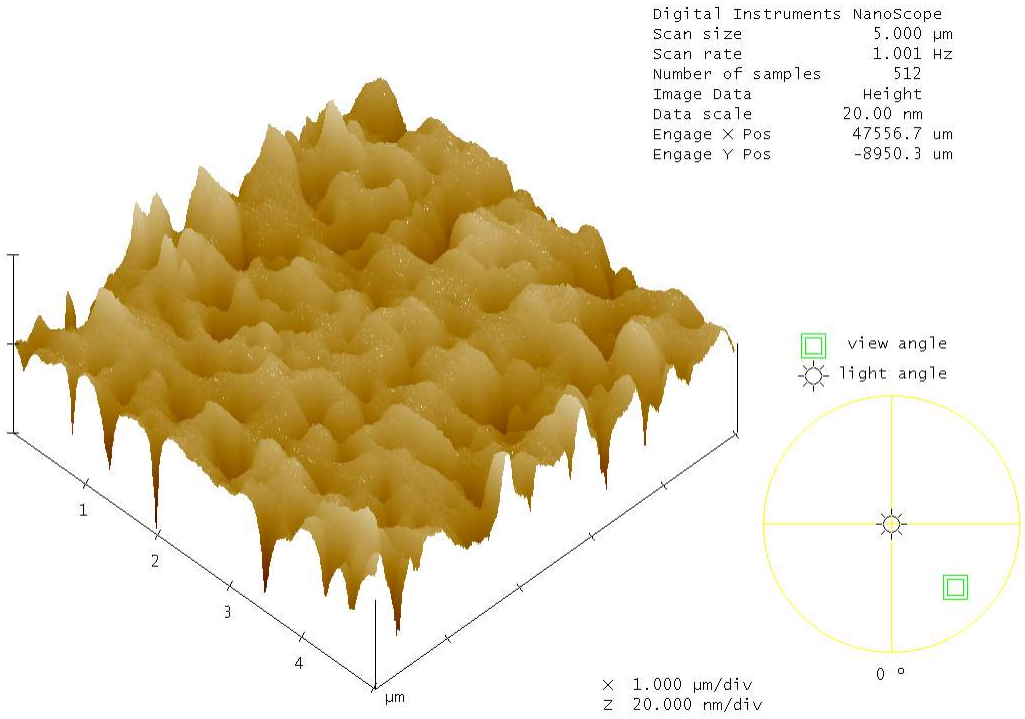
- ***$Si_{1-x}Ge_x$ (x=18 %)***
- ***Active region 100 nm***
- ***SPC 550 ℃***
- ***<u>CMP surface treatment process</u>***
- ***Gate oxide 500Å***
- ***Ion Imp. & annealing***
- ***Plasma treatment***

Fig. 6.1 Process flow for SiGe TFTs.

Table 6.1 Parameters of CMP process condition

Parameter	Down Force	Platen/ Carrier Speed	Platen Pad	Time	Removal Rate	Slurry (CABOT)	p.H
Value	3 psi	50/50 cyc.	Politex	10,20 sec.	25A /sec.	S.S.-25:H2O 1:9	11.5

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Scan rate 1.001 Hz
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Data scale 20.00 nm
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Engage Y Pos -8950.3 um
view angle
light angle
0 °
1
2
3
4
µm
X 1.000 µm/div
Z 20.000 nm/div
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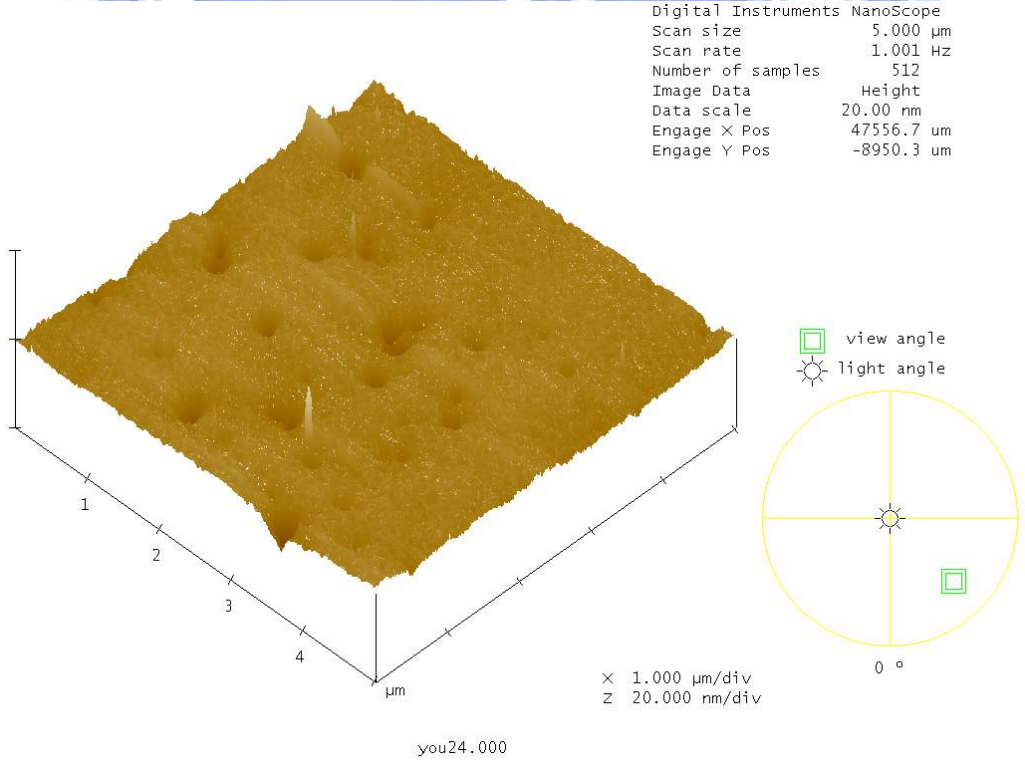
(a)


Digital Instruments NanoScope
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Data scale 20.00 nm
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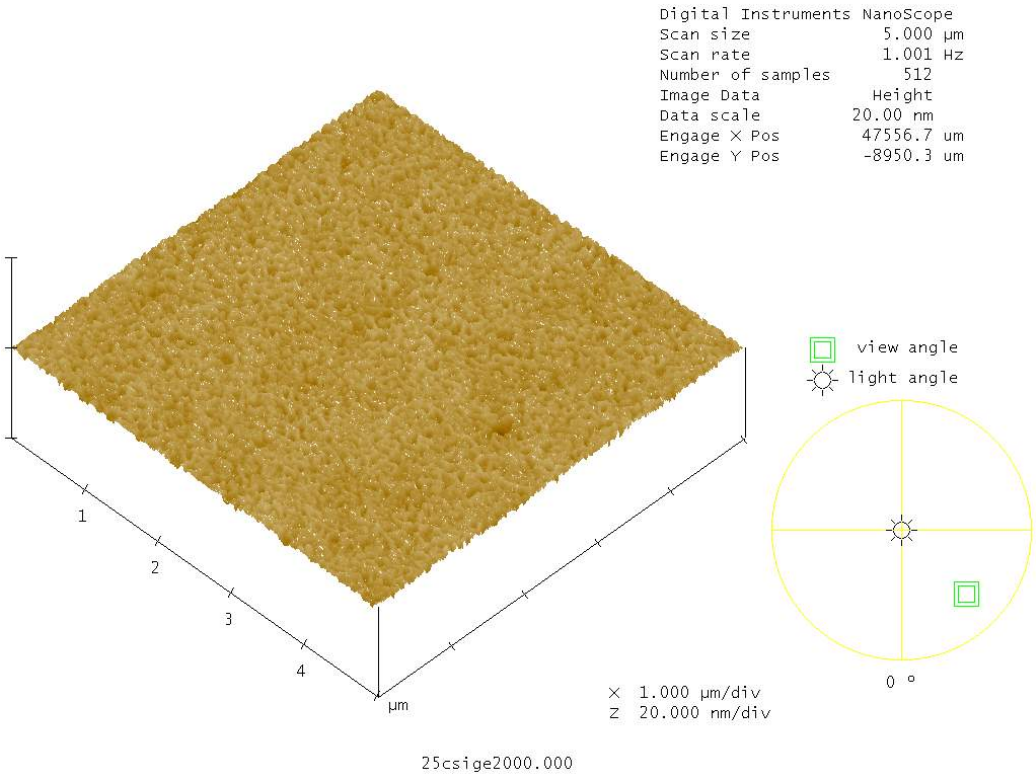
Engage Y Pos -8950.3 um
view angle
light angle
0 °
1
2
3
4
µm
X 1.000 µm/div
Z 20.000 nm/div
you24.000

(b)



(c)

Fig. 6.2 Three-dimensional AFM images of SiGe film surface (a)before CMP process, and after CMP polishing process for (b)10 seconds and(c)20 seconds, respectively.

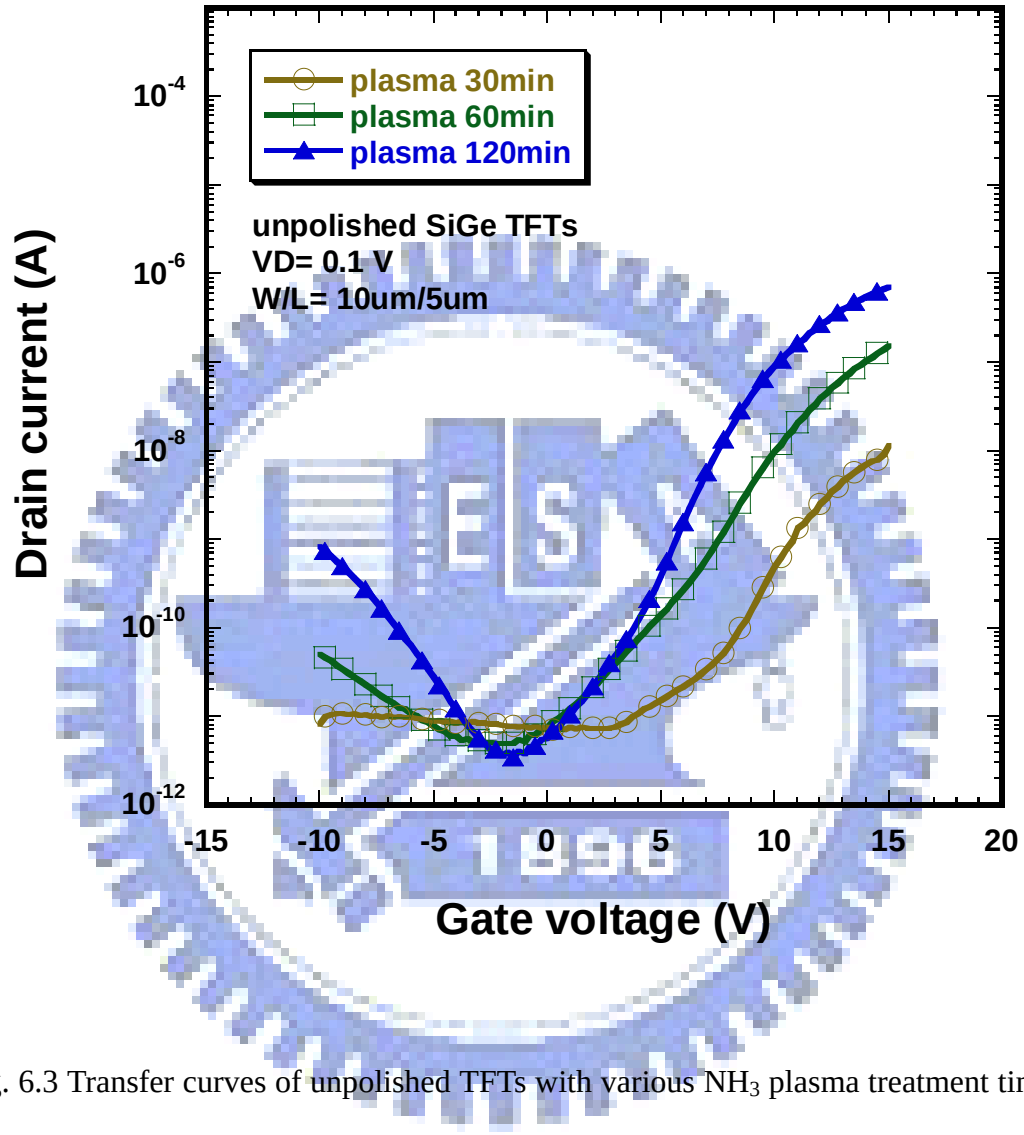


Fig. 6.3 Transfer curves of unpolished TFTs with various NH_3 plasma treatment times in 30, 60, 120 minutes.

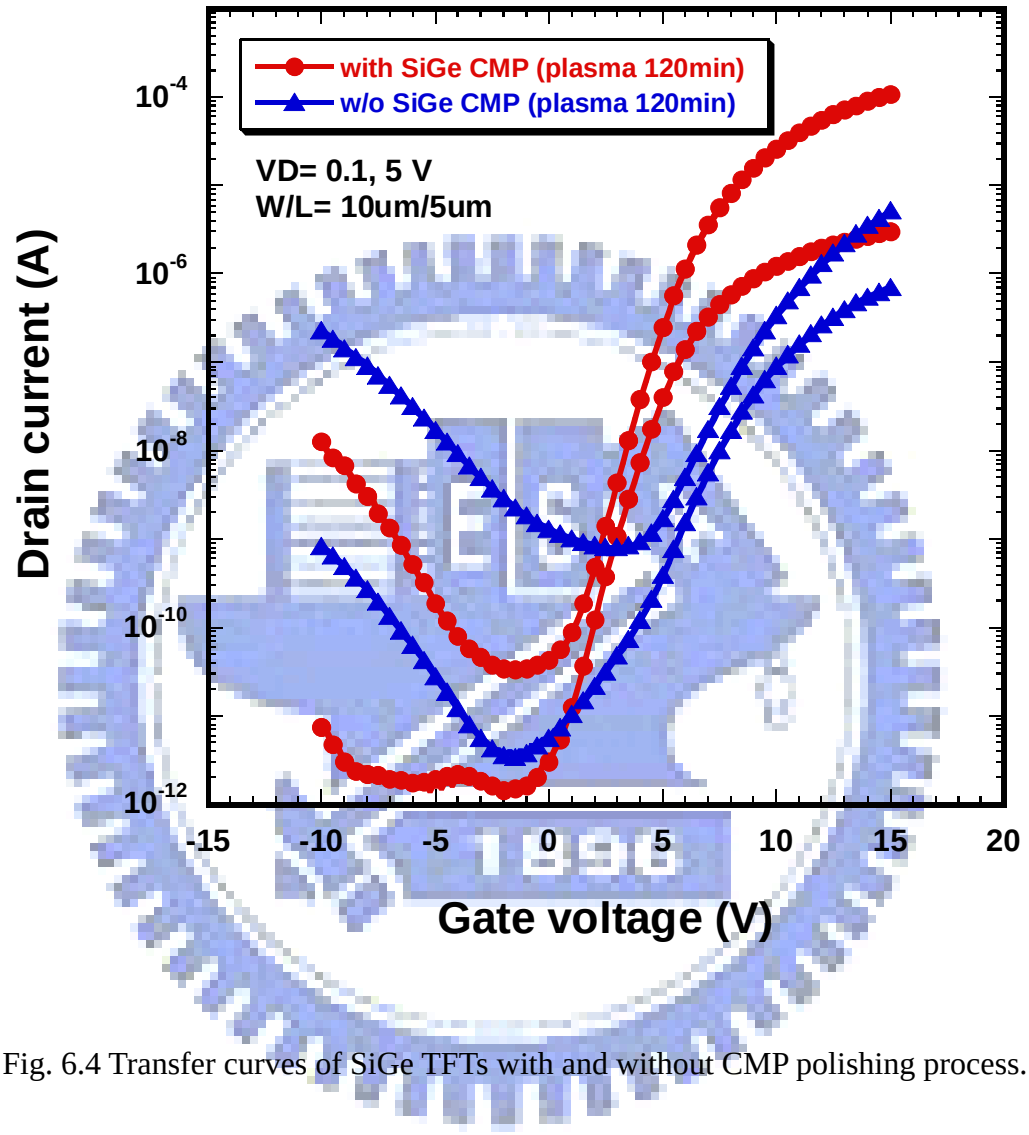


Fig. 6.4 Transfer curves of SiGe TFTs with and without CMP polishing process.

Table 6.2 Characteristics of TFTs with and without CMP process

	Vth (V)	S. S. (V/dec.)	μeff (cm^2/V.s)	Ion@ VG=15V (A)	Ioff	ON/OFF Ratio	Nt (cm^{-2})
SiGe TFTs w/o CMP	**10.3**	**2.1**	**6.3**	**7.16×10^{-7}**	**1.21×10^{-11}**	**5.92×10^{4}**	**6.42×10^{13}**
SiGe TFTs with CMP	**5.75**	**1.25**	**12.5**	**3.06×10^{-6}**	**1.42×10^{-12}**	**2.15×10^{6}**	**1.42×10^{13}**

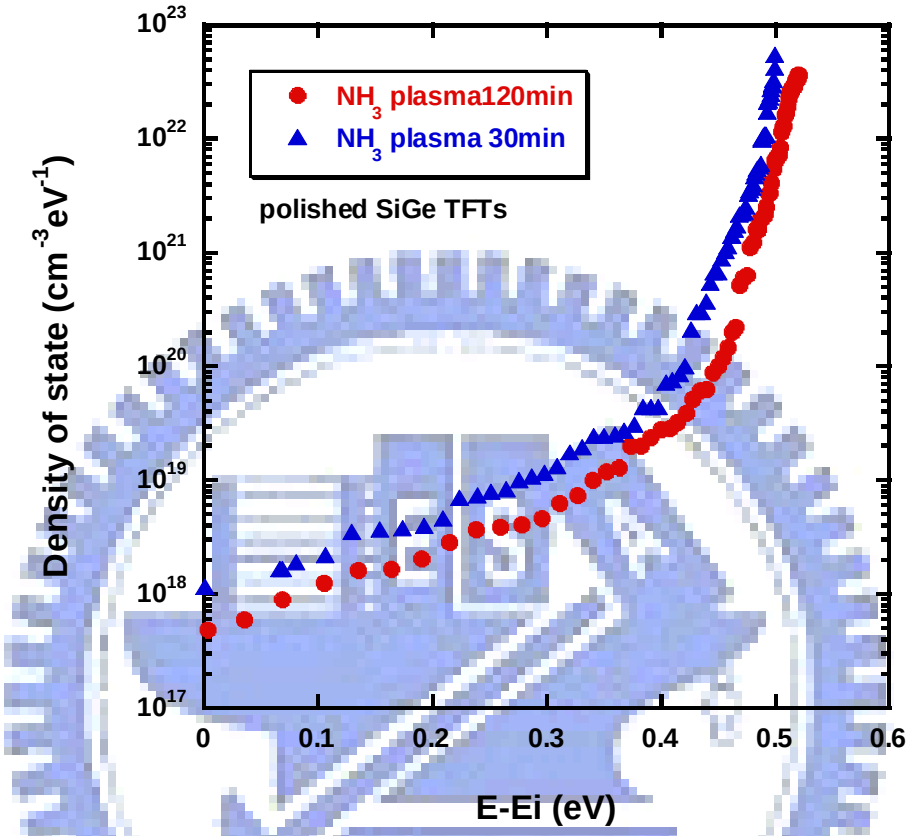


Fig. 6.5 Density of states in band gap of the device using the polished SiGe film as channel with different NH_3 plasma treatment times.

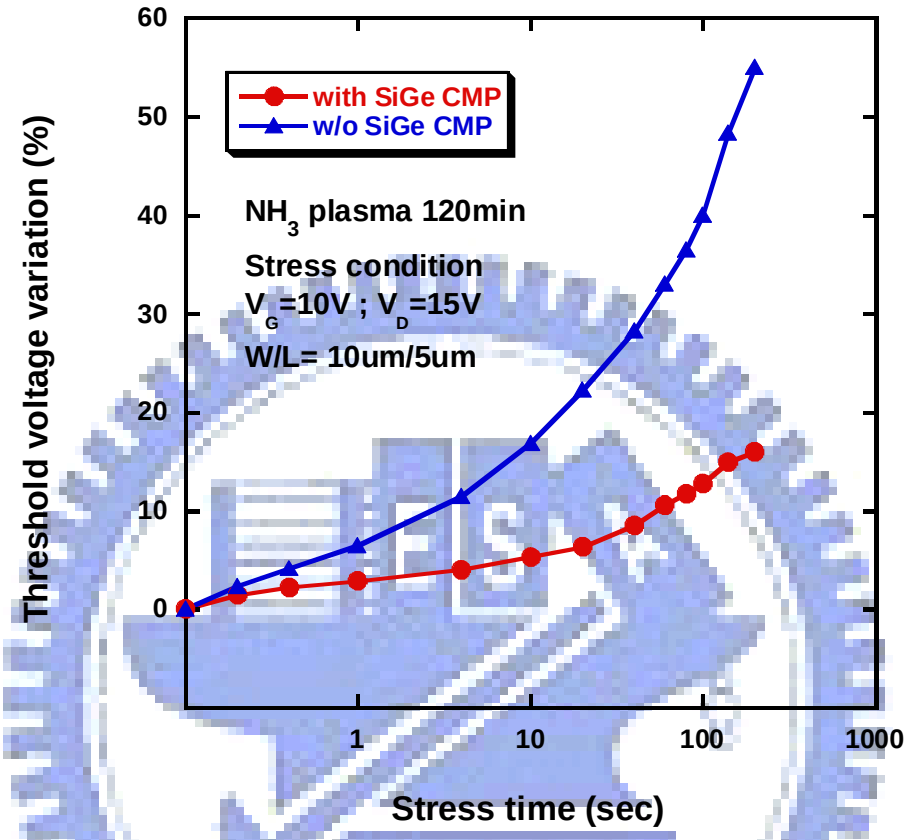


Fig. 6.6 Threshold voltage degradation as a function of stress time under hot-carrier stress.

Chapter 7

Conclusions and Further Recommendations

7.1 Conclusions

In this thesis, the applications of these two kinks of epitaxy films were investigated. Planarization of rough surfaces of strain-relaxed $Si_{0.8}Ge_{0.2}$ buffer layer was done by CMP and post-CMP cleaning. It was found that soften polish pad can be eliminated SiGe surface roughness. The optimum conditions can achieve the strained-Si surface roughness of 0.6 nm. For the post-CMP cleaning process, various cleaning solutions have been applied to the SiGe buffer layer. By adding the surfactant (TMAH) and chelating agent (EDTA) into the diluted ammonium solution, removal efficiency of particles and metallic impurities is increased. The electrical performances of capacitors such as breakdown voltage, leakage current and Q_{bd} are significantly improved for post-CMP cleaning. Furthermore, the optimal condition of SC1+TE sample has increased about 10 % in drive current. This post-CMP cleaning process is useful for planarization of strain-relaxed SiGe virtual substrates in MOSFET application.

We have developed a novel n-channel $Si_{1-y}C_y$ interlayer heterostructure DTMOS structure. This layer could effectively reduce the diffusion of boron beneath the channel region. A low surface channel impurity with heavily doped substrate can be achieved simultaneously. The excellent performances obtained in the $Si_{1-y}C_y$ interlayer DTMOS are due to both the same substrate doping concentration and lower channel surface impurity concentration. DTMOS have superior characteristics in terms of the higher transconductance and saturation current. So its surface impurity scattering could be reduces and it can offer a superior performance in future scaled

devices. This device achieves 1.2 times higher Gm and 1.8 times larger drain current. It appears to be a very promising technology for nano-scale device and ultra-low voltage application.

Next the application of poly-Si and poly SiGe were investigated. We demonstrate the fabrication process and the electrical characteristics of n-channel polycrystalline silicon Thin-Film Transistors with different numbers of channel stripes. The device's electrical characteristics, such as on-current, threshold voltage, and subthreshold swing, were improved by increasing the number of channel stripes due to the enhancement of gate control. However, the electric field strength near the drain side was enlarged in multi-channel structures, causing severe impact ionization. The degradation of device's reliability under various electrical stress conditions was suggested. A severe reliability was found which can be attributed to the enlargement of the electric field at drain side. Therefore, for the fabrication of highly reliable devices and to improve the yield of multi-channel TFTs, the channel structures must be carefully designed.

The improvement of poly-SiGe TFTs using NH_3 passivation and chemical mechanical polishing (CMP) process was examined. Experimental results indicated that NH_3 passivation could effectively improve the turn on characteristics. Moreover, the TFTs fabricated on polished poly-SiGe film exhibit higher carrier mobility, better subthreshold swing, lower threshold voltage, and higher on/off current ratio due to the smooth poly-SiGe interface.

7.2 Further Recommendations

There are some topics that are suggested for future work:

(1) For the post CMP cleaning solution, we can study the solution used in front end application, or the TFTs fabricated on polished poly-Si or SiGe film.

(2) We have developed a super-steep-retrograde (SSR) SiC interlayer channel profiles. For short channel device consideration, the SSR can provide a heavily substrate doping concentration and lower channel surface impurity concentration. An optimized, vertically and laterally nonuniform doping profile is needed to control the short-channel effect to substitute for super halo structure.

(3) Also, by the carbon retardation boron TED effect, we can develop an ultra shallow junction in this interlayer structure.

(4) We can use the LDD structure to alleviate the electrical field near the drain side in the multi-channel TFTs.

(5) Using various plasma treatments (CF_4, N_2O), and incorporation of nitrogen and fluorine can be used to improvement the SiGe TFT chatacteristics. And the surface roughness can also be improved by introducing an interlayer by high density plasma oxide, such as ECR, ICP.

(6) Instead of CMP process, a spin on chemical solution process can be used to reduce the poly-SiGe surface roughness.

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博士論文題目:

矽鍺與矽碳薄膜應用於金氧半場效電晶體和複晶矽鍺與多通道薄膜電晶體之研究

Study on SiGe and SiC Films in MOSFETs and Poly-SiGe and Multi-Channel Poly-Si in TFTs

Publication Lists

1. International Journal:

[1] Wen Luh Yang, **Ming shan Shieh**, Yu Min Chen, Tien Sheng Chao,Don-Gey Liu and Tan Fu Lei, "Improvement of Polysilicon Oxide Integrity Using NF3-Annealing," *Jpn. J. Appl. Phys.*, vol. 39, no. 6B, pp. L562-L565, 2000.

[2] **M. S. Shieh**, Y. J. Lin, C. M. Yu and T. F. Lei, "Characterization of Polysilicon Thin-Film Transistors with Asymmetric Source/Drain Implantation," *Nuclear Inst. and Methods in Physics Research, B, Elsevier Science*, 237(1), pp. 223-227, 2005.

[3] **Ming-Shan Shieh**, Pang-Shiu Chen, M. –J. Tsai and Tan Fu Lei, "The CMP Process and Cleaning Solution for Planarization of Strain-Relaxed SiGe Virtual Substrates in MOSFET Application," *Journal of Electrochemical Society*, vol. 153, no. 2, pp. G144-G148, 2006.

[4] **Ming Shan Shieh**, Jen Yi Sang, Chih Yang Chen, Shen De Wang and Tan Fu Lei, "Electrical Characteristics and Reliability of Multi-channel Polycrystalline Silicon Thin-Film Transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 4B, pp. 3159-3164, 2006.

[5] **Ming-Shan Shieh**, Chih-Yang Chen, Yuan-Jiun Hsu, Shen-De Wang, Wen-Luh Yang and Tan-Fu Lei, "Improved Silicon Germanium Thin Film Transistor Characteristics and Reliability by using Chemical Mechanical Polished," submitted to *IEEE Trans. Dev. Mater. Rel.*.

[6] Chih-Yang Chen, Shen-De Wang, **Ming-Shan Shieh**, Wei-Cheng Chen, Hsiao-Yi Lin, Kuan-Lin Yeh, Jam-Wen Lee and Tan-Fu Lei, "Plasma-Induced Damage on the Performance and Reliability of Low Temperature Polycrystalline Silicon Thin Film Transistors," submitted to *Journal of Electrochemical Society*.

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2. International Letter:

[1] Wen Luh Yang, Chih-Yuan Cheng, Ming-Shih Tsai, Don-Gey Liu, **Ming-Shan Shieh**, "Retardation in the Chemical-Mechanical Polish of the Boron-Doped Polysilicon and Silicon," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 218-220, 2000.

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3. International Conference:

[1] **M. S. Shieh**, Y. J. Lin, C. M. Yu, T. F. Lei, "Characterization of Polysilicon Thin Film Transistors with Asymmetric Source/Drain Implantation," *15th International Conference on Ion Implantation Technology (IIT 2004)*, pp. 150-151.

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4. Local Conference:

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