Chapter 4
Electrical and optical improvement of Si nanocrystal based LED

4.1 Si nanocrystal based LED with Si nano-pyramid

4.1.1 Introduction

Plasma enhanced chemical vapor deposition (PECVD) grown Si-rich SiO_2 or SiO_x with embedded Si nanocrystals (nc-Si) of extremely high density have been extensively investigated as a new class of light emitting material over decades [1-6]. To obtain room temperature electroluminescence (EL), both the metal/SiO_x/Si and the metal/n-Si/SiO_x/p-Si based light emitting diodes (LEDs) were demonstrated [7, 8], in which Fowler-Nordheim (F-N) and direct p-n junction barrier tunneling mechanisms were known to play important roles for the light emission from Si nanocrystals. However, the EL responses of such devices are usually not efficient due to the requirement of extremely high electric field for carriers tunneling through the insulating oxide channel [9, 10]. Therefore, versatile solutions have recently been developed to enhance the carrier injection efficiency, such as changing the contact metals, shrinking the optical bandgap, decreasing the barrier height, and reducing the resistivity of the host material, etc. In this work, we discuss the effect of PECVD grown nano-roughened SiO_x/Si interface on the enhancement of F-N tunneling in an indium tin oxide (ITO)/SiO_x/p-Si based metal-oxide-semiconductor light emitting diode (MOSLED). The surface density of roughened interfacial Si nano-pyramid structure and its correlation with the threshold electric field strength for initiating the F-N tunneling mechanism is determined.

4.1.2 Sample preparation and experimental setup

The Si-rich SiO_x film was deposited on *p*-type (100)-oriented Si substrate by PECVD at chamber pressure of 60 mtorr. The N_2O and SiH_4 fluences were controlled at 150 and 30 sccm, respectively, while the inductively couple plasma (ICP) power was varied from 60 to 30 watts. The Si substrate temperature was detuned between 200 and 400 ^oC during 5-min deposition. Typically, the sample was deposited at substrate temperature of 300^oC with an ICP power of 40-45 watts. To roughen the SiO_x/Si interface, the substrate temperature were raising up to 400 ^oC and the ICP power was decreasing to nearly threshold condition (25-30 watts), leading to the pre-deposition of randomized Si nano-pyramids on Si substrate prior to the growth of the SiO_x. To investigate the carrier transport, a 2000-Å ITO film layer (resistivity 33 Ω-cm) was deposited on the top of SiO_x with diameter of 0.8 mm to form the ITO/SiO_x/p-Si MOSLED. A 5000-Å Al contact was coated on the bottom of Si substrate following by an alloying process at 450 ^oC for 7.5 min.

4.1.3 Fowler-Nordheim Tunneling Enhanced Light Emission

First of all, the interface morphology of the PECVD grown SiO_x samples with different recipes was analyzed by high resolution transmission electron microscope (HRTEM) analysis, as shown in Fig. 1. For example, the cross-sectional view of the normally PECVD grown Si-rich SiO_x film shows smooth SiO_x/Si interface and precipitated Si nanocrystals with crystalline electron diffraction pattern. In contrast, the TEM photograph of the SiO_x sample grown at high substrate temperature and threshold ICP power further reveals the existence of dense Si nano-pyramids at the

SiO_x/Si interface, while the interfacial Si nano-pyramid exhibits completely same electro diffraction pattern with that of the Si substrate. Under growing at the ICP powers of 35, 40, and 45 watts, the area densities of the interfacial Si nano-pyramids are estimated as 1.6×10^{11} cm^{-2}, 10^{9} cm^{-2}, and $<10^{8}$ cm^{-2}. Similar surface nano-pyramid density of 1.1×10^{11} cm^{-2} for the sample preparing at ICP power of 35 watts was also observed by AFM analysis. The Si nano-pyramids exhibit identical orientation with that of the Si substrate. The electric field (E) dependent emission current (I) can be described and the current-field plot can thus be fitted by F-N tunneling equations (3-4): [11]

By linearly fitting the F-N plot of log (I/E^2) vs $1/E$, the F-N tunneling behavior can be confirmed according to the observation on the linear transferred function characteristic in the F-N plot, as shown in Fig. 2. The threshold electric fields to initiate F-N tunneling in three samples are ranging from 1.4 to 7 MV/cm, which indicates the effective potential barrier of the sample becomes smaller as the density of interfacial Si nano-pyramids increases. This essentially corroborates with the reduction on threshold electric field of F-N tunneling occurred in the sample grown at lower ICP powers.

If we further illustrate the threshold F-N tunneling electric field as a function of the area density of Si nano-pyramids, a linear correlation can apparently be obtained and shown in Fig. 3. Obviously, the F-N tunneling mechanism has further been enhanced by increasing the area density of interfacial Si nano-pyramids. Due to the existence of Si nano-pyramids which behave like field emitters, the electrons will easily be gathered around the cone of the Si nano-pyramid and tunneled into the Si nanocrystals from the tip of the Si nano-pyramid, which consequently enhances the current injection and the electron-hole recombination. Similar phenomena have

previously been observed in other material systems. Gong *et al*. [12] have observed that the roughness at the poly-Si/SiO_2 interface on both p- and n-well capacitors gives rise to higher electric fields and lower barrier heights and the breakdown degrades more with rising temperature. Maydell *et al.* [13] have investigated the electronic transport in laser-crystallized P-doped poly-Si, they concluded that the potential barrier height at the grain boundaries decreases with increasing electron concentration. This is due to a fact that the Fermi level in the grain may shift towards the band edge due to the doping, whereas the Fermi level at the grain boundary is pinned around the midgap due to the large amounts of dangling bonds on the poly-Si surface. Moreover, Ushiyama *et al*. [14] demonstrated with an atomic force microscope that the phosphorus-implanted poly-Si gate with an implanted dose below 10^{16} cm^{-2} and a low-temperature oxide annealing condition, could result in a smoother poly-Si/SiO_2 gate interface associated with a higher barrier. That is, the smooth interface with few defect are more resistant to the F-N tunneling process. Ohmi *et al*. [15] find the electric-field breakdown to be related to silicon surface micro-roughness, and Sugino *et al*. [16] have reported that the surface roughness effectively facilitates the reduction of the turn-on electric field and the effective potential barrier height, while the F-N tunneling based electron emission is enhanced by the boron-nitride nano-film with a more rough surface as compared to that of the Si substrate.

4.1.4 Performances of the Interfacial Si Pyramid based Si Nanocrystal MOSLED

Since the Si nano-pyramids also introduce the surface roughness on Si substrate, a large amount of the dangling bonds and associated defects could also exist at the SiO_x

/ Si interface. Under the large bias or high electric filed, the band structure of Si near the SiO_x/Si interface could be seriously bended, as shown in Fig. 4, where the charge distribution in the Si substrate would be inverted. With the increasing bias voltage, the energy level of the conduction band of Si will be lower than that of the defects distributed with the Si nano-pyramids, and the electrons trapped by these defects become free electrons. This also enhances the carrier transport and enlarges the tunneling current of the MOSLED at the same biased condition. In contrast, the band diagram of the sample without Si nano-pyramids shown in Fig. 4 is almost defect-free, in which the electrons (minority carriers) require a higher biased electric filed to tunnel through the barriers of the MOS structure. This also elucidates the significant reduction of threshold electric field and turn-on voltage of the ITO/SiO_x/p-Si/Al diode with interfacial Si nano-pyramids. The current-voltage (I-V) and current-optical power (I-P) characteristics of three ITO/SiO_x/p-Si/Al MOSLEDs with different densities of interfacial Si nano-pyramids are illustrated in Fig. 5. It is clearly seen that both the smallest bias and the largest output power can be achieved if we reduce the ICP power of the PECVD system to facilitate the maximum growth of interfacial Si nano-pyramids. In particular, the EL power of the ITO/SiO_x/p-Si/Al MOSLED with the highest Si nano-pyramid density can be enlarged by two times as compared to that of the similar device without any interfacial Si nano-pyramids. From HRTEM analysis for the annealed SiO_x film with and without interfacial Si nano-pyramids, as shown in Fig. 6. The densities of nc-Si within the SiO_x grown without and with interfacial Si nano-pyramids are 5.7×10^{18} cm^{-3} (left part of Fig. 6) and 3.7×10^{19} cm^{-3} (right part of Fig. 6). It is thus corroborated that the density of nc-Si embedded in SiO_x significantly decreases as the interfacial Si nano-pyramids occurs. Therefore, the slope efficiency of the ITO/SiO_x/p-Si/Al MOSLED with interfacial Si nano-pyramids is inevitably reduced as the buried nc-Si dilutes (see Fig.

5). The EL spectra of ITO/SiO_x/p-Si/Al MOSLEDs with and without interfacial Si nano-pyramids biased at maximum output condition are compared, as shown in Fig. 7. For the MOSLED samples without interfacial Si nano-pyramids, the nc-Si related near-infrared EL with dual peaks at 455 and 740 nm is observable at biased voltage larger than 160 V. The nc-Si dependent EL component slightly blue-shifts from 740 to 690 nm as the biased voltage increases from to 160 V to 200V, whereas the blue-green EL peak wavelengths remain unchanged. Such a blue-shifted near-infrared EL peak clearly indicates different luminescent mechanisms occurred as the band bending becomes serious under an extremely high electric field, leading to the carriers between adjacent nc-Si tunneled from first-order quantized state (n=1) to second-order quantized state (n=2). [10] In addition, the unanticipated EL peaks at central wavelength of 455 nm also grows up with increasing biases, which are contributed by oxygen dependent structural defects such as the neutral oxygen vacancy (NOV) centers [4] generated in the oxide layer when biased at nearly breakdown condition. Alternatively, the ITO/SiO_x/p-Si/Al MOSLED with interfacial Si nano-pyramids biased at 70 V reveals an EL spectra with smaller defect-dependent emissions. The nc-Si dependent broad spectra ranging between 650 and 850 nm is not shifted with the increasing bias. The operation of a MOSLED at such a lower electric field could not contribute to serious band bending, thus avoiding the cold-carrier tunneling process happened between adjacent nc-Si. In this case, the blue-shifted near-infrared EL phenomenon no longer exists on the Si nano-pyramid enhanced MOSLED device. Furthermore, the lower electric field required for the EL under the assistance of interfacial Si nano-pyramids prevent the generation of structural damage as well as the corresponding NOV defects, thus attenuating the defect related EL at blue-green region as compared to the typical MOSLED without interfacial Si nano-pyramids.

For comparison, all of the key device parameters of the samples grown at different ICP powers were listed in Table I. These oxygen-correlated interfacial states play dominant roles on the white-light emission from ITO/SiO_x/p-Si/Al MOSLED at the high electrical field, which are unstable as a highly biased condition is required to trigger the defect-enhanced EL. The bias dependent surface-emitting EL patterns of a diode made on the Si-rich SiO_x with and without interfacial Si nano-pyramids are shown in Fig. 8. Larger EL power obtained for the typical ITO/SiO_x/p-Si/Al MOSLED without Si nano-pyramids is partially attributed to the radiant defects generated in damaged SiO_x structure operated under such a nearly breakdown condition ($E_{breakdown} \approx 10$ MV/cm). The radiative defects usually contribute to a broadened EL at shorter wavelength region, which inevitably results in an EL pattern with a bright color (see upper row in Fig. 8). Although the ITO/SiO_x/p-Si/Al MOSLED with interfacial Si nano-pyramids can not reach the same EL power as compared to those without Si nano-pyramids at same biased condition, which is still able to emit larger EL power at higher current and lower biased conditions. In contrast to the conventional MOSLEDs operated at biases nearly breakdown, the interfacial Si nano-pyramids also behaves like tipped field emitters to release breakdown of the MOSLEDs. On the other hand, a release on the critical emitting angle which is needed to avoid total internal reflection (TIR) has also been considered in previous studies of the LEDs [17, 18], which facilitates a larger fraction of light emitted from the active region of LED. Versatile methods of surface roughening have been introduced to improve the external quantum efficiency of LEDs. In our results, the interfacial Si nano-pyramids on the surface of Si substrate also acts like a novel surface roughened layer, which not only enlarge the current injection by enhancing F-N tunneling in the ITO/SiO_x/p-Si/Al MOSLED, but also improve the external quantum efficiency of light emission by releasing the critical TIR angle

limitation with the roughened SiO_x/Si interface. Consequently, the external quantum efficiency and the maximum EL output power of the ITO/SiO_x/p-Si/Al MOSLED with interfacial Si nano-pyramids can be increasing at a lower biased condition, as shown in Fig. 5. If we further characterize the lifetime for three different samples, it is clearly seen that the typical device without Si nano-pyramids will be damaged within 10 minutes even operating at below breakdown condition, as shown in Fig. 9. The lifetime of the MOSLED device can be effectively lengthened to several hours by introducing the Si nano-pyramids which reduces the biased field away from the breakdown. The radiant defects although contributes the EL power, however, which also degrade the lifetime performance of the MOSLED device. Our experimental results have interpreted the importance of PECVD growing condition on the synthesis of Si nano-pyramids, which rely on adjusting a large desorption rate of the SiH_4 under a oxygen-deficient environment, following by the deposition of the defect-free Si-rich SiO_x film at high substrate temperature and threshold ICP power condition. In comparison, the growth condition of lower substrate temperature and higher ICP power inevitably contribute to a faster deposition rate with smaller excess Si density under an oxygen-rich environment, which degrades the precipitation of the interfacial Si nano-pyramids and fails to enhance the carrier transport in the diode.

4.1.5 Conclusion

In conclusion, the premier observation on the enhanced F-N tunneling mechanism from the novel SiO_x/nano-Si-pyramid/Si structure is demonstrated. Dense Si nano-pyramids can be synthesized at the SiO_x/Si interface by reducing the ICP power during the PECVD growth of Si-rich SiO_x on Si with high substrate temperature. The correlation between the surface density of interfacial Si

nano-pyramids and the threshold F-N tunneling field has been illustrated. With these interfacial Si nano-pyramids at a surface density of 1.6×10^{11} cm^2, the F-N threshold can be reduced from 7 to 1.4 MV/cm. The elucidation on the role of the Si nano-pyramids played on the improved carrier transport and enhanced light emission properties are addressed. The existence of Si nano-pyramids greatly reduces the biased voltage from 200 to 65 V, which is required to obtain sufficient EL power from the MOSLEDs. Consequently, a more stable near-infrared electroluminescence is emitted from the ITO/SiO_x/p-Si/Al MOSLED with interfacial Si nano-pyramids, providing a narrowing linewidth and a lengthened lifetime to >3 hours at room temperature operation. To date, an output EL power of nearly 150 nW under a biased voltage of 75 V and current density of 32 mA/cm^2 is reported.

4.2 Si nanocrystal based LED with Si nano-pillar

4.2.1 Introduction

The increasing interest in low dimensional Si structures has extended over past decade due to potential optoelectronic applications such as being nano probe, [19] surrounding gate or super junction bipolar transistors, [20] memory cell, [21] biosensor, [22] photonic crystal waveguide devices, [23] field electron emitter [24] and field emission light emitting devices. [25] Typically, the fabrication of Si nano-pillars mainly relies on the electron-beam (E-beam) lithography and inductively couple-plasma reactive ion etching (ICP-RIE) process.[26-28] The <10-nm Si nano-pillar array can be produced under the assistance of E-beam lithography. [29] Nowadays, the self-assembled metallic nano-dots have emerged to produce functional nano-sensor or nano-mask. Ni has been considered as an alternative to the noble metal (Au or Ag) for fabricating high-aspect-ratio Si nano-pillars. Nevertheless, the

self-aggregation of Ni nano-dot from a Ni film coated on a Si substrate usually takes up to 10 min and the generated Si nano-pillars are too sparse. [30] In this letter, we demonstrate the formation of dense Si nano-pillar array by reactive-ion etching the oxide-covered Si substrate encapsulated with the self-assembled Ni nano-dot mask. Anomalous micro-photoluminescence (μ-PL) spectra of Si nano-pillars at visible and near-infrared (NIR) spectral regions are also investigated.

4.2.2 Sample preparation and experimental setup

A silicon dioxide (SiO_2) buffered layer with thickness of 200Å is deposited by plasma enhanced chemical vapor deposition (PECVD) under standard recipe. A 50nm-thick Ni film is evaporated on the SiO_2/Si substrate using an E-beam evaporator with Ni deposition rate of 0.1 Å/s. Subsequently, the rapid thermal annealing (RTA) process at 850^{o}C for 22 seconds under the N_2 flowing gas of 5 sccm is performed to assemble Ni nano-dot pattern on SiO_2/Si substrate, which is employed as an etching mask to dry-etch the Si substrate in a ICP-RIE system (SAMCO ICP-RIE 101iPH) at RF frequency of 13.56 MHz with different ICP/Bias power ratios. An etching gas mixture of CF_4 and Ar with pressure ratio of CF_4/Ar = 40sccm/40sccm was introduced to etch SiO_2/Si and to increase the vertical-etching potential, respectively. The dimension and density of the Si nano-pillar array were analyzed by the scanning electron microscope (SEM, Hitachi FE-SEM S-5000). Room-temperature μ-PL was performed in a confocal microscope with 1-μm spatial resolution by using a 325-nm HeCd laser and a 532-nm second-harmonic-generated (SHG) Nd:YAG laser as the pumping sources. A 15X objective lens of numerical aperture 0.32 is used to collect the on-axis PL from the sample, which was received by a monochromator with a photo-multiplying tube.

4.2.3 Precipitation of Ni nano-dots

The SiO_2/Si substrate exhibits an extremely low thermal conductivity to facilitate heat accumulation of the evaporated thin Ni film and to enhance self-aggregation of Ni nano-dot array during RTA. [31] To assist the self-assembly of metallic nano-dots, phase deformation and thermal vibration amplitude, and the melting point of metal atoms can apparently be detuned by thinning the deposited metal layer. [32] As a result, the density of the hemisphere-like Ni nano-dots with <40-nm diameter increases up to 7.2×10^{10} cm^{-2} at an optimized Ni film thickness of 50 Å (see Fig. 10). Lengthening the RTA duration could further shrink the nano-dot size at a cost of reduced density. Low-pressure ICP-RIE was subsequently employed for obtaining high-aspect-ratio Si nano-pillars with the Ni nano-dot mask, as high-pressure condition enlarges the etching rate at a risk of over-etching Ni nano-dots and deforming Si nano-pillars. Furthermore, the shape and aspect ratio of the Si nano-pillars are significantly improved by decreasing the RF/Bias power ratio, whereas the long-term enhanced isotropic etching at large RF/Bias power ratio further erodes the Si nano-pillars. Minor difference between vertical and horizontal etching rates inevitably provides pyramid-like shape of large size and reduced height. The RF/bias power ratio is thus decreased from 3 to 0.5 for obtaining straight Si nano-pillars with perpendicular sidewall and high aspect ratio (see Fig. 11). The density, diameter, height and corresponding aspect ratio of Si nano-pillars are 2.8×10^{11} cm^{-2}, 30-44 nm, 320 nm, and up to 8, respectively (see Fig. 11(d)). These results are relatively comparable with the reported aspect ratios between 7 and 12. [29, 33] In contrast, a straight but short Si nano-pillar shown in Fig. 11(c) was formatted at the RF/Bias power ratio of 1, while an extremely large vertical etching rate leads to the extinguishment on selective etching between Ni nano-dot mask and Si substrate

during ICP-RIE. The SEM illustrated in Fig. 12 reveals significant variation on diameter and density of Si nano-pillars formatted under different RF/Bias power ratios. ICP-RIE at higher RF and Bias powers at a constant ratio may contribute to uniform but smaller Si nano-pillars due to insufficient etching rate.

4.2.4 μ-PL of Si nano-pillar

A peak μ-PL at around 430 nm is observed after removing Ni and SiO_2 nano-dots on top Si nano-pillars (see Fig. 13 (a)), in which two decomposed luminescent centers at 425 and 475 nm are obtained with their spectral linewidths of 60 and 110 nm, respectively, corresponding to oxygen-related structural-defects on the surface of Si nano-pillars, such as weak oxygen bond (WOB), O_2^- defect center, neutral oxygen vacancy (NOV), and the non-bridge oxygen hole center (NBOHC) at 415, 430, 455 and 630 nm, respectively. [34-39] Such intense blue PL emissions were preliminarily found in the electrochemically etched porous Si (PS) structures after rapid-thermal-oxidation, [40] providing a strong evidence on the influence of oxygen related defects within surface SiO_2 due to a strong correlation between the observed blue PL and the Si–O infrared absorption. Ito *et al*. [41] and Chen *et al*. [42] have also corroborated the effect of the highly oxidized PS surface on the broadened 430-nm PL peak. The oxygen atoms would be incorporated in SiH_x backbones as ambient oxidation proceeds, a SiO_2 film naturally grows upon the surface of Si nano-pillars with a maximum oxygen penetrating depth of 3 nm. Such a SiO_2 based PL model is widely accepted to corroborate that the blue PL from Si nano-pillars is correlated with oxygen-related defects in naturally formed SiO_2 on Si nano-pillar in atmosphere environment.

Later on, the Si nano-pillar-related infrared PL excited by a SHG Nd:YAG laser at

532 nm was characterized. Note that both the Si nano-pillars and the unprocessed Si wafer reveal the same PL signal around 700-750 nm with two distinct peak wavelengths at 703 and 740 nm (see Fig. 13(b)). All Si nano-pillar samples with different sizes were characterized to confirm the invariability of the 750-nm PL, which is not directly correlated with the Si nano-pillar structure but can be attributed to other irradiative defects in the Si matrix. To perform such an analysis, the size of Si nano-pillar samples at 30-50 nm was reduced by successive natural oxidation in atmospheric environment and chemical etching in buffer-oxide-etching solution. A plan-view SEM picture shows the smallest size of obtained Si nano-pillar is about 6 nm (see the inset of Fig. 14). The PL of all Si nano-pillar samples was taken immediately after oxidation and etching. Experimental results preliminarily elucidate that neither the SiO_2 nor the Si nano-pillar can contribute to 750-nm PL, since the SiO_2 film on Si nano-pillar surface was completely removed.

In contrast to the significant PL spectrum at 700-750 nm, a tiny PL between 800 and 900 nm was also observed from the sample with Si nano-pillar size smaller than 7.2 nm (see Fig. 13 (c)). The relatively small PL intensity is primarily due to the insufficient density of the Si nano-pillars (only with a surface density of $2.8\times10^{10}/cm^2$). A blue-shifted PL phenomenon with its wavelength decreasing from 874 to 826 nm was clearly observed as the Si nano-pillar size shrinks from 7.2 to 6 nm (see Fig. 13(d)). The SEM observed Si nano-pillar size correlates well the theoretical value of $\lambda=1.24/(1.12+3.73/d^{1.39})$ as reported by Delerue *et al*. [43], which estimates the rod size of the etched Si nano-pillars ranging from 7 to 5.7 nm according to their corresponding PL wavelengths. The broadened linewidth of PL from the Si nano-pillar sample was shrunk from 50 to 17 nm, due to the formation of the Si quantum-pillar. As the Si nano-pillar size becomes larger than 7.2 nm, the PL gradually decreases due to diminishing quantum-confinement effect (QCE). It is

concluded that the size dependent PL can only be observed when the size of Si enters the quantum-confined regime, which is directly attributed to the recombination of quantum-confined electron and hole pairs in the Si nano-pillars. Prior to the successive oxidation and etching, the Si nano-pillar with average size of >30 nm and height of 320 nm is unavailable to contribute any QEC related luminescence, except the defect dependent PL remaining unchanged at 700-750 nm. The evolution of the peak PL wavelength for different etched Si nano-pillars as a function of size is shown in Fig. 14.

4.2.5 Optical property of the Si nanocrystal based LED with Si nano-pillar

By rapid thermal annealing a 5-nm thick Ni film evaporated on a 20-nm thick SiO_2 layer covered Si substrate, we have successfully demonstrated the self-aggregation of two-dimensional randomized Ni nano-dot mask on a p-type (100) Si wafer with a 200-Å-thick SiO_2 based heat-accumulated layer (see Fig. 15(a)). [44] With an inductive-coupled-plasma reactive-ion-etching process, a high-aspect-ratio Si nano-pillar array with rod diameter of 30 nm and height of 350 nm can be formatted on Si substrate (see Fig. 15(b)). Afterwards, the Si-rich SiO_x film with thickness of 240 nm was grown on the Si nano-pillar substrate by using plasma-enhanced chemical vapor deposition (PECVD) and furnace-annealed at 1100^{o}C to precipitate nc-Si. [45, 46] The device structure of the nc-Si based MOSLED on silicon nano-pillar array is illustrated in Fig. 15(c). The top view of a Cu-wire-bonded ITO/SiO_x:nc-Si/Si-nano-pillar/Si/Al MOSLED with circular contact diameter of 0.8 mm is shown in Fig. 15(d).

After annealing, a broadband PL spectrum with two distinguished peaks at 550

and 770 nm are observed with maximum emitting intensity obtained at a 60min annealed SiO_x film made on Si nano-pillars. The PL intensity at 770 nm rapidly increases by 5 times due to the significant precipitation of nc-Si after annealing time lengthening from 15 to 60 min. Regrowth of SiO_2 matrix as well as re-oxidation of nc-Si occurs at longer annealing is evident from the observation of attenuated near-infrared PL intensity. In contrast, a normalized PL spectrum of the 60 min-annealed SiO_x film grown on a smooth Si substrate with a single peak wavelength of 770 nm was shown in Fig. 16(a). The abnormal PL at 550 nm is possibly contributed by the emission from small-size nc-Si precipitated among dense Si nano-pillar array with a spacing less than 20 μm. The localized deposition of Si-rich SiO_x with in the space region of Si nano-pillars facilitates the confinement on nc-Si size after annealing. On the other hand, three EL peaks at 410, 550 and 760 nm contributed by neutral oxygen vacancy (NOV) [47, 48] defects and nc-Si were observed from the nc-Si MOSLED made on Si substrate with and without Si nano-pillar array, as shown in Fig. 16(c) and 16(d). The EL powers at 410 and 550 nm were significantly enhanced due to the tunneling of carriers into NOV defects and small-size nc-Sis. In particular, the much stronger EL power at these peak wavelengths were observed at the sample made on Si nano-pillar array (see Fig. 16(d)), which were mainly attributed to the enhanced carrier injection from Si nano-pillars to the aforementioned luminescent centers.

4.2.6 Fowler-Nordheim tunneling enhanced light emission Si nanocrystal based LED with Si nano-pillar

The turn-on voltage of nc-Si based MOSLED on Si nano-pillar array is around 30 volts, which is much lower than the same device made on smooth Si wafer ($V_{turn\text{-}on}$ ~42 volts), as shown in Fig. 17. The current-voltage (I-V) slopes of the nc-Si based MOSLEDs with and without Si nano-pillars are 62.5 and 21.4 μA/V, respectively, which also corroborate the contribution of the Si nano-pillars to the larger carrier-injection density as well as higher EL power. However, this is not the only role the Si nano-pillars play in the MOSLED. The optical intensity, turn-on current and power-current slope of the nc-Si based MOSLED on Si nano-pillars are 140 $\mu W/cm^2$, 5 μA and 2±0.8 mW/A, respectively, which are better that the performances of a typical device with corresponding values of 18.5 $\mu W/cm^2$, 25 μA and 1.1±0.5 mW/A. To date, a highest optical power of 0.7 μW is obtained at biased current and voltage of 375 μA and 36V, respectively, which is almost one order of magnitude larger than that of a same device made on smooth Si wafer (see P-I plot in Fig. 17). A clear EL picture of an nc-Si based MOSLED with Si nano-pillars is shown in the inset of Fig. 17. Electrical analysis has concluded that the Fowler-Nordheim tunneling based carrier transport through the Si nano-pillar array is more pronounced than the smooth Si wafer. [49] Such Si nano-pillars functions like a field-emission tips to facilitate the carrier tunneling into nc-Si within the SiO_x film. The external quantum efficiency of a bulk-Si LED usually limits to 10^{-5} if we define the external quantum efficiency as the rate of the output photon number and input electron number described by,

$$\eta_{ext} = \int_{t_0}^{t_1} \frac{P(t)}{h\nu} dt \Big/ \int_{t_0}^{t_1} \frac{I(t)}{e} dt = \frac{P_{opt}}{I_{bias} \times (1.24/\lambda)}, \quad (1)$$

where λ is wavelength, P_{opt} and I_{bias} are the constant optical output power and biased current, respectively. The external quantum efficiency of the nc-Si based MOSLED with Si nano-pillars is up to 0.1% under a power conversion ratio of 5×10^{-5}. This is a relatively high quantum efficiency ever reported for the nc-Si based MOSLEDs.

4.2.7 Surface roughen enhanced external quantum efficiency

In addition, roughening the top surface of an LED is also one of the efficient methods for increasing the light extraction rate to improve the external quantum efficiency of the LED. For an nc-Si based MOSLEDs, the refractive indexes of nc-Si ($n_{nc\text{-}Si}$) and the air (n_{air}) are 1.8 and 1, respectively. In this case, the critical angle ($\theta_c = \sin^{-1} n_{air}/n_{nc\text{-}Si}$) for the light generated in the active region to escape is about 33.7°. Assuming the output power is uniformly distributed over the whole half-spherical surface, the emitting solid angle of the MOSLED limited by the total internal reflection (Ω_{TIR}) is 0.34π. Only a small fraction of light (about 17%) can escape from the nc-Si based MOSLED even though the refractive index of the top ITO contact layer is nearly the same with the Si-rich SiO_x film to prevent additional reflection. The improvement on light-extraction efficiency of the nc-Si based MOSLED relies on the angular randomization or scrambling of the photons via surface roughening effect. Figure 18 (a) illustrates the possible photon paths at the interface between the nc-Si layer and surrounding air for nc-Si based MOSLEDs without surface roughening. If the top surface of the MOSLED is roughened by

grown the Si-rich SiO_x film on the Si nano-pillar array, the angular randomization of photons can be achieved by surface scattering from the roughened top surface of the MOSLED, as shown in Fig. 18 (b). Such a Si nano-pillar roughened structure essentially results in an enlarged EL power from the nc-Si based MOSLED, as shown in Fig. 17. The comparison on the nc-Si based MOSLED made on Si nano-pillar array and smooth Si substrates under the same biased current of 150 μA clearly shows an increase on output EL power by a 3.8 times. The power enhancing factor of our devices is better than those ever reported on other material based devices. For example, the surface roughening induced power enhancement on GaN- or InGaN-based LEDs of 1.4-3 times were reported by Fujii *et al*. [50] and Huang *et al*.[51] Our experiments concludes that the Si nano-pillar array not only improves the carrier tunneling but also enhances the light extraction in the nc-Si MOSLED.

4.3 Conclusion

In conclusion, anomalous μ-PL characteristics of dense Si nano-pillars fabricating by dry-etching a SiO_2 covered Si substrate with Ni nano-dot mask is investigated. The optimum ICP-RIE recipes for Si nano-pillars with the highest density and aspect-ratio are under a chamber pressure of 0.66 Pa and a RF/Bias power ratio of 0.5. After ICP-RIE for 5 minutes, the obtained density, diameter, and height of the Si nano-pillars are up to 2.8×10^{10} cm^{-2}, 30 nm, and 320 nm, respectively. Both the visible and NIR PLs from the high-aspect-ratio Si nano-pillars were observed. The blue-green PL at around 430 nm is mainly attributed to oxygen-related defects formed on the surface of the Si nano-pillars. The defect-related NIR PL at 703 and 740 nm from Si substrate remain unchanged before and after formatting Si nano-pillars, while a blue-shifted PL phenomenon with its

wavelength decreasing from 874 nm to 826 nm is clearly observed as the Si nano-pillar size shrinks from 7.2 to 6 nm. Such a rod-size dependent PL preliminarily confirms the occurrence of QCE on Si nano-pillars at diameter <7 nm. The nc-Si based MOSLED on Si nano-pillar array is demonstrated. Rapid self-aggregation of Ni nanodots on Si substrate covered with a thin SiO_2 buffered layer is employed as the etching mask for obtaining Si nano-pillar array. Dense Ni nanodots with size and density of 30 nm and 2.8×10^{10} cm^{-2}, respectively, can be formatted after rapid thermal annealing at 850 °C for 22 s. EL spectrum of Si nanocrystals grown on high-aspect-ratio Si nano-pillars is greatly enhanced. The optical intensity, turn-on current and power-current slope of the MOSLED are 140 $\mu W/cm^2$, 5 μA and 2±0.8 mW/A, respectively. The external quantum efficiency of up to 0.1% can be obtained under a power conversion ratio of 5×10^{-5}. One order-of-magnitude improved maximum EL power of 0.7 μW is obtained at biased current of 375 μA. Growth of Si-rich SiO_x layer on the Si nano-pillar array greatly enhances the roughness on top surface and bottom SiO_2/Si interface of the nc-Si MOSLED, which not only releases the total-internal reflection effect but also strengthens the Fowler-Nordheim tunneling effect. The reducing turn-on threshold and enhancing light-scattering performances of the nc-Si based MOSLED made on Si nano-pillar array essentially raises the possibility of its EL power toward μW regime.

Table I Key parameters of the MOSLEDs with interfacial Si nano-pyramids (Si-nps) of different densities.

Parameters	S1	S2	S3
Si-nps Area Density (cm^{-2})	0	10^9	1.6×10^{11}
$E_{F\text{-}N\ threshold}$ (V/cm)	7×10^6	3.2×10^6	1.4×10^6
$V_{turn\text{-}on}$ (V)	187	105	50
$I_{turn\text{-}on}$ (mA/cm^2)	1.5	0.25	0.1
P_{max} (nW)	9	20	150
P-I slope (mA/W)	0.75	3	5.2
$\eta_{external\ efficiency}$ (%)	6.6×10^{-5}	5.8×10^{-4}	2.1×10^{-3}

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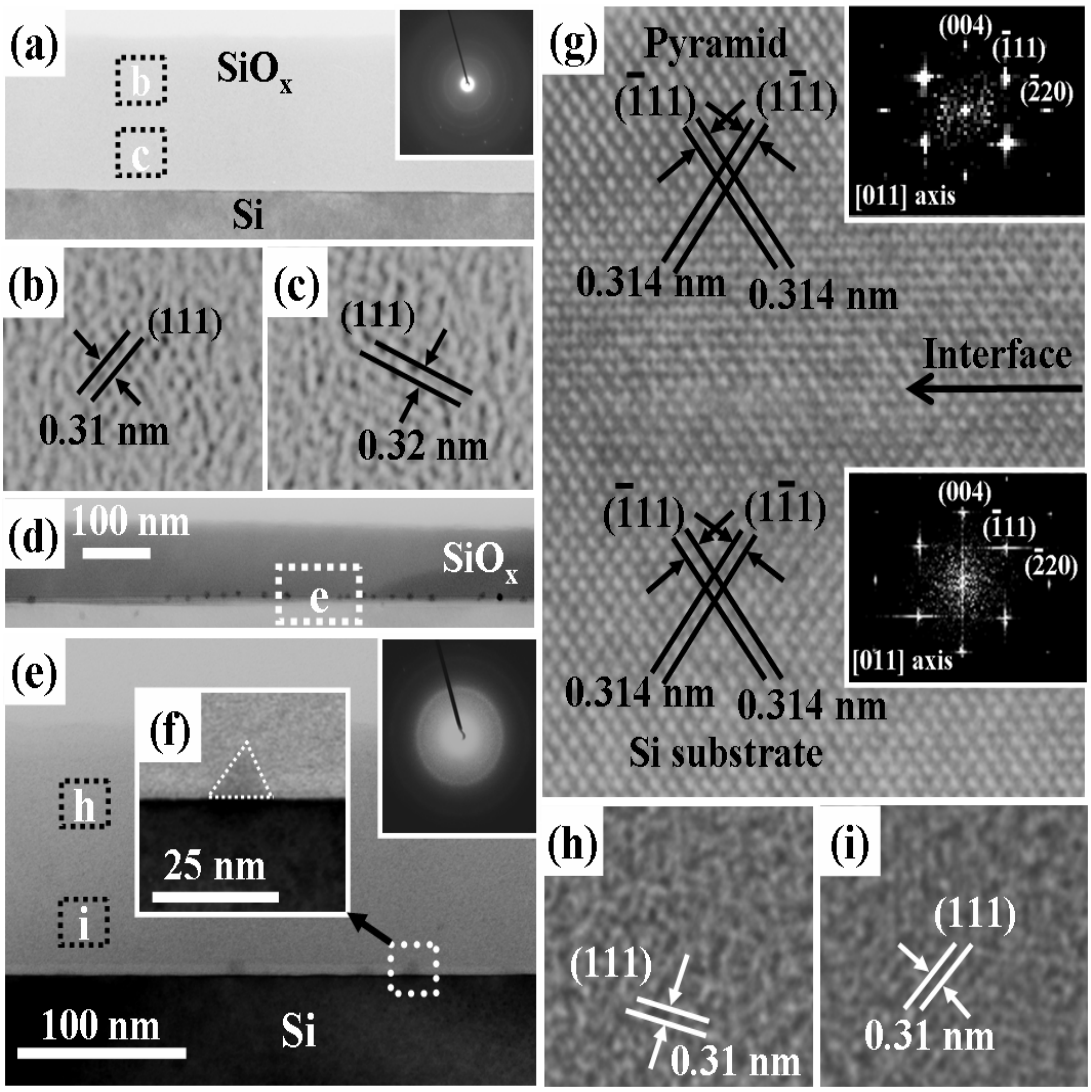

Fig. 1 Cross-sectional HRTEM photographs and corresponding electron diffraction patterns of Si-rich SiO_x grown at ICP powers of 45 (upper left) and 35 (lower left) watts. (a) The cross-sectional TEM photograph of the SiO_x film PECVD grown at normal ICP power. Inset: the electron diffraction pattern of the PECVD-grown SiO_x film. (b) and (c): the lattice parameter and orientation of the Si nanocrystals in PECVD-grown SiO_x film. (d) The cross-sectional TEM photograph of Si-rich SiO_x film with dense interfacial Si nano-pyramids grown at threshold ICP power. (e) The magnified cross-sectional TEM photograph of the Si-nano-pyramid embedded Si-rich SiO_x/Si interface. (f) The magnified TEM photograph for a single Si nano-pyramid and its electron diffraction pattern shown in the inset. (g): The observed orientations for the Si nano-pyramid (upper part) and Si substrate (lower part). (h) and (i): the orientation of the Si nanocrystals in the PECVD-grown Si-rich SiO_x film at threshold ICP-power condition.

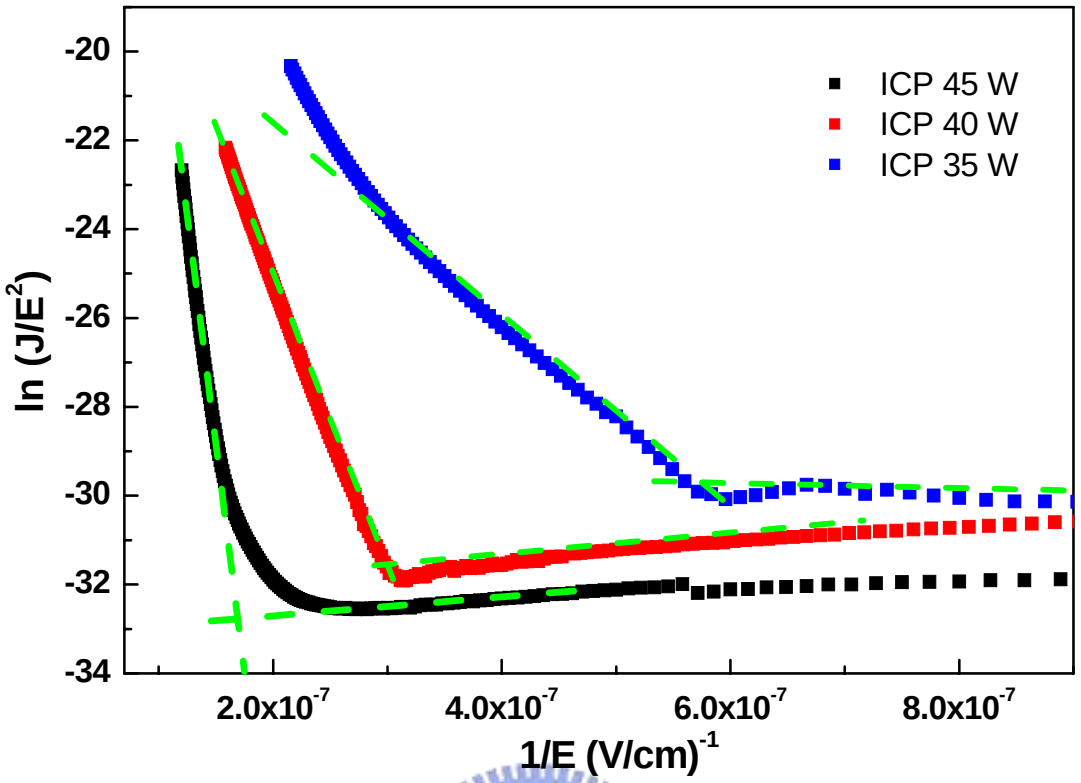

Fig. 2 The plots of $\ln(I/E^2)$ as a function of $1/E$ for three MOSLED samples with their SiO_x films PECVD grown at different ICP powers.

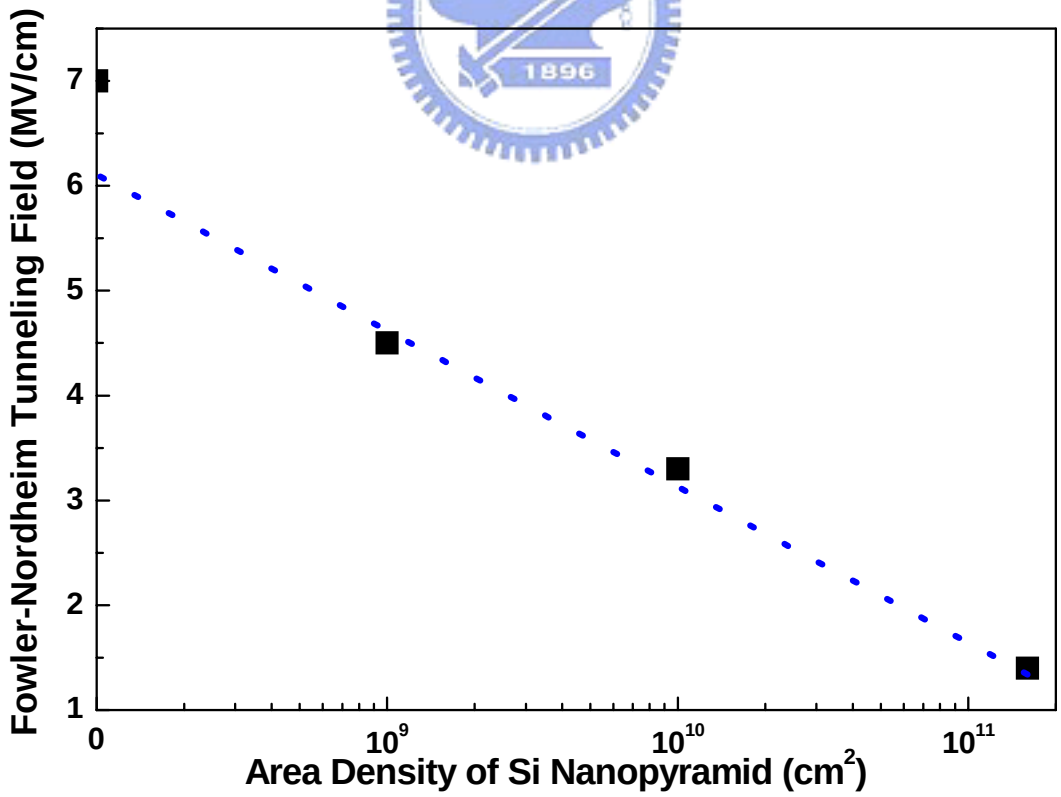

Fig. 3 Threshold F-N tunneling electric field as a function of the area density of Si nano-pyramids.

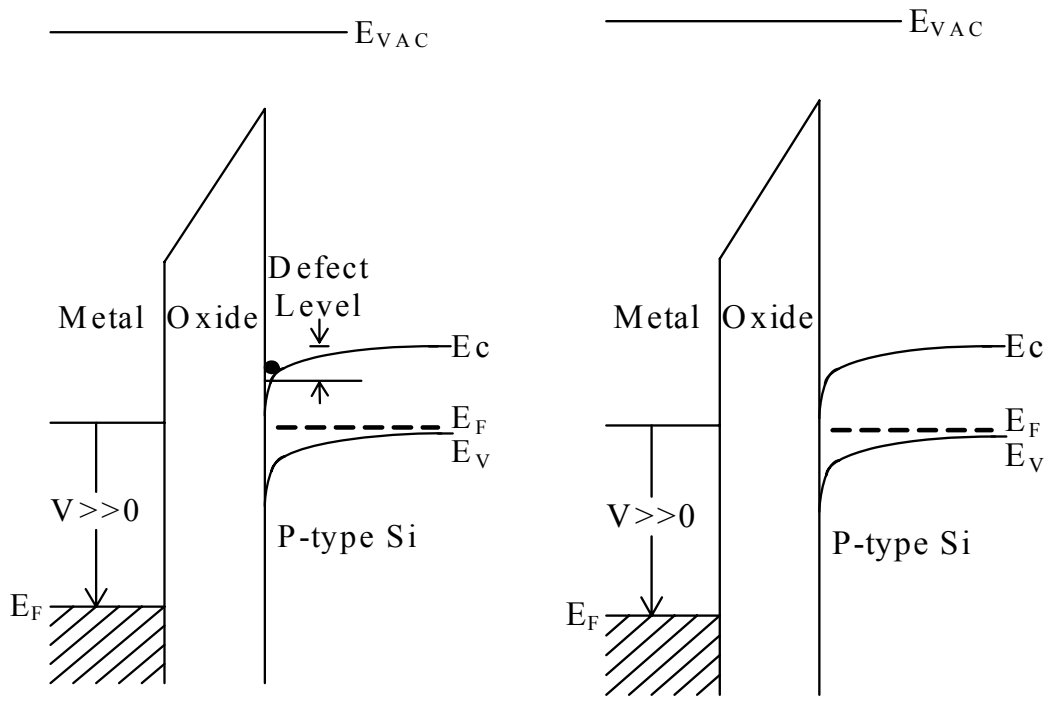

Fig. 4 The energy band diagrams of a highly biased MOSLEDs using SiO_x grown at different PECVD conditions. Left: the SiO_x grown at normal ICP power without Si nano-pyramids but with dense interfacial radiant defects. Right: the SiO_x grown at threshold ICP power with Si nano-pyramids at the SiO_x/Si interface.

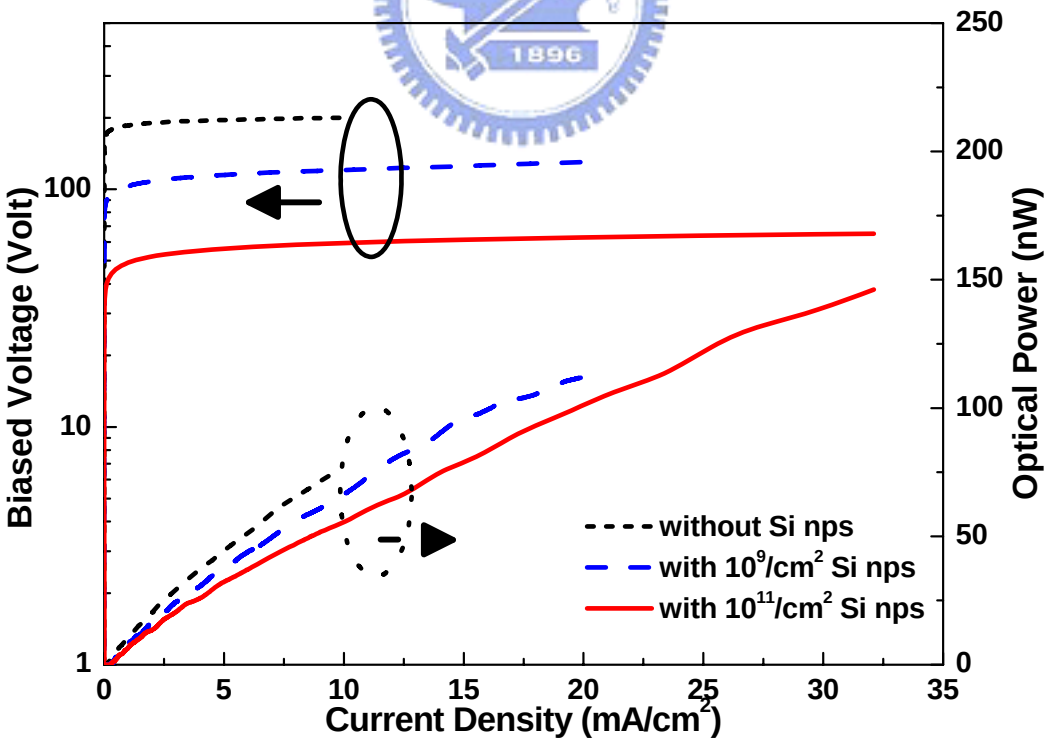

Fig. 5 The I-V and I-P curves of the ITO/SiO_x/p-Si/Al MOSLEDs with SiO_x films grown at different ICP powers. Upper: ICP power of 45 W. Middle: ICP power of 40 W. Lower: ICP power of 30 W.

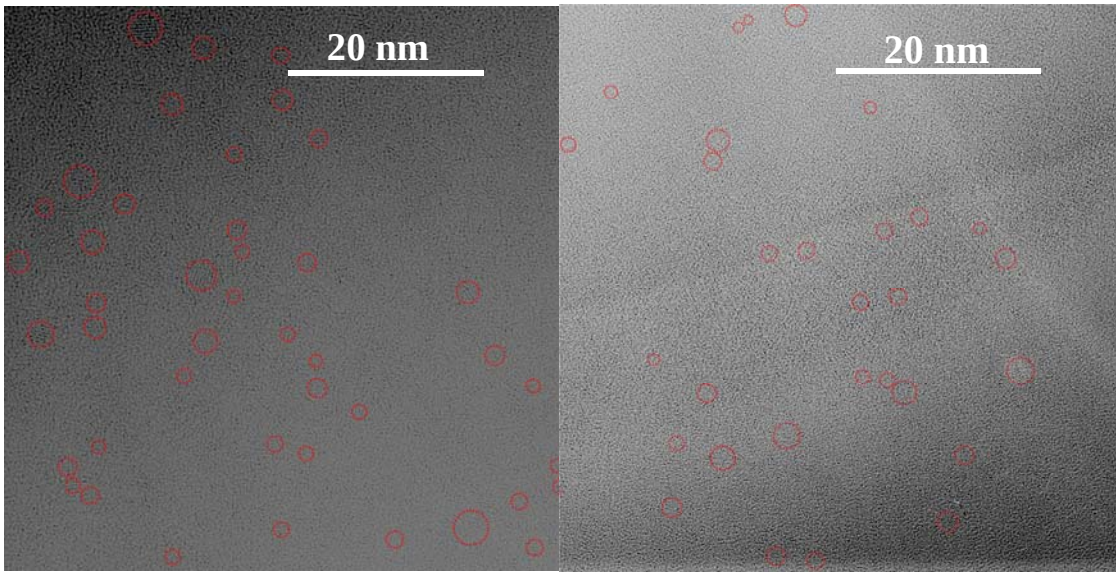

Fig. 6 TEM images of nc-Si within the annealed SiO_x film grown without (left) and with (right) interfacial Si nano-pyramids.

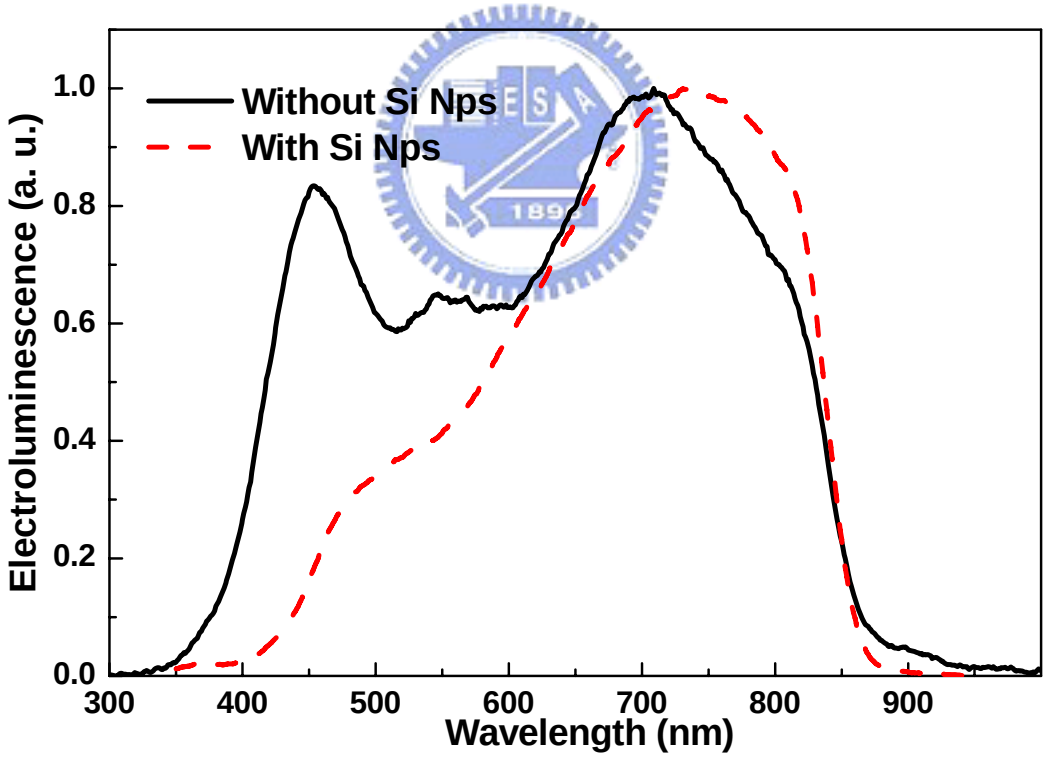

Fig. 7 EL spectra of ITO/SiO_x/p-Si/Al MOSLEDs with (solid) or without (dashed) interfacial Si nano-pyramids.

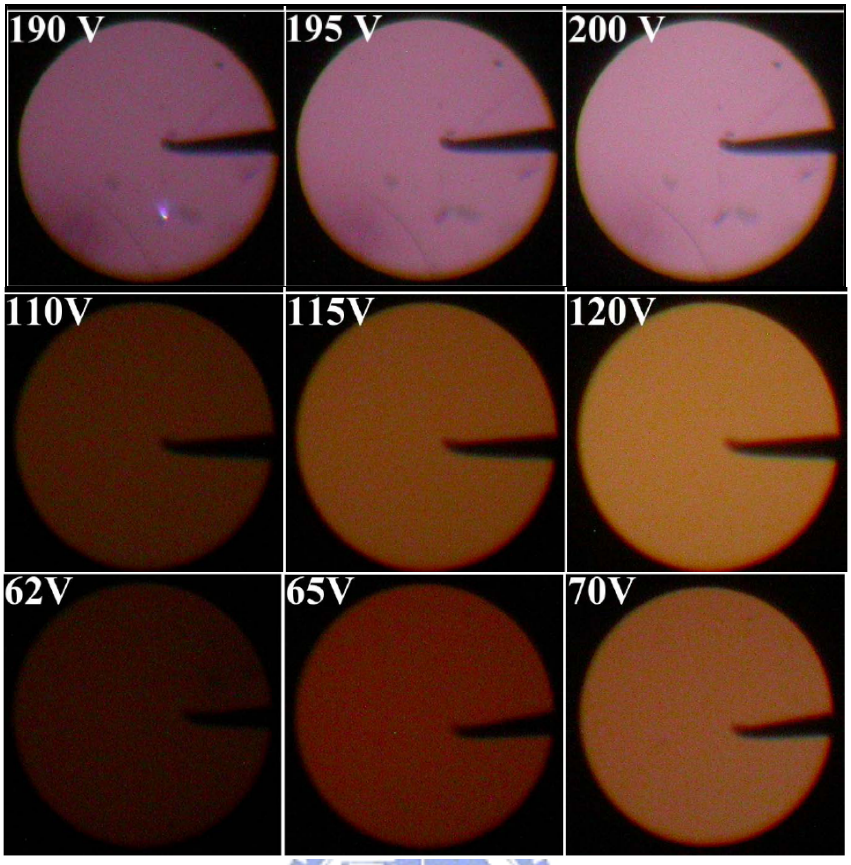

Fig. 8 EL patterns of three MOSLED samples without (upper) and with Si-nano-pyramid concentrations of $\rho=10^{9}/cm^{2}$ (middle) and $\rho=10^{11}/cm^{2}$ (lower).

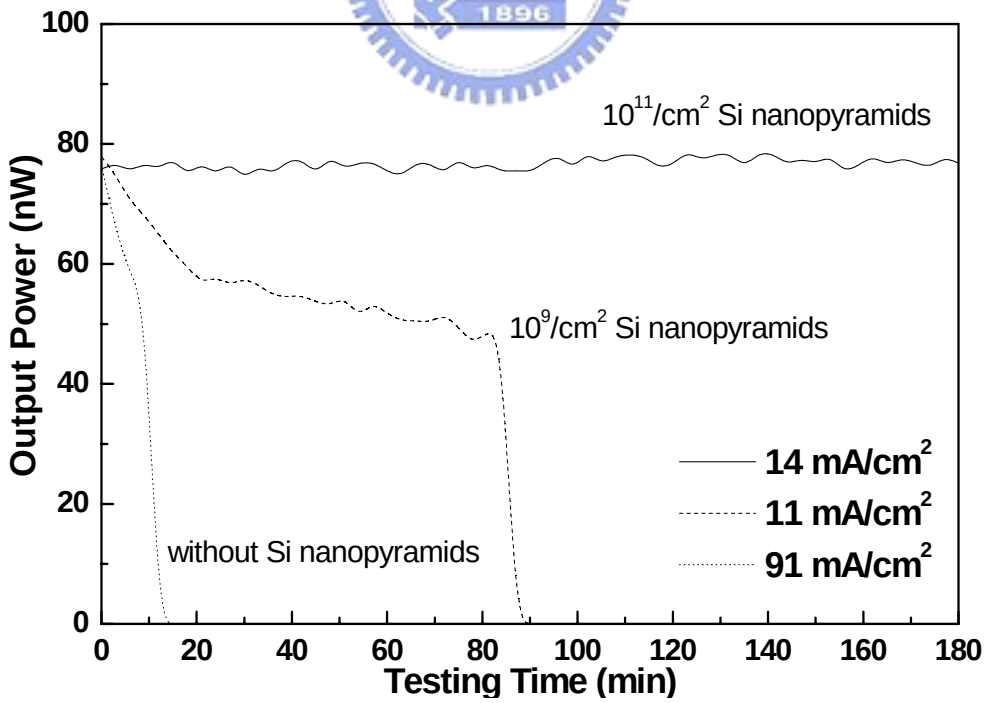

Fig. 9 Output power stability of three MOSLED samples with different Si-nano-pyramid concentrations.

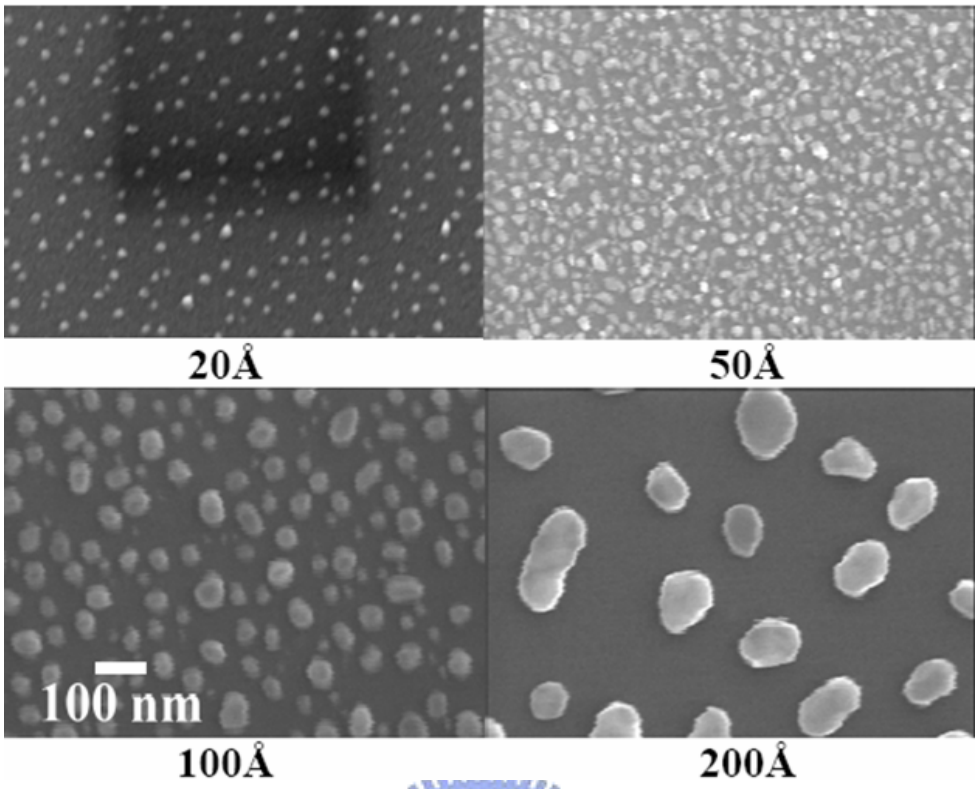

Fig. 10 SEM image of Ni nano-dots precipitated from the evaporated Ni film on SiO_2/Si with different film thickness.

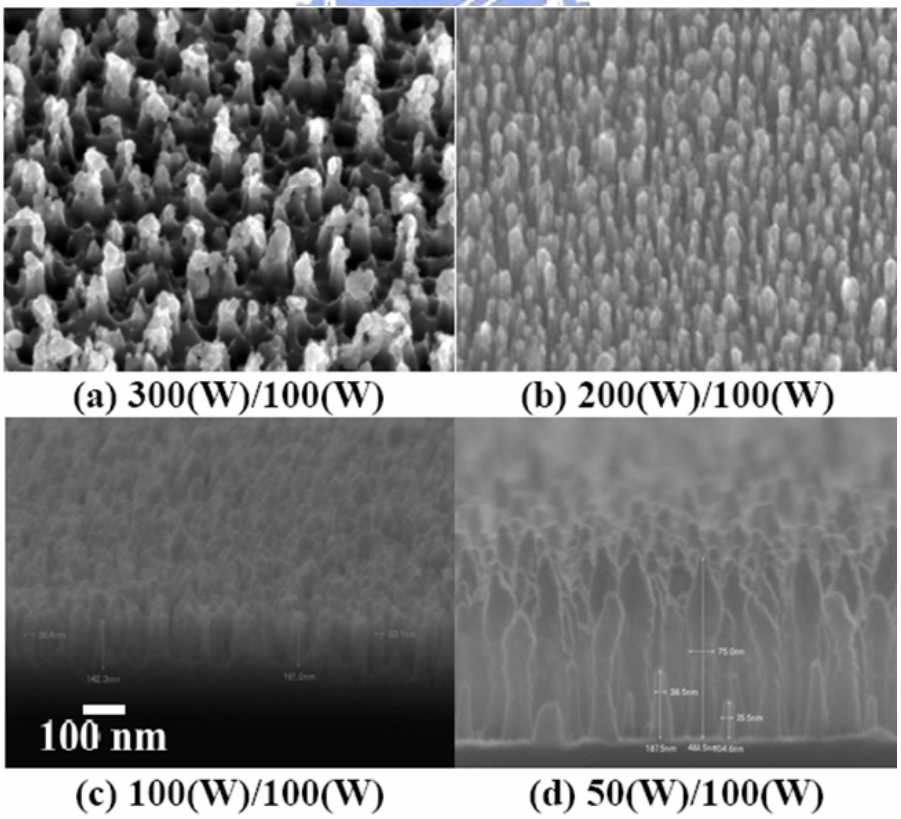

Fig. 11 SEM image of Si nano-pillars formed after ICP-RIE with different RF/Bias power recipes.

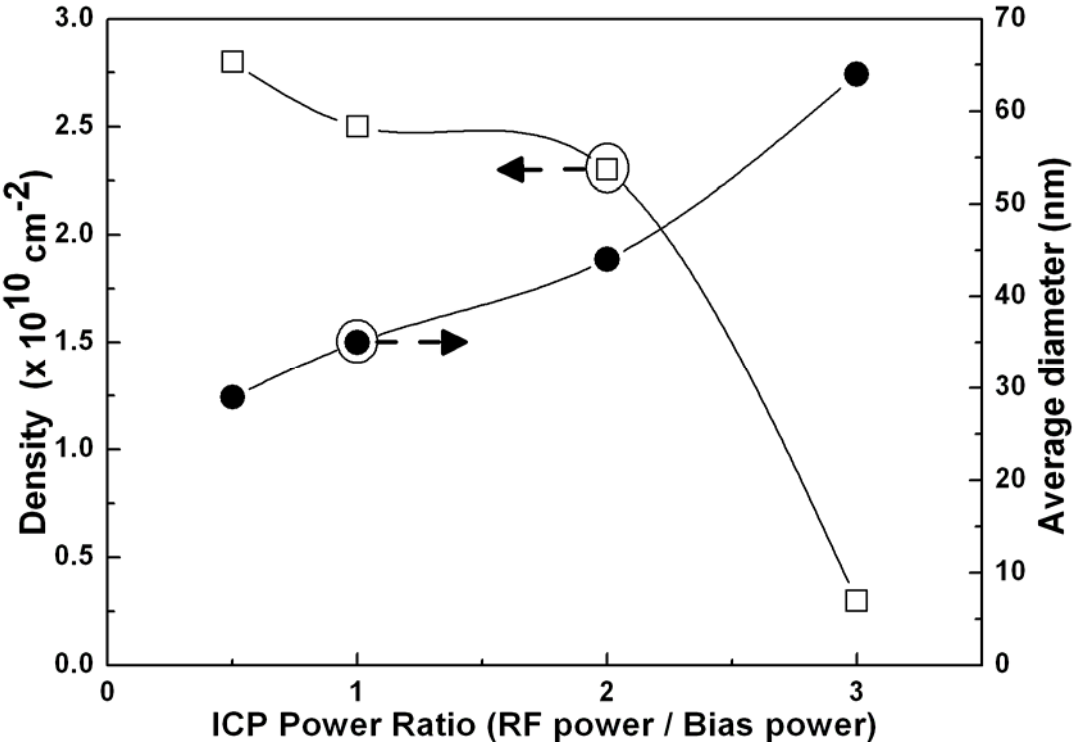

Fig. 12 Density and average diameter of Si nano-pillars on Si substrate as a function of RF/Bias power ratio in ICP-RIE system

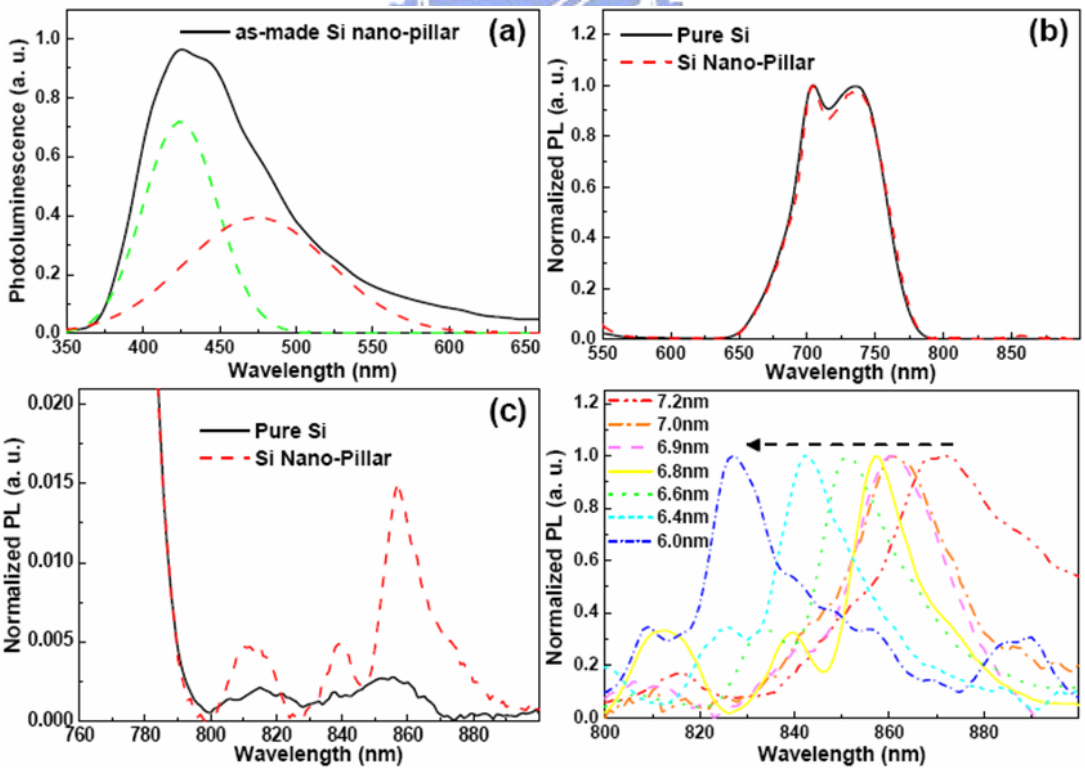

Fig. 13 (a) Micro-PL spectrum of as-made Si nano-pillar array. (b) Normalized PL spectra of unprocessed pure Si wafer and etched Si nano-pillar. (c) Si nano-pillar related PL and pure Si PL spectrum. (d) PL spectra of etched Si nano-pillars.

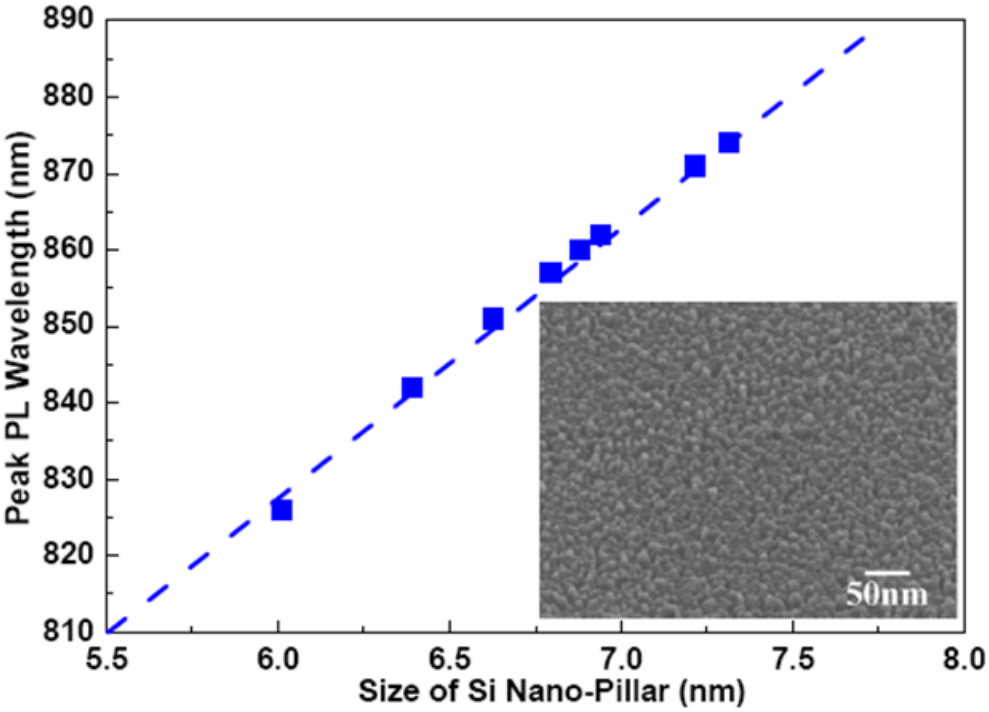

Fig. 14 Peak wavelength of Si nano-pillar as a function of rod size. Inset: Plan-view SEM picture of etched Si nano-pillars.

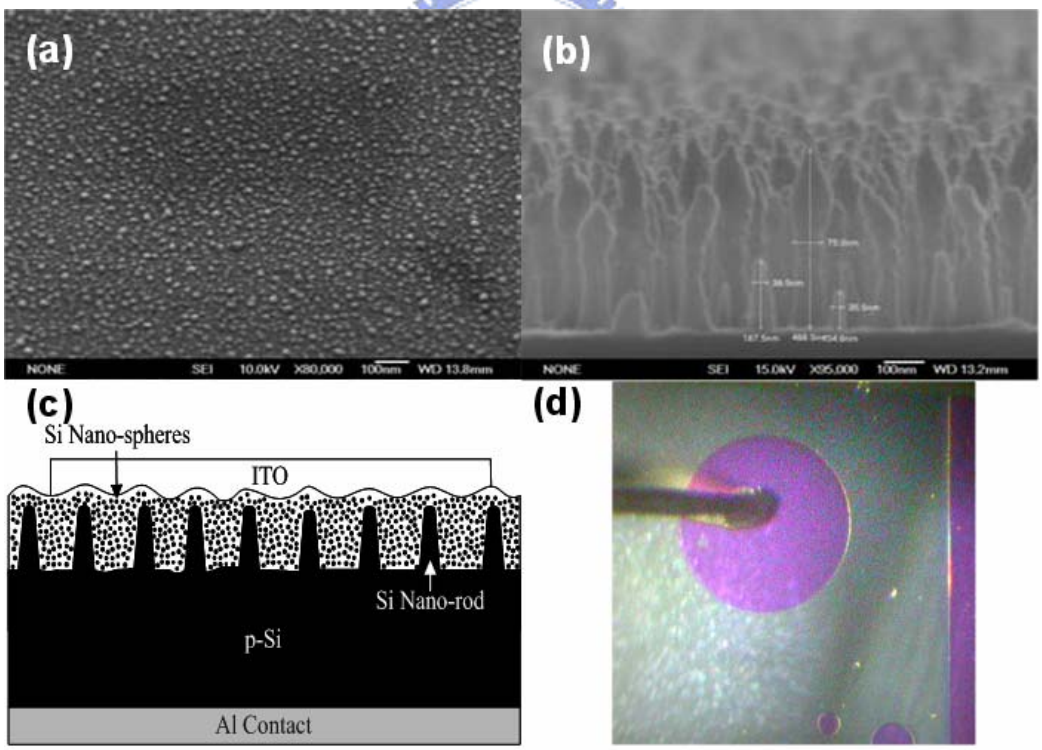

Fig. 15 (a) SEM image of Ni nano-dots precipitated from the evaporated Ni film on SiO_2/Si. (b) SEM image of Si nano-pillars formed after ICP-RIE with RF/Bias power recipe of 50/100W. (c) Device structure of a silicon nanocrystal based MOSLED on Si nano-pillar array. (d) An ITO/SiO_x/Si/Al diode with a circular contact diameter of 0.8 mm.

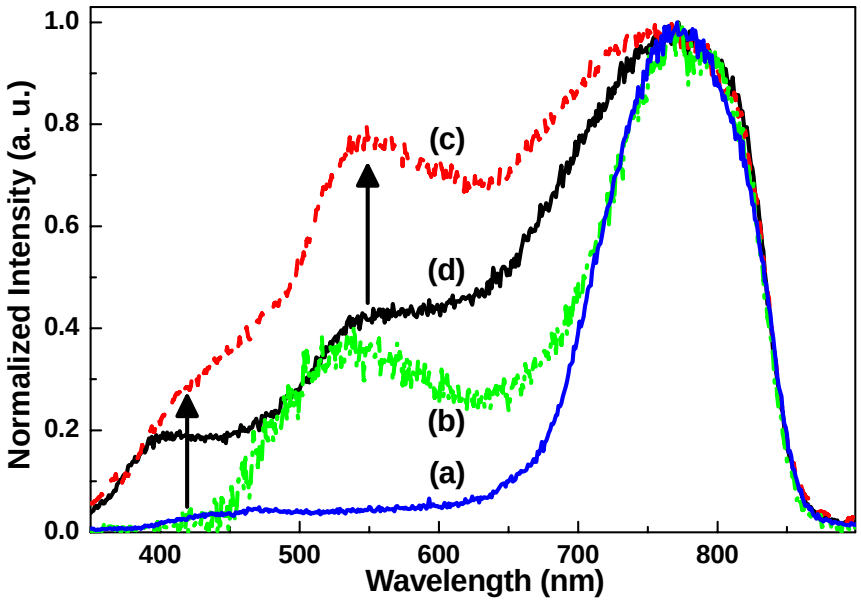

Fig. 16 Normalized PL spectra of nc-Si based MOSLEDs (a) without and (b)with Si nano-pillars. Normalized EL spectra of nc-Si based MOSLEDs (c) with and (d) without Si nano-pillars.

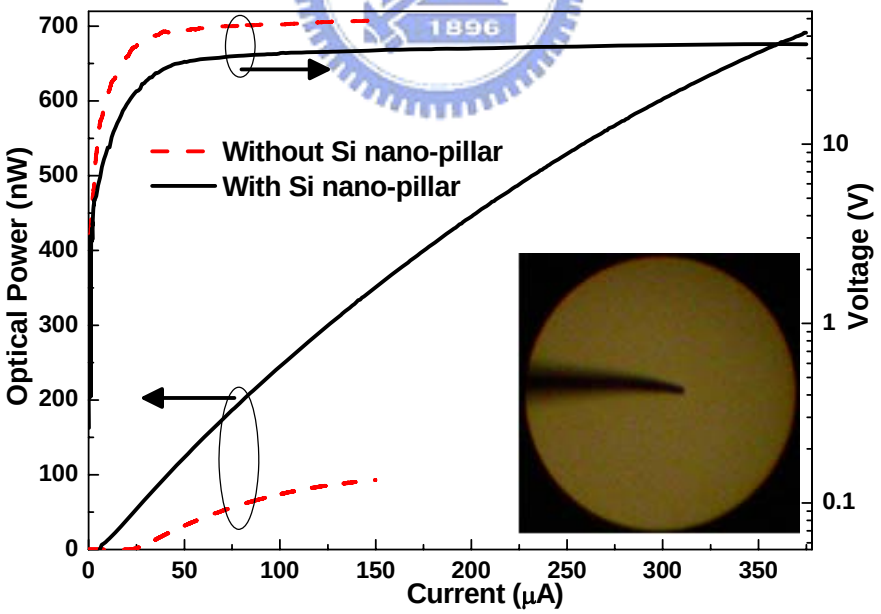

Fig. 17 I-V and I-P curves of nc-Si based MOSLEDs with/without Si nano-pillars. Inset: EL pattern of nc-Si based MOSLED with Si nano-pillars.

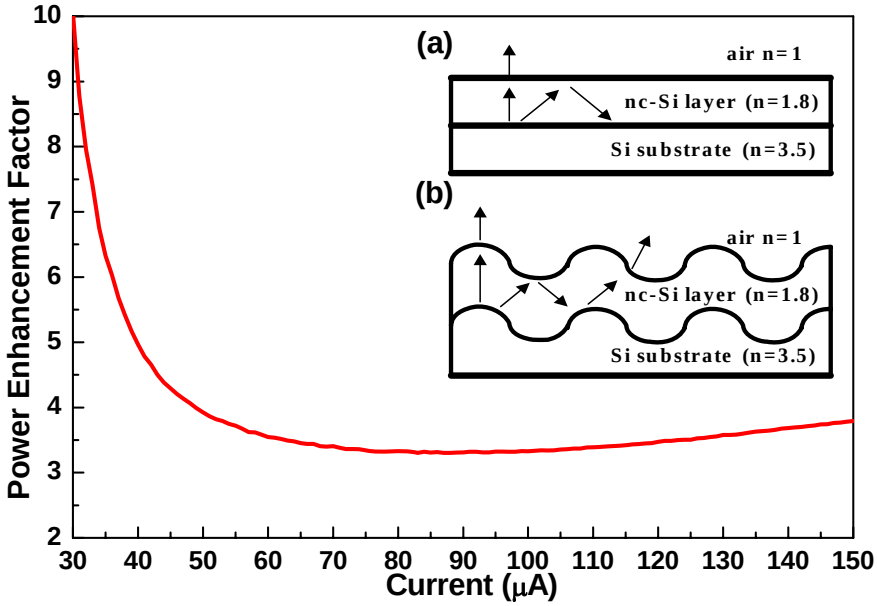

Fig. 18 The ratio of the EL power from nc-Si MOSLED made on Si nano-pillar to that made on smooth Si wafer at different biased current.