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Using electroless plating Cu technology for TFT-LCD application

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ABSTRACT

This study investigates the feasibility of using electroless plating (ELP) technology to manufacture copper (Cu) gate electrodes in thin film transistors (TFTs). The problem of poor adhesion between Cu and glass substrates is overcome by introducing ELP nickel–phosphorus (NiP) layers. Copper pattern formation with a desired taper can be self-aligned subsequently on a NiP layer without any layer etching process. ELP Cu film shows an obvious (111) preferred orientation, which may enhance the electrode's anti-electromigration ability. The electrical characteristics of the ELP Cu gate TFT are also similar to those of the sputter-deposited Cu gate TFT.

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1. Introduction

In a thin film transistor liquid crystal display (TFT-LCD), a typical pixel circuit consists of a TFT backplane with cross interconnects of row (scan) and column (data) electrode lines. The row and data electrode lines can be modeled as a distributed resistance-capacitance network. As TFT-LCD panels become larger and provide higher resolution, it is becoming increasingly difficult to achieve uniform image display because of the induced signal propagation delay time from the row and column lines [1,2]. Replacing high-resistivity metallic alloys with other low resistivity alloys is an effective solution to the propagation delay problem. Copper (Cu), which has a resistivity below 3 μΩ cm, is a promising candidate for the interconnection material in TFT-LCD applications. However, Cu TFT technology contains several process issues, including poor adhesion with the glass substrates and the challenge of using the etching process to form tapered gate electrodes with a desired taper angle [3]. Many previous documents reported that buffer layers like Mo, Co, or Mg deposited by sputtering or chemical vapor deposition (CVD) can resolve the adhesion issue [3,4]. These proposed methods all require high-cost equipments with vacuum systems and gas pipes. Cu electroplating (EP) and electroless plating (ELP) technologies have been attractive because of the ease of the process and no need for vacuum systems. Nevertheless, EP technology has a limit on the application for large-scale TFT-LCD displays due to the non-uniform current distribution while electrochemically depositing the Cu film [5,6]. In contrast with EP Cu, the ELP Cu technology has received much more attention due to its several desired features such as film deposition uniformity, no electric power and low-cost process [7–9]. To date, although previous studies have examined the ELP Cu technology for Cu gate TFT applications, the Cu patterns are still formed by chemical etchants [10]. Therefore, this study demonstrates the feasibility of ELP Cu/NiP technology to manufacture Cu gate TFT device without the etch process of copper film. The issues regarding the film adhesion and the challenge to form taper Cu electrode are also addressed in this work. Furthermore, the electrical characteristics of ELP Cu gate TFT devices were compared with the sputter-deposited Cu gate TFT devices.

2. Experimental details

Fig. 1 depicts the ELP Cu/NiP deposition processes for Cu gate TFTs. After cleaning the glass substrate surface, the base surface was sensitized using a mixture of 20 g/L of $SnCl_2$ in 5 vol.% HCl and 1 g/L of $PdCl_2$ in 0.25% HCl solutions for 210 sec. An ultra-thin palladium (Pd) layer was deposited on the surface by the following chemical reaction:

$$Sn^{2+} + Pd^{2+} \Rightarrow Sn^{4+} + Pd \quad (1)$$

A surface activation process using an aqueous solution of NaH_2PO_2 for 30 s was critical to obtain the desired NiP deposition after the reaction in Eq. (1). This activation step reduced the oxidative Sn^{4+} on the surface, and promoted reductive NiP deposition. A NiP film was then formed with a mixture of $NiSO_4$, and NaH_2PO_2 precursors as a source of Ni, and P, respectively. The NaH_2PO_2 worked as a reducing agent. Tri-sodium citrate and $(NH_4)_2SO_4$ were also added as a complex formation agent and pH buffer, respectively. A 50 nm-thick ELP NiP layer formed after 1 min, and this layer served as an adhesion promotion layer. After the NiP layer was patterned by wet etching, samples were catalyzed by being immersed into AgNO3 in NH4OH to make ultra-thin silver on NiP

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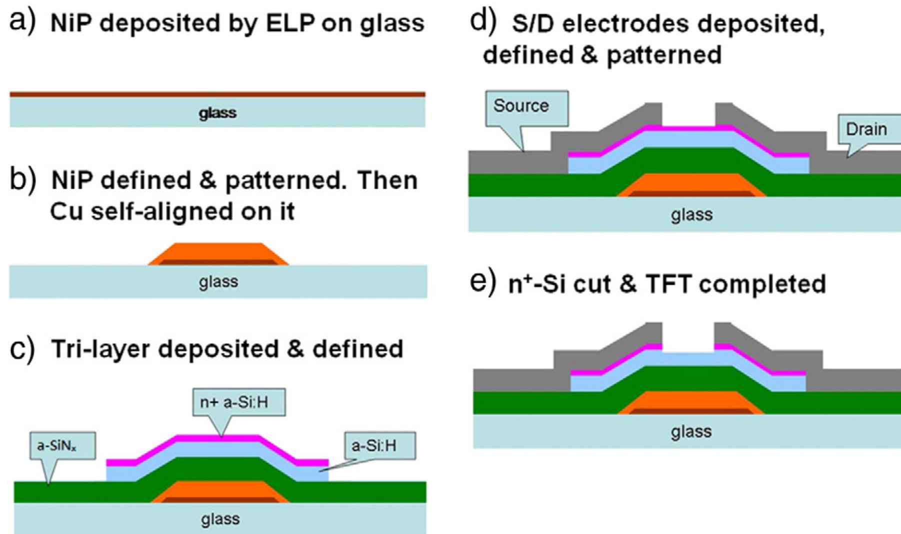

Fig. 1. Process flow of an ELP Cu Gate TFT with a back-channel-etched (BCE) inverted-staggered TFT structure.

surface which served as the self-assemble monolayer (SAM). The step is carried out for 10 s and was beneficial for the sequential Cu film deposition. Finally, samples were immersed into a chemical solution of 7.5 g/L of $CuSO_4$ as a Cu source. This step formed a 250 nm-thick ELP Cu gate electrode with the desired taper shape on the NiP film, which may presumably be related to the structures of SAM adsorbed obliquely toward NiP surface on the corner of pattern [11,12]. The details of this ELP Cu/NiP formation process were reported in our previous work [13,14] and detailed mechanism of SAMs on the tapered pattern shape will be discussed further in our next study work. Hydrogenated amorphous silicon (a-Si:H) TFT devices were fabricated by a tri-layer deposition process involving a 380 nm-thick silicon–nitride (SiNx), a 150 nm-thick a-Si:H active film, and a 30 nm-thick n+-a-Si:H layer. As for silicon–nitride (SiNx), the ratio of SiH_4/NH_3 was 0.12 and the NH_3 flow was 7800 sccm. These layers were formed on the ELP Cu/NiP gate using plasma enhanced chemical vapor deposition (PECVD). The deposition RF power was 650 W and deposition temperature at 300 °C. The deposition rate is about 0.64 nm/s. After the channel layers were formed islands, an alumina (Al) layer was deposited by a thermal coater and patterned using a wet etching process to form source/drain electrodes. Finally, the n+-a-Si:H layers on the back-channel region of the TFT were etched off using the source/drain pattern electrodes as an etching mask. For comparison, an a-Si:H TFT device with a sputter-deposited Cu gate (250 nm) on ELP NiP layer (50 nm) acting as control sample was also fabricated by using DC sputter system with a 4N purity copper target. The sputtering power is 150 W at a pressure of 3×10^{-3} Torr with an argon (Ar) flow rate of 24 sccm. The total thickness of ELP Cu/ELP Ni layers or sputter-deposited Cu/ELP Ni layers were all fixed at 300 nm. Sample preparation for X-ray diffraction (XRD, Bede, D1, 2Theta scanning mode), field-emission scanning electron microscope (FESEM, JOEL 7000F operated at 15.0 kV) and tapping-mode atomic force microscope (AFM) analyses were schematically sketched in the inset of Fig. 2. Both ELP Cu and sputter-deposited Cu were formed on glass substrate with 50 nm-thick ELP NiP on it. The grazing incidence of XRD was 3°. The wavelength of the XRD was 0.154 nm. The scanning size of our specimen for AFM measurement was about 1 μm × 1 μm square. Electrical characteristics were measured using a Keithley 4200 semiconductor parameter analyzer. Both the channel width (W) and length (L) of the TFT device was all fixed at 40 μm, so that the ratio of W/L was equal to 1. A constant 35 V gate voltage was applied to the Cu gate a-Si:H TFT devices at room temperature and 60 °C, respectively, for 180 min in the dark, to investigate the effect of Cu diffusion on device electrical characteristics.

3. Results and discussion

The roughness of ELP Cu measured by atomic force microscope (AFM) was about 17.6 nm after deposition process and 17.0 after 300 °C annealing in vacuum environment. The annealing process for ELP Cu film was used to simulate the case of ELP Cu film during sequential manufacture. The ELP Cu film in this work showed a low resistivity of approximately 2.6 μΩ cm measured by the four-point probe method. This performance is quite good for gate electrode applications, and especially compared with the typical AlNd alloy gates (4~5 μΩ cm) in current TFT-LCD displays. Fig. 2 shows the X-ray diffraction (XRD) results of the as-deposited ELP Cu and the sputter-deposited Cu on ELP NiP films. The inset of Fig. 2 presents a schematic sketch of Cu and NiP film structures. The main diffraction peaks (2θ) of both the ELP and the sputter-deposited Cu were approximately 43.4 and 50.6, referring to the (111) and (200) orientation directions for copper film [4]. The relative intensity of the (111) peak to the (200) peak was used to gauge the degree of preferred crystal orientation in the Cu thin film. The ratio of related peak intensity of I(111)/I(200) was 4.5 in the ELP Cu film and 2.5 in the sputter-deposited Cu film, respectively, indicating that the ELP Cu film had a greater preference for the (111) direction than the sputter-deposited Cu. Electrons experienced less resistance flowing in the (111) directions than in

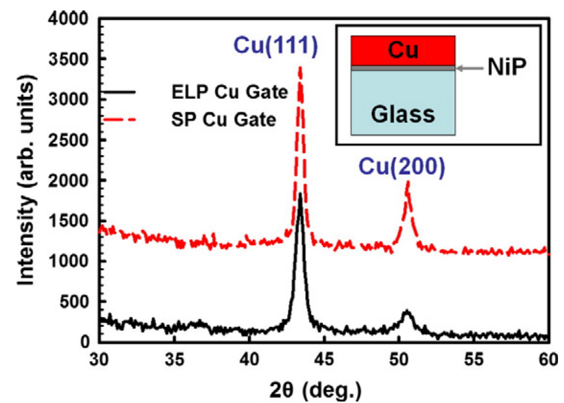

Fig. 2. XRD patterns of ELP Cu/NiP and sputter-deposited Cu on ELP NiP films. The inset indicates the sample structure. The main diffraction peaks (2θ) of both samples were around 43.4° and 50.6°, which were referred to the (111) and (200) orientation directions for copper film. The ratio of related peak intensity of $I_{(111)}/I_{(200)}$ was 4.5 in the ELP Cu film and 2.5 in the sputter-deposited Cu film.

other directions [15,16]. Therefore, the (111) direction may offer the best anti-electromigration performance inside a Cu grain. Based on these XRD results, the ELP Cu film might possess better anti-electromigration performance than the sputter-deposited films.

Fig. 3(a) and (b) present a scanning electron microscope (SEM) image of the interface between ELP Cu/NiP film and cross section view of the ELP Cu/NiP gate electrode in TFT. In Fig. 3(a) it was clearly observed the thickness of ELP NiP and Cu were about 50 nm and 250 nm, respectively. As for Fig. 3(b), the Cu etch process was not necessary, as the Cu film was self-aligned on the patterned NiP layer. Furthermore, the Cu electrode shape revealed the desired taper angle (50°) for TFT device manufacturing. Suitable tape angles between 45° and 70° contribute to the improvement of thin film step coverage and prevent pinhole formation through the gate insulators [5]. These SEM results show the compatibility of the proposed self-aligned ELP Cu technology with TFT fabrication. The transfer characteristics of a-Si:H TFT with a ELP Cu gate and a sputter-deposited Cu gate are shown in Fig. 4, which were measured at drain voltages (V_D) of 1 and 10 V, respectively. The proposed TFT with ELP Cu gate demonstrated a field-effect mobility of 0.57 cm^2/Vs, a subthreshold slope (S.S) of 0.9 V/dec, a threshold voltage (V_{th}) of 4.55 V, and the I_{ON}/I_{OFF} ratio of 10^7 extracted from the saturation I_D–V_G plot, where V_D = 10 V. The ELP Cu

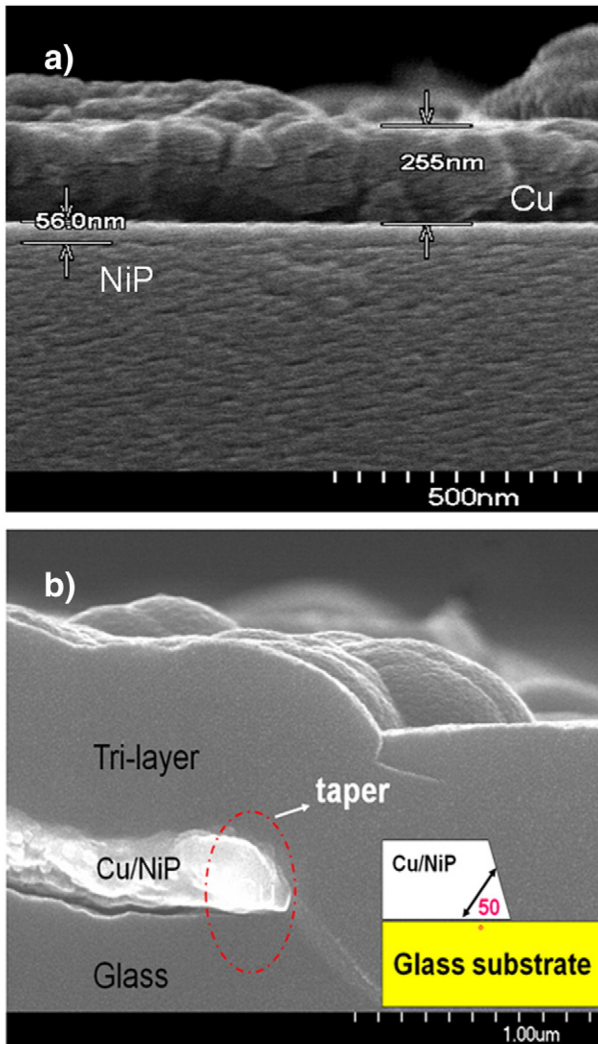

Fig. 3. (a) The cross section view of ELP NiP/Cu. The thickness and interface between ELP NiP and Cu can be obviously observed. (b)The SEM image of a self-aligned ELP Cu gate electrode on the NiP layer with top tri-layers of SiNx/a-Si:H/n^+-a-Si:H dielectrics. The taper angle of the self-aligned Cu film was about 50°, which is suitable for the TFT manufacturing process.

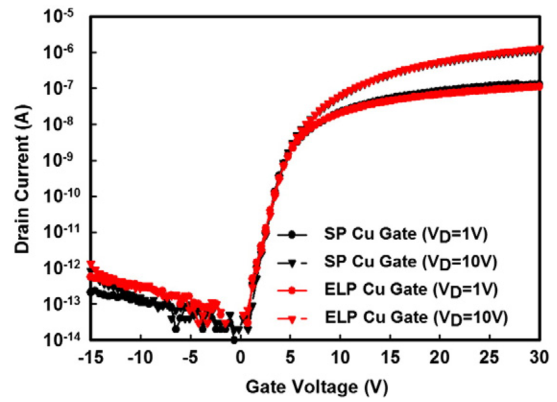

Fig. 4. Transfer characteristics of the sputter-deposited Cu gate TFT (called the SP Cu Gate) and ELP Cu gate TFT (called the ELP Cu Gate). The inset indicates the electrical parameters, which were extracted from the saturation region at V_D = 10 V. Nearly the same electrical performance was observed for both ELP Cu gate and sputter-deposited Cu gate TFTs.

gate TFT and the sputter-deposited Cu gate TFT have similar electrical characteristics, indicating the feasibility of the proposed approach for TFT fabrication (Table 1). The gate leakage current through the gate insulator was less than 10^{-13} A. This low gate leakage current was attributed to the superior formation of the Cu gate electrode with the desired taper angle, and no apparent hillocks.

Cu plays a deep level acceptor role in silicon based material. The presence of Cu ions inside the dielectric will cause excessive leakage currents between gate electrodes and source/drain electrodes. Therefore, Cu gate electrodes and dielectric will be needed to ensure that whether Cu diffuse in dielectric layer or not. In order to investigate the positively charged Cu ions diffusion through dielectrics, TFTs with ELP and sputter-deposited (SP) gate were applied by positive gate bias stress. Fig. 5(a) presents the V_{th} shifts (ΔV_{th}) of a-Si:H TFT with an ELP Cu gate and a SP Cu gate after gate bias stress. Two main physical mechanisms were reported for the V_{th} shift of a-Si:H TFTs caused by DC gate bias stress. One is carrier trapping in the gate insulator, and the other is point defect creation in the a-Si:H layer or at the a-Si:H/a-SiNx interface. [17–19] The defect creation also will increase the density of deep-gap states. Charge trapping was associated with a logarithmic time dependence, which can be represented as follows:

$$\Delta V_{th}(t) = r_d \log(1 + t / t_0) \quad (2)$$

where r_d is a constant and t_0 is some characteristic value for time. In contrast, defect state creation was characterized by a power law dependence of ΔV_{th} over time. The complete relationship is mapped as followed:

$$\Delta V_{th}(t) = A(V_{ST} - V_{TI})^{\alpha} t^{\beta} \quad (3)$$

where VST is the applied gate bias stress, V_{TI} is the initial threshold voltage, and β is the stretched-exponential exponent which is temperature dependent and α is the power factor of ΔV_{th} and stress time taken on a value of unity and A is a constant. For most cases, the degradation mechanism of a-Si:H TFT includes both effects of defect station creation and carrier trapping. By characterizing the dependence between extracted V_{th} and stressing time, the domination effects of defect station creation or carrier trapping can be

Table 1
The electrical performance comparison of TFT with SP Cu and TFT with ELP Cu.

	V_{th} (V)	S.S (V/decade)	μ(cm^2N s)
TFT with SP Cu	4.44	0.96	0.56
TFT with ELP Cu	4.55	0.90	0.57

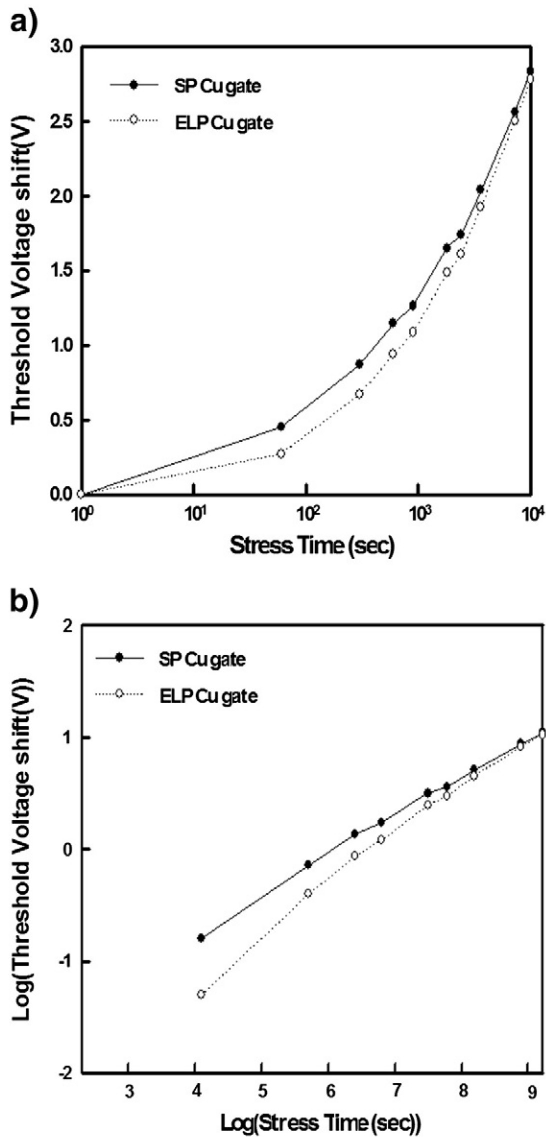

Fig. 5. (a) The threshold voltage shifts as a function of stress time for the sputter-deposited Cu gate TFT and ELP Cu gate TFT stressed at a gate voltage of 35 V for 3 h at room temperature. (b) V_{th} shifts as a function of stress time in logarithm relation, clearly showing a power law relationship.

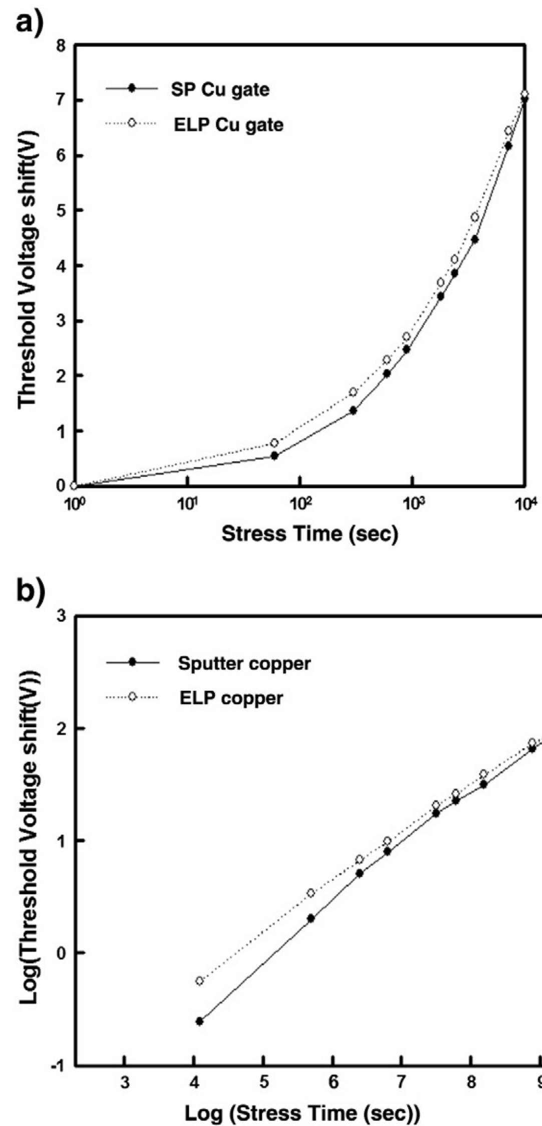

Fig. 6. (a) The threshold voltage shifts as a function of stress time for the sputter-deposited Cu gate TFT and ELP Cu gate TFT stressed at a gate voltage of 35 V for 3 h at 60 °C. (b) V_{th} shifts as a function of stress time in logarithm relation, clearly showing a power law relationship.

distinguished. However, even the domination one can be told from electrical analysis, both factors of defect station creation or carrier trapping still existed in stress experiments. In order to confirm the dominant mechanism for the electrical reliability of Cu gated a-Si TFTs, the relationship between V_{th} shift and stress time is studied and plotted in logarithm as shown in Fig. 5(b). It is clearly observed that a linear relationship between ΔV_{th} and (V_{ST}–V_{Ti}) while ΔV_{th} has a power dependence on bias stress time following Eq. (3) (defect state creation) instead of Eq. (2) (Charge trapping, fitting not shown here). The similar trend of V_{th} shifts after gate bias stress at room temperature were also observed for both of ELP Cu and SP Cu gate TFTs, as shown in Fig. 5(a) and (b). Previous studies on the sputter-deposited Cu gate TFT after bias temperature stress (BTS) reported that no Cu diffusion issue occurred, while using PECVD SiN_x layer as gate insulator. This means PECVD SiNx has great potential for diffusion barrier against Cu penetration [4,20]. In this study, both effects of defect station creation and carrier trapping did result in the electrical degradation of gate bias stressed TFT devices. The similar results on the V_{th} shift of TFTs with SP Cu gate and ELP Cu gate can support that there were no copper diffusion happening for ELP Cu gate TFT. As shown in Fig. 6(a), there were still no Cu diffusion observed, even the ELP Cu gate TFT under BTS test at 60 °C. The linear relationship of V_{th} shifts and stress time also indicates defect state creation is the dominant mechanism for the device behavior after BTS stress, as shown in Fig 6(b).

4. Conclusion

In summary, a-Si:H TFT with self-aligned ELP Cu gate was developed for TFT-LCD applications. The ELP NiP film acted as a buffer layer, promoting adhesion between the Cu film and the glass substrate. In addition, XRD results indicate that the ELP Cu film exhibited better anti-electromigration than sputter-deposited Cu film due to a high intensity ratio of orientation (111) to (200). SEM images indicate the formations of self-aligned ELP Cu electrodes with a desired taper angle on the bottom ELP NiP layer without Cu etching. These tapered Cu electrodes improve the step coverage of sequential film deposition and help form hillock-free dielectric films. The resulting ELP Cu gate TFT also exhibited low gate leakage. The electrical characteristics were similar to those of a TFT based on a

typically sputter-deposited Cu gate. Finally, the bias temperature stress method was used to confirm that copper diffusion issues will not appear at the ELP Cu gate TFT. This shows that the proposed a-Si:H TFT with self-aligned taper copper gate technology has great potential for the TFT-LCD applications.

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