Trigated Poly-Si Nanowire SONOS Devices for Flat-Panel Applications

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***Abstract*—A new method is proposed and demonstrated to fabricate planar thin-film transistors and trigated nanowire (NW) devices simultaneously on the same panel. By using an oxide–nitride–oxide stack as the gate dielectric, the NW devices could also serve as nonvolatile Si–oxide–nitride–oxide–Si (SONOS) memory devices. Our results indicate that the combination of trigate and NW channels help to improve the device performance in terms of steppers subthreshold swing and reduced threshold voltage. Improvement in programming and erasing efficiency of the nonvolatile SONOS memory devices is also demonstrated with the trigated NW structure.**

***Index Terms*—Field-effect transistor, multiple gate, nanowire (NW), poly-Si, Si–oxide–nitride–oxide–Si (SONOS).**

I. Introduction

AFTER decades of research and development efforts, thin-film transistors (TFTs) fabricated on insulating substrates have become fundamental building blocks for large-area electronics such as flat-panel display. Among several TFT technologies, poly-Si one is especially attractive. Due to the great improvement in film crystallinity over the amorphous counterparts, poly-Si TFTs exhibit high carrier mobility and make possible the integration of other circuit components like the driver, digital-to-analog (D–A) converters, controllers, processors, and even memories on the same panel [1]. The so-called system-on-panel (SOP) approach not only improves the performance and reliability, but also reduces the manufacturing cost.

Certainly poly-Si TFTs face several challenges that need to be carefully addressed. One of them is related to the granular structure of the poly-Si films. The presence of grain boundaries in the film may impede the carrier transport. Moreover, defects presenting in the grain boundaries act as charge trapping centers. For conventional TFT structures having a planar thin film as the channel, the abundant defects contained in the channel tend to retard the gate modulation of the channel surface potential during the operation of field-effect transistors. As a result, the subthreshold swing and threshold voltage (V_{TH}) of the device are dramatically increased. This, in turn, would also increase the operation voltage needed to achieve the required drive performance, accompanied by the penalty of larger power consumption. Such concern also stands for thin-film memory devices that usually require high voltages for programming and erasing (P/E) operations.

A useful approach to overcome the negative impacts of the granular structure of the poly-Si film is to reduce the total amount of defects by thinning down the channel body. In line with this, poly-Si nanowire (NW) transistors were recently proposed and demonstrated to exhibit steep subthreshold swing ($\sim$100 mV/dec or smaller), small threshold voltage, and high ON/OFF current ratio ($>10^7$) [2]–[7]. Concurrently, NW Si–oxide–nitride–oxide–Si (SONOS) devices have recently been demonstrated as a good candidate for high-density nonvolatile memory applications [8], [9]. Due to the high surface-to-volume ratio of the NW channel, the P/E operation could be performed at a lower voltage and much faster speed over the planar counterpart [8]. However, the fabrication of the NW devices typically requires advanced lithographic tools and/or complicated process flow. These are not compatible with the manufacturing of flat-panel products where the device feature size is generally several micrometers or larger. In this paper, we propose a simple and cost-effective approach to fabricate planar poly-Si TFTs and trigated poly-Si NW SONOS devices simultaneously without resorting to advanced lithographic tools. Greatly enhanced P/E speed with the proposed trigated NW structure is clearly demonstrated.

II. Device Fabrication

Fig. 1 shows the process sequence to fabricate simultaneously planar poly-Si TFTs together with the trigated NW SONOS devices. In addition to the cross-sectional view of the completed device structure at each step, the top views of device layout at some key steps are also shown to help elucidate the process features. The fabrication began on Si wafers capped with thermal oxide to simulate the glass substrate. First, a 50-nm-thick tetraethoxysilane (TEOS) oxide and a 50-nm-thick silicon nitride were deposited on the wafer surface sequentially by low-temperature chemical vapor deposition [LPCVD, as shown in Fig. 1(a)]. Next, an anisotropic etching step was performed to etch the nitride and TEOS oxide, and form a dummy structure, as shown in Fig. 1(b). Then, an HF-based wet etching step was performed to selectively remove the TEOS layer and form cavities underneath the nitride at the sidewalls of the dummy structure [see Fig. 1(c)], followed by the deposition of an

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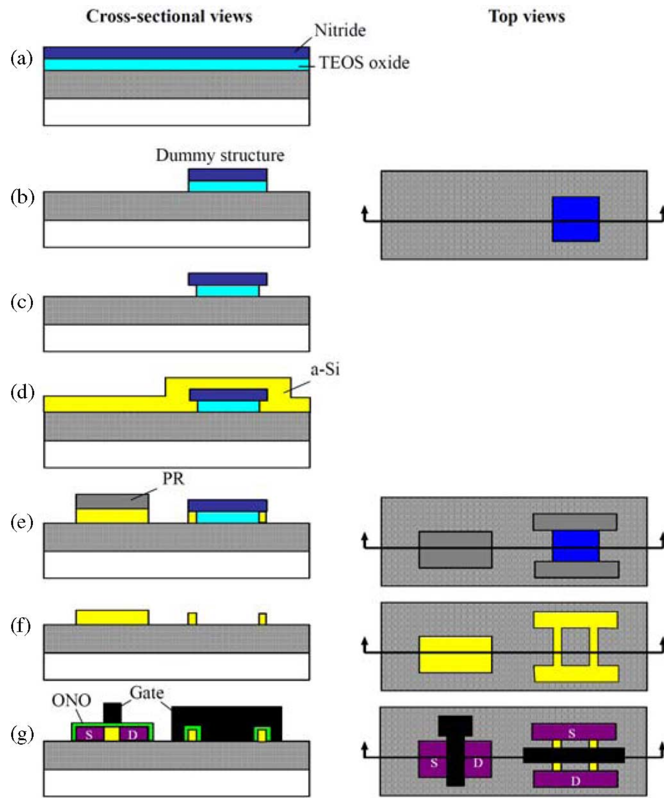

Fig. 1. Process flow for the simultaneous fabrication of the planar and NW SONOS devices. Top views at some key steps are shown in the right side. The straight lines denote the direction corresponding to the cross-sectional views shown in the left.

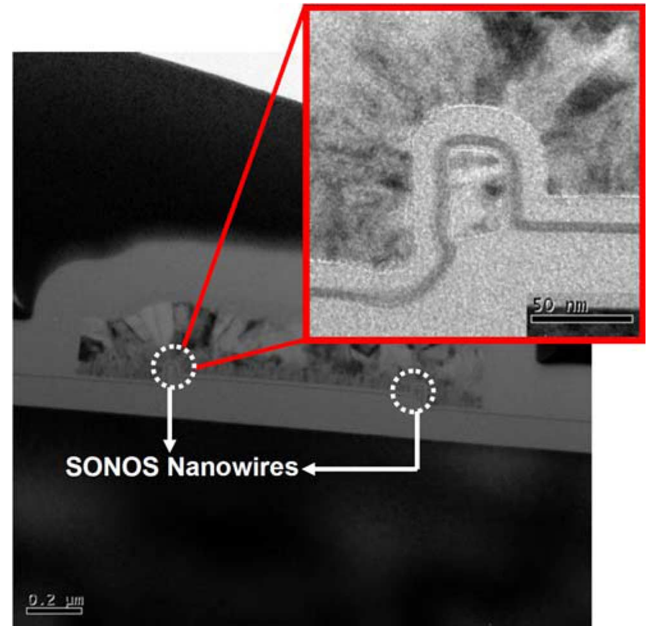

Fig. 2. Cross-sectional TEM image of a NW SONOS device.

amorphous silicon (a-Si) layer by LPCVD [see Fig. 1(d)]. In this step, the cavities were fully refilled with the a-Si layer that was subsequently transformed into polycrystalline phase by solid-phase crystallization (SPC) treatment (at 600 °C in N_2 ambient for 12 h). Then, a lithographic step was used to define the active regions including the source/drain (S/D) and channel for both planar and NW devices, followed by an anisotropic etching step to define the active region [see Fig. 1(e)]. Afterwards, the Si layers remaining in the cavities snugly formed the NW channels once the top hard mask and side TEOS oxide were selectively removed [see Fig. 1(f)]. Then, an oxide–nitride–oxide (ONO) (4 nm/7 nm/13 nm) stack and an n^+ poly-Si layer were sequentially deposited. Gate formation was subsequently performed. Self-aligned phosphorous ion implant (30 keV, 10^{15} cm^{-2}) was executed to dope the S/D region [see Fig. 1(g)]. After the S/D activation step, a passivation oxide layer was deposited to cover the fabricated devices, followed by normal metallization procedure to form the test pads.

A transmission electron microscopic (TEM) picture of a NW SONOS device is shown in Fig. 2. The height and width of the NW are around 50 and 25 nm, respectively. From the enlarged view of the structure, we can see that the NW is trigated by the conformal ONO and the n^+ poly-Si layers. It should be noted that at one side of the NW, the underlying oxide layer is recessed as a result of the etching step stated in Fig. 1(f) during fabrication.

III. Electrical Characteristics

With the proposed scheme, both planar and NW TFTs can be fabricated simultaneously and integrated easily on the same panel. Typical subthreshold and output characteristics of planar and NW devices are shown in Figs. 3 and 4, respectively. The use of ONO as the gate dielectric for the planar TFTs has been described previously [10]. Well-behaved device characteristics are indeed demonstrated in this paper. More importantly, the NW device shows steeper subthreshold swing and better ON/OFF current ratio than the planar one. This is attributed to the trigated configuration, which provides better gate controllability over the channel potential [11], and the use of NW channels with significantly reduced defects [12]. In addition, much better control over the device fluctuation is demonstrated with the NW structure, as shown in Fig. 5. As has been pointed out in one of our previous studies [13], such improvement is again attributed to the shrinkage of channel volume with the NW structure.

For P/E operations, a high voltage is applied to the gate, while the source and drain are both grounded. Fig. 6 shows the V_{TH} shift versus programming time of NW SONOS devices with gate bias ranging from 11 to 14 V. In this study, V_{TH} is simply defined as the gate voltage at a drain current of 10^{-9} A. For a fixed period, the V_{TH} shift increases with increasing gate bias. It can be seen that a memory window of 3 V can be achieved within 1 ms with an applied voltage of 14 V, as shown in Fig. 7. We apply this operation condition to program fresh devices to study the erasing characteristics. Fig. 8 shows the results of V_{TH} shift as a function of erasing time with gate bias of −9, −10, and −11 V, respectively. The V_{TH} shift increases with increasing magnitude (i.e., absolute value) of the gate voltage and/or operation time. It can be seen that the rate of V_{TH} shift slows down when erasing time is longer than 100 ms with gate

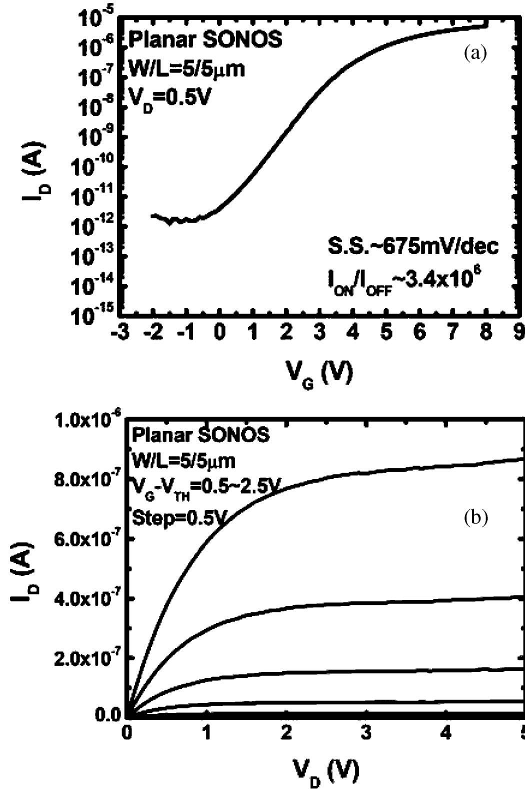

Fig. 3. (a) Subthreshold and (b) output characteristics of a planar device.

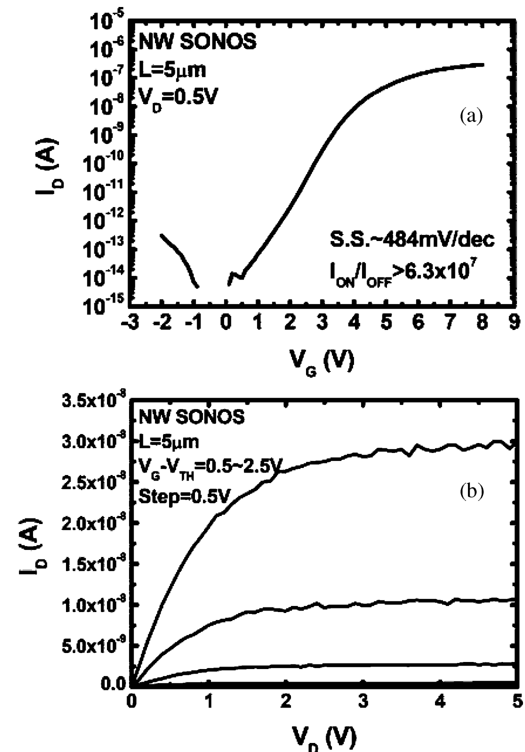

Fig. 4. (a) Subthreshold and (b) output characteristics of a NW SONOS device.

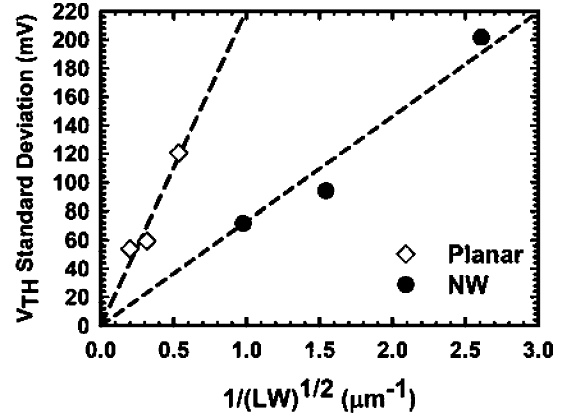

Fig. 5. Pelgrom plot indicating that the NW SONOS devices exhibit improved $V_{\rm TH}$ fluctuation control.

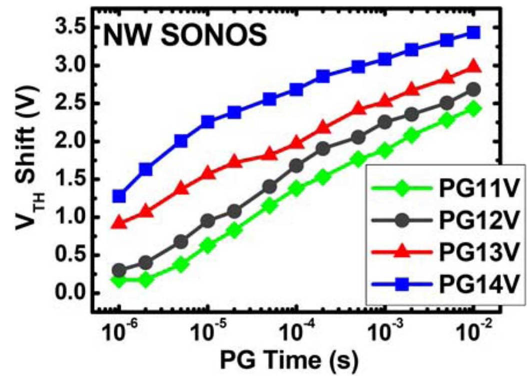

Fig. 6. $V_{\rm TH}$ shift as a function of programming (PG) time for NW SONOS devices stressed under different voltage. ($L = 0.7$ μm).

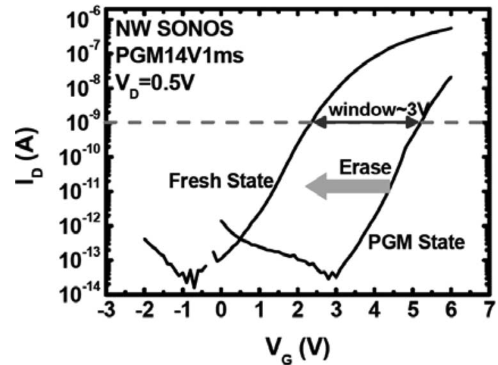

Fig. 7. Fresh and programmed subthreshold characteristics of NW SONOS devices. ($L = 0.7$ μm).

bias of -11 V. This is probably due to the injection of electrons from the gate, and can be alleviated with the adoption of gate electrode with a high work function [14].

Fig. 9 compares the programming characteristics of planar and NW SONOS devices. To compare the programming capability, we apply the same gate bias of 14 V to both planar and NW devices. For the NW one, $V_{\rm TH}$ shift is over 1 V when the

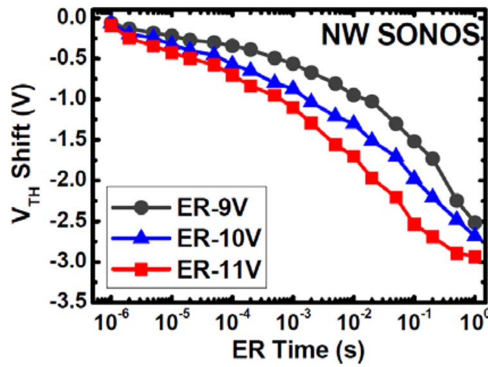

Fig. 8. $V_{\rm TH}$ shift as a function of erasing (ER) time for NW SONOS devices stressed under different voltage.

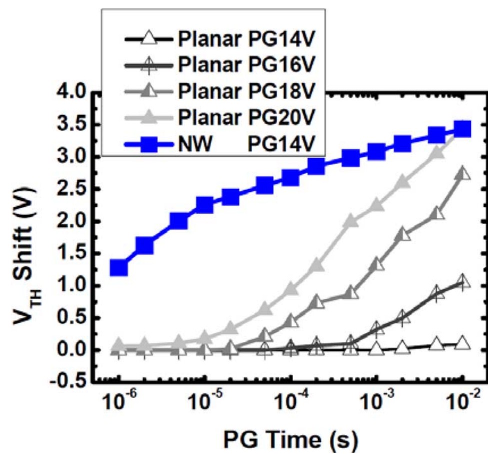

Fig. 9. $V_{\rm TH}$ shift as a function of programming time for NW ($L = 0.7$ μm) and planar ($L/W = 0.7/5$ μm) SONOS devices stressed under different voltage.

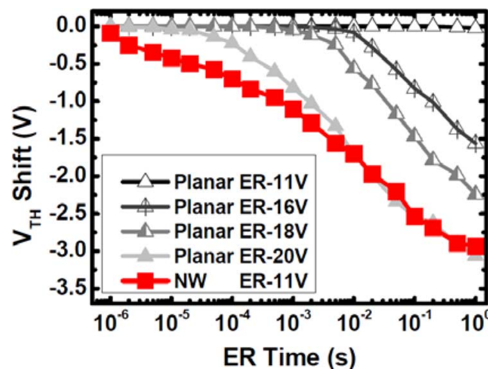

Fig. 10. $V_{\rm TH}$ shift as a function of erasing time for NW ($L = 0.7$ μm) and planar SONOS ($L/W = 0.7/5$ μm) devices stressed under different voltage.

programming time is merely 1 μs. On the contrary, $V_{\rm TH}$ shift of the planar device is less than 0.1 V even when the programming time increases to 10 ms. In order to obtain the same $V_{\rm TH}$ shift as the NW device at 10 ms, a gate bias of 20 V is needed for the planar device. Similar trends also occur in the erasing characteristics, as shown in Fig. 10. If we apply gate voltage of -11 V to

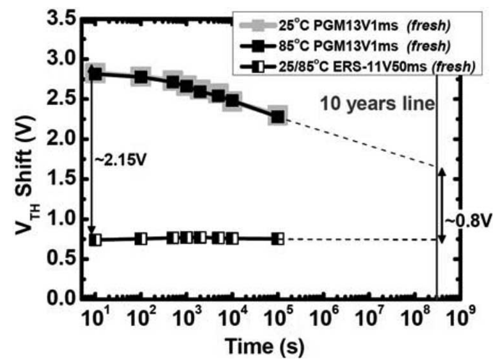

Fig. 11. Retention characteristics of NW SONOS devices characterized at different temperature. $L = 0.7$ μm.

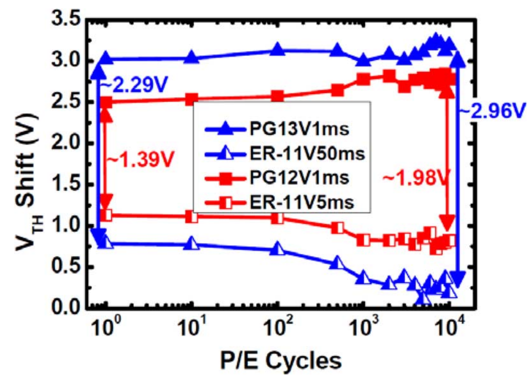

Fig. 12. Endurance characteristics of NW SONOS devices under two P/E conditions. $L = 0.7$ μm.

the planar device for 1 s, the programmed device exhibits only negligible shift. To attain comparable erasing speed to that of the NW device biased with gate voltage of -11 V, the gate bias of the planar device must be raised to -20 V. The aforementioned findings and comparisons on P/E characteristics between planar and NW devices are basically consistent with those previously reported for devices with monocrystalline Si NW channels. Improved P/E efficiency with the use of NW channels is attributed to the enhanced carrier injection through the channel due to the enhanced field strength at the channel surface [9].

Data retention characteristics of fresh devices measured at 25 °C and 85 °C, respectively, are shown in Fig. 11. If we program the devices with gate bias of 13 V for 1 ms, and -11 V with 50 ms for erasing, the memory window can be around 0.8 V after ten years at room temperature. Moreover, the temperature dependence of memory window at ten years is weak. The weak temperature dependence tends to imply that the data lost paths of the fabricated NW SONOS devices are through Frenkel–Poole emission and tunneling effect.

The endurance characteristics are shown in Fig. 12. It is seen that the P/E cycles can be more than 10^4 with acceptable memory window. Nevertheless, window opening is observed in our NW SONOS devices. The memory windows in the beginning are about 1.39 and 2.29 V for the two P/E conditions specified in

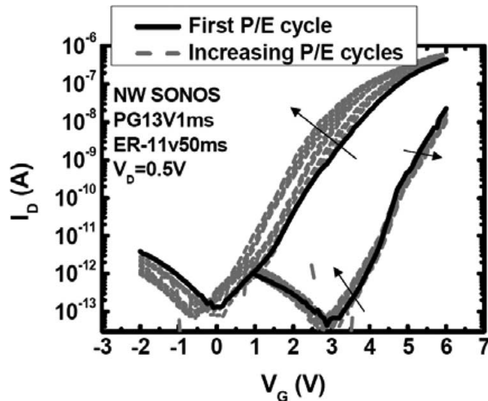

Fig. 13. Evolution of subthreshold characteristics of NW SONOS devices with increasing P/E cycles. The arrows indicate the evolution direction. ($L = 0.7\ \mu$m).

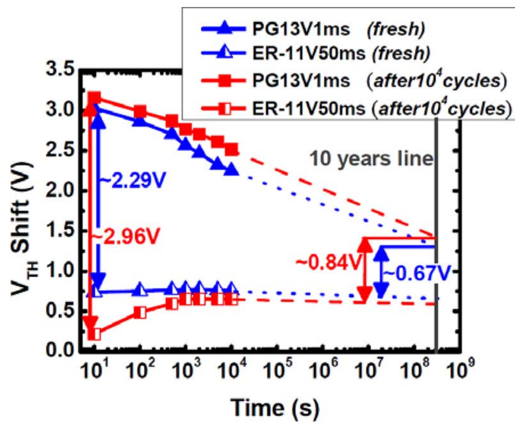

Fig. 14. Retention characteristics of NW SONOS devices after 10^4 P/E cycles. Results for fresh device are also included for comparison. ($L = 0.7\ \mu$m).

the figure. As stressing cycles increase, the windows extend from 1.39 and 2.29 V to 1.98 and 2.96 V, respectively. Note that the window opening is due to an increase in $V_{\rm TH}$ of the programmed state and a decrease in $V_{\rm TH}$ of the erased state. To gain insights into the origins, we also measured and inspected the evolution of subthreshold characteristics during the P/E operations. Fig. 13 shows the I_D–V_G characteristics of the device corresponding to the measured points shown in Fig. 12. The arrows contained in the figure indicate the evolution of the *I–V* curves. In the figure, we conclude that the increase in subthreshold swing due to the generation of interface states is responsible for the increase in $V_{\rm TH}$ of the programmed state. In Fig. 13, we also observe a negative shift in $V_{\rm TH}$ of the erased state, implying the occurrence of hole trapping in the gate dielectric. To make it clear, we also characterized the retention characteristics of the device after 10^4 P/E cycles. The results are shown in Fig. 14, together with the retention characteristics of a fresh device as a reference. It can be seen that, for the stressed device in the erased state, most of the negative $V_{\rm TH}$ shift recovers within the first 1000 s. This indicates that most of the trapped holes are located close to the oxide/channel interface.

IV. Conclusion

In summary, a new method is proposed and demonstrated for the simultaneous integration of planar TFTs and NW SONOS devices. The proposed method can be easily implemented in modern flat-panel manufacturing without resorting to costly advanced lithography. The combination of trigated configuration and NW structure help to improve the device performance in terms of steeper subthreshold swing and decreased $V_{\rm TH}$. Moreover, the P/E efficiency of NW SONOS devices is greatly improved. Based on the results obtained in this paper, the proposed method appears to be very promising for the realization of SOP in the future.

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