Analog Integr Circ Sig Process (2010) 63:255–271
DOI 10.1007/s10470-009-9387-6

A low-cost CMOS dual-mode AC/DC data converter for signal measuring technique

Cheng-Ta Chiang · Li-Lung Kao · Yu-Chung Huang

Received: 9 March 2009 / Revised: 17 August 2009 / Accepted: 27 August 2009 / Published online: 17 September 2009

Abstract A low-cost CMOS dual-mode AC/DC data converter for signal measuring technique is newly proposed. Instead of traditional full wave rectification, the realized synchronous rectification circuit is more attractive due to the easier integration and lower cost. In this paper, the design strategies of implementing the signal processing of AC and DC modes in the integrated circuit are discussed completely. Proven through SIMULINK in system level and SPICE simulations in circuit level, simulation results show that the proposed dual-mode AC/DC data converter achieves 8-bit resolution in DC mode and 7-bit resolution in AC mode. Measurement results have successfully verified the correct functions and performance of the proposed data converter and confirmed it for AC/DC signal measuring technique. The area of this chip is 710 × 630 μm^2 and the measured power consumption is 5.1 mW. The proposed dual-mode AC/DC data converter is suitable for the system of analog and mixed-signal boundary scan.

Keywords Analog to digital conversion · Data converter · Dual mode dual slope ADC · Synchronous rectification · AC/DC signal measuring technique · Analog and mixed-signal boundary scan

C.-T. Chiang (✉)
Mixed Signal Design Technologies Division, SoC Technology Center, Industrial Technology Research Institute, Hsinchu 310, Taiwan, ROC
e-mail: ctchiang23.ee90g@nctu.edu.tw

C.-T. Chiang · L.-L. Kao · Y.-C. Huang
Measurement Techniques Laboratory, Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Room 206, Engineering Building 4th, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan, ROC

L.-L. Kao
Realtek Semiconductor Corporation, Hsinchu 310, Taiwan, ROC

1 Introduction

Recently, efficient processes of the AC and DC signals have been an attractive research. Until now, some achievements [1–14] involving in measuring AC signals have been presented. [1–9] have been suitably used in wattmeter and digital multimeter, etc. [10–14] are investigated on the topic of root-mean-square (RMS) converter. To perform AC signal processing, a suitable data converter is required. For example, the data converter in [14] is based on the algorithm of the delta-sigma modulator. Although the system performance of [14] is outstanding, the overall hardware cost will be higher due to the back-end digital signal processing, such as decimation filters. Without the delta-sigma modulator, a new design to process AC signals by using a dual slope analog-to-digital converter (ADC) is thus investigated in this work. Besides, a rectification circuit is also an important circuit. In the traditional full wave rectifier, such kinds of circuit structure need some passive components, such as diodes. Although MOS diodes in the integrated circuits can replace traditional diodes, some issues on the long time reliability should be especially considered. In order to avoid the reliability problems, a synchronous rectification circuit to sample AC signals [15] is more attractive due to the easier integration and lower cost. Based on the technique of the synchronous rectification circuit of [15], the novel design strategies are firstly and completely addressed in this work.

In this paper, a low-cost CMOS dual-mode AC/DC data converter for signal measuring technique is newly proposed. Based upon the device parameters of 0.25 μm 1P5M

CMOS technology with 3.3 V power supply, all the functions and performance of the proposed dual-mode AC/DC data converter are correctly tested and proven through SIMULINK in system level and SPICE simulations in circuit level [16]. Measurement results have successfully verified the correct functions and performance of the proposed data converter and confirmed it for AC/DC signal measuring technique. The proposed dual-mode AC/DC data converter is suitable for the system of analog and mixed-signal boundary scan.

The system level analysis and behavior model simulations are described in the Sect. 2. Section 3 shows the circuit level implementation and simulation results. Section 4 demonstrates measurement results. Finally, conclusions and future works are given in Sect. 5.

2 System level analysis and behavior model simulations

Now, the system level analysis and behavior model of the proposed dual-mode AC/DC data converter are analyzed and simulated. The operational amplifier's (OPAmp) slew rate, unity gain bandwidth, DC gain, and the −3 dB bandwidth and the oversampling ratio of the comparator are the critical points in this circuit. These requirements are different in DC and AC modes, and they should be analyzed individually. By following the Sect. 2, the configurations, operation principles, and circuit specifications of all the function blocks will be described completely. In the system level, all blocks are severely designed in the specification of 10-bit resolution. In the circuit level, the proposed dual-mode AC/DC data converter is requested to achieve 8-bit resolution in DC mode and 7-bit resolution in AC mode. Moreover, in AC mode, the OPAmp itself should be designed to support the 100 kHz of AC signal bandwidth. The requirements on the resolution and AC signal bandwidth are fitted to the system of analog and mixed-signal boundary scan.

Figure 1 shows the architecture of the proposed dual-mode AC/DC data converter. The proposed data converter consists of an input buffer, a polarity controller, an integrator, a comparator, a polarity prejudgment circuit, and the digital control circuits. The polarity prejudgment circuit and controller form the synchronous rectification circuit. The switching signals supplied to analog circuits are given by the digital control circuits. Based on the proposed architecture, the DC and AC signal measuring technique can be combined into a single chip. Thus, the hardware cost is reduced.

2.1 The requirements of the OPAmp's slew rate in DC and AC mode

Firstly, the problem induced by the OPAmp's finite slew rate is investigated in DC mode. The OPAmp's finite slew rate will lead to the integration error. This error could not be canceled during the charging and discharging periods. The worst case of the integration error is given by

$$\Delta Q_{\mathrm{ERROR}} = \int i\,\mathrm{dt} = \int \frac{V_{\mathrm{IN}}}{R}\,\mathrm{dt} = \int \frac{\mathrm{SR}\cdot t}{R}\,\mathrm{dt} = \frac{\mathrm{SR}}{2\cdot R}\cdot \Delta t_{\mathrm{k}}^2$$

$$\Delta V_{\mathrm{ERROR}} = \frac{\Delta Q_{\mathrm{ERROR}}}{C} = \frac{\mathrm{SR}}{2\cdot R\cdot C}\cdot \Delta t_{\mathrm{k}}^2$$

$$\Delta V_{\mathrm{ERROR}}|_{\mathrm{MAX}} = \frac{V_{\mathrm{FS}}^2}{8\cdot R\cdot C\cdot \mathrm{SR}} \tag{1}$$

To make $\Delta V_{\mathrm{ERROR}}|_{\mathrm{MAX}} < \frac{\mathrm{LSB}}{2}$, thus

$$\frac{V_{\mathrm{FS}}^2}{8\cdot R\cdot C\cdot \mathrm{SR}} < \frac{V_{\mathrm{FS}}}{2^{N+1}} \tag{2}$$

where $\Delta Q_{\mathrm{ERROR}}$ is the mis-integration charge on the integrator capacitor, V_{FS} the full scale voltage, R the resistor used in integrator, C the capacitor used in integrator, SR the

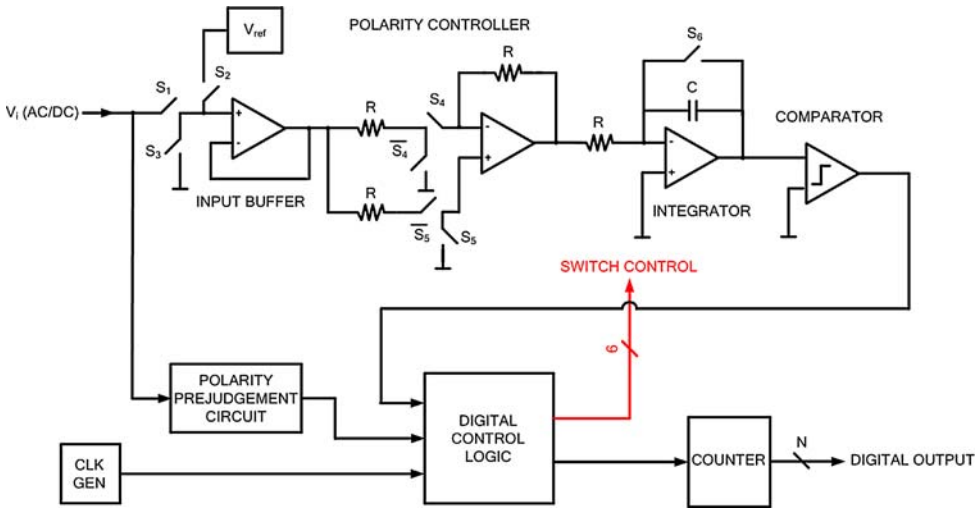


Fig. 1 The architecture of the proposed dual-mode AC/DC data converter

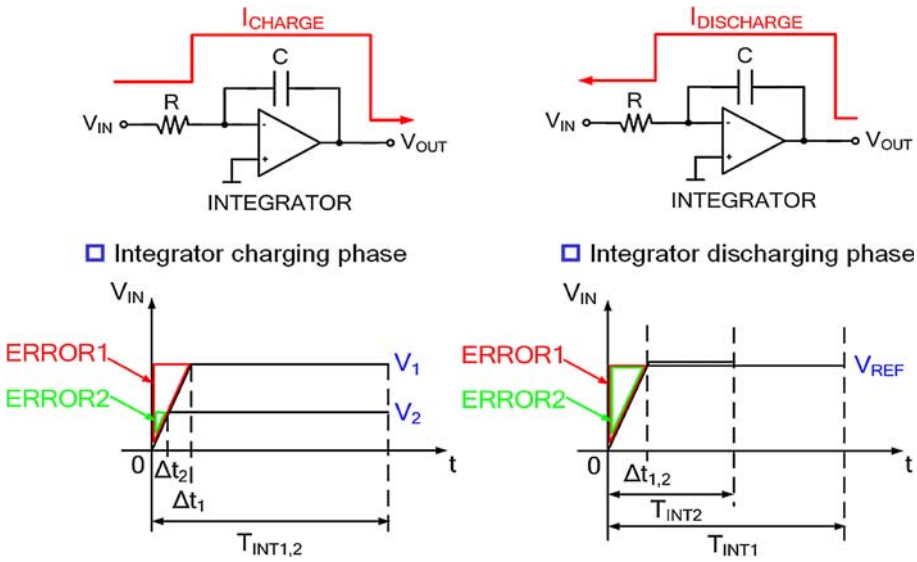


Fig. 2 The error induced by slew rate under two different input signals

OPAmp's slew rate, and Δt_k the delay induced by finite slew rate. Taking Fig. 2 as an analysis, where N is the overall ADC resolution in bits, Δt_i the time margin until signal has settled, and T_{INT} the integration period, the requirements of slew rate can be derived by Eq. 2

$$\mathrm{SR}_{\substack{\text{INPUT BUFFER\_OP}\\ \text{and POLARITY}\\ \text{CONTROLLER\_OP}}} > \frac{V_{FS}\cdot 2^{N-2}}{R\cdot C} = \frac{1.5\,\mathrm{V}\times 2^{10-2}}{50\,\mathrm{M\Omega}\cdot 330\,\mathrm{pF}} = 23.2\frac{\mathrm{V}}{\mathrm{ms}} \tag{3.1}$$

and

$$\mathrm{SR}_{\mathrm{INTEGRATOR\_OP}} > \frac{\frac{V_{FS}}{2}}{T_{INT}} = \frac{\frac{1.5\,\mathrm{V}}{2}}{16.6\,\mathrm{ms}} = 45\frac{\mathrm{V}}{\mathrm{s}} \tag{3.2}$$

Hence, slew rate of the OPAmp used in buffer and polarity controller is 23.2 V/ms and slew rate of the OPAmp used in integrator is 45 V/s. The integration error induced by slew rate is demonstrated in Table 1. In AC mode, slew rate is defined as the maximum slope $\Delta V_o/\Delta t$ of each OPAmp. Thus, the requirements of slew rate can be derived as

$$V_{IN} = V_o = \frac{V_{SWING}}{2}\sin(\omega t)$$
$$\mathrm{SR} = \left.\frac{\mathrm{dV_o}}{\mathrm{dt}}\right|_{MAX} = \left.\frac{V_{SWING}}{2}\omega\cos(\omega t)\right|_{MAX} = \left.\frac{1.5\,\mathrm{V}}{2}(2\pi\times 100\,\mathrm{kHz})\cos(\omega t)\right|_{MAX} = 0.471\frac{\mathrm{V}}{\mu\mathrm{s}} \tag{4}$$

Table 1 The integration error induced by slew rate

Slew rate (V/ms)	Integrating error (%)
0.225	5.0 (4-bit resolution)
2.250	0.5 (7-bit resolution)
22.500	→ 0.05 (10-bit resolution)

$$V_{IN} = \frac{V_{SWING}}{2}\sin(\omega t) \quad V_O = -\frac{1}{s\cdot R\cdot C}V_{IN}$$
$$\mathrm{SR} = \left.\frac{\mathrm{dV_o}}{\mathrm{dt}}\right|_{MAX} = -\frac{1}{R\cdot C}\frac{V_{SWING}}{2}\sin(\omega t)\Big|_{MAX} = -\frac{1}{50\,\mathrm{M\Omega}\cdot 330\,\mathrm{pF}}\frac{1.5}{2}\sin(\omega t)\Big|_{MAX} = -45.4\frac{\mathrm{V}}{\mathrm{s}} \tag{5}$$

According to Eqs. 4 and 5, slew rate of the OPAmp used in buffer and polarity controller is 0.471 V/μs, and the absolute value of slew rate of the OPAmp used in integrator is 45.4 V/s.

2.2 The requirements of the OPAmp's unity gain bandwidth in AC and DC mode

The OPAmp's finite unity gain bandwidth will lead to gain error, and produce additional pole in the overall transfer function. This effect is modeled as a DC gain error and a signal delay. In AC and DC modes, the output responses of non-ideal input buffer with ideal integrator, non-ideal polarity controller with ideal integrator, and non-ideal integrator, are derived as

$$V_{\mathrm{OUTPUT}}(t)|_{A_{\mathrm{DC}}\text{ large enough}} \cong \frac{1}{R\cdot C\cdot\omega_{\mathrm{IN}}} + \left[\frac{\frac{\mathrm{GBW}}{R\cdot C\cdot\omega_{\mathrm{IN}}}}{\mathrm{GBW}+\frac{\omega_{\mathrm{IN}}^2}{\mathrm{GBW}}} - \frac{1}{R\cdot C\cdot W_{\mathrm{IN}}}\right]\cdot \mathrm{e}^{-\mathrm{GBW}\cdot t} - \frac{\frac{\mathrm{GBW}}{R\cdot C\cdot\omega_{\mathrm{IN}}}}{\mathrm{GBW}+\frac{\omega_{\mathrm{IN}}^2}{\mathrm{GBW}}}\cdot\cos(\omega_{\mathrm{IN}}\cdot t) - \frac{\frac{\mathrm{GBW}}{R\cdot C}}{\mathrm{GBW}^2+\omega_{IN}^2}\cdot\sin(\omega_{\mathrm{IN}}\cdot t) \tag{6.1}$$

$$V_{\mathrm{OUTPUT}}(t)|_{A_{\mathrm{DC}}\text{ large enough}} \cong \frac{\mathrm{GBW}}{\mathrm{GBW}+\frac{1}{R\cdot C}}\cdot\frac{1}{\omega_{\mathrm{IN}}}\cdot\frac{1}{\mathrm{R}\cdot\mathrm{C}} - \left[\frac{\frac{\mathrm{GBW}}{\mathrm{GBW}+\frac{1}{R}}}{\omega_{\mathrm{IN}}^2+\left(\mathrm{GBW}+\frac{1}{R\cdot C}\right)^2}\cdot\frac{\omega_{\mathrm{IN}}}{R\cdot C}\right]\cdot \mathrm{e}^{-\left(\mathrm{GBW}+\frac{1}{R\cdot C}\right)\cdot t} - \frac{\mathrm{GBW}}{\mathrm{GBW}+\frac{1}{R}}\cdot\frac{1}{R\cdot C}\cdot\left[\frac{\omega_{\mathrm{IN}}}{\omega_{\mathrm{IN}}^2+\left(\mathrm{GBW}+\frac{1}{R\cdot C}\right)^2}-\frac{1}{\omega_{\mathrm{IN}}}\right]\cdot\cos(\omega_{\mathrm{IN}}\cdot t) - \left[\frac{\frac{\mathrm{GBW}}{R\cdot C}}{\omega_{\mathrm{IN}}^2+\left(\mathrm{GBW}+\frac{1}{R\cdot C}\right)^2}\right]\cdot\sin(\omega_{\mathrm{IN}}\cdot t) \quad (6.2)$$

$$V_{\mathrm{OUTPUT}}(t)|_{A_{\mathrm{DC}}\text{ large enough}} \cong \frac{1}{R\cdot C\cdot\omega_{\mathrm{IN}}} + \left[\frac{\frac{\frac{\mathrm{GBW}}{2}}{R\cdot C\cdot\omega_{\mathrm{IN}}}}{\frac{\mathrm{GBW}}{2}+\left(\frac{\omega_{\mathrm{IN}}^2}{\frac{\mathrm{GBW}}{2}}\right)}-\frac{1}{R\cdot C\cdot\omega_{\mathrm{IN}}}\right]\cdot\mathrm{e}^{-\frac{\mathrm{GBW}}{2}t} - \frac{\frac{\frac{\mathrm{GBW}}{2}}{R\cdot C\cdot\omega_{\mathrm{IN}}}}{\frac{\mathrm{GBW}}{2}+\frac{\omega_{\mathrm{IN}}^2}{\left(\frac{\mathrm{GBW}}{2}\right)}}\cdot\cos(\omega_{\mathrm{IN}}\cdot t) - \frac{\frac{\frac{\mathrm{GBW}}{2}}{R\cdot C}}{\left(\frac{\mathrm{GBW}}{2}\right)^2+\omega_{\mathrm{IN}}^2}\cdot\sin(\omega_{\mathrm{IN}}\cdot t) \quad (6.3)$$

$$V_{\mathrm{OUTPUT}}(t)|_{A_{\mathrm{DC}}\text{ large enough}} \cong -\frac{\frac{1}{RC}}{\mathrm{GBW}}+\frac{\frac{1}{RC}}{\mathrm{GBW}}\cdot\mathrm{e}^{-\mathrm{GBW}\cdot t} - \frac{1}{RC}\cdot t \quad (7.1)$$

$$V_{\mathrm{OUTPUT}}(t)|_{A_{\mathrm{DC}}\text{ large enough}} \cong -\frac{\frac{1}{RC}}{\left(\frac{\mathrm{GBW}}{2}\right)}+\frac{\frac{1}{RC}}{\left(\frac{\mathrm{GBW}}{2}\right)}\cdot\mathrm{e}^{-\left(\frac{\mathrm{GBW}}{2}\right)\cdot t} - \frac{1}{RC}\cdot t \quad (7.2)$$

$$V_{\mathrm{OUTPUT}}(t)|_{A_{\mathrm{DC}}\text{ large enough}} \cong \frac{1}{R\cdot C}\cdot\left(-\frac{1}{\mathrm{GBW}+\frac{1}{R\cdot C}}+t+\frac{1}{\mathrm{GBW}+\frac{1}{R\cdot C}}\cdot\mathrm{e}^{-\mathrm{GBW}\cdot t}\right)\cdot\frac{\mathrm{GBW}}{\mathrm{GBW}+\frac{1}{R\cdot C}} \quad (7.3)$$

where GBW is the OPAmp's unity gain bandwidth, and ω_{IN} the frequency of input signal. Equations (6.1, 6.2, 6.3 is derived for AC mode and Eqs. 7.1, 7.2, 7.3 is derived for DC mode. The curves shown in Fig. 3 represent the output responses of each integrator under different unit gain bandwidth. The frequency range is swept from 150 kHz to 10 MHz. These results conclude that if the unit gain bandwidth is not large enough, the larger integration error will be obtained. Besides, this error will not be <1 least significant bit (LSB) of the 10-bit resolution. By the same way, the analysis in DC mode is also performed as shown in Fig. 4. The requirements of the unity gain bandwidth and the integration error are calculated in Tables 2 and 3.

2.3 The requirements of the OPAmp's DC gain

The error induced by the OPAmp's finite DC gain is a constant value. It could be canceled during the charging and discharging period as shown in Fig. 5. The counter evaluation time t_{X} is given by

$$\frac{V_{\mathrm{IN}}}{R\cdot C}\cdot\frac{A_{\mathrm{DC1}}}{A_{\mathrm{DC1}}+1}\cdot\frac{A_{\mathrm{DC2}}}{A_{\mathrm{DC2}}+2}\cdot T_{\mathrm{INT}} = \frac{V_{\mathrm{REF}}}{R\cdot C}\cdot\frac{A_{\mathrm{DC1}}}{A_{\mathrm{DC1}}+1}\cdot\frac{A_{\mathrm{DC2}}}{A_{\mathrm{DC2}}+2}\cdot t_{\mathrm{X}} \quad (8)$$

where V_{IN} is the input signal, A_{DC1} the DC gain of the OPAmp used in the input buffer, and A_{DC2} the DC gain of the OPAmp used in the polarity controller. Basically, the DC gain requested for 10-bit resolution should be larger than 60 dB. Although this value is suitably performed in

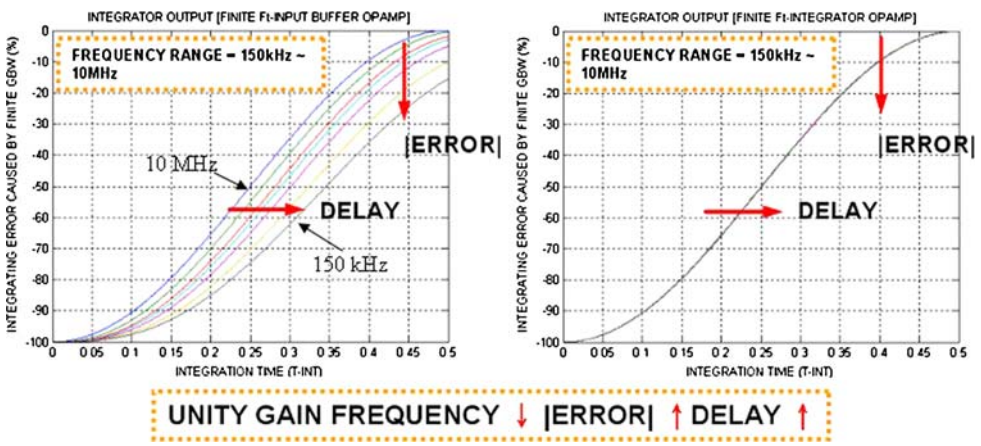


Fig. 3 In AC mode, the output response of the integrator under sweeping the unit gain bandwidth from 150 kHz to 10 MHz

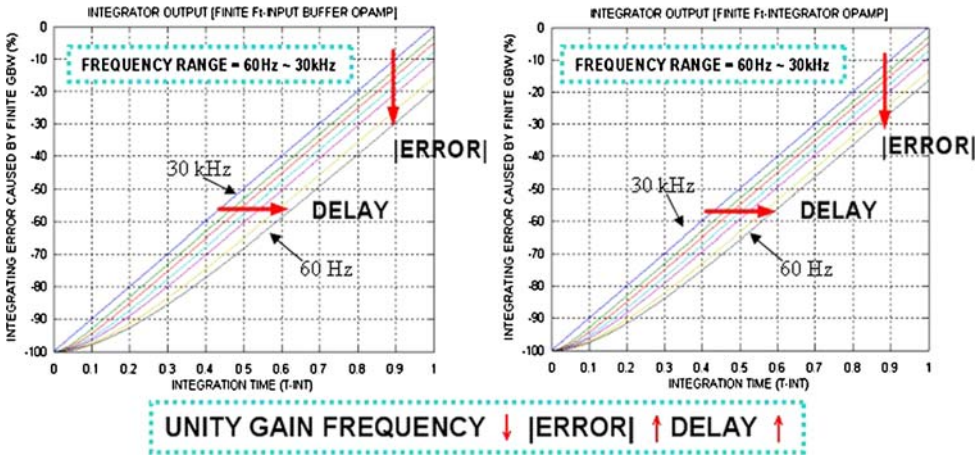


Fig. 4 In DC mode, the output response of the integrator under sweeping the unit gain bandwidth from 60 Hz to 30 kHz

Table 2 The requirements for OP unity gain bandwidth and integration error in AC mode

OPAmp	F_T (MHz)	Error
Input buffer	4	5e-4
Polarity controller	8	5e-4
Integrator	25	5e-4

Table 3 The requirements for OP unity gain bandwidth and integration error in DC mode

OPAmp	F_T (kHz)	Error
Input buffer	15	5e-4
Polarity controller	30	5e-4
Integrator	15	5e-4

the behavior model, the DC gain is slightly increased to 65 dB due to the margin of circuit design.

2.4 The requirements of the synchronous rectification circuit

Now, the requirements of the synchronous rectification circuit are addressed. The clock frequency of the comparator used in the synchronous rectification circuit directly affects the overall ADC resolution. The reason is that when AC sine wave is going below the voltage V_{REF}, the comparator used in the polarity prejudgment circuit needs a clock cycle time to sense the voltage variation as displayed in Fig. 6. Thus, the clock cycle time will directly affect the quality of rectification. The integration error is given by

$$\begin{aligned} V_{\text{ERROR}} &= \left(\frac{2}{R \cdot C} \cdot \int_{\frac{T_{IN}}{2}}^{\frac{T_{\text{IN}}}{2}+T_C} \frac{V_{\text{FS}}}{2} \cdot \sin(\omega_{\text{in}} \cdot t)\text{d}t \right) \cdot \left(\frac{2T_{\text{INT}}}{T_{\text{IN}}} - 1 \right) \\ &= \frac{V_{\text{FS}}}{\omega_{\text{in}} \cdot R \cdot C} \left(\frac{2 \cdot T_{\text{INT}}}{T_{\text{IN}}} - 1 \right) (1 - \cos(\omega_{\text{in}} \cdot T_C)) \\ &\cong \frac{V_{\text{FS}} \cdot \omega_{\text{IN}} \cdot T_C^2}{2 \cdot R \cdot C} \left(\frac{2 \cdot T_{\text{INT}}}{T_{\text{IN}}} - 1 \right) \end{aligned} \tag{9}$$

The error voltage should <0.5 LSB, thus

$$\frac{V_{\text{FS}} \cdot \omega_{\text{in}} \cdot T_C^2}{2 \cdot R \cdot C} \left(\frac{2 \cdot T_{\text{INT}}}{T_{\text{IN}}} - 1 \right) \leq \frac{1}{2} \cdot \text{LSB} = \frac{1}{2} \cdot \frac{V_{\text{FS}}}{2^N}$$

Finally,

$$F_{\text{CLK}} \approx \geq 2^{\frac{N}{2}+1} \cdot \sqrt{\pi} \cdot F_{\text{IN}} \tag{10}$$

where T_C is the clock cycle time, T_{IN} the RC time constant, T_{INT} the integration time, and F_{IN} the input frequency, F_{CLK} the frequency of the comparator used in the polarity prejudgment circuit. The overall ADC resolution versus the comparator oversampling ratio is shown in Fig. 7 and Table 4. In the specification of 10-bit resolution, the

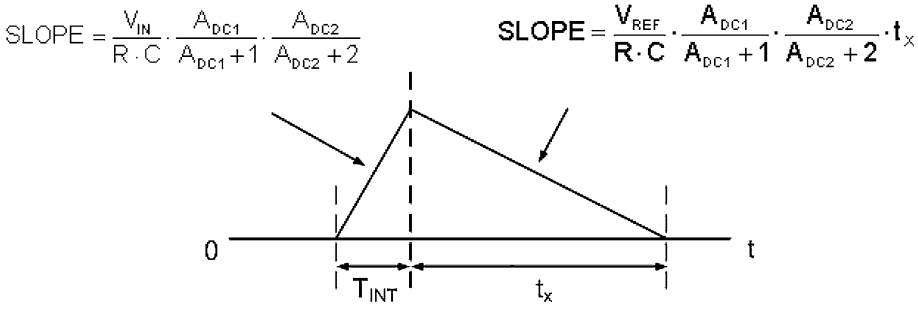


Fig. 5 The integrator's output affected by the OPAmp's finite DC gain during the charging and discharging period

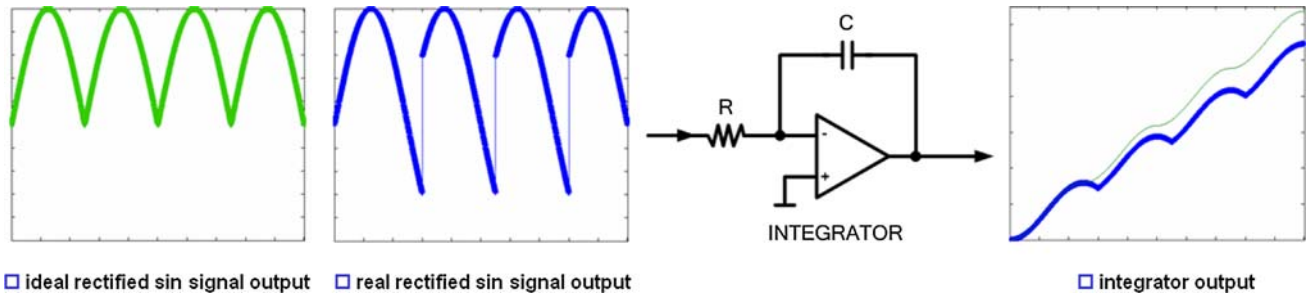


Fig. 6 Ideal rectification versus real rectification. The fine-type line is the ideal rectified sine wave and the *boldface*-type *line* is the real rectified sine wave

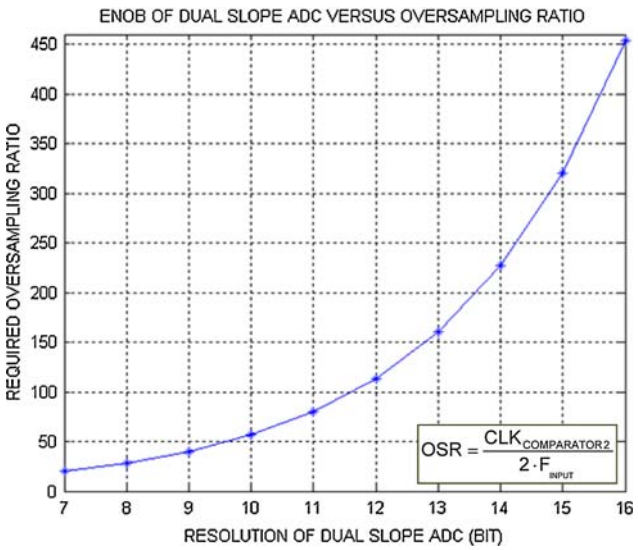


Fig. 7 The comparator oversampling ratio versus ADC's resolution

oversampling ratio should be 56.7. Finally, all the circuit specifications discussed above are organized in Tables 5 and 6.

Table 4 Overall ADC resolution versus the comparator oversampling ratio

	OSR
Resolution = 16 (BIT)	453.6
Resolution = 15 (BIT)	320.8
Resolution = 14 (BIT)	226.8
Resolution = 13 (BIT)	160.4
Resolution = 12 (BIT)	113.4
Resolution = 11 (BIT)	80.2
Resolution = 10 (BIT)	56.7
Resolution = 9 (BIT)	40.1
Resolution = 8 (BIT)	28.4
Resolution = 7 (BIT)	20.0

Table 5 The specifications for OPAmp used in buffer, gain controller, and integrator

	Spec for OPAmp used in buffer and gain controller	Spec for OPAmp used in integrator
Input/output swing	1.5 V	1.5 V
DC gain	65 dB	65 dB
Slew rate (DC/AC mode)	23.2 V/ms 0.471 V/us	45 V/s 45.4 V/s
Unity gain frequency (DC/AC mode)	15/30 kHz 10 MHz	15 kHz 0.1 MHz
Phase margin	>65°	>65°
Target error tolerance	<0.25 LSB	<0.25 LSB

Table 6 The specifications for comparator used in polarity prejudgment circuit and behind integrator

	Spec for comparator used in polarity prejudgement circuit	Spec for comparator used behind integrator
Offset voltage (mV)	<5	<3
Input/output swing (V)	1.5	1.5
DC gain of preamplifier	10	10
3 dB bandwidth of preamplifier (MHz)	10	0.1
Clock frequency	12 MHz	7.68 kHz

2.5 The whole system model

The whole system model is incorporated and performed by SIMULINK. The overall model shown in Fig. 8 is built, and the four operational phases are demonstrated in Fig. 9. Firstly, the simulations in DC mode are performed. The inputting DC signal is 0.375 V. All operational phases are the reset phase (0–16.6 ms), the integration phase (16.6–33.3 ms), the negative integration phase (33.2–50 ms), and the output phase (50–66.4 ms). In Fig. 10(b), the

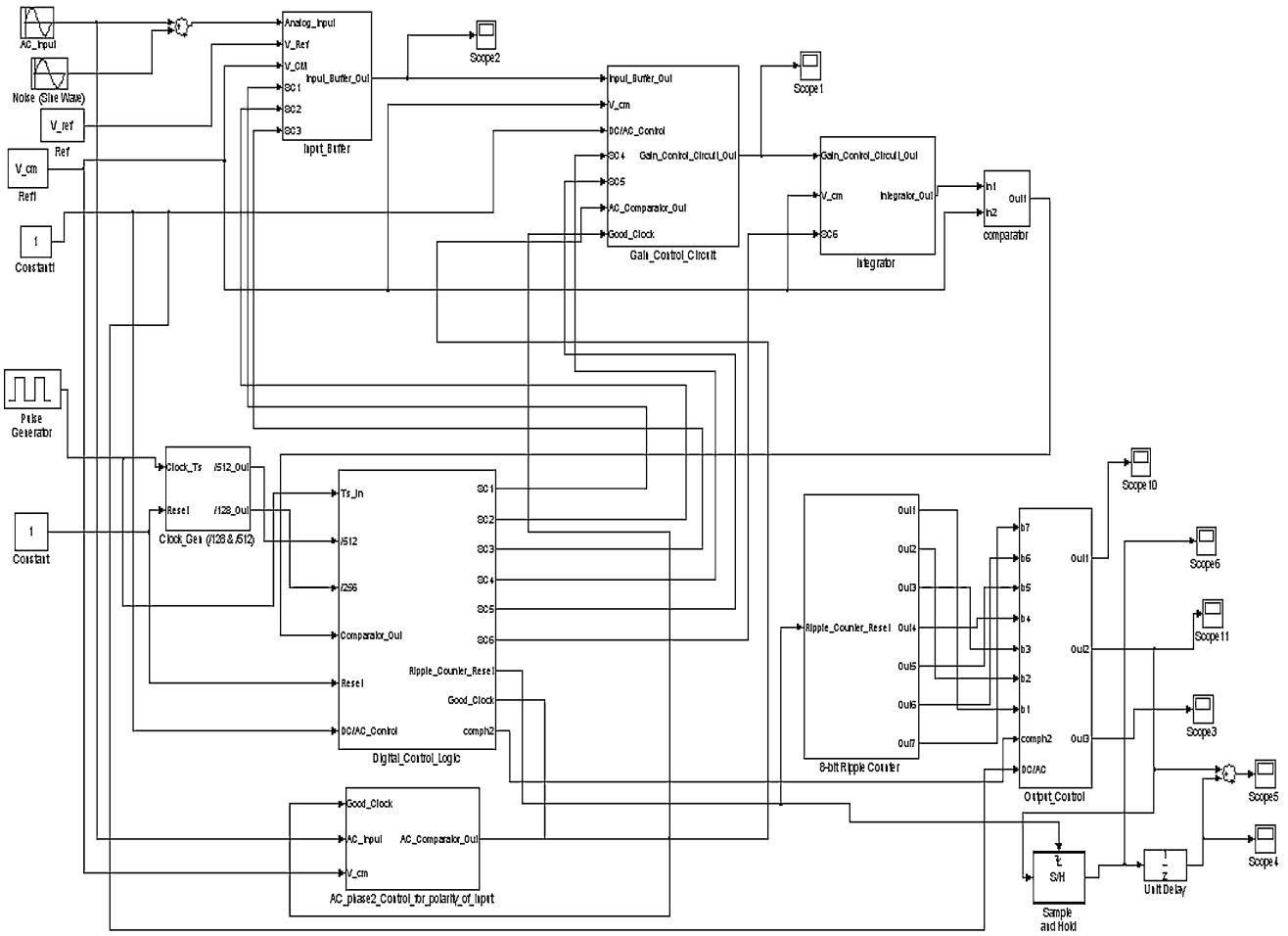


Fig. 8 The proposed dual-mode AC/DC data converter modeled in SIMULINK

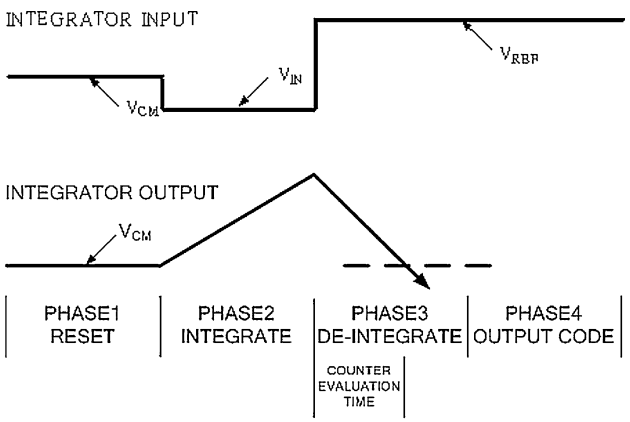


Fig. 9 The four operational phases

integration is performed to discharge the output of the integrator to −0.375 V. Finally, the counter will evaluate the corresponding digital number as shown in Fig. 10(c). The error between the ideal and real digital number is 0.5 LSB. Thus, the requirement of 8-bit resolution in DC mode is successfully achieved.

Then, the simulations in AC mode are performed. The inputting AC signal is 1.5 Vpp. In the Fig. 11(a, b), the operations of the synchronous rectification and integration are correctly shown, respectively. Finally, the digital counter will be triggered until the output voltage of the integrator exceeds the reference voltage (0 V). As shown in Fig. 11(c), the error in AC mode is 0.7 LSB. Thus, the requirement of 7-bit resolution is fulfilled. The whole system model is successfully matched to the designed ADC resolutions. All the circuit descriptions and simulation results of the proposed dual-mode AC/DC data converter are addressed in the next section.

3 Circuit level implementation and simulation results

Based on the specifications discussed in Sect. 2, the OPAmps, comparators, and the digital control circuits will be designed and verified in this section.

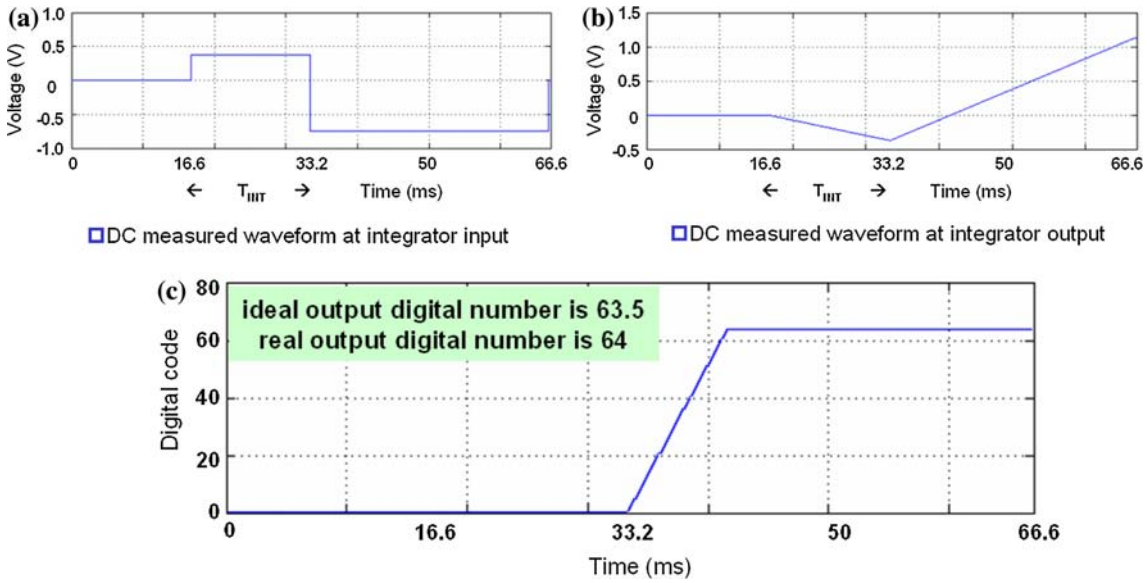


Fig. 10 In DC mode, the **a** input **b** output of the integrator, and **c** the output digital number of the counter

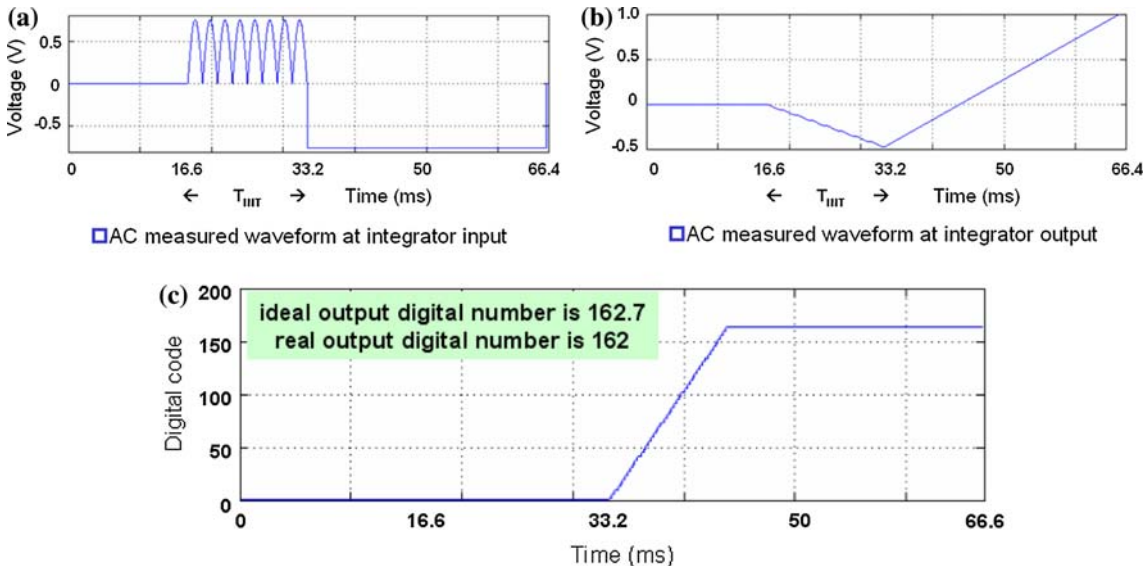


Fig. 11 In AC mode, the **a** input **b** output of the integrator, and **c** the output digital number of the counter

3.1 The OPAmp

Figure 12 shows the circuit structure of folded-cascoded OPAmp. The pertinent design relationships are derived as

$$A_{\mathrm{DC}} = g_{\mathrm{m1}} \cdot R_{\mathrm{OUT}} \tag{11.1}$$

$$R_{\mathrm{OUT}} = [g_{\mathrm{m6}} \cdot r_{\mathrm{o6}} \cdot (r_{\mathrm{o6}} || r_{\mathrm{o4}})] || g_{\mathrm{m8}} \cdot r_{\mathrm{o8}} \cdot r_{\mathrm{o10}} \tag{11.2}$$

$$\omega_T = \frac{g_{\mathrm{m1}}}{C_{\mathrm{L}}} \tag{11.3}$$

$$\omega_{\mathrm{pdom}} = \frac{1}{R_{\mathrm{OUT}} \cdot C_{\mathrm{L}}} \tag{11.4}$$

$$\omega_{\mathrm{pnon-dom}} = \frac{g_{\mathrm{m5}}}{C_{\mathrm{X}}} \tag{11.5}$$

where g_{m} is the transistor transconductance, r_{o} the transistor resistance, C_{x} and C_{L} the capacitance loading, A_{DC} the overall gain of the OPAmp, R_{OUT} the output resistance of the OPAmp, ω_{T} the unit gain frequency, ω_{Pdom} the dominant pole frequency, $\omega_{\mathrm{Pnon\ -\ dom}}$ the non-dominant pole frequency. Based on Eqs. 11.1, 11.2, 11.3, 11.4, 11.5, the SPICE simulations of the folded-cascoded OPAmp used in the input buffer, polarity controller, and integrator are shown in Figs. 13 and 14, respectively. Besides,

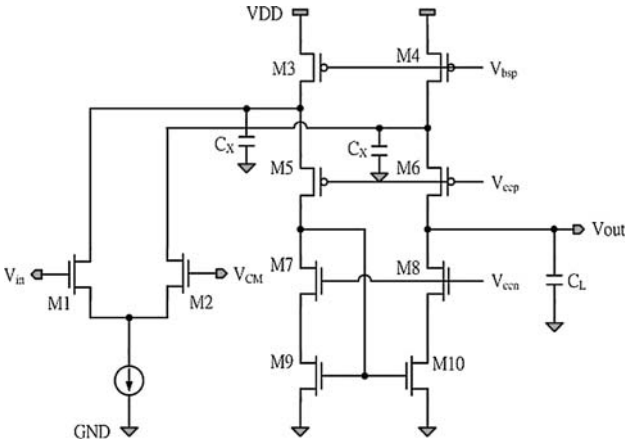


Fig. 12 The circuit schematic of the folded-cascoded OPAmp

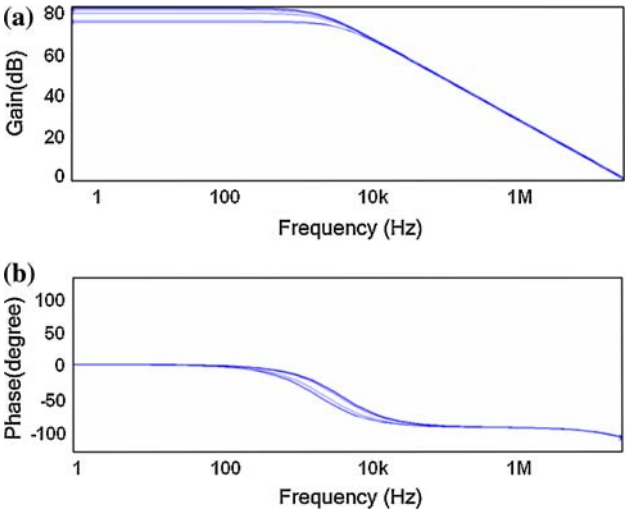


Fig. 13 The (**a**) gain (**b**) phase of the folded-cascoded OPAmp used in the input buffer and polarity controller

simulations in five design corners are listed in Tables 7 and 8. All the requirements are successfully matched.

3.2 The comparator

The comparator demonstrated in Fig. 15 is implemented as a preamplifier plus a latch stage. The gain of the preamplifier is derived as

$$A_{\text{pre\_amp}} = \frac{g_{\text{m1}}}{g_{\text{m3}}} \tag{12}$$

where g_{m} is the transistor transconductance. The combination of the diode-connected transistors of the gain stage and the transistors of the positive-feedback loop acts as a moderately large impedance, and gives gain from the preamplifier stage to the track-and-latch stage. The offset

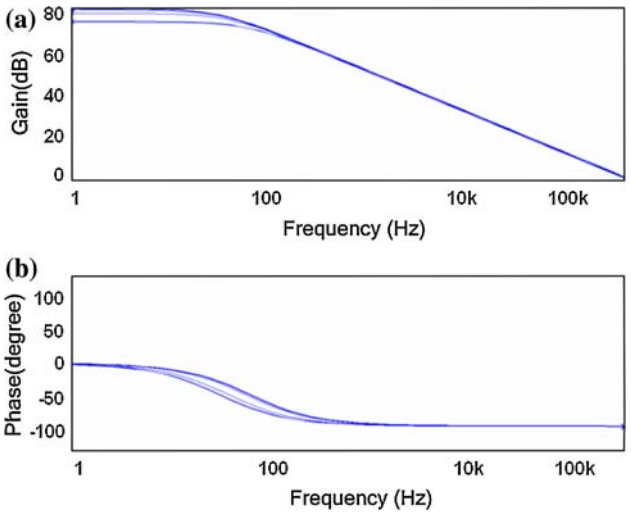


Fig. 14 The (**a**) gain (**b**) phase of the folded-cascoded OPAmp used in the integrator

Table 7 The SPICE simulations of the folded-cascoded OPAmp used in the input buffer and polarity controller

	TT	FF	SS	SF	FS
DC gain (dB)	79.8	76.1	82.1	81.5	75.6
PM	75.5°	75.5°	75.5°	75.8°	75.1°
F_t (MHz)	23.9	22.9	24.7	23.8	24.0
Power (mW)	1.57	1.54	1.63	1.61	1.53

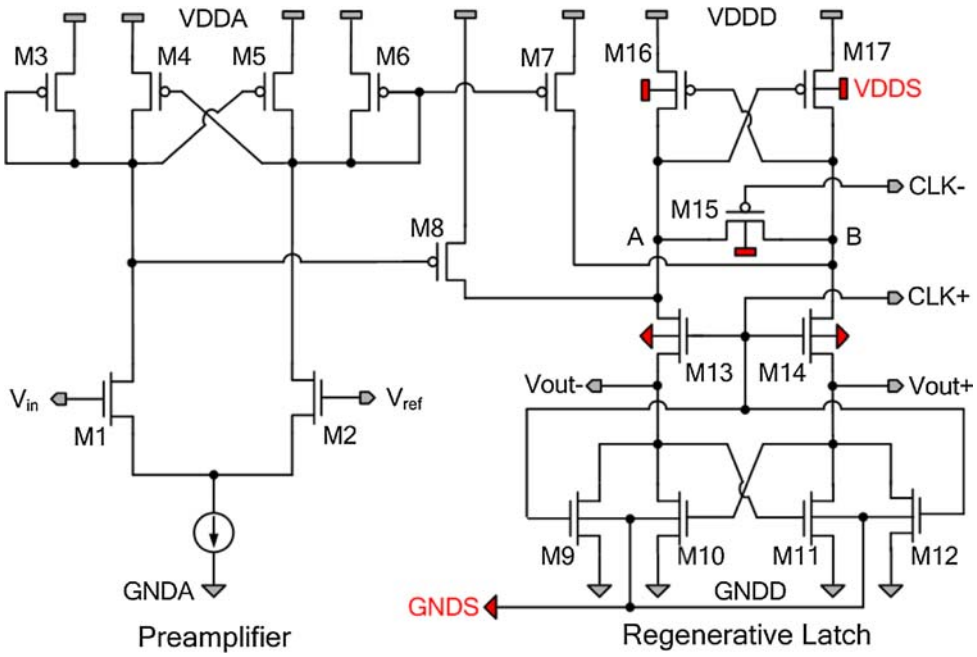
Table 8 The SPICE simulations of the folded-cascoded OPAmp used in the integrator

	TT	FF	SS	SF	FS
DC gain (dB)	79.8	76.1	82.1	81.5	75.6
PM	89.7°	89.7°	89.7°	89.7°	89.7°
F_t (MHz)	0.382	0.366	0.394	0.380	0.384
Power (mW)	1.57	1.54	1.63	1.61	1.53

simulations of the comparators used in the polarity prejudgment circuit and behind the integrator are demonstrated in Figs. 16 and 17. The offset voltages are 5 and 2.5 mV, respectively. The offset voltages are all <1 LSB, and matched to the requirement of resolution. Finally, the functions and output voltages of the comparator in the latch and pre-amplification are all correctly verified.

3.3 The digital control circuits and the whole system

The block diagram of the digital control circuits is displayed in Fig. 18. The digital control circuits consist of a



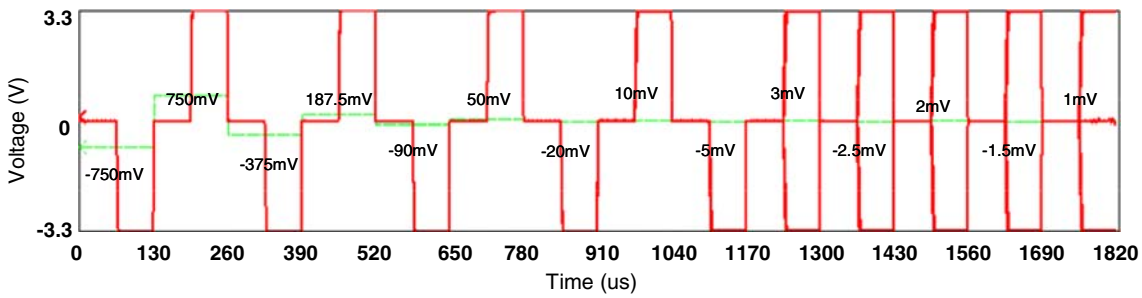


Fig. 15 The circuit schematic of the comparator

Fig. 16 The offset simulation of the comparator used in the polarity prejudgment circuit

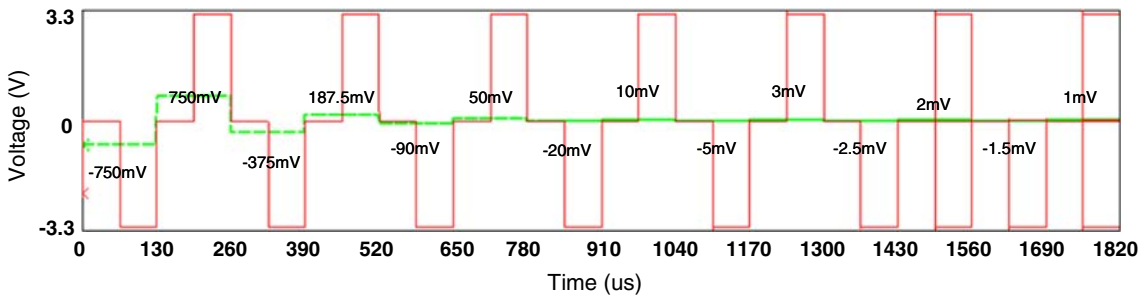


Fig. 17 The offset simulation of the comparator used behind the integrator

divider, a Johnson counter, AC control logic, DC control logic, switching control logic, a 7-bit counter, and a 8-bit adder. Firstly, they generate all the switching signals to control analog circuits. When DC mode is chosen, the proposed dual-mode AC/DC data converter is operated as a general dual slope ADC. On the contrary, if AC mode is chosen, the output of the comparator used in the polarity prejudgment circuit will send to the switching control

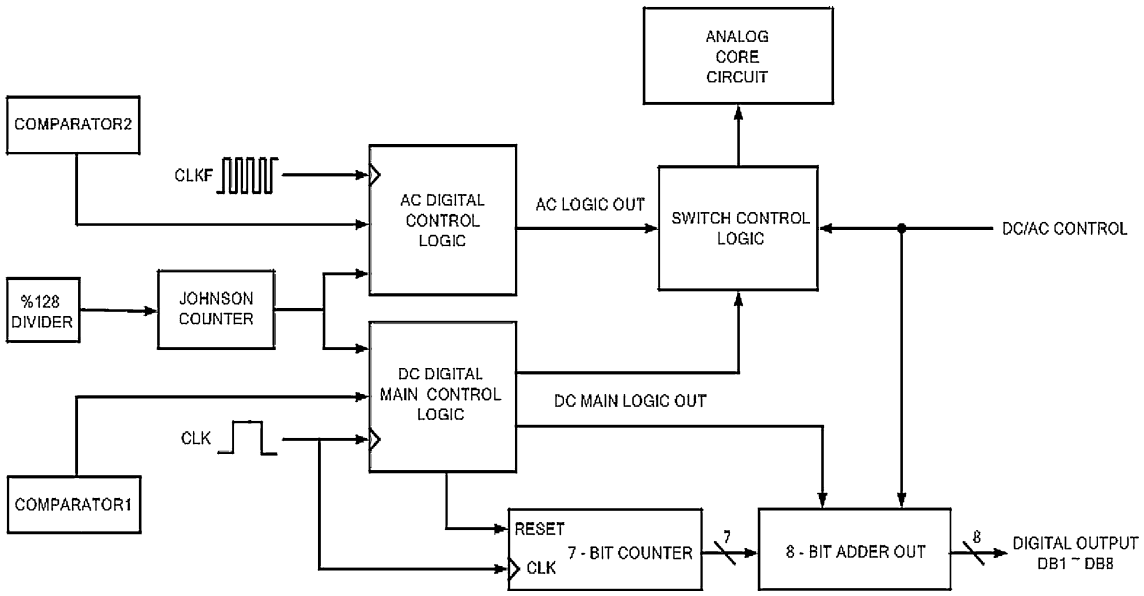


Fig. 18 The *block diagram* of the digital control circuits

Table 9 The digital control signals for switches used in polarity prejudgment circuit

	Control signal (DC/AC)	Control signal (DC/AC)	Control signal (DC/AC)	Control signal (DC/AC)
Switch 1	0/0	1/1	0/0	0/0
Switch 2	0/0	0/0	1/1	1/1
Switch 3	1/1	0/0	0/0	0//0
Switch 4	0/0	1/1	1/1	1/1
Switch 5	1/1	1/0	$0(V_{in} < V_{cm})$ or $1(V_{in} < V_{cm})/0$	$0(V_{in} < V_{cm})$ or $1(V_{in} < V_{cm})/0$
Switch 6	1/1	0/0	0/0	0/0

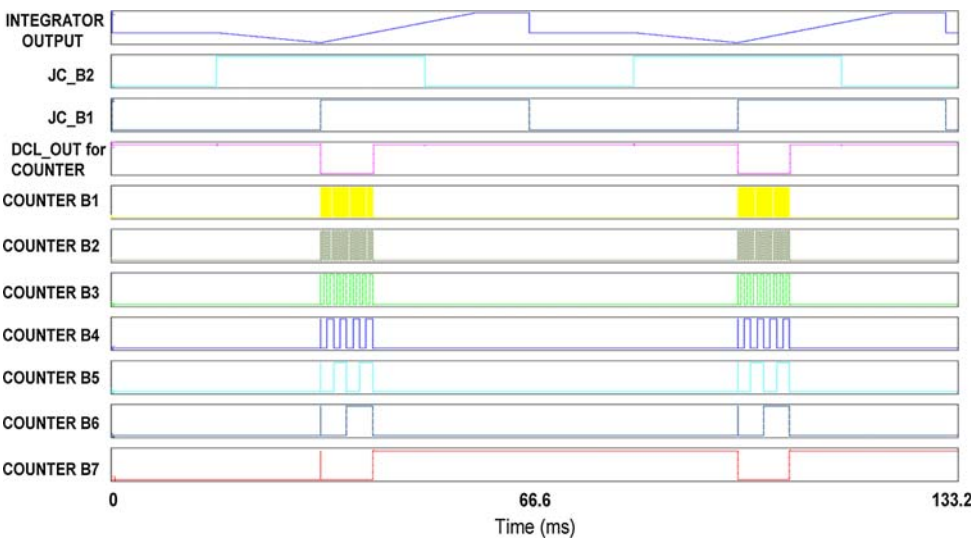


Fig. 19 The SPICE simulations of the digital control circuits

logic. The entire digital control signals are as listed in Table 9. For example, the AC input is the sine wave. Once the sine wave is below the reference voltage of comparator, the sine wave will be inverted. At the same time, the integration phase is also operated. Finally, they convert the output signals of analog circuits into digital

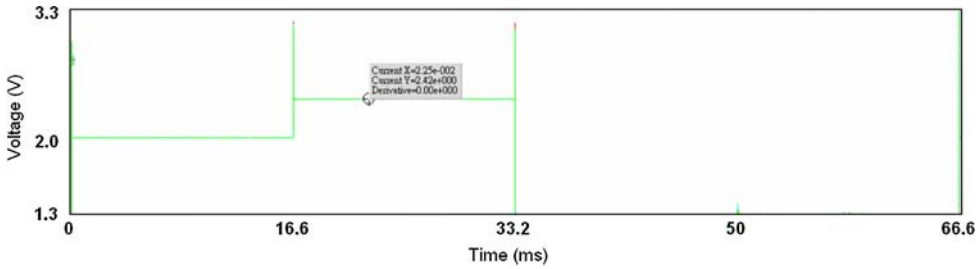
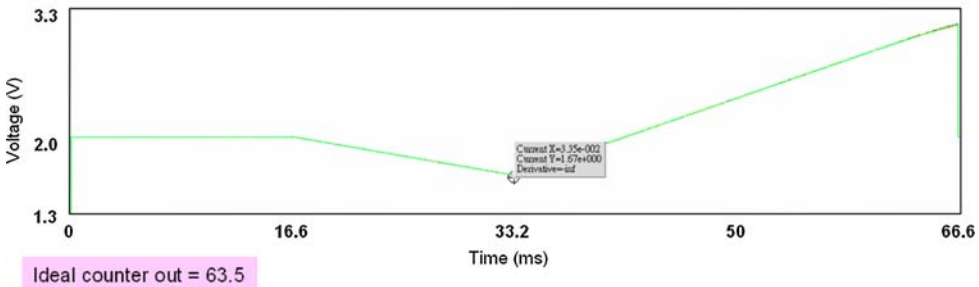


Fig. 20 In DC mode, the input and output of the integrator under the DC input voltage of $-V_{FS}/4$



Ideal counter out = 63.5

corner	TT	FF	SS	SF	FS
counter out	64	64	64	64	64

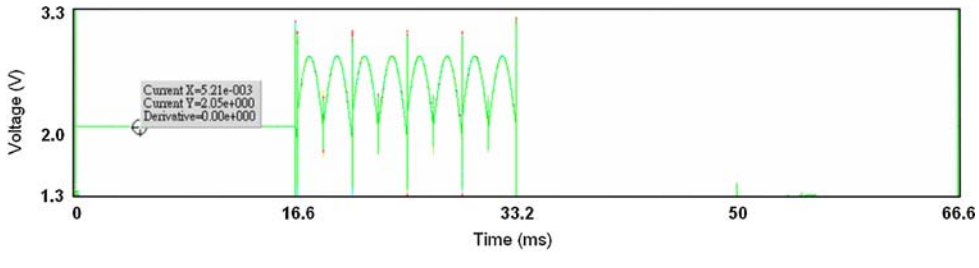
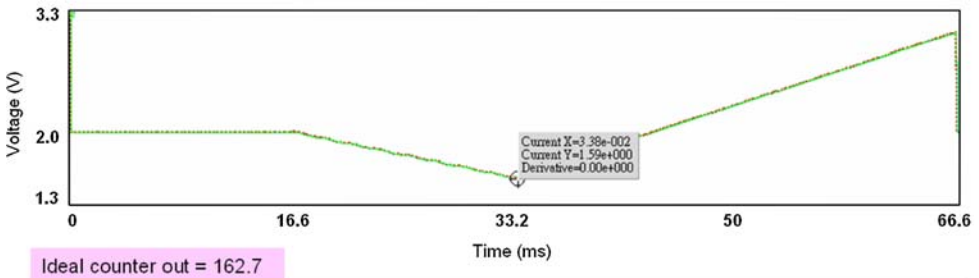


Fig. 21 In AC mode, the input and output of the integrator under the AC input amplitude of $V_{FS}/2$



Ideal counter out = 162.7

corner	TT	FF	SS	SF	FS
counter out	160	160	160	160	160

codes. The SPICE simulations of the digital control circuits are demonstrated in Fig. 19. The integrator's output shows the four operational phases successfully, and the digital codes are correctly generated. Finally, the whole system is built and simulated in SPICE. Figure 20 shows the input and output of the integrator under the DC input voltage of $-V_{FS}/4$. Besides, the AC input amplitude is $V_{FS}/2$, and the input and output of the integrator are shown in Fig. 21. The circuit operations and the SPICE results are correctly matched to the system level analysis and behavior model simulations as described in Sect. 2. All the functions and performance of the proposed dual-mode AC/DC data converter are successfully tested and proven through SPICE simulations.

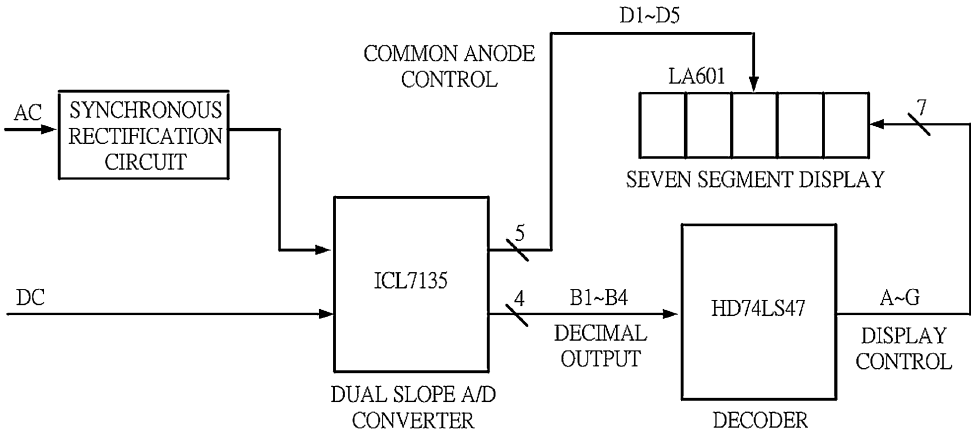


Fig. 22 The measurement setup of the proposed dual-mode AC/DC data converter built by the discrete components

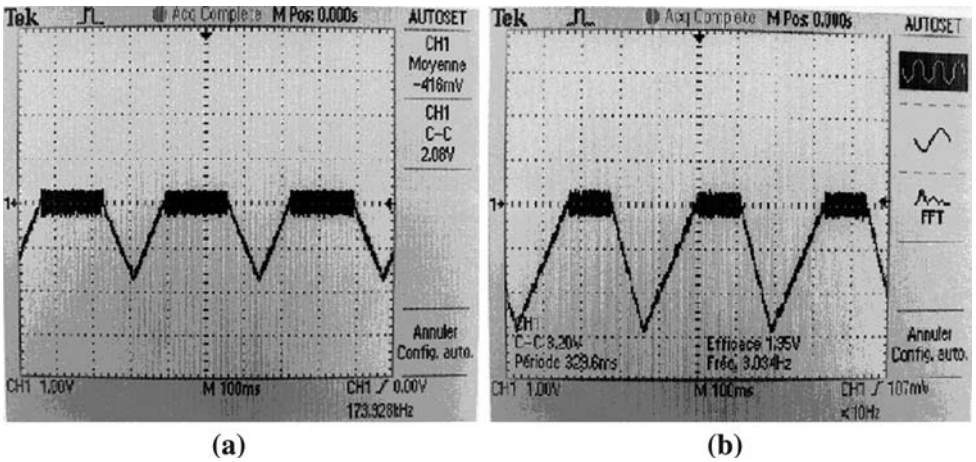


Fig. 23 The outputs of the integrators under the (**a**) DC input voltage of 1 V and (**b**) AC input amplitude of 1 V

4 Measurement results

Firstly, the circuits of the proposed dual-mode AC/DC data converter are built by discrete components to verify circuit operations. The measurement setup is shown in Fig. 22. The switches, the OPAmps, a decoder, a LED display, and a dual-slope ADC, are implemented by CD4066, LF411, HD7474, LA601, and ICL7135, respectively. Figure 23(a, b) show the outputs of the integrators under the DC input voltage of 1 V and the AC input amplitude of 1 V. As demonstrated, the circuit operations in DC and AC modes are all successfully performed as discussed in the Sect. 2. All the measured results are plotted in Fig. 24, and the accuracy is within $\pm 1.46\%$. Thus, all the circuit operations of the proposed dual-mode AC/DC data converter are successfully verified.

Finally, a low-cost CMOS dual-mode AC/DC data converter for signal measuring technique has been implemented. Each mode can be selected by an external pin, which is labeled as *DC/AC Selector*. Figure 25(a, b)

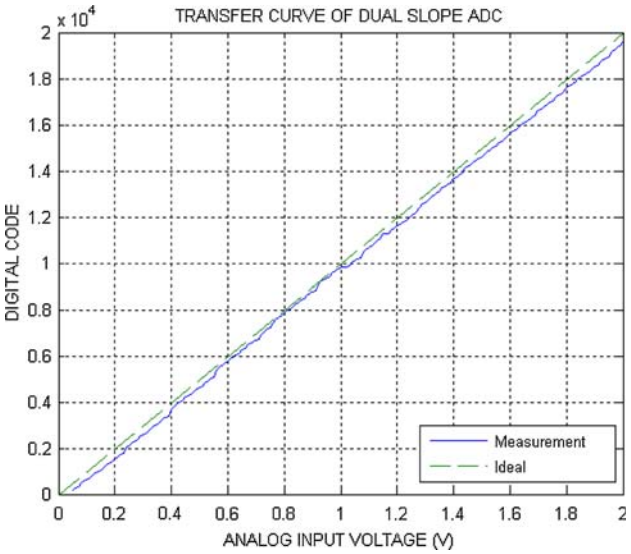


Fig. 24 The measured transfer curve of the proposed dual-mode AC/DC data converter built by the discrete components

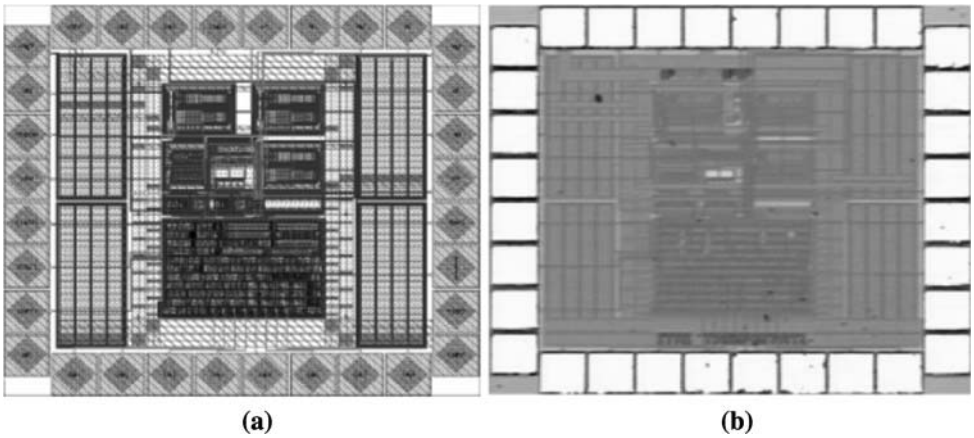


Fig. 25 **a** The physical layout **b** the photograph of the proposed dual-mode AC/DC data converter. The area of this implemented chip is $710 \times 630\ \mu m^2$

Table 10 The characteristics of the proposed dual-mode AC/DC data converter and comparisons with conventional methodology [14]

	This work	[14]
Technology	0.25 μm	0.8 μm
Supply voltage	3.3 V	±3 V
Clock sampling methodology	Oversampled	Oversampled
Chip output	Digital	Analog
Need back-end signal processing? (decimation filters)	No	Yes
Signal bandwidth	100.2 kHz	50 kHz
Signal swing	1.3–2.8 V	0.4 V_{rms}
Resolution	DC mode: 8 bits AC mode: 7 bits	DC mode: none AC mode: 14.6 bits (SNR = 88 dB)
Power consumption	5.1 mW	40 mW
Physical layout area	$710 \times 630\ \mu m^2$	$1{,}000 \times 1{,}000\ \mu m^2$
DNL	DC mode: +0.185 to −0.224 LSB AC mode: +0.168 to −0.154 LSB	NA
INL	DC mode: +0.422 to −0.087 LSB AC mode: +0.138 to −0.164 LSB	NA
Application field	AC/DC signal measuring	True RMS conversion

demonstrate the physical layout and photograph of the proposed dual-mode AC/DC data converter, respectively. The area of this implemented chip is $710 \times 630\ \mu m^2$ and the power consumption is 5.1 mW. The system clock frequency is 7.69 kHz and another clock signal for the comparator used in the polarity prejudgment circuit is 12 MHz. Firstly, oscilloscope waveforms of the input sine wave and the output synchronous rectified signals are demonstrated in Fig. 26(a–f). As shown, the correct circuit operations of the integrated synchronous rectification circuit are successfully proven. Next, a total of 32768 digital codes are collected by the logic analyzer Agilent 16702A. The differential nonlinearity error (DNL) and integral nonlinearity error (INL) are computed through the SANDWORK software. In DC mode, the input signal is a ramp signal with frequency 0.1 Hz, and the input signal is a sine wave with frequency 8 kHz in AC mode. After the computation, the DNL and INL are all demonstrated in Figs. 27 and 28. In these two modes, the DNL and INL are all <0.5 LSB. Thus, the whole system is correctly verified and successfully matched to the designed ADC resolutions, which is 8-bit in DC mode and 7-bit in AC mode. Measurement results have successfully verified the correct functions and performance of the proposed data converter and confirmed it for AC/DC signal measuring technique. All the characteristics of the proposed data converter and comparisons with conventional methodology [14] are summarized in Table 10.

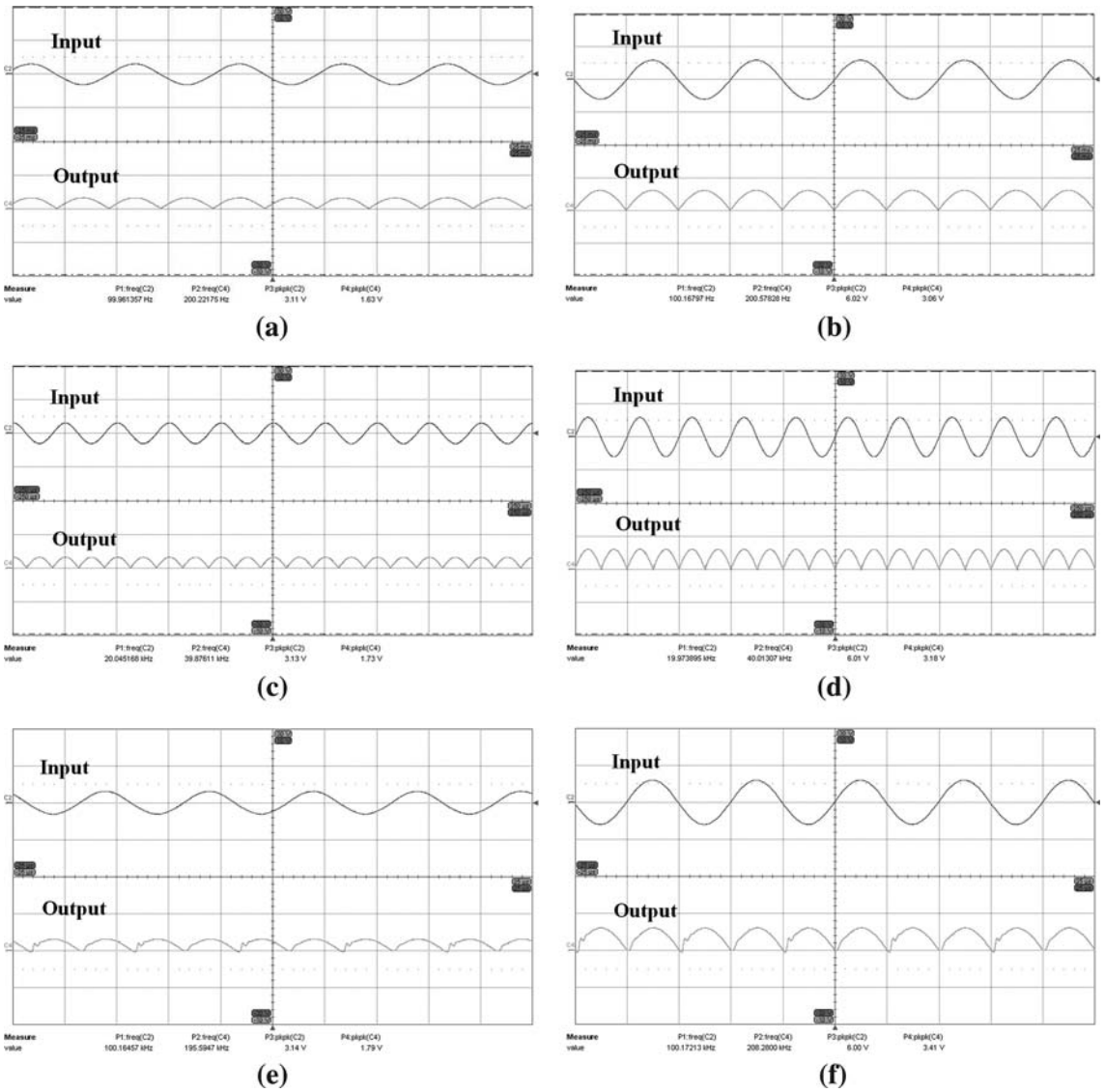


Fig. 26 Oscilloscope waveforms of the input sine wave and the output synchronous rectified signals under the input signal with **a** frequency 100 Hz and 0.75 V amplitude **b** frequency 100 Hz and 1.5 V amplitude **c** frequency 20 kHz with 0.75 V amplitude **d** frequency 20 kHz with 1.5 V amplitude **e** frequency 100 kHz with 0.75 V amplitude **f** frequency 100 kHz with 1.5 V amplitude

5 Conclusion

A low-cost CMOS dual-mode AC/DC data converter for signal measuring technique is newly proposed. Instead of traditional full wave rectification, the realized synchronous rectification circuit is more attractive due to the easier integration and lower cost. All the functions and performance of the proposed dual-mode AC/DC data converter are tested and proven through SIMULINK in system level and SPICE simulations in circuit level. Measurement results have successfully verified the correct functions and performance of the proposed data converter and confirmed it for AC/DC signal measuring technique. By following this paper, readers can understand how to reduce hardware cost and to implement the synchronous rectification circuit in the integrated circuits. Besides, without using conventional back-end digital signal processing, another design strategy to simplify overall system complexity is demonstrated in this work. In the future research, the proposed dual-mode AC/DC data converter will be researched on analog and mixed-signal boundary scan. On the other hand, by following all the design strategies addressed above, the resolution of the proposed dual-mode AC/DC data converter can be extended. Thus it can be adaptively applied to high-resolution applications.

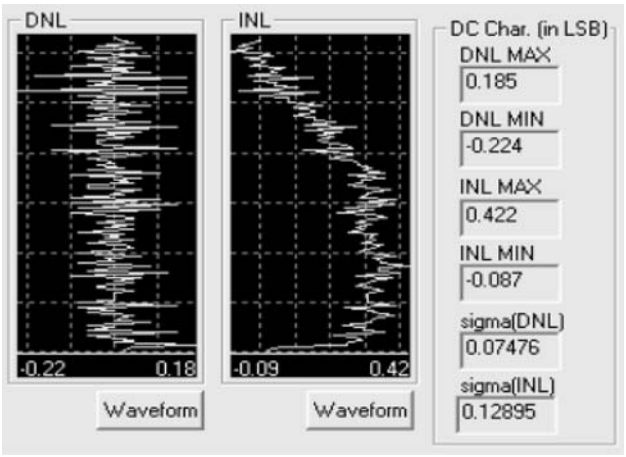


Fig. 27 The DNL and INL in DC mode. The input signal is a ramp signal with frequency 0.1 Hz

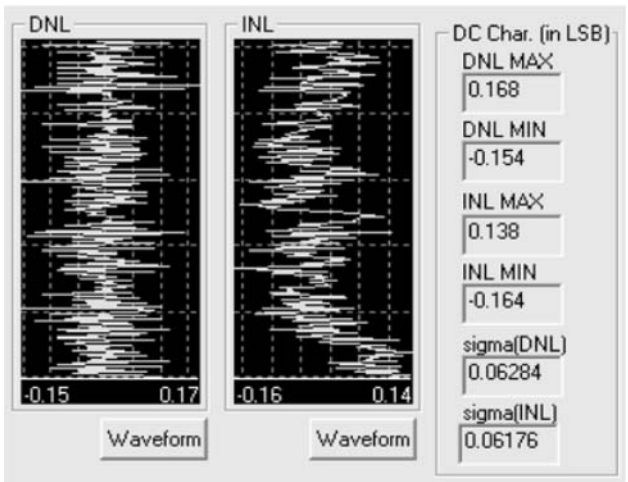


Fig. 28 The DNL and INL in AC mode. The input signal is a sine wave with frequency 8 kHz

Acknowledgments The authors acknowledge the SoC Technology Center of Industrial Technology Research Institute, Taiwan, for their support in chip fabrication. This work was supported by the National Science Council, ROC, under contracts NSC92-2218-E-009-011.

References

1. Turgel, R. S. (1974). Digital wattmeter using a sampling method. *IEEE Transactions on Instrumentation & Measurement, IM-23*, 337–341.
2. Young, C.-P., & Devaney, M. J. (1998). Digital power metering manifold. *IEEE Transactions on Instrumentation & Measurement, 47*(1), 224–228.
3. Toivonen, L., & Morsky, J. (1995). Digital multirate algorithms for measurement of voltage, current, power and flicker. *IEEE Transactions on Power Delivery, 10*, 116–126.
4. Waltrip, B. C., & Oldham, N. M. (1997). Wideband wattmeter based on RMS voltage measurements. *IEEE Transactions on Instrumentation & Measurement, 46*(4), 781–783.
5. Xi, J., & Chicharo, J. F. (1996). A new algorithm for improving the accuracy of periodic signal analysis. *IEEE Transactions on Instrumentation & Measurement, 45*, 827–831.
6. Petrovic, P. (2004). New digital multimeter for accurate measurement of synchronously sampled AC signals. *IEEE Transactions on Instrumentation & Measurement, 53*(3), 716–725.
7. Petrovic, P., Marjanovic, S., & Stevanovic, M. (2000). Measuring of slowly changing AC signals without sample-and-hold circuit. *IEEE Transactions on Instrumentation & Measurement, 49*(6), 1245–1248.
8. Petrovic, P., Marjanovic, S., & Stevanovic, M. (2003). Digital multimeter-watthourmeter based on usage of slowly ADC with possibility of processing without special sample-and-hold circuit. Serbia and Montenegro Patent No. 033/03, Jan. 21.
9. Petrovic, P., & Stevanovic, M. (2007). Digital processing of synchronously sampled AC signals in the presence of interharmonics and subharmonics. *IEEE Transactions on Instrumentation & Measurement, 56*(6), 2584–2598.
10. Britz, W. (2002). Precision RMS measurement. U.S. Patent 6 469 492, Oct 22.
11. Arseneau, R., & Zelle, J. (1988). RMS measuring apparatus for AC/DC voltages. U.S. Patent 4 786 859, Nov 22.
12. Williams, J. M., & Longman, T. L. (1986). A 25 MHz thermally-based RMS-to-DC converter. *ISSCC Digest of Technical Papers, XXIX*, 20–21.
13. van Drieenhuizen, B. P., & Wolffenbuttel, R. F. (1995). Integrated micromachined electrostatic true RMS-to-DC converter. *IEEE Transactions on Instrumentation & Measurement, 44*(2), 370–373.
14. Wey, W.-S., & Huang, Y.-C. (2000). A CMOS delta-sigma true RMS converter. *IEEE Journal of Solid-State Circuits, 35*(2), 248–257.
15. Osseiran, A. (1999). *Analog and mixed-signal boundary-scan*. Boston: Kluwer Academic Publishers.
16. Chiang, C.-T., Kao, L.-L., & Huang, Y.-C. (2008). A low-cost integrated dual-mode dual-slope ADC with synchronous rectification circuit for AC/DC signal measuring technique. In *Proceedings of IEEE International Instrumentation and Measurement Technology Conference*, *I²MTC'08*, pp. 165–169.

Cheng-Ta Chiang (S'00-M'05) was born in Taiwan, ROC, in 1977. He received the B.S. degree in electronics engineering from Chung Yuan Christian University, Jhongli, Taiwan, in 1999, the M.S. degree in biomedical engineering from the National Cheng Kung University, Tainan, Taiwan, in 2001, and the Ph.D. degree in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 2006. He was a Visiting Scholar with the Department of Electrical and Computer Engineering, The Johns Hopkins University, Baltimore, MD, from October 1, 2004 until November 30, 2005. He was included in *Marquis Who's Who in Science and Engineering 2006–2007* and *Marquis Who's Who in the World 2008*. He was a review committee member of the National Chip Implementation Center, Hsinchu. He is currently with Mixed Signal Design Technologies Division, SoC Technology Center, Industrial Technology Research Institute, Hsinchu. His main research interests include analog integrated circuits, biomedical electronics, image sensor circuits and systems, sensor signal conditioning and

transducers, Nyquist A/D converters, and high-resolution delta-sigma modulator. Dr. Chiang is a journal reviewer for the IEEE Transactions on Instrumentation and Measurement, IEEE Industrial Electronics, IEEE Sensors Journal, and an editorial advisory board member for the Sensors & Transducers Journal.

Li-Lung Kao was born in Taiwan, Republic of China, in 1980. He received the B.S. degree in electronics engineering from National Tsing-Hua University and the M.S. degree in electronics engineering from National Chiao-Tung University, Taiwan, ROC, in 2004 and 2007, respectively. He currently services in Realtek Semiconductor Corporation, Hsinchu, Taiwan, ROC. His main research interests have been in analog integrated circuits, delta-sigma A/D converter, and low-speed data converters.

Yu-Chung Huang received the M.S. degree in electrical engineering and Ph.D. degree in process engineering from the Technology University of Berlin, Berlin, Germany, in 1982 and 1985, respectively. Since 1985, he has been a Professor in the Department of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, ROC His research interests are sensors and measuring technologies. Prof. Huang is a member of the Committee of the Chinese Metrology Society and a member of the Micromechanical Science Institute, ROC.