A Novel Charge-Pumping Method for Extracting the Lateral Distributions of Interface-Trap and Effective Oxide-Trapped Charge Densities in MOSFET Devices

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***Abstract*— A novel charge-pumping method using dc source/drain biases and specified gate waveforms is proposed to extract the lateral distributions of interface-trap and effective oxide-trapped charge densities. The surface potential redistribution due to the oxide-trapped charges is treated by an iteration process in order to accurately determine their lateral distributions. The proposed novel method is feasible for accurately extracting the distributions of interface-trap and effective oxide-trapped charge densities generated by the hot-carrier stress and can be further used to predict the device lifetime.**

NOMENCLATURE

V_{FB}	Flatband voltage.
$V_{GH}(V_{GL})$	High (low) voltage of the gate pulses.
$T_H(T_L)$	Time of the high (low) gate bias per cycle.
L	Effective channel length.
$V_{\rm th}$	Threshold voltage.
$n_s(p_s)$	Surface electron (hole) concentration.
$v_{\rm th}$	Thermal velocity.
$\sigma_{p0}(\sigma_{n0})$	Hole (Electron) capture cross section.
E_i	Intrinsic Fermi energy.
n_i	Intrinsic carrier concentration.
N_{it} $(\overline{N}_{it})$	(Average) Interface-trap density per unit energy.
Q_{it}	Effective oxide trapped charge density.
E_t	Trap energy level.
q	Elementary charge.
W	Effective channel width.
f	Frequency of gate pulses.
x	Lateral position along the channel.
$I_{cp}(I_{\rm sat})$	(Maximum) Charge pumping current.
$Q_{cp}(Q_{\rm sat})$	(Maximum) Recombined charge density per cycle.
$S_R(S_F)$	Absolute slope of the rise (fall) edges of the gate pulses.
k	Boltzmann constant.
T	Absolute temperature.
$t_{eme}(t_{emh})$	Non-steady-state electron (hole) emission time.
$I_D(I_S)$	Drain (source) current.
V_{SUB}	Substrate voltage.
$V_{DS}(V_{SD})$	Drain-to-source (Source-to-drain) voltage.

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I. INTRODUCTION

WITH THE continuing scaling of MOS devices, the hot-carrier-induced device degradation has become a major reliability concern in sub- and deep-submicronmeter MOSFET's. It is believed that the degradation is mainly due to the effects of the generated oxide-trapped charges and interface-traps at the Si-SiO_2 interface. In general, the large electric field is strongly localized near the drain, therefore, carrier injection and interface-trap creation are similarly concentrated. The strongly inharmonious characters of hot-carrier injection and resulted damages present a considerable challenge to both experimental and modeling efforts.

One well-known experimental approach for measuring the Si-SiO_2 interface-traps created by the hot-carrier stress is the charge-pumping technique [1]–[11]. In 1988, the ac drain pulse technique had been proposed to measure the spatial variations of hot-carrier-induced interface-trap density near the drain from small-geometry MOSFET's [12]. After then, a similar technique had been developed to measure the lateral distribution of effective oxide-trapped charges [13]. However, according to our recent research [14], it is shown that the physical basis of using the ac source/drain pulses is incorrect and the charge-pumping current is shown to be not sensitive to surface electric field in the inversion region but only sensitive to surface carrier concentration. Moreover, the extracted results using the ac source/drain method are sensitive to the applied waveforms and the delay time between the gate and source/drain pulses. Recently, a simple method has been proposed to derive the spatial distribution of hot-carrier induced interface-trap density [15], however, this method can only be applied for the case without oxide-trapped charges; moreover, its accuracy is poor.

In this paper, a novel charge-pumping method using dc source/drain biases is proposed to extract the lateral distributions of both interface-trap and effective oxide-trapped charge densities. Based on the proposed new method, we can

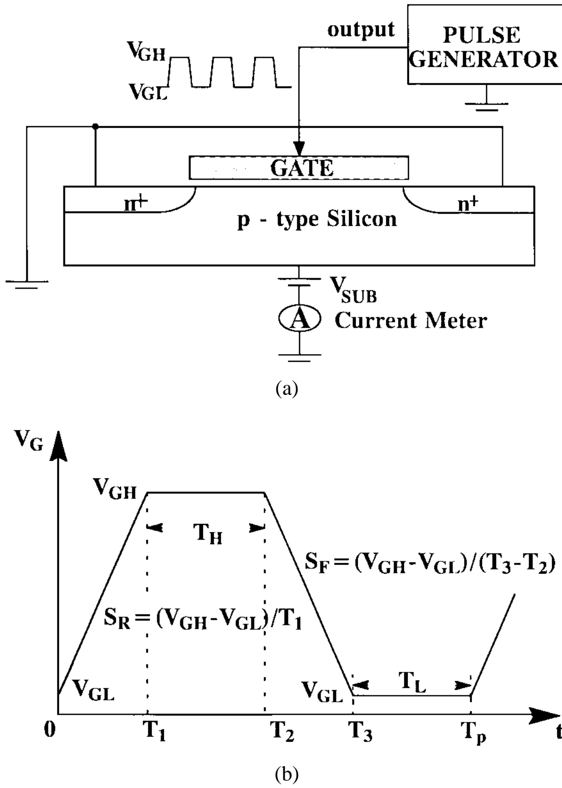


Fig. 1. (a) The experimental setup and (b) the applied gate pulse waveform for charge-pumping current measurement.

obtain the same damage profiles from the measured data under different gate or substrate biases. A detailed description of the proposed new method is given in Section I, which includes model derivations, applied gate waveform for measurements, and iteration process to obtain the accurate interface-trap density distribution. In Section II, the experimental results are presented, in which both the spatial damage distributions along the channel direction and the energy distribution of the interface traps in the bandgap have been extracted. In the last section, conclusions are made.

II. Model Derivations and Extraction Method

Based on a new charge-pumping current model [14] for a long-channel n-MOSFET with uniform interface-trap density distribution, the charge-pumping current per cycle related to the minimum gate voltage $V_{\rm GL}$ can be expressed as

$$\frac{I_{\rm cp}}{f}(V_{\rm GL}) = \frac{I_{\rm sat}}{f}\left[1-\exp\left(-\left(\frac{v_{\rm th}\sigma_{p0}}{1-\beta}p_s(V_{\rm GL})T_L\right)^{1-\beta}\right)\right] \quad (1)$$

where $I_{\rm sat}$ is the saturation charge pumping current when the silicon surface is strongly inverted at $V_{\rm GH}$, which is the function of S_L, S_F, and $V_{\rm SUB}; \beta$ and σ_{p0} can be obtained easily from the $I_{\rm cp}/f - V_{\rm GL}$ curves of a long-channel MOS device [14]; the $p_s(V_{\rm GL})$ value can be obtained from two-dimensional (2-D) numerical analysis. Note that the waveform used is important to obtain the correct results, the S_R, S_F, T_H, T_L, and $V_{\rm SUB}$ values are kept constant and the period is varied with $V_{\rm GL}$ to obtain β and σ_{p0}. The experimental setup and the applied waveforms for the gate pulse are shown in Fig. 1. Similarly, the charge-pumping current per cycle related to the maximum gate voltage $V_{\rm GH}$ can be expressed as

$$\frac{I_{\rm cp}}{f}(V_{\rm GH}) = \frac{I_{\rm sat}}{f}\left[1-\exp\left(-\left(\frac{v_{\rm th}\sigma_{n0}}{1-\alpha}n_s(V_{\rm GH})T_H\right)^{1-\alpha}\right)\right] \quad (2)$$

where α and σ_{n0} can also be extracted from the $I_{\rm cp}/f - V_{\rm GH}$ curves of a long-channel MOS device. For n-MOSFET's used in this paper, α and β are 0.326 and 0.388; σ_{n0} and σ_{p0} are 1.08E-17 and 2.16E-16 cm^{-2}, respectively.

From (1), the charge density recombined in a cycle can be expressed as

$$Q_{\rm cp}(V_{\rm GL}) = \frac{I_{\rm cp}}{fWL} = Q_{\rm sat} \cdot \left[1-\exp\left(-\left(\frac{v_{\rm th}\sigma_{p0}}{1-\beta}p_s(V_{\rm GL})T_L\right)^{1-\beta}\right)\right]. \quad (3)$$

For a device with nonuniform interface-trap density, (3) can be rewritten as

$$Q_{\rm cp}(V_{\rm GL}, x) = Q_{\rm sat}(x)\left[1-\exp\left(-\left(\frac{v_{\rm th}\sigma_{p0}}{1-\beta}p_s(V_{\rm GL}, x)T_L\right)^{1-\beta}\right)\right] \quad (4)$$

where x is the position along the channel direction, and $Q_{\rm sat}(x)$ can be approximately expressed as

$$Q_{\rm sat}(x) \simeq q\int_{E_1(x)}^{E_2(x)} N_{\rm it}(E,x)\,dE = q\overline{N_{\rm it}}(x)(E_2(x)-E_1(x)) \quad (5)$$

with

$$E_1(x) = E_i + \frac{kT}{q}\log(\sigma_{p0}v_{\rm th}n_i t_{\rm emh}(x)) \quad (6)$$

and

$$E_2(x) = E_i - \frac{kT}{q}\log(\sigma_{n0}v_{\rm th}n_i t_{\rm eme}(x)). \quad (7)$$

Note that $\overline{N_{\rm it}}$ is the average interface-trap density from E_1 to E_2; $t_{\rm emh}(t_{\rm eme})$ is the nonsteady-state hole(electron) emission time [5]. For simplicity, $Q_{\rm sat}(x)$ at the proximity of the source/drain junction is assumed to be only related to the interface-trap density, i.e., E_1 and E_2 are independent of x, and $t_{\rm emh}$ and $t_{\rm eme}$ can be separately approximated as

$$t_{\rm emh} = \frac{V_{\rm th}-V_{\rm FB}}{S_R} \quad (8)$$

and

$$t_{\rm eme} = \frac{V_{\rm th}-V_{\rm FB}}{S_F}. \quad (9)$$

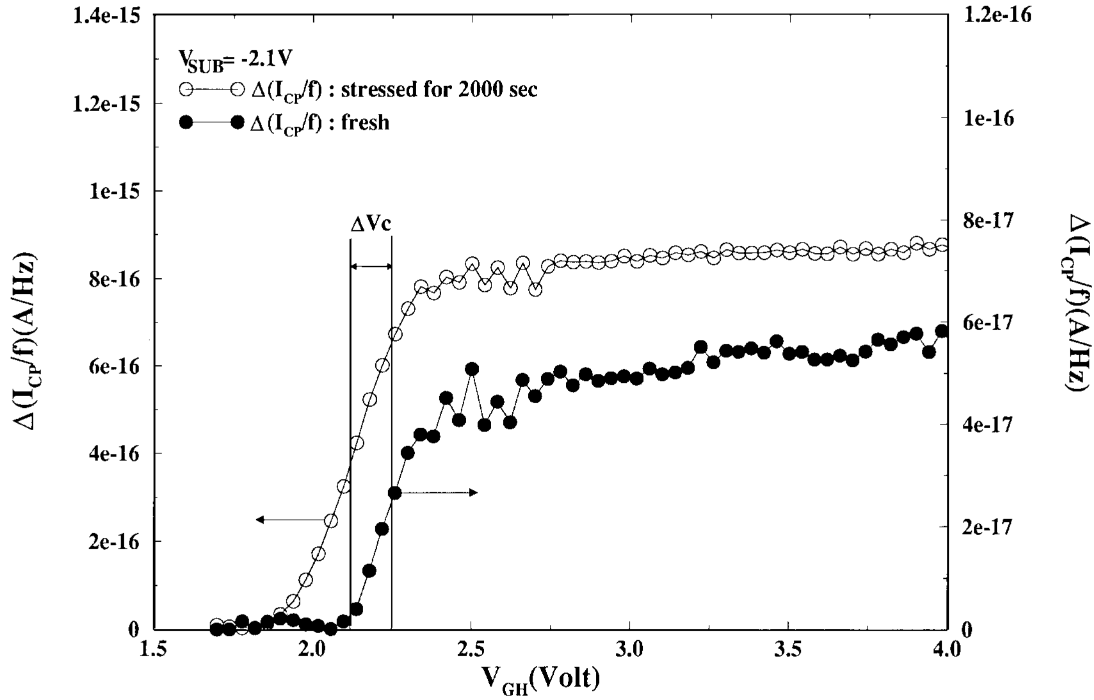


Fig. 2. The determination of ΔV_c induced by the hot-carrier stress.

From (8) and (9), it is clear that $Q_{\rm sat}$ is a function of $V_{\rm SUB}$ through $V_{\rm th}$. The total charge-pumping current per cycle for a device can be written as

$$\frac{I_{\rm cp}}{f}(V_{\rm GL}, V_{\rm SUB}, S_R, S_F) = W\int Q_{\rm sat}(V_{\rm SUB}, S_R, S_F, x)F(V_{\rm GL}, V_{\rm SUB}, x)\,dx \qquad (10)$$

where

$$F(V_{\rm GL}, V_{\rm SUB}, x) = 1 - \exp\left(-\left(\frac{v_{\rm th}\sigma_{p0}}{1-\beta}p_s(V_{\rm GL})T_L\right)^{1-\beta}\right). \qquad (11)$$

If the silicon surface is accumulated at $V_{\rm GL}, F$ is equal to 1 in the middle of the channel and decreases to 0 rapidly at somewhere near the source/drain junction. The principal concept for obtaining the local interface-trap density is to measure the charge-pumping current contributed by a local area. In the previous methods [12], [13], the difference of the charge-pumping current measured with different substrate biases is used to extract the local interface-trap density. However, because $Q_{\rm sat}$ changes with $V_{\rm SUB}$, it becomes difficult to obtain accurately the charge-pumping current difference contributed completely by a local area. Using (8)–(9), it is obvious that if we keep $V_{\rm SUB}, S_R$, and S_F unchanged, then (10) can be expressed as

$$\frac{I_{\rm cp}}{f}(V_{\rm GL}, V_{\rm SUB}) = W\int_{-\infty}^{\infty} Q_{\rm sat}(V_{\rm SUB}, x)F(V_{\rm GL}, V_{\rm SUB}, x)\,dx \qquad (12)$$

and the charge pumping current difference per cycle measured from two low gate voltages (V_{GL1} and V_{GL2}) can be written as

$$\Delta\frac{I_{\rm cp}}{f} = qW(E_2 - E_1)\int_{-\infty}^{\infty} \overline{N_{\rm it}}(F(V_{GL1}, V_{\rm SUB}, x) - F(V_{GL2}, V_{\rm SUB}, x))\,dx. \qquad (13)$$

If the device is symmetrical, (13) can be rewritten as

$$\Delta\frac{I_{\rm cp}}{f} = 2qW(E_2 - E_1)\int_{0}^{\infty} \overline{N_{\rm it}}(F(V_{GL1}, V_{\rm SUB}, x) - F(V_{GL2}, V_{\rm SUB}, x))\,dx \qquad (14)$$

where $x = 0$ is located at the center of the channel. If V_{GL1} and V_{GL2} are low enough to have the accumulated silicon surface, $(F(V_{GL1}, V_{\rm SUB}, x) - F(V_{GL2}, V_{\rm SUB}, x))$ will be a highly localized weighting function near the junction, then we can obtain (15), shown at the bottom of the page, where

$$\overline{N_{\rm it}}(\overline{x}) \simeq \frac{\Delta\frac{I_{\rm cp}}{f}}{2qW(E_2 - E_1)\int_{0}^{\infty}(F(V_{GL1}, V_{\rm SUB}, x) - F(V_{GL2}, V_{\rm SUB}, x))\,dx} \qquad (15)$$

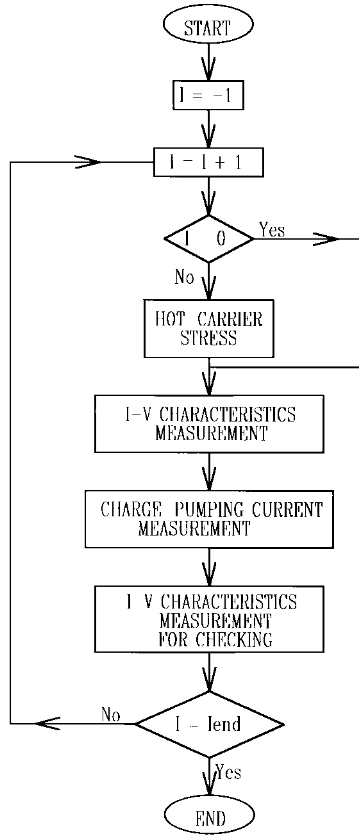


Fig. 3. A flowchart showing the extraction process.

$$\overline{x} = \frac{\int_0^\infty x(F(V_{GL1}, V_{\text{SUB}}, x) - F(V_{GL2}, V_{\text{SUB}}, x))\,dx}{\int_0^\infty (F(V_{GL1}, V_{\text{SUB}}, x) - F(V_{GL2}, V_{\text{SUB}}, x))\,dx}. \tag{16}$$

Note that V_{GH} used to measure $\Delta(I_{\text{cp}}/f)$ should be high enough to strongly invert the silicon surface. Calculating p_s at V_{GL1} and V_{GL2} using a 2-D device simulator, we can obtain interface-trap density distribution using (15).

If there is no long-channel device to extract the parameters (β and σ_{po}), an alternative method can be used. Using the "effective area" approach [16], we have

$$\begin{aligned} F(V_{\text{GL}}, V_{\text{SUB}}, x) &= 0 \quad \text{if } p_s(V_{\text{GL}}, V_{\text{SUB}}, x) > p_c \\ F(V_{\text{GL}}, V_{\text{SUB}}, x) &= 1 \quad \text{if } p_s(V_{\text{GL}}, V_{\text{SUB}}, x) < p_c \end{aligned} \tag{17}$$

TABLE I
DEVICE PARAMETERS OF THE n-MOSFET USED IN THIS PAPER

Parameters \ Device	Conventional n-MOSFET
Flatband Voltage, V_{FB}(Volt)	–0.845
Gate Oxide Thickness, T_{ox}(Å)	143
Source/Drain Junction Depth, r_j(um)	0.22
Lateral S/D diffusion factor, f	0.7
Metallurgical Channel Length, L_{met}(um)	0.58
Substrate Dopant Concentration, N_B(cm^{-3})	3.5E15
Implantation Dose, Φ_1(cm^{-2})	1.04E13
Implantation Depth, R_{p1}(um)	0.51
Standard Deviation of Implantation, ΔR_{p1}(um)	0.75
Contact Resistance, R_{co}(ohm)	4.0

where p_c can be obtained from two MOSFET's with different channel lengths. Using (17), (15) can be rewritten as

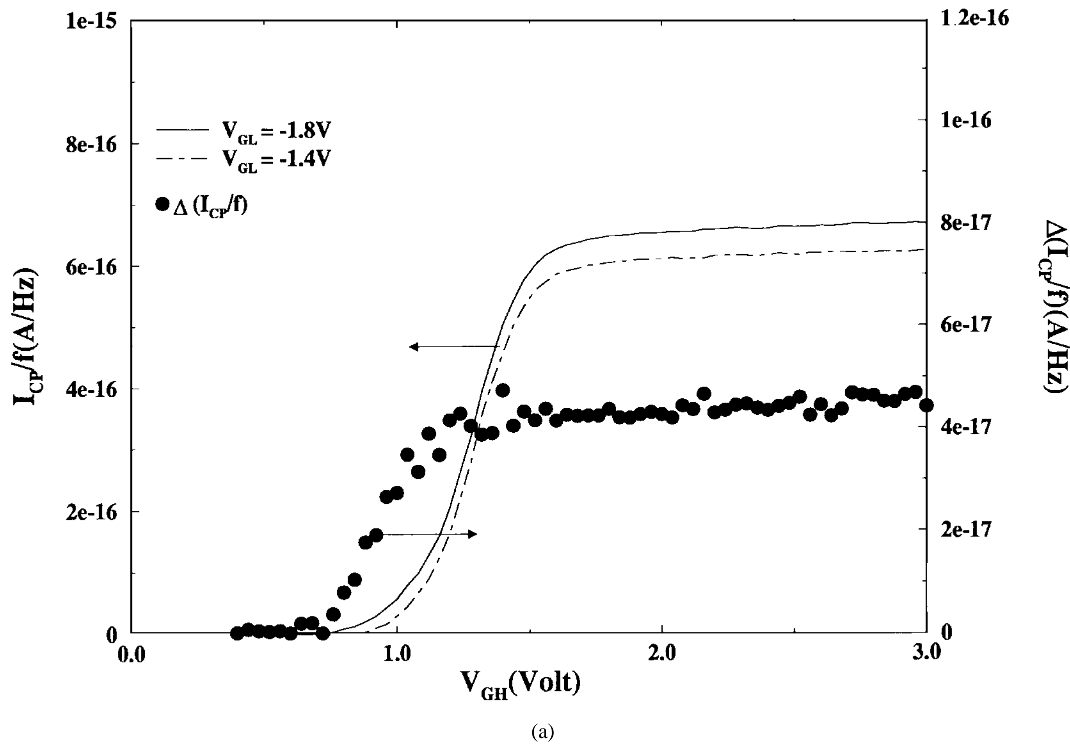
$$\overline{N_{\text{it}}}\left(\frac{x_1 + x_2}{2}\right) \simeq \frac{\Delta \dfrac{I_{\text{cp}}}{f}}{2qW(E_2 - E_1)(x_1 - x_2)} \tag{18}$$

where x_1 and x_2 can be obtained from $p_s(V_{GL1}, V_{\text{SUB}}, x_1) = p_c$ and $p_s(V_{GL2}, V_{\text{SUB}}, x_2) = p_c$. However, the accuracy of (18) becomes poor when the interface-trap density is a fast changing function along the channel direction. Note that (15) and (18) can be used to calculate the interface-trap density of the unstressed devices. For the hot-carrier-stressed devices, one should measure the charge-pumping current before and after stress. Assuming the hot-carrier-induced damages only happen near the drain side, the increased interface-trap density can be written as (19), shown at the bottom of the page, or

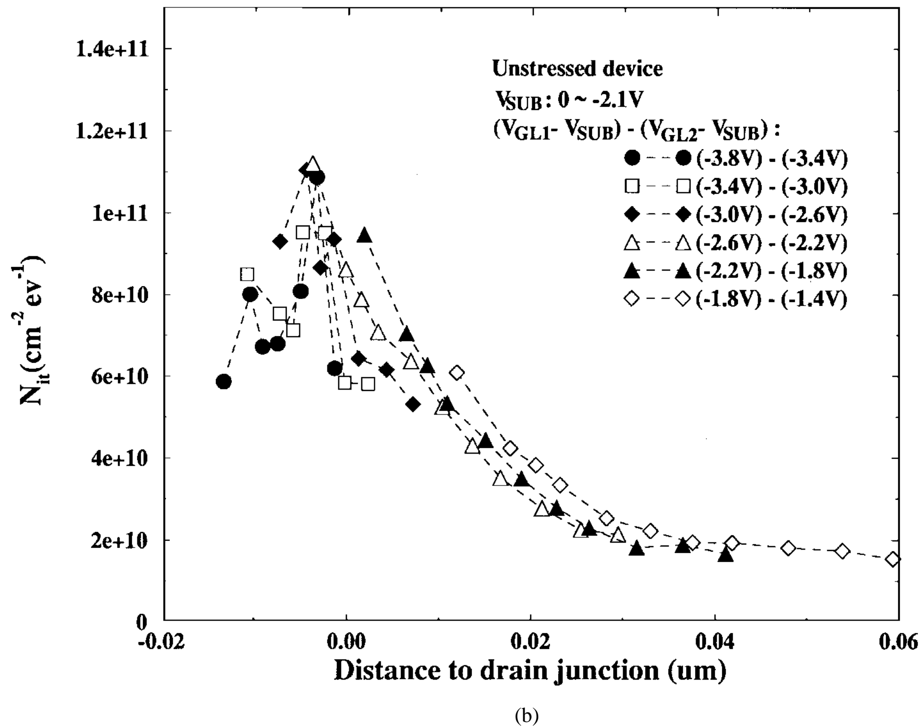
$$\Delta\overline{N_{\text{it}}}\left(\frac{x_1 + x_2}{2}\right) \simeq \frac{\left(\Delta\dfrac{I_{\text{cp}}}{f}\right)_{\text{stressed}} - \left(\Delta\dfrac{I_{\text{cp}}}{f}\right)_{\text{unstressed}}}{qW(E_2 - E_1)(x_1 - x_2)}. \tag{20}$$

Note that the integral range in (19) is limited in the drain side; F is the distribution function after stress, which will be discussed later.

$$\Delta\overline{N_{\text{it}}}(\overline{x}) \simeq \frac{\left(\Delta\dfrac{I_{\text{cp}}}{f}\right)_{\text{stressed}} - \left(\Delta\dfrac{I_{\text{cp}}}{f}\right)_{\text{unstressed}}}{qW(E_2 - E_1)\int_0^\infty (F(V_{GL1}, V_{\text{SUB}}, x) - F(V_{GL2}, V_{\text{SUB}}, x))\,dx} \tag{19}$$



(a)



(b)

Fig. 4. The measured (a) $\Delta(I_{\rm cp}/f) - V_{\rm GH}$ curves and (b) interface-trap density distribution near the source/drain junction before stress.

To check whether the self-consistent result can be obtained, the charge-pumping current can be measured with different substrate biases. To keep the integral range in the bandgap to be the same for all measurements, S_R and S_F should change with $V_{\rm SUB}$ to keep E_2 and E_1 (i.e., $t_{\rm eme}$ and $t_{\rm emh}$) unchanged. According to (8) and (9), S_R and S_F for different $V_{\rm SUB}$ can be approximated as

$$S_R(V_{\rm SUB}) = \frac{V_{\rm th}(V_{\rm SUB}) - V_{\rm FB} + |V_{\rm SUB}|}{V_{\rm th}(0) - V_{\rm FB}} S_R(0) \qquad (21)$$

and

$$S_F(V_{\rm SUB}) = \frac{V_{\rm th}(V_{\rm SUB}) - V_{\rm FB} + |V_{\rm SUB}|}{V_{\rm th}(0) - V_{\rm FB}} S_F(0). \qquad (22)$$

One of the major benefits of the proposed new method using dc source/drain biases and varied $V_{\rm GL}$ is that we can obtain the accurate $\Delta(I_{\rm cp}/f) - V_{\rm GH}$ curves contributed by a small region near the source/drain junction, as shown in Fig. 2. Using the method with ac source/drain biases [13], overshoot or undershoot is usually found in the $\Delta(I_{\rm cp}/f) - V_{\rm GH}$ curves and

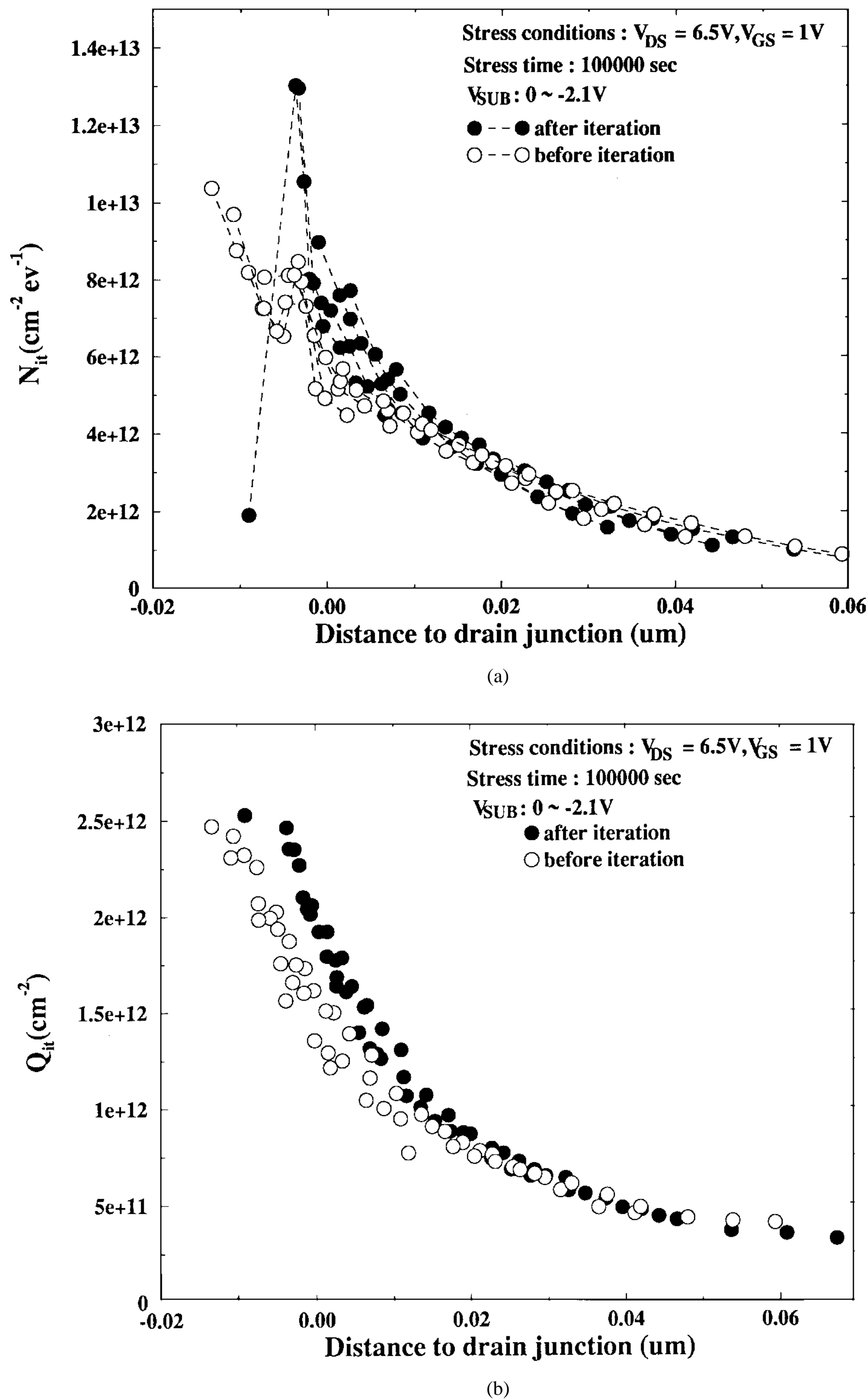


Fig. 5. Comparisons of (a) the interface-trap density and (b) the effective oxide-trapped charges before and after the adjustment of the surface potential changes.

the accuracy of the extracted effective oxide-trapped charge density becomes very poor. The effective oxide-trapped charge density can be derived from the V_c difference after stress

$$Q_{\rm it}(\overline{x}) = \Delta V_c C_{\rm OX} \tag{23}$$

where V_c is the voltage related to the half-maximum value of the $\Delta(I_{\rm cp}/f) - V_{\rm GH}$ curves, as shown in Fig. 2. Note that V_c of the unstressed device is a function of x and will decrease when closing to the drain junction.

In general, adjustment of the surface potential variation after the hot-carrier stress is needed if the induced damages vary the F function in (19) seriously. In that case, the iteration of the F function and the calculated $N_{\rm it}(x)$ and $Q_{\rm it}(x)$ profiles are needed: the F function of the fresh device calculated by a 2-D device simulator is used to calculate $N_{\rm it}(x)$ and $Q_{\rm it}(x)$

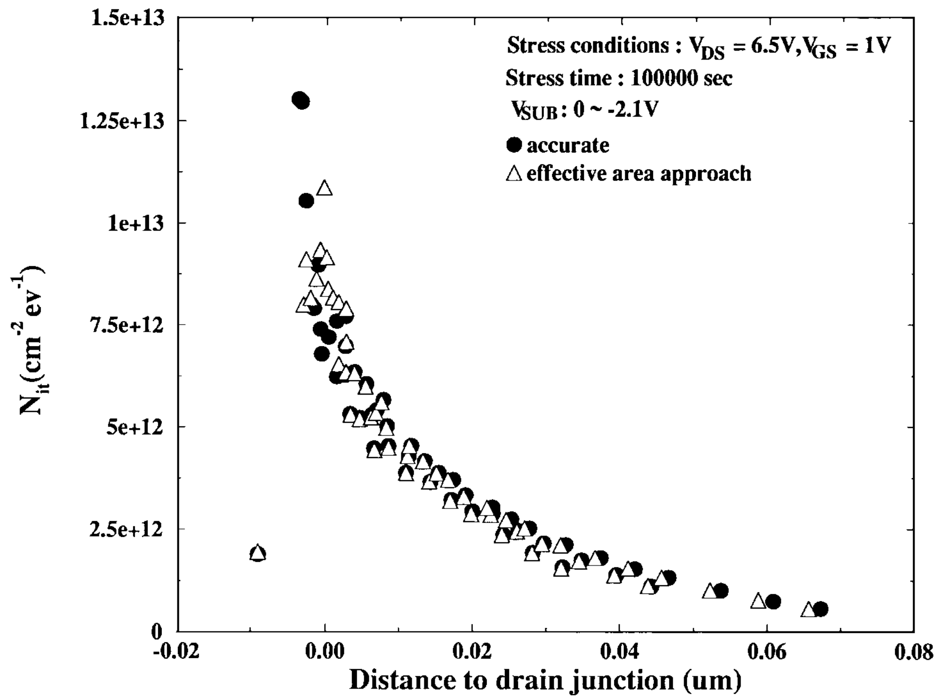


Fig. 6. Comparisons of the interface-trap density distribution obtained from (19) and (20).

initially, and then the calculated $N_{\rm it}(x)$ and $Q_{\rm it}(x)$ are used to simulate the new F function, and the process is repeated until the convergence is obtained. Usually, it takes three or four iterations to derive the final results.

III. Experimental Results and Simulation

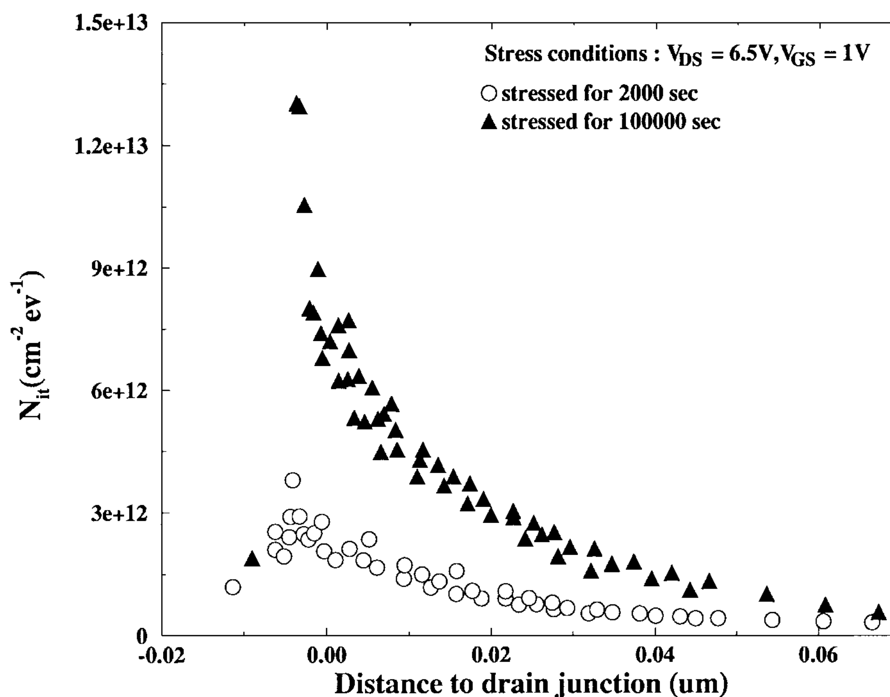
In this section, the hot-carrier stress experiments are presented, the induced interface-trap and effective oxide-trapped charge densities are extracted. The experimental transistor used to demonstrate the novel method proposed in this paper is the same as that used in [14], [16] and is an n-channel MOSFET with the effective channel length of 0.58 μm and the channel width of 100 μm. The device structure parameters given in Table I are measured or extrated for accurately simulating the $I-V$ characteristics of the fresh sample, in which the source/drain junction depth of 0.22 μm was determined by SIMS analysis. Note that the metallurgical junction depth in lateral $(f \cdot r_j)$ is determined by the source/drain junction depth (r_j) and the lateral diffusion factor (f) through $I-V$ simulation. From Table I, it is shown that the location of lateral metallurgical source/drain junction depth is $f \cdot r_j = 0.7 \times 0.22$ μm $= 0.154$ μm, which is only used as the reference point for profiling the distributions of interface trap and oxide-trapped charge. The extraction process for the hot-carrier stress induced $N_{\rm it}$ and $Q_{\rm it}$ is shown in Fig. 3. Note that the $I-V$ characteristics are measured before and after the charge-pumping current measurement to check whether or not the gate pulses used in the charge-pumping current measurement have degraded the device. To our experience, the charge-pumping current measurement could induce the device damages when the surface is strongly accumulated with $V_{\rm GL}$ and the source/drain junction is applied with a high reverse bias. Therefore, this check becomes very important to prevent the wrong analysis for the hot-carrier induced damages. The dc stress conditions used in this work are $V_G = 1$ V, $V_{DS} = 6.5$ V and $V_{\rm SUB} = 0$ V. The charge-pumping current is measured for different stress times to observe the time dependences of interface-trap and oxide-trapped charge generation.

A. $N_{\rm it}$ Distribution of the Unstressed Device

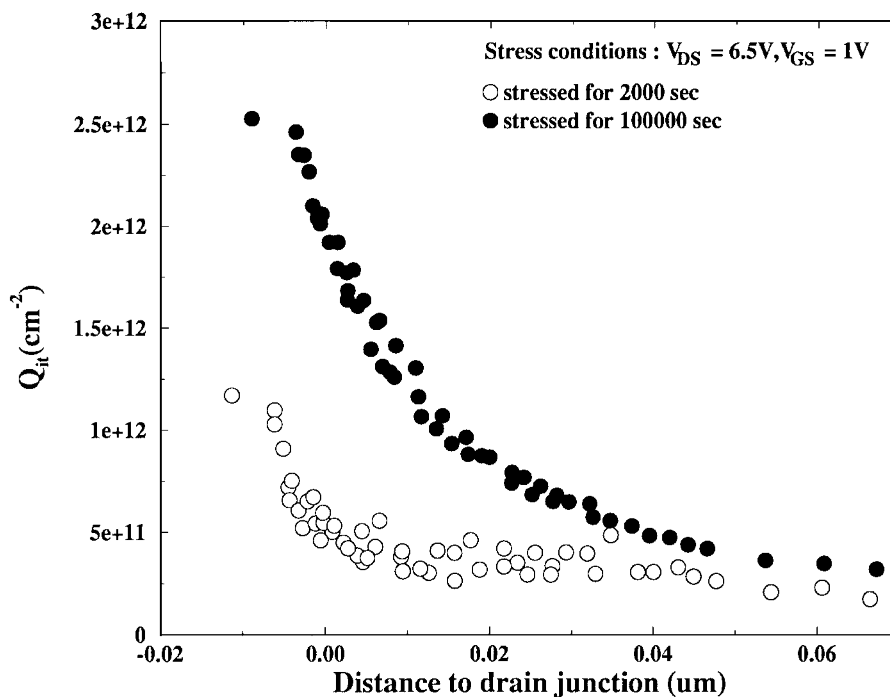
Using (15), the interface-trap density near the junction can be obtained. The $I_{\rm cp}/f - V_{\rm GH}$ curves are measured with $V_{\rm GL}$ varying from $-2.8 + V_{\rm SUB}$ to $-1.2 + V_{\rm SUB}$ and $V_{\rm SUB}$ varying from 0 to -2.7 V. The typical $I_{\rm cp}/f - V_{\rm GH}$ and $\Delta(I_{\rm cp}/f) - V_{\rm GH}$ curves of an unstressed device are shown in Fig. 4(a). It is obvious that the $\Delta(I_{\rm cp}/f) - V_{\rm GH}$ curves obtained from different $V_{\rm GL}$ are smooth and can be used to derive V_c of the unstressed device. The saturation values of the $\Delta(I_{\rm cp}/f) - V_{\rm GH}$ curves are used to calculate $N_{\rm it}$ of the unstressed device, and both $S_R(0)$ and $S_F(0)$ are 2E6 V/s. As shown in Fig. 4(b), the $N_{\rm it}$ distributions derived from different $V_{\rm GL}$ and $V_{\rm SUB}$ are self-consistent, and this means that the developed technique is stable and reliable. It is clearly shown that the interface-trap density is constant in the center of the channel and increases when closing to the source/drain junction, and the peak value appears at the proximity of the junction. It is the first time that the spatial interface-trap density distribution of an unstressed device can be measured so well.

B. Spatial Distributions of $N_{\rm it}$ and $Q_{\rm it}$ Induced by Hot-Carrier Stress

The process of the charge-pumping current measurement for the stressed MOSFET devices is the same as that of the



(a)



(b)

Fig. 7. The extracted (a) interface-trap density and (b) effective oxide-trapped charges for different stress times.

unstressed case, but (19) and (23) are used for N_{it} and Q_{it} extractions. Because serious positive oxide-trapped charges are found after stress and the change of the surface potential near the drain junction cannot be ignored. Therefore, the iteration process mentioned in the previous section is necessary to obtain the accurate distribution. At the beginning, the F function of the unstressed device is used to calculate N_{it} and Q_{it}, and after four iterations, the calculated N_{it} and Q_{it} values have converged to the stable values, and the values derived from different measuring conditions are shown to be self-consistent, as shown in Fig. 5. The N_{it} distribution derived from (20) is shown in Fig. 6 and is compared to that derived from (19), it is obvious that the difference appears at the proximity of the drain junction because of the inharmonious N_{it} distribution near the drain junction. Therefore, (20) is a good approximation only for the case with smooth N_{it}

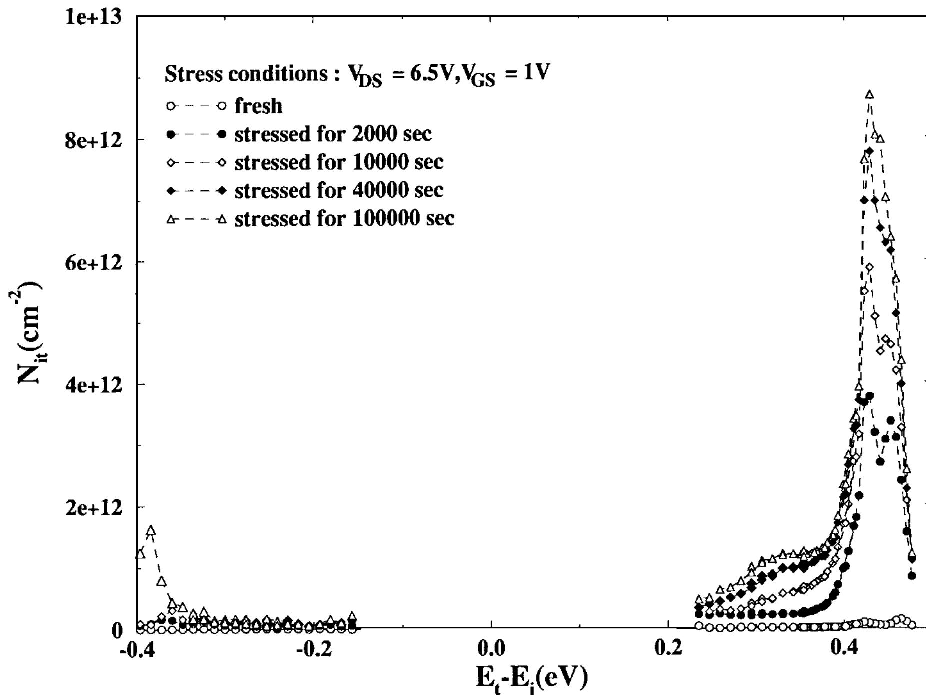


Fig. 8. The measured interface-trap density distribution in the bandgap for different stress times.

distribution. Note that the similar "effective area" approach for (20) had been used in all previous works to extract the spatial $N_{\rm it}$ distribution, and this approach could induce obvious error because the peak of the $N_{\rm it}$ distribution will be smoothed out. The $N_{\rm it}$ and $Q_{\rm it}$ distributions after several stress times are shown in Fig. 7. Although the structure parameters shown in Table I have two decades numeral, they are only used to determine the reference point ("0" point) in lateral. The spatial distributions of interface-trap and effective oxide-trapped charge densities relative to the reference point ("0" point) are computed iteratively by the charge-pumping equations given in Section II from the measured charge-pumping data; therefore, the resolution of three-decades numeral can be obtained. Note that the peak $N_{\rm it}$ profiled by our novel charge-pumping technique isn't located at the lateral drain junction, but is located in the gate-overlapped drain. This phenomenon is reasonable because the nonlocal effect [17], [18] of hot electrons will displace the peak distribution of hot electrons from the peak lateral electric field. The distance from the lateral drain junctions and the generated peak interface traps is about 0.003 μm (30 Å) and this magnitude is approximately equal to the mean-free-path of hot electron and optical surface-phonon scattering.

C. Energy Distribution of $N_{\rm it}$ in the Bandgap

Assuming that the energy distribution is independent of the spatial position, the distribution of $N_{\rm it}$ in the upper part of the bandgap can be expressed as [11]

$$\overline{N_{ite}}(E_2) = -\frac{t_f}{qWfkT\int F(V_{\rm GL}, V_{\rm SUB}, x)\,dx}\frac{dI_{\rm cp}}{dt_f} \quad (24)$$

and that in the lower part of the bandgap can be expressed as

$$\overline{N_{ite}}(E_2) = -\frac{t_r}{qWfkT\int F(V_{\rm GL}, V_{\rm SUB}, x)\,dx}\frac{dI_{\rm cp}}{dt_r}. \quad (25)$$

Note that measuring the energy distribution of interface traps after the hot-carrier stress is useful for the 2-D numerical simulation of the stressed IV characteristics. The extracted distributions related to several stress times are shown in Fig. 8. There appear two peaks in the upper band, this means that there are two kinds of major interface-traps generated during the hot-carrier stress.

IV. Conclusions

An accurate and reliable charge-pumping method using dc source/drain biases is developed to extract the lateral distributions of both interface-trap and effective oxide-trapped charge densities. Using the specified gate pulses with fixed T_H, T_L, and the varied S_R, S_F with $V_{\rm SUB}$, the smooth $\Delta(I_{\rm cp}/f) - V_{\rm GL}$ curves related to a localized area near the drain(source) junction can be easily obtained and the interface-trap and effective oxide-trapped charge densities related to this area can be calculated at the same time. The effects of the hot-carrier-stress induced $N_{\rm it}$ and $Q_{\rm it}$ on the surface potential are considered in this work to derive the accurate results. It is shown that the $N_{\rm it}$ and $Q_{\rm it}$ distributions derived from different $V_{\rm GL}$ or $V_{\rm SUB}$ are self-consistent. It should be emphasized that the developed method can also be applied to p-channel or LDD MOSFET's. Therefore, the developed novel charge-pumping method will give the accurate analysis of the hot-carrier

generated interface-trap and oxide-traps, which becomes the basis for future hot-carrier lifetime prediction.

REFERENCES

[1] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Trans. Electron Devices*, vol. 36, pp. 1318, 1989.
[2] J. S. Burgler and P. G. Jespers, "Charge pumping in MOS devices," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 297, 1969.
[3] A. B. Elliot, "The use of charge pumping currents to measure surface state densities in MOS transistors," *Solid-State Electron*, vol. 19, pp. 241, 1976.
[4] T. J. Russ L. Wilson, and M. Gaitan "Determination of the spacial variation of interface trapped charge using short-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1662, 1983.
[5] G. Groeseneken, H. Maes, N. Beltran, and R. DeKeersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 42, 1984.
[6] U. Cilingiroglu, "A general model for interface-trap charge-pumping effects in MOS devices," *Solid-State Electron.*, vol. 28, pp. 1127, 1985.
[7] W. L. Tseng, "A new charge pumping method of measuring Si-SiO_2 interface states," *J. Appl. Phys.*, vol. 62, pp. 591, 1987.
[8] F. Hofmann and W. H. Krantschneider, "A simple technique for determining the interface trap distribution of submicron MOS transistors by the charge pumping method," *J. Appl. Phys.*, vol. 65, pp. 1358, 1989.
[9] J. E. Chung and R. S. Muller, "The development and application of a Si-SiO_2 interface-trap measurement system based on the staircase charge-pumping technique," *Solid-State Electron.*, vol. 32, pp. 867, 1989.
[10] N. S. Saks and M. G. Ancona, "Determination of interface trap capture cross sections using three-level charge pumping," *IEEE Electron Device Lett.*, vol. 11, pp. 339, 1990.
[11] G. Van den Bosch, G. V. Groeseneken, P. Heremans, and H. E. Maes, "Spectroscopic charge pumping: A new procedure for measuring interface trap distributions on MOS transistors," *IEEE Trans. Electron Devices*, vol. 38, pp. 1820, 1991.
[12] M. G. Ancona, N. S. Saks, and D. McCarthy, "Lateral distribution of hot-carrier-induced interface traps in MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, pp. 2221, 1988.
[13] W. Chen and T. P. Ma, "A new technique for measuring lateral distribution of oxide Charge and Interface traps near MOSFET junctions," *IEEE Electron Device Lett.*, vol. 12, pp. 393, 1991.
[14] H. H. Li and C. Y. Wu, "A new simplified charge-pumping current model and its model parameter extraction," *IEEE Trans. Electron Devices*, vol. ED-43, p. 1857, 1996.
[15] P. Habas, "Charge-pumping characteristics of virgin and stressed lightly doped drain MOSFET's," *Solid-State Electron.*, vol. 33, pp. 287, 1995.
[16] H. H. Li and C. Y. Wu, "A novel extraction technique for the effective channel length of MOSFET devices," *IEEE Trans. Electron Devices*, vol. 42, pp. 856, 1995.
[17] N. Goldsman and J. Frey, "Efficient and accurate use of the energy transport method in device simulation," *IEEE Trans. Electron Devices*, vol. 35, pp. 1524, 1988.
[18] D. Chen, E. C. Kan, U. Ravaioli, C. W. Shu, and R.W. Dutton, "An improved energy transport model including nonparabolicity and non-Maxwellian distribution effects," *IEEE Electron Device Lett.*, vol. 13, pp. 26, 1992.

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