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The fabrication of a programmable via using phase-change material in CMOS-compatible technology

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Abstract
We demonstrate an energy-efficient programmable via concept using indirectly heated phase-change material. This via structure has maximum phase-change volume to achieve a minimum on resistance for high performance logic applications. Process development and material investigations for this device structure are reported. The device concept is successfully demonstrated in a standard CMOS-compatible technology capable of multiple cycles between on/off states for reconfigurable applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

A programmable via using phase-change materials is an enabling technology for high performance reconfigurable logic applications with disruptive improvements in area and power efficiencies. Reconfigurable circuits play important roles in a wide range of microelectronic applications, such as repair of defective memory elements [1, 2] and field-programmable gate arrays (FPGAs) [3]. For repair of defective memory elements, the anti-fuse approach, often applied to DRAM repair, and the electrical fuse (eFUSE) are utilized for programmable circuits. However, both structures can be only used once and require high programming voltages [1, 2] or currents [4–6]. Regarding the FPGA concept, an array of configurable logic blocks is arranged with switches to rearrange the interconnections between the logic blocks. However, current FPGAs use flash memory and require extra space for the flash transistor. In particular, the process is not standard CMOS-compatible. Therefore, it can be seen that the current challenges for programmable circuits include 'multiple operation' and 'CMOS-compatible fabrication'.

To date, phase-change materials have drawn the most attention from semiconductor memory developers as a possible replacement for flash memory [7–10]. In contrast to phase-change memory, in which the phase-change volume is to be minimized for the smallest possible memory cell size, the volume of the phase-change material in a programmable via is to be maximized for the lowest contact resistance. In this paper, we introduce and review an indirect-heating concept to fabricate a programmable via with minimal consuming area [10]. Logic circuits associated with the programmable via are decoupled from the configuration circuits by using an independently contacted heater electrode. Since this device structure can be fabricated with CMOS-compatible processes and can be operated for multiple cycles between OFF/ON (RESET/SET) states, it shows the great potential in future reconfigurable applications. In addition, process development and material investigations of this device are reported.

2. Concept of the device structure

The schematic diagram of this programmable via device structure is shown in figure 1. The via is filled with phase-change material ($Ge_2Sb_2Te_5$), which can be switched between resistive (OFF–amorphous–RESET) and conductive (ON–crystalline–SET) states. An external heater using doped TaN material is integrated with the programmable via. The switching process is based upon the 'programming' current pulse passed through the heater. During the OFF switching operation, an abrupt high-current pulse is used to melt and quench/amorphize a thin region of phase-change via adjacent to the heater. The ON switching operation is accomplished by

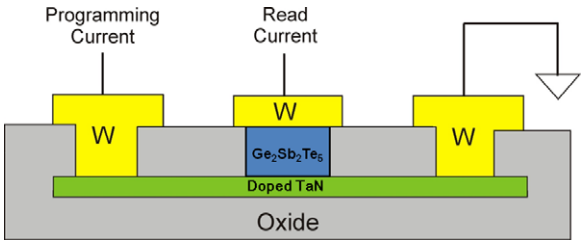

Figure 1. Schematic diagram of the programmable via concept using phase-change material ($Ge_2Sb_2Te_5$) and indirect-heating material (doped TaN). Tungsten (W) is used for electrical connection.

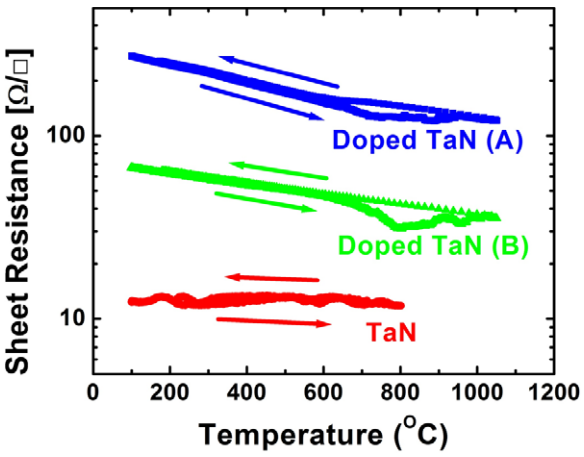

Figure 2. Sheet resistance behaviors of pure and doped TaN materials during temperature operation.

a relatively low but long current pulse applying through the heater. The heat generating from the current on the heater is capable of annealing the amorphous phase-change materials to the crystalline state. It should be noted that, in this concept demonstration, the via resistance has been measured between the top contact of the via and one of the heater contacts by a 'read' current, as shown in figure 1.

For the heater design, in order to achieve the best efficiency of electrical–thermal transformation from heater to via, the heater should be a thin layer and its material should be a refractory metal with relatively high resistivity and low thermal conductivity. Therefore, a doped TaN material is used as the heater because of its low thermal conductivity and high sheet resistance [11]. Figure 2 shows two examples of doped TaN materials with different doping concentrations.

3. Device fabrication

The device fabrication includes three sections using a standard CMOS technology: (a) heater, (b) programmable via and (c) electrical connection. First, the heater fabrication started from deposition of the doped TaN film above the silicon oxide film on the Si wafer. After the pattern of the heater was defined on the doped TaN film by RIE (reactive ion etching), another silicon oxide film was deposited to cover the heater.

The programmable via fabrication was followed by the heater fabrication. The via was defined by lithographic process

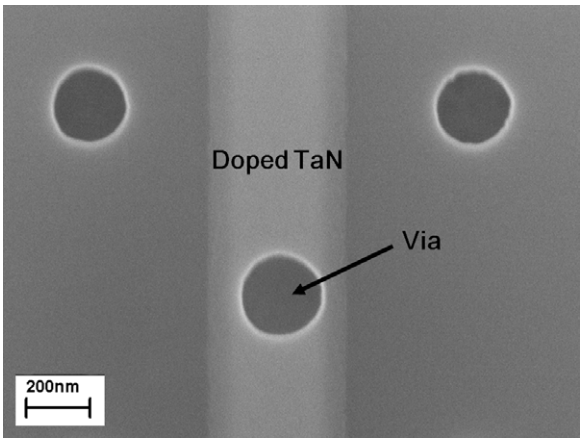

Figure 3. SEM image showing the via hole clearly defined on the doped TaN heater region.

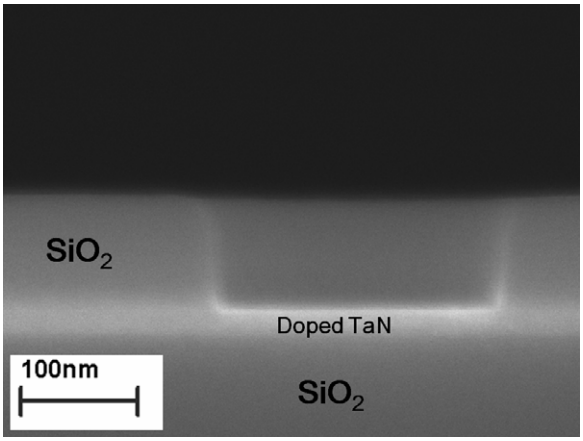

Figure 4. Cross-sectional SEM image showing that the bottom of the via hole lands well on top of the doped TaN heater.

then etched by RIE. The etched process required a good etching selectivity between oxide and doped TaN. Figures 3 and 4 show the via hole is clearly defined and its bottom lands well on top of the doped TaN heater. The aspect ratio of the via is better than 1:1, which is helpful for the later phase-change material ($Ge_2Sb_2Te_5$) deposition. After depositing TiN (diffusion barrier), Ti (adhesion layer) and $Ge_2Sb_2Te_5$ onto the via, a CMP (chemical–mechanical polishing) process was performed to removed $Ge_2Sb_2Te_5$/Ti/TiN materials outside the via. In order to prevent any contamination into the $Ge_2Sb_2Te_5$ via, a TiN cap layer, which was designed to be larger than via size, was fabricated to fully coverage the $Ge_2Sb_2Te_5$ via. Figures 5 and 6 show SEM images of device structures after the cap layer was fabricated. During the $Ge_2Sb_2Te_5$/Ti/TiN CMP process, when the CMP polishing pad was reaching the oxide surface, the polishing rate of $Ge_2Sb_2Te_5$ in the via was higher than that of oxide. This rate difference led to the via level lower than the adjacent oxide level after the CMP process. Therefore, it can be seen that the central region of the cap layer, which is corresponding to the via area, is lower than the adjacent region, as shown in figure 6.

The final section of device fabrication is electrical connection. Two W vias were fabricated to connect the

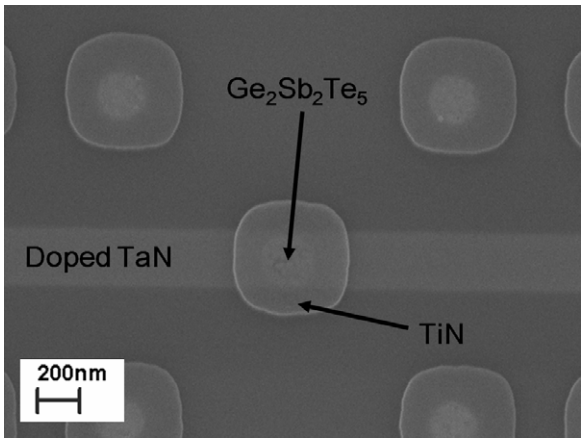

Figure 5. Top-down SEM image of the device structure after the cap layer was fabricated.

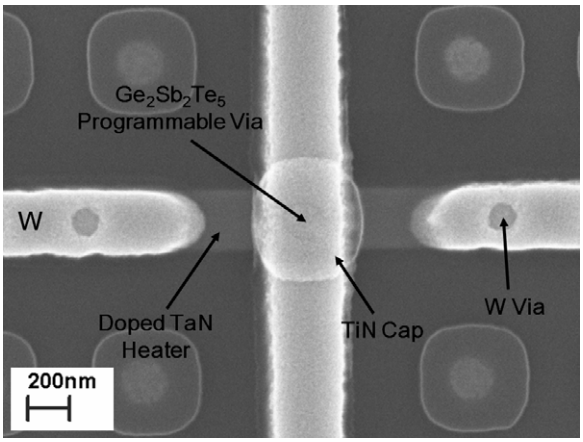

Figure 7. SEM image of the programmable via region of the final device.

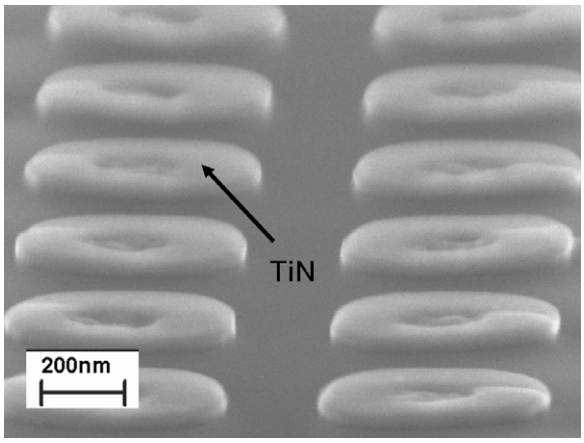

Figure 6. SEM image of the device structure after the cap layer was fabricated. The central region of the cap layer, which is corresponding to the via area, is lower than the adjacent region.

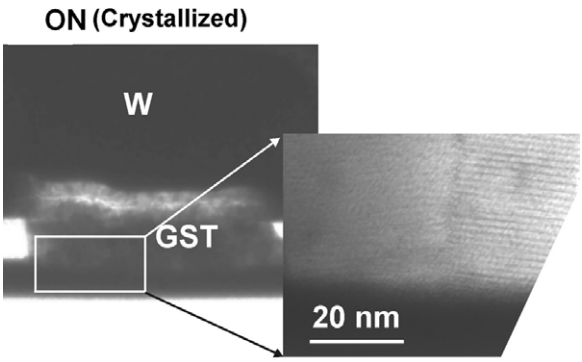

Figure 8. Cross-sectional TEM image of the via–heater interface region after ON switching operation.

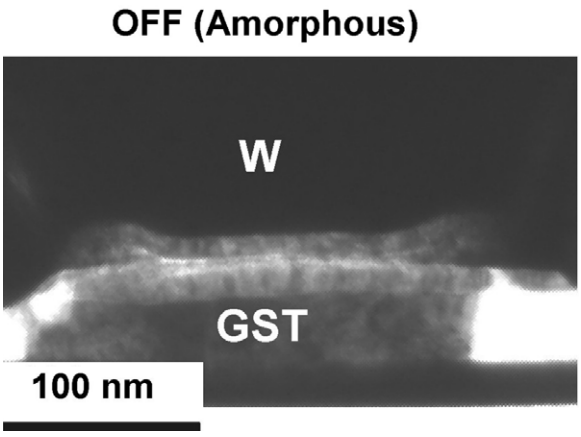

Figure 9. Cross-sectional TEM image of the via–heater interface region after OFF switching operation.

heater for electrical current delivery in the heater. The device structure was completed after the testing W pads were fabricated. Figure 7 shows the SEM image of the programmable via region of the final device. Vias with diameters of 200–280 nm were fabricated atop 20 nm thick TaN heaters that had the same width as the via diameter, and a length-to-width ratio of 6. The resistance of the doped TaN heater is ∼1700 Ω and the resistivity of the doped TaN is 6×10^{-4} Ω cm.

4. Electrical characterization

Figure 8 shows a TEM image of the via/heater interfacial region after ON switch operation. Clear crystalline and grain structures of the phase-change material are observed near the heater interface after the ON operation, indicating a crystalline state. Figure 9 shows a TEM image of the via/heater interfacial region after OFF switch operation. No crystalline and grain structure of the phase-change material are observed near the heater interface after the OFF operation, indicating an amorphous state.

Figures 10 and 11 show the R–I switching characteristics of the programmable via without device history. In figure 10, starting from the OFF state, 1 μs pulses with gradually increased power were applied to the heater. When the pulse current reached around 0.9 mA, the via resistance started to

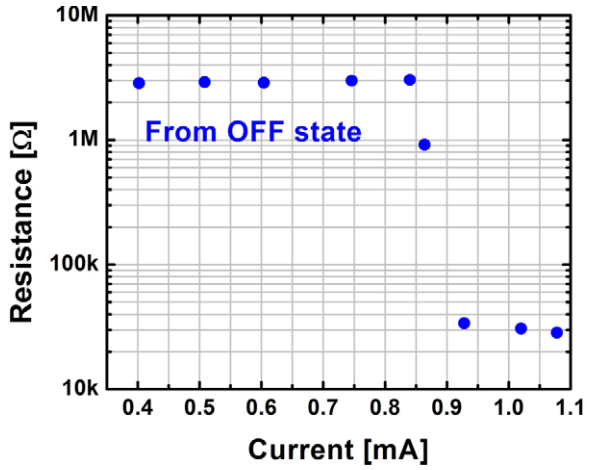

Figure 10. *R–I* characteristics for switching to the ON state. Via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm. ON pulse = 200 ns ramp up + 1000 ns plateau + 200 ns ramp down.

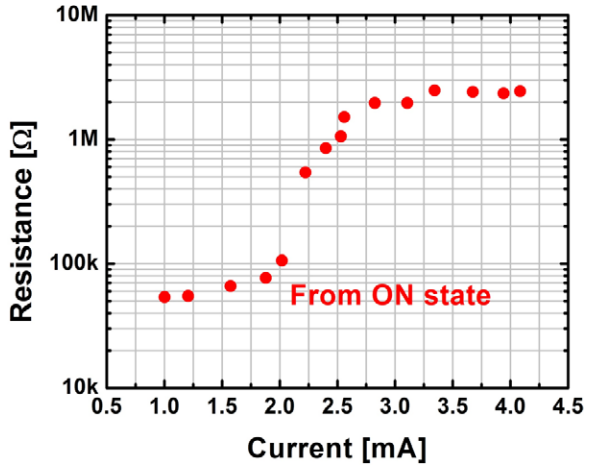

Figure 11. *R–I* characteristics for switching to the OFF state. Device geometry is as listed in the caption of figure 10. OFF pulses are 19 ns rise time and 2 ns fall time.

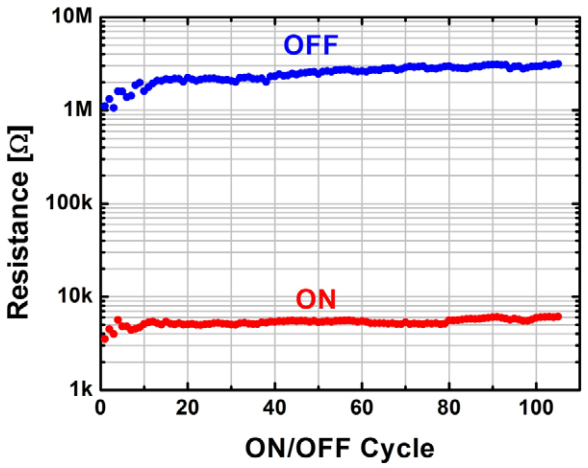

Figure 12. Cycling data from endurance tests at room temperature. Device geometry and pulse conditions are as listed in the captions of figures 10 and 11.

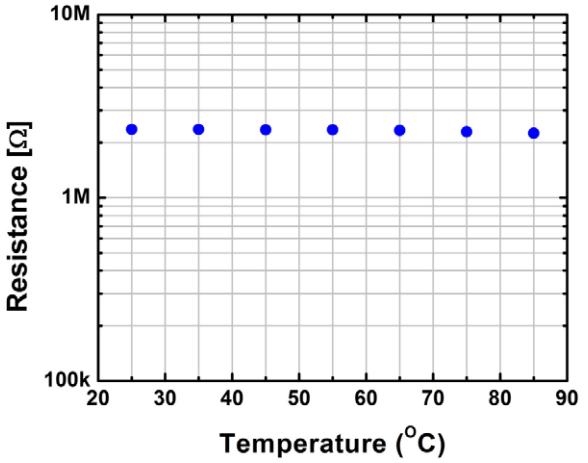

Figure 13. Measured temperature dependence of resistance in OFF state.

decrease and finally implemented switching of the device to the ON state. In figure 11, 50 ns pulses with gradually increased power were applied to the heater from the ON state. After each pulse, the via was switched back to the ON state. When the pulse current reached around 2 mA, the via resistance started to increase and finally reached the OFF state. The endurance test results in figure 12 show stable OFF/ON ratios around 400 without obvious degradation. An estimated OFF/ON ratio of an ideal four-terminal device can reach 1000 when resistance contribution from the heater to ON resistance becomes small. The temperature dependence of resistance in the OFF state is shown in figure 13.

5. Simulation

In order to further understand the behavior and predict the performance of this energy-efficient programmable via structure, several simulations were performed and compared with the experimental results of the prototype device. Figure 14 shows simulated required OFF current and programmable via dimension. Here via size = heater width = 1/6 × heater length; heater thickness = 20 nm; 50 ns width OFF pulses with 19 ns rise time and 2 ns fall time. The experimental data of this device structure is also marked in the figure, showing good prediction. Figure 15 shows the simulated OFF current and pulse time at plateau. Here, via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm. OFF pulses were 19 ns rise time and 2 ns fall time. Again, the experimental data, as marked in the figure, showing good prediction within reasonable range from the simulation. These simulation results provide references for future device performance predictions.

6. Conclusions

A programmable via using an indirectly heated phase-change switch is proposed and demonstrated in this paper. In addition

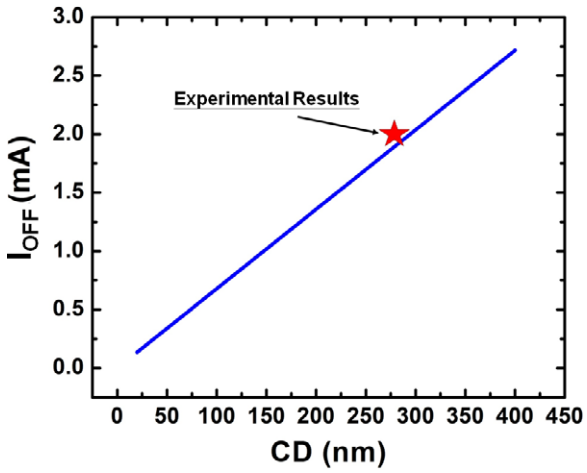

Figure 14. Simulated required OFF current and programmable via dimension. Via size = heater width = 1/6 × heater length; heater thickness = 20 nm; 50 ns width OFF pulses with 19 ns rise time and 2 ns fall time.

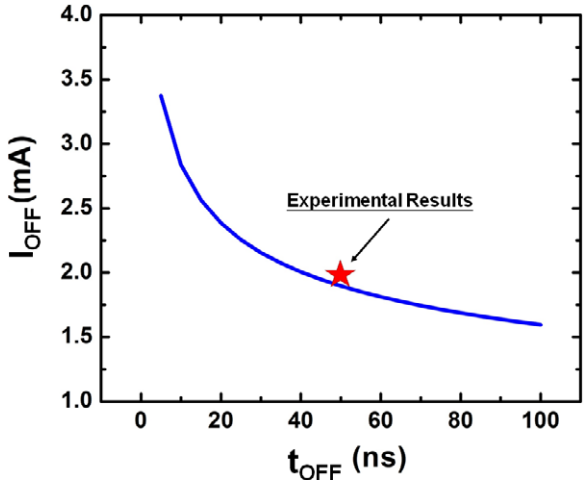

Figure 15. Simulated OFF current and pulse time at plateau. Via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm; OFF pulses with 19 ns rise time and 2 ns fall time.

to excellent electrical characterization, the device fabrication is processed in a standard CMOS technology and the device is capable of multiple operations. Therefore, this structure can be utilized for reconfigurable logic applications. Finally the good experimental data matching the simulated results demonstrates the feasibility of advanced device applications.

Acknowledgments

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