Wide-IF-Band CMOS Mixer Design

Pei-Yuan Chiang, Chao-Wei Su, Sz-Yun Luo, Robert Hu, and Christina F. Jou

***Abstract*—A wide-IF-band transistor mixer has been designed using a 0.13-μm RF-CMOS process where its RF frequency is 8.7–17.4 GHz, local oscillator (LO) fixed at 17.4 GHz, and IF up to 8.7 GHz. Proper layout arrangement for the Marchand balun has been discussed and then implemented; the output amplitude and phase imbalance are less than 0.5 dB and 1° measured in the RF bandwidth. Related theories for the core mixing circuit are explored extensively and verified through simulation; broad bandwidth of the resistive double-balanced mixer is then confirmed in the IF aspect. The designed mixer has more than 10-dB conversion gain, matched RF, IF, and LO ports, and good port isolation over the intended wide bandwidth. The input-referred P1 dB is −17.5 dBm at 9 GHz and −16 dBm at 13 GHz. The third-order input intercept point is −6 dBm at 9 GHz and −5 dBm at 13 GHz. The noise figure is 7 dB at 9 GHz and 12.6 dB at 13 GHz. The power consumption is 40 mW for this 1.3-mm^2 mixer chip.**

***Index Terms*—Conversion matrix, Marchand balun, wideband mixer.**

I. Introduction

IN DEVELOPING the millimeter-wave array for efficient and accurate detection of the anisotropy of cosmic microwave background radiation across the W-band, the front-end receivers of the array are preferred to be wideband [1]. As for the system shown in Fig. 1, the incoming 78–113-GHz radio-astronomical signals will first be cryogenically amplified and down-converted to quasi-dc–34.8 GHz. Four adjacent bands of 8.7 GHz each can then be separated and extracted simultaneously using power dividers, bandpass filters, and low-pass filters, amplifiers, and three mixers of wide IF bandwidth. For example, the first such wide-IF-band mixer needs to have its RF cover 8.7–17.4 GHz, local oscillator (LO) frequency fixed at 17.4 GHz, and IF equal to dc–8.7 GHz; the second and third mixers will have the same 8.7-GHz IF bandwidth, but with RF of 17.4–26.1 and 26.1–34.8 GHz, respectively. In terms of absolute or the more restricting relative IF bandwidth, it seems resistive diode mixers made of compound semiconductors can best fulfill this wideband requirement while keeping low power consumption. Successfully delivering though they have been,

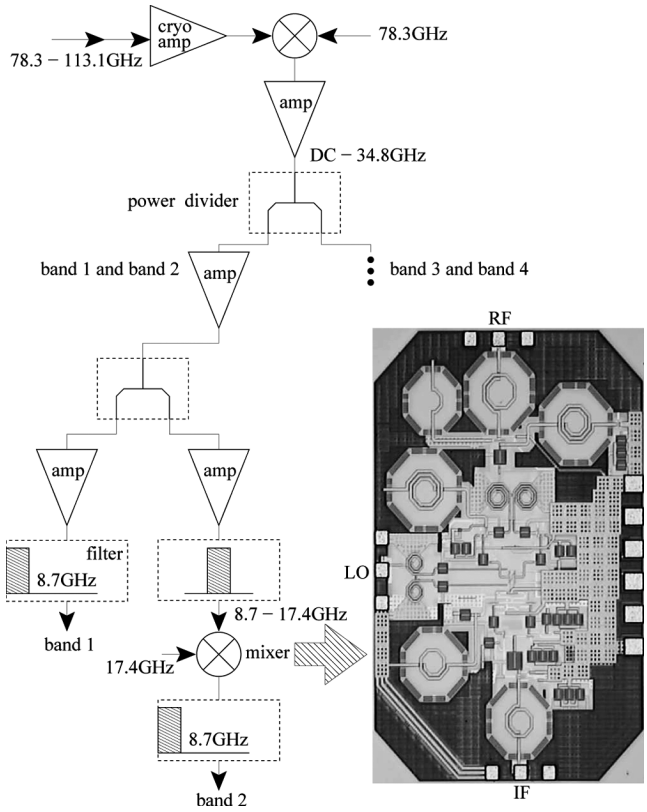

Fig. 1. Schematic of the wideband receiver. The incoming 78–113-GHz signal will be cryogenically amplified, down-converted, and split into four adjacent bands. The wide-IF-band mixer used for band 2 needs to have both its RF and IF bandwidth equal to 8.7 GHz at least, and LO fixed at 17.4 GHz. Also shown is a photograph of our designed wide-IF-band mixer using commercial 0.13-μm RF-CMOS process.

these diode mixers nonetheless have discernible conversion loss, moderate port isolation, and poor input matching for all three RF, IF, and LO ports. On the other hand, transistor mixers made of silicon-related processes continue pushing their operating frequencies and promise further integration with other circuits like amplifiers, oscillators, and even antennas [2]–[7]. All this, therefore, prompts us to the challenge of designing a well-performing wide-IF-band transistor mixer using a commercial RF-CMOS process. Since most of the transistor mixers tend to have their wideband proclamation illustrated by shifting the LO frequency across the intended RF frequency range while keeping the IF bandwidth relatively small, these mixers are, in fact, of wide RF band, but narrow IF band; therefore, not all the design techniques for mixers can be freely adopted here. For instance, to boost the conversion gain of a double-balanced mixer and suppress the unwanted common-mode signals, a differential-pair with current source and active load can be used in the IF stage. With increasing IF frequency, however, this approach starts losing its appeal, as the output impedance of

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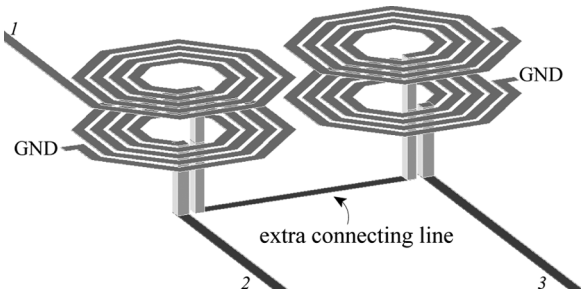

Fig. 2. Broadside-coupled Marchand balun with extra connecting line between the spirals. Port 1 is the input; port 2 and port 3 are the output. The existence of this extra connecting line will affect the output amplitude and phase imbalance.

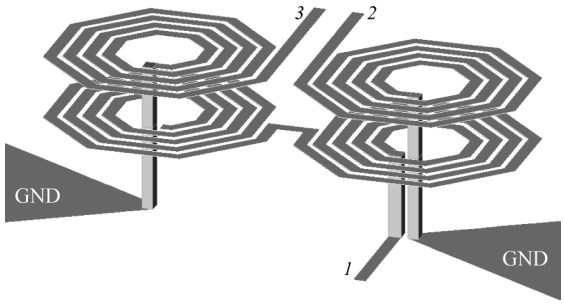

Fig. 3. Proposed broadside-coupled Marchand balun with no connecting line between the spirals. Port 1 is the input; port 2 and port 3 are the output.

both the current source and active load diminish rapidly with increasing frequency. Likewise, to obtain large conversion gain in the case of narrow IF band, a finite drain–source bias voltage $V_{\rm ds}$ is opted for the core mixing transistors. In this paper, we are going to demonstrate that the zero-$V_{\rm ds}$, i.e., resistive bias scheme can simply be used for achieving wide IF bandwidth, even though this peculiar bias scheme is originally proposed for its high linearity [8], [9].

To simplify the circuit analysis and design, the proposed mixer is divided into three parts. The first is the input RF circuit where the incoming 8.7–17.4-GHz signal will be amplified and transformed into its differential-mode counterpart by a passive wideband balun. The second is the core mixing circuit where the resistive double-balanced circuit configuration is employed. Here we will focus on the derivation of the closed-form expression for the mixing circuit's conversion resistance, as the mathematics involved can best illustrate the wide-IF-band property of this mixer. The third is the output IF circuit where the differential-mode IF signal of dc–8.7 GHz will be merged and amplified. Layout and measured results of the mixer are then presented and compared, whenever possible, with the simulated ones. Though initiated by our own scientific mission, knowledge, and experience gained in designing this wide-IF-band mixer will be invaluable for the further development of wideband surveillance and communication industries in the near future.

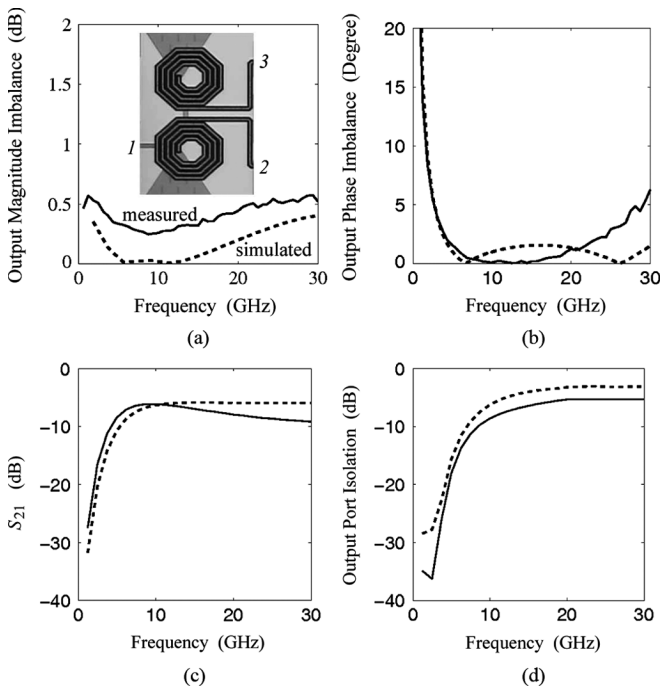

Fig. 4. Measured and simulated results of our proposed 8.7–17.4-GHz balun, where the solid curves are the measured results and the dotted curves are the simulated counterparts. (a) Output magnitude imbalance. Also shown is the photograph of the fabricated balun. (b) Output phase imbalance. (c) Magnitude of S_{21} in decibels. The measured and simulated S_{31} curves are not shown here since they are inseparable from their respective S_{21} curves. (d) Output port isolation, i.e., magnitude of S_{32}, in decibels.

II. Wide-IF-Band Mixer Design

A. Input RF Circuit Design

The most critical component in the input RF circuit of a double-balanced mixer is the balun that converts the single-ended signal into its differential-mode counterpart, and here we use the Marchand balun, which, ideally, can have its S_{21} and S_{31} expressed as

$$S_{21} = j\frac{2C\sqrt{1-C^2}}{1+C^2} = -S_{31} \tag{1}$$

where C is the coupling coefficient of the constituting coupled lines [10]–[12]. By setting $C = 1/\sqrt{3}$, there will be $S_{21} = -S_{31} = j/\sqrt{2}$. In the layout arrangement shown in Fig. 2, an extra connecting line needs to be used to form a complete balun. If we designate the transmission coefficient of this additional nonreflective line segment as t, which takes into account the corresponding signal loss and phase delay, and define T as $-j\sqrt{1-C^2}$, we then have

$$\begin{aligned} S_{21} &= -CT + \frac{CT^3t}{1+C^2} \\ S_{31} &= CTt - \frac{CT^3t}{1+C^2}. \end{aligned} \tag{2}$$

Thus, with nonunitary t, the two output signals are no longer of equal magnitude and 180° out-of-phase.

On the other hand, if the layout for the balun is arranged such as that shown in Fig. 3, then the extra connecting line can be almost omitted and the performance is expected to be improved. Now we are ready to have the proposed balun configuration fabricated using a commercial 0.18-μm RF-CMOS process. The output magnitude and phase imbalance of the balun are shown in Fig. 4, where the solid curves are the measured results, and the

TABLE I
BALUN COMPARISON

Ref.	[11]	[14]	[15]	[16]	This Work
Freq. (GHz)	4–16	7–19	8.2–30	6–10	8.7–17.4
S21 (dB)	-12	-5	-7.5	-5	-7.4
△Mag (dB)	2	1	1	0.45	0.5
△Phase (deg)	> 10	5	10	7	1
Process	SiGe	GaAs	GaAs	CMOS	CMOS

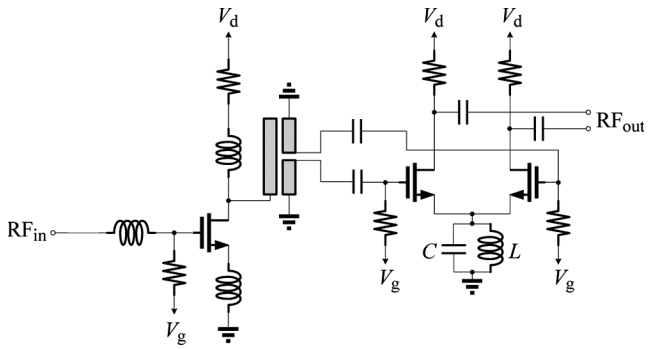

Fig. 5. Schematic of the input RF circuit where the input transistor stage can attain wideband input matching. The LC tank of the differential pair resonates at around 17 GHz.

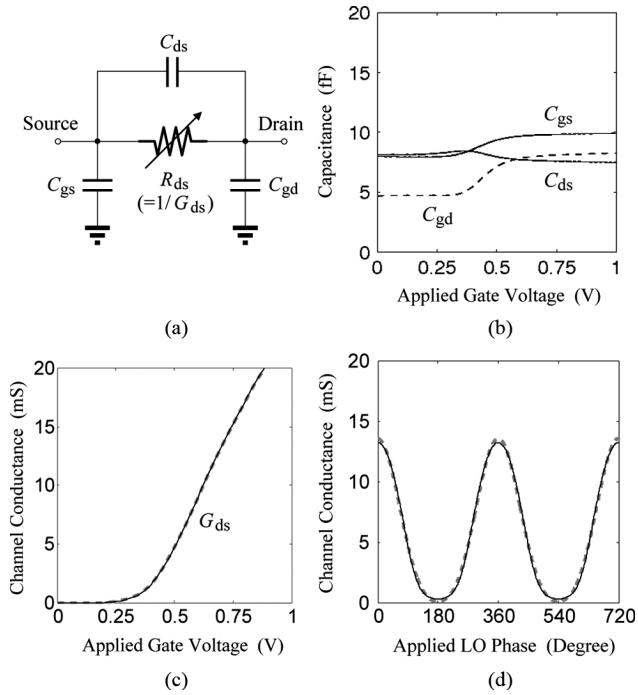

Fig. 6. Modeling of the resistive transistor used in the double-balanced mixer. (a) Transistor's equivalent circuit when zero-V_{ds} is applied. (b) Values of C_{gs}, C_{gd}, and C_{ds} versus the applied gate voltage. (c) Channel conductance G_{ds} versus the applied gate voltage where the solid line is derived using the S-parameters at each bias point, while the overlapping dotted curve is extracted from the transistor's dc characteristics, i.e., *I–V* curve. (d) LO-modulated channel conductance versus the LO phase where the solid curve is from the simulation, while the dotted curve is calculated using the Fourier series G_0, G_1, and G_2. The dc bias for the gate is 0.5 V, and the gate voltage swing due to the applied LO is 0.4 V.

dashed curves are their simulated counterparts. Here, the output magnitude imbalance in decibels is defined as the absolute value of $20\log(|S_{21}/S_{31}|)$, and the output phase imbalance in degree is defined as the absolute value of $180° - |\angle(S_{21}/S_{31})|$ [13]. The substrate loss is assumed $10\,\Omega\cdot$cm in the simulation, and each of the four-and-one-quarter-turn spirals has 18-μm inner radius, 6-μm linewidth, and 2-μm line separation. In the intended 8.7–17.4-GHz frequency range, the measured output magnitude and phase imbalance are less than 0.5 dB and 1°, respectively. Also shown in this figure are the measured and simulated $|S_{21}|$ and $|S_{32}|$, i.e., output port isolation. With the proper de-embedding procedure for removing the impacts of the RF pads and surrounding ground metals, the difference between measurement and simulation in the output magnitude imbalance can be minimized.

Measured results of different baluns with similar operating frequency as ours are listed in Table I. Though our balun has only comparable or slightly better amplitude imbalance (△ Mag), our phase imbalance (△ Phase) outperforms the other four. Capable of generating the differential-mode signal needed for the double-balanced mixer, the remaining concern of this balun is its loss; an amplifier can, therefore, be added in front of it. In Fig. 5, the input RF circuit starts with a single-stage transistor, which can easily achieve a wideband input matching by fine tuning both its source inductor and loading impedance [17], and it will provide the voltage gain to compensate for the insertion loss of the following Marchand balun. As explained, this balun converts the RF signal into its differential-mode counterpart, which will then be fed into the differential pair for amplification and further suppression of the residual common-mode signals at 17 GHz. The resistive drain bias scheme is preferred over the active load for its reliable high-frequency performance.

B. Core Mixing Circuit

The double-balanced circuit configuration is used in designing our core mixing circuit so that good port isolation and conversion efficiency can be achieved [18], [19]. To maintain minimal frequency dependency, and thus make feasible the wideband performance, the bias voltage V_{ds} of the four constituting transistors are all set to zero. Fig. 6(a) shows the transistor's equivalent circuit under this bias scheme, which is mainly a variable resistor $R_{ds}(= 1/G_{ds})$ with small parasitic capacitors C_{ds}, C_{gs}, and C_{gd} [20]. Fig. 6(b) displays the values of these parasitics versus the applied gate voltage. Value of the dominating channel conductance G_{ds} under different V_{gs} is shown in Fig. 6(c) where the solid curve is derived using the simulated S-parameters at different gate bias voltage, while the dotted curve is extracted from the transistor's dc characteristics, i.e., *I–V* curve. With 0.4-V gate voltage swing, i.e., 0.5 ± 0.2 V, the channel conductance G_{ds} will vary between 0.31–13.28 mS. Mathematically, the LO-modulated G_{ds} in the time domain can be expressed as

$$G_{ds}(t) = G_0 + \sum_{m=1}^{\infty} 2G_m \cos(m\omega_{LO}t). \tag{3}$$

Conceptually, G_0 is the dc channel conductance, G_1 is responsible for the fundamental-frequency mixing, G_2 is for sub-harmonic mixing, and so on. Once the G_i's are known, we can

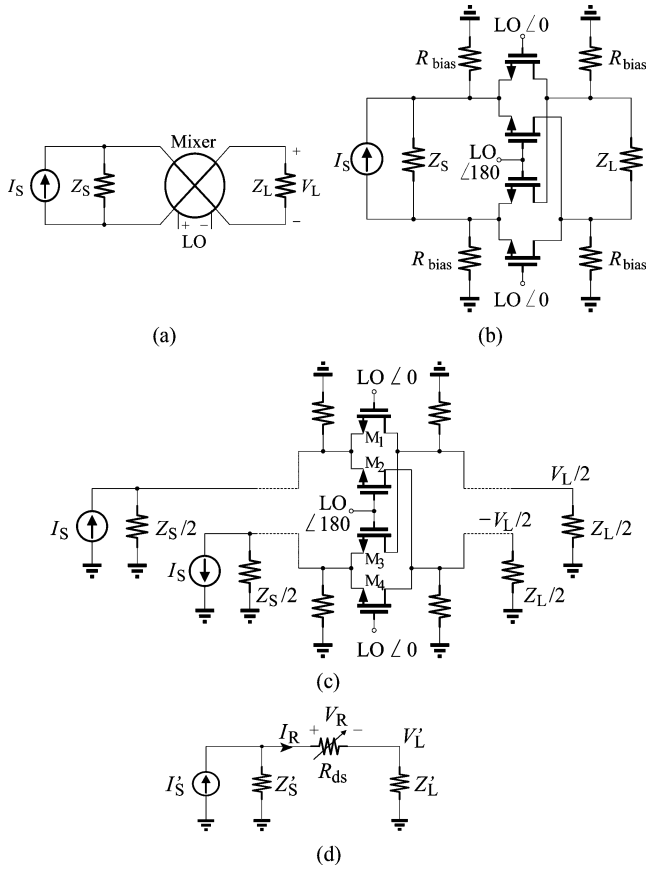

Fig. 7. Schematic of the core mixing circuit. (a) Conversion resistance $R_{\otimes}$ of a mixer can be defined as $V_L^{\rm IF}/I_S^{\rm RF}$, where $V_L^{\rm IF}$ is the IF component of V_L, and $I_S^{\rm RF}$ is the RF component of I_S. (b) Double-balanced mixer is made of four resistive transistors whose dc bias voltage $V_{\rm ds}$ is maintained at zero by having the large 2-kΩ resistors $R_{\rm bias}$ connected to ground. Also included in the schematic are the current source I_S, source impedance Z_S, and loading impedance Z_L. (c) Rearranged schematic of the double-balanced mixer. (d) Equivalent one-transistor circuit.

readily obtain the corresponding R_i's through matrix transformation. Fig. 6(d) shows the channel conductance swing due to the applied LO in two cycles. The solid curve is the simulated result; the overlapping dashed curve is its calculated counterpart using the fitted $G_{0\sim2}$.

For a double-balanced mixer, as shown in Fig. 7(a), we assume that the current I_S out of the RF differential pair is transformed by the mixer into the voltage V_L, which, in turn, drives the IF differential pair, and both the source impedance Z_S and loading impedance Z_L are frequency dependent. Apparently, a proper measure of the mixer's efficiency in this case will be the conversion resistance $R_{\otimes}$, which is defined as

$$R_{\otimes} \equiv \left| \frac{V_L^{\rm IF}}{I_S^{\rm RF}} \right| \tag{4}$$

where $V_L^{\rm IF}$ is the IF component of the loading voltage V_L, and $I_S^{\rm RF}$ is the RF component of the source current I_S. Intuitively, we can see that the larger the conversion resistance, the better the mixer's efficiency. Knowing conversion resistance, the corresponding voltage conversion gain G_v can be readily obtained as $G_v = R_{\otimes}/Z_S^{\rm RF}$. Fig. 7(b) shows the circuit arrangement of the double-balanced mixer, and it can be rearranged as that of Fig. 7(c), where the two opposite source currents I_S are coming from the RF differential pair and the two loading voltages are assigned as $V_L/2$ and $-V_L/2$, respectively. Here it is reasonable assuming that the two common source nodes of transistors $M_{1\sim4}$ are virtual ground for LO and IF signals, and the two common drain nodes of the four transistors are virtual ground for RF and LO signals. Therefore, the corresponding one-transistor equivalent circuit can be constructed as that shown in Fig. 7(d), where

$$\begin{aligned} I_S'^{\rm RF} &= \frac{I_S^{\rm RF}}{2} \quad Z_S'^{\rm RF} = Z_S^{\rm RF} \quad Z_S'^{\rm IF} = 0 \\ V_L'^{\rm IF} &= \frac{V_L^{\rm IF}}{2} \quad Z_L'^{\rm IF} = Z_L^{\rm IF} \quad Z_L'^{\rm RF} = 0. \end{aligned} \tag{5}$$

The four large $R_{\rm bias}$ are used to keep the drain and source of the mixing transistors dc grounded, and thus, can be omitted in our analysis.

First, the source current $I_S'^{\rm RF}$ brings upon the current $I_R^{\rm RF}$ that flows through the variable resistor

$$I_R^{\rm RF} = \frac{Z_S'^{\rm RF} \cdot I_S'^{\rm RF}}{Z_S'^{\rm RF} + R_0 + Z_L'^{\rm RF}}. \tag{6}$$

Here we assume that this variable resistor is dominated by its dc value; therefore, in the quasi-linear situation where only one frequency, either RF or IF, is involved, we can have $R_{\rm ds}$ replaced by R_0. Though seemingly too bold an assumption, this will nevertheless help us understand the basic principle of mixing. Now this RF current $I_R^{\rm RF}$ is ready to generate the IF voltage $V_R^{\rm IF}$ across the variable resistor, as

$$V_R^{\rm IF} = I_R^{\rm RF*} \cdot R_1 = \frac{Z_S'^{\rm RF*} \cdot I_S'^{\rm RF*}}{Z_S'^{\rm RF*} + R_0 + Z_L'^{\rm RF*}} \cdot R_1 \tag{7}$$

and we have

$$V_L'^{\rm IF} = V_R^{\rm IF} \cdot \frac{Z_L'^{\rm IF}}{Z_S'^{\rm IF} + R_0 + Z_L'^{\rm IF}} \tag{8}$$

therefore,

$$R_{\otimes} = \left| \frac{Z_S^{\rm RF*}}{Z_S^{\rm RF*} + R_0} \cdot R_1 \cdot \frac{Z_L^{\rm IF}}{Z_L^{\rm IF} + R_0} \right|. \tag{9}$$

Thus, from this mathematical formulation, we can see that large values of $Z_S^{\rm RF}$ and $Z_L^{\rm IF}$ are desired, and $|R_1|$ will be the upper limit of any available $R_{\otimes}$.

Appealing though it is, we still want to compare this seemingly trivial mathematics with results derived using other formal methods such as the conversion matrix technique [21]–[26]. In doing so, we hope that our intuitive approach can help reveal the underlying meanings of the more complicated formulations. Using the conversion matrix technique, the voltage V_R and current I_R on the variable resistor can be arranged as

$$\begin{aligned} V_R(t) &= \left[V_R^{\rm RF} e^{j\omega_{\rm RF}t} + V_R^{\rm IF} e^{j\omega_{\rm IF}t} + \cdots\right] \\ &\quad + \left[V_R^{\rm RF} e^{j\omega_{\rm RF}t} + V_R^{\rm IF} e^{j\omega_{\rm IF}t} + \cdots\right]^* \\ I_R(t) &= \left[I_R^{\rm RF} e^{j\omega_{\rm RF}t} + I_R^{\rm IF} e^{j\omega_{\rm IF}t} + \cdots\right] \\ &\quad + \left[I_R^{\rm RF} e^{j\omega_{\rm RF}t} + I_R^{\rm IF} e^{j\omega_{\rm IF}t} + \cdots\right]^* \end{aligned} \tag{10}$$

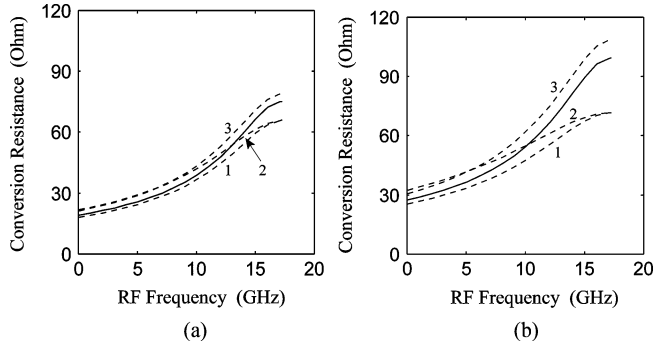

Fig. 8. Conversion resistance $R_{\otimes}$ of the double-balanced resistive mixer for two different gate voltage swings. (a) In the case of 0.4 –V gate voltage swing for each mixing transistor, the solid curve is the simulated result, dashed curve 1 is calculated using (9), dashed curve 2 is from (15), and dashed curve 3 is by (16). The source impedance Z_S is 200 Ω; the loading impedance Z_L is the impedance of a 125-fF capacitor. The LO responsible for gate voltage swing is fixed at 17.4 GHz. (b) Case with 1.4 –V gate voltage swing for each mixing transistor.

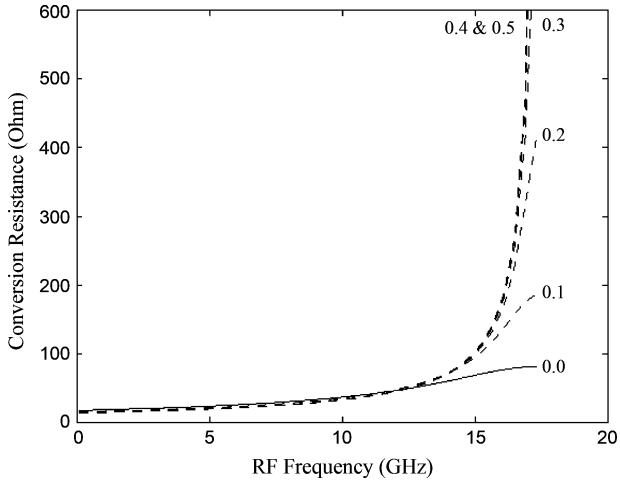

Fig. 9. Conversion resistance $R_{\otimes}$ for different bias voltage $V_{\rm ds}$. The number next to each curve indicates the corresponding $V_{\rm ds}$. All the gate bias is fixed at 0.5 V, with 0.4-V gate voltage swing. The source impedance Z_S is 200 Ω; the loading impedance Z_L is the impedance of a 125-fF capacitor. The LO responsible for gate voltage swing is fixed at 17.4 GHz.

where $\omega_{\rm IF} = \omega_{\rm LO} - \omega_{\rm RF}$ for this lower sideband down-converting mixer. Since $V_R(t)$ is equal to $R_{\rm ds}(t) \cdot I_R(t)$ in this variable resistor, we have

$$\begin{bmatrix} V_R^{\rm RF*} \\ V_R^{\rm IF} \end{bmatrix} = \begin{bmatrix} G_0 & G_1 \\ G_1 & G_0 \end{bmatrix}^{-1} \begin{bmatrix} I_R^{\rm RF*} \\ I_R^{\rm IF} \end{bmatrix} \tag{11}$$

where the effect of the image (IM) signal is temporarily neglected. As $V_S'(t)$ is equal to $Z_S' \cdot [-I_R(t) + I_S'(t)]$ at the source Z_S', we can have the corresponding matrix expressed as

$$\begin{bmatrix} V_S'^{\rm RF*} \\ V_S'^{\rm IF} \end{bmatrix} = \begin{bmatrix} Z_S'^{\rm RF*} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} -I_R^{\rm RF*} + I_S'^{\rm RF*} \\ -I_R^{\rm IF} + 0 \end{bmatrix}. \tag{12}$$

Likewise, since $V_L'(t)$ is equal to $Z_L' \cdot I_R(t)$ at the loading Z_L', there is

$$\begin{bmatrix} V_L'^{\rm RF*} \\ V_L'^{\rm IF} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & Z_L'^{\rm IF} \end{bmatrix} \begin{bmatrix} I_R^{\rm RF*} \\ I_R^{\rm IF} \end{bmatrix}. \tag{13}$$

Since the source voltage is the same as the loading voltage plus the voltage across the variable resistor, we then have

$$V_L'^{\rm IF} = \frac{-Z_L'^{\rm IF} \cdot R_1 \cdot Z_S'^{\rm RF*}}{\left(R_0 + Z_S'^{\rm RF*}\right)\left(R_0 + Z_L'^{\rm IF}\right) - R_1^2} \cdot I_S'^{\rm RF*} \tag{14}$$

i.e.,

$$R_{\otimes} = \left| \frac{Z_S^{\rm RF*} \cdot R_1 \cdot Z_L^{\rm IF}}{\left(Z_S^{\rm RF*} + R_0\right)\left(Z_L^{\rm IF} + R_0\right) - R_1^2} \right| \tag{15}$$

and this $-R_1^2$ term in the denominator will make $R_{\otimes}$ calculated using conversion matrix different from our intuitively best guess. Still, when both $Z_S^{\rm RF}$ and $Z_L^{\rm IF}$ are very large, $R_{\otimes}$ will be close to $|R_1|$.

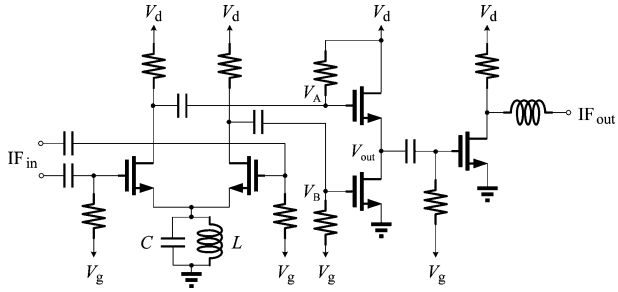

Fig. 10. Schematic of the output IF circuit. The LC tank of the differential pair resonates at around 8.7 GHz, and thus allows it to suppress the unwanted common-mode signals at high frequency, while the following in-cascade transistors will inhibit the low-frequency common-mode signals. An output gain stage is also added.

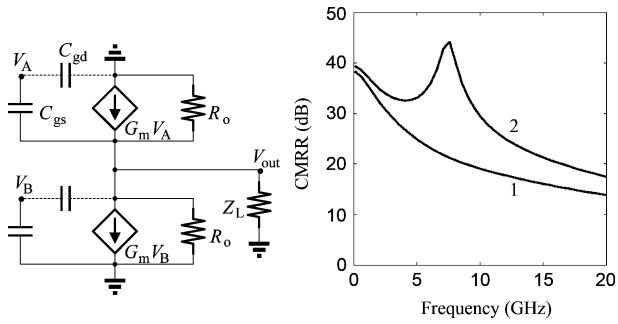

Fig. 11. Characteristic of the in-cascade transistors. (a) Schematic where the two transistors are identical. (b) Simulated CMRR where curve 1 is with the in-cascade transistors only; curve 2 is that of the total IF circuit, i.e., differential-pair plus in-cascade. The intended IF frequency range is dc–8.7 GHz.

When the IM signal is taken into consideration, we can have the expression of the conversion resistance revised as

$$R_{\otimes} = \left| \frac{Z_S^{\rm RF} \cdot R_1 \cdot Z_L^{\rm IF}}{\left(Z_S^{\rm RF} + R_0 + R_2\right)\left(Z_L^{\rm IF} + R_0'\right) - 2R_1^2} \right| \tag{16}$$

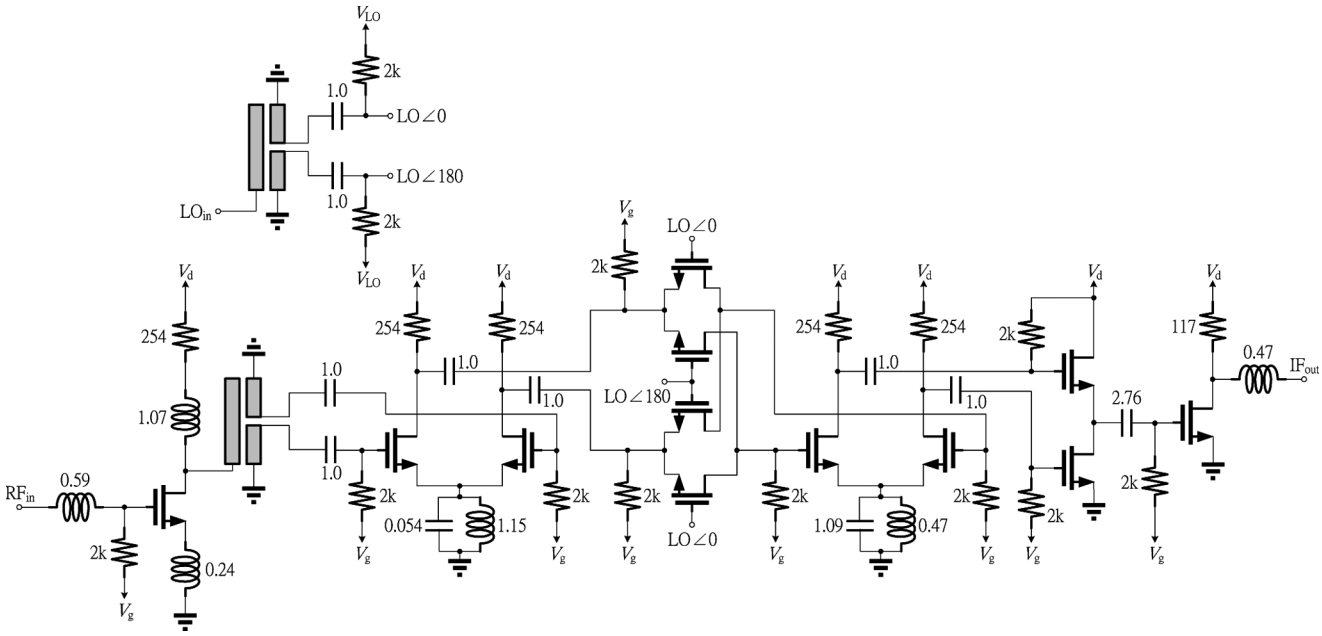

Fig. 12. Schematic of the wide-IF-band mixer. Both the source and drain voltage of the four mixing transistors have been lifted to $V_g (= 0.5\ \mathrm{V})$, and the gate voltage to $V_{\mathrm{LO}} (= 1\ \mathrm{V})$, thus the dc-blocking capacitors between the mixing circuit and the IF stage can be removed. The units for resistance, capacitance, and inductance are ohms, picofarads, and nanohenries, respectively.

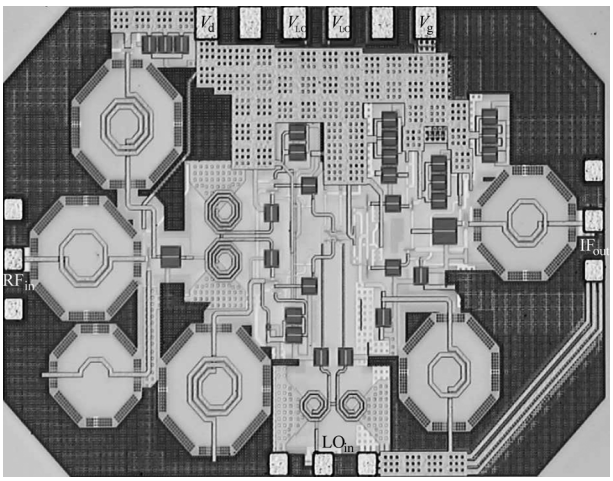

Fig. 13. Photograph of the wide-IF-band mixer. It is made of 0.13-μm RF-CMOS process and takes an area of $0.94 \times 1.38 = 1.3\ \mathrm{mm}^2$.

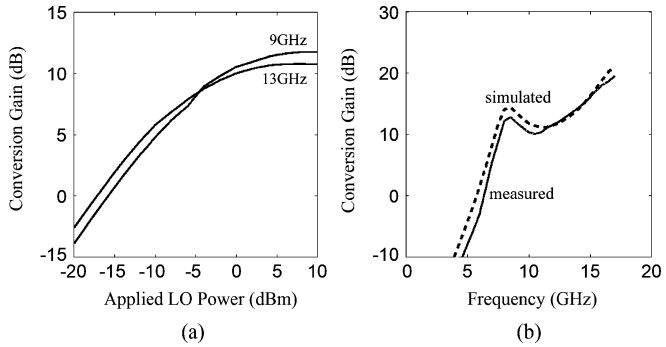

Fig. 14. Conversion gain of the mixer. (a) Measured 9- and 13-GHz conversion gain with different LO power. (b) Conversion gain versus RF frequency with the power of 17.4-GHz LO fixed at 5 dBm. The solid curve is the measured result, while the dashed curve is the simulated counterpart. In the 8.7–17.4-GHz RF band, the conversion gain is larger than 10 dB.

where the source impedance is assumed to be resistive and the $[R]$ matrix comes from the fitted $[G]$ matrix, i.e.,

$$\begin{bmatrix} R_0 & R_1 & R_2 \\ R_1 & R_0' & R_1 \\ R_2 & R_1 & R_0 \end{bmatrix} = \begin{bmatrix} G_0 & G_1 & G_2 \\ G_1 & G_0 & G_1 \\ G_2 & G_1 & G_0 \end{bmatrix}^{-1}. \qquad (17)$$

Fig. 8(a) shows the values of $R_{\otimes}$ derived by using these three different approaches, where Z_S^{RF} is assumed 200 Ω (two 100-Ω resistors in series) and Z_L^{IF} is the impedance of the 125-fF capacitor (two 250-fF capacitors in series). The solid curve comes from the simulation; dashed curve 1 is calculated using (9), dashed curve 2 is using (15), and dashed curve 3 is calculated using (16). The gate voltage swing is 0.4 V, i.e., 0.5 ± 0.2 V, for each mixing transistor. Fig. 8(b) shows the corresponding values of $R_{\otimes}$ when the gate voltage swing is 1.4 V, i.e., 0.5 ± 0.7 V, for each mixing transistor.

As mentioned at the beginning of this section, the adoption of zero-V_{ds} allows the mixing transistors to be modeled as variable resistors with minimal frequency dependency, and thus extends the mixer's bandwidth. Fig. 9 shows the simulated $R_{\otimes}$ for different V_{ds} (and I_{ds}) where the LO is fixed at 17.4 GHz and the bias-T's (not shown) are assumed ideal. It is true that if the IF bandwidth is a mere hundreds of megahertz, a large V_{ds} should be applied, as the conversion resistance can now easily reach 100 Ω and more. When IF bandwidth increases, however, the large frequency dependency of $R_{\otimes}$ will make this large V_{ds} choice less and less appealing, and the solution can be using some frequency compensation techniques [27], or simply adopting a small V_{ds} (and I_{ds} too), or both. In our case of 8.7-GHz IF bandwidth, the use of zero-V_{ds} can easily reach

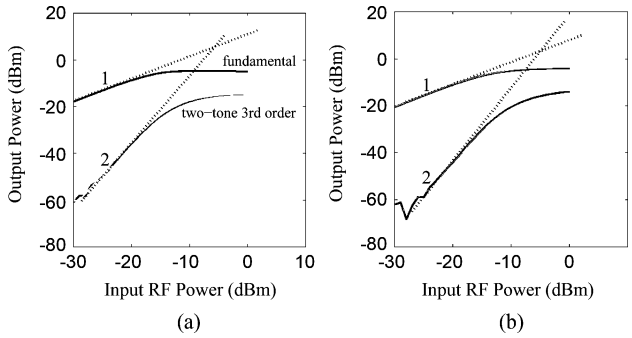

Fig. 15. Linearity of the mixer at 9 and 13 GHz. (a) Solid curves 1 and 2 are the measured fundamental-frequency and two-tone third-order intermodulation output with two slightly different RF signals centered around 9 GHz; the dotted lines are used to obtain the intercept point. At 9 GHz, the input referred P1 dB is -17.5 dBm and the IIP3 is -6 dBm. (b) Corresponding curves for 13-GHz RF, where the the input referred P1 dB is -16 dBm and the IIP3 is -5 dBm.

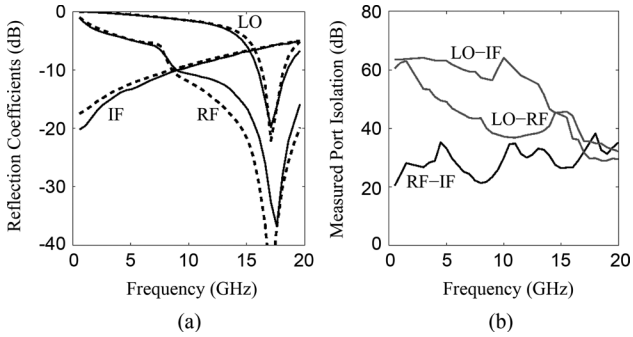

Fig. 16. Input reflection coefficient and port isolation. (a) Input reflection coefficients of the RF, LO, and IF ports. The solid curves are the measured results; the dotted curves are their simulated counterparts. All the three ports have small input reflection coefficients in their respective bandwidth. (b) Measured RF-IF, LO-RF, and LO-IF port isolation.

a good overall mixing performance while allowing a small system voltage and low power consumption.

C. Output IF Circuit

At the output of the mixing circuit, both the differential-mode IF signal and the unintended common-mode RF leakage (and other spurious common-mode ones) can be detected; therefore, how to reach a high common-mode rejection ratio (CMRR) from dc to more than 8.7 GHz will be the focus in designing our IF circuit. The problem with passive IF balun is that it takes too much chip area for effectively covering the entire IF frequency range; worst still, we would like the lowest frequency to start from zero. As shown in Fig. 10, an active balun made of a differential pair followed by two identical transistors in cascade is then used to render a large CMRR over the whole IF band [28]. By fine tuning the LC tank's resonance frequency, the differential-pair could provide a good CMRR at around 8.7 GHz; at much lower frequency, it is the two in-cascade transistors that eliminates the common-mode signals because, as shown in Fig. 11(a), there is now

$$V_{\text{out}} = \frac{Z_L' G_m}{1 + Z_L' G_m} (V_A - V_B) \tag{18}$$

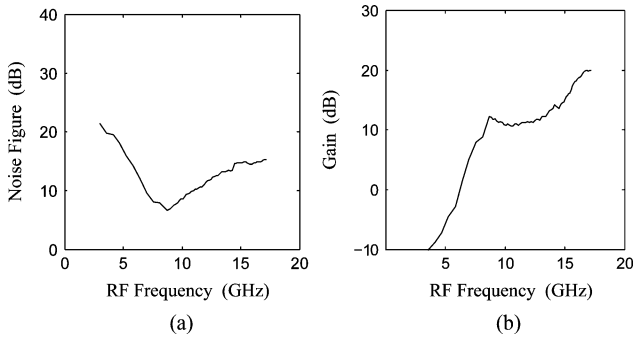

Fig. 17. Measured noise figure and gain of the mixer versus the incoming RF frequency. (a) Noise figure measured using noise figure analyzer. It is 7 dB at 9 GHz, and 12.6 dB at 13 GHz. (b) Corresponding gain.

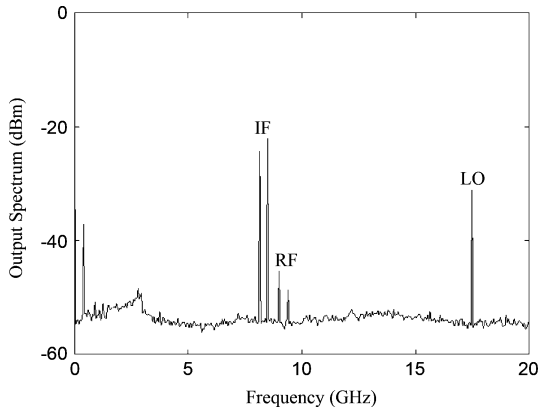

Fig. 18. Measured IF output spectrum with two -30-dBm input RF signals of 9 and 9.375 GHz.

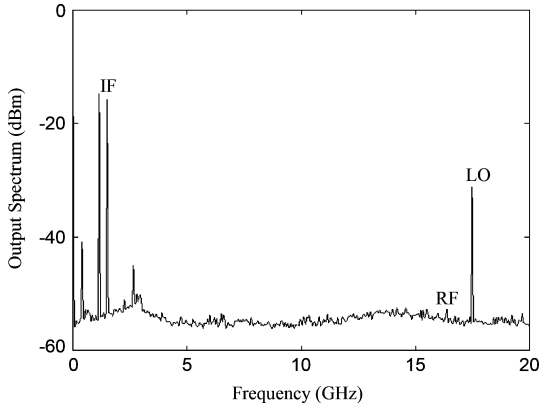

Fig. 19. Measured IF output spectrum with two -30-dBm input RF signals of 16 and 16.375 GHz.

with $1/Z_L' = 2/R_o + 1/Z_L$, and C_{gd} being neglected. Therefore, V_{out} exists for differential-mode input, but is zero for the common-mode one when the frequency is close to zero. Fig. 11(b) shows the simulated CMRR. Curve 1 is with the in-cascade transistors only, where the CMRR can reach 38 dB at very low frequency, but it decreases steadily as frequency increases. Curve 2 is the CMRR with the complete IF stage (differential pair plus in-cascade) where the differential-pair helps increase the CMRR to 44 dB at 8.7 GHz, thus broadens the IF bandwidth in this respect. Of course, a differential pair with a high-impedance current source can also be used to get

TABLE II
MIXER COMPARISON

References	[19]	[31]	[32]	[33]	[34]	[35]	[36]	This Work
RF frequency (GHz)	22.5–24.5	18.3–19.7	4–18	14–22	4.5–7	10.8–11.7	20–23.5	8.7–17.4
IF frequency (GHz)	1.5–3.5	2–3.4	2–16	DC–8	DC–2.5	1.05–1.95	DC–3.5	DC–8.7
Conversion gain (dB)	0.7	1	-5	-6	-8	17	5	14.5
Noise figure (dB)	N/A	9	N/A	7	8	12.4	17	9.8
RF return loss (dB)	-10	-10	-10	-15	-5	N/A	-10	-10
IF return loss (dB)	-4	-10	N/A	-10	-12	N/A	-10	-10
LO return loss (dB)	N/A	N/A	-10	-12	-7	N/A	-10	-10
LO power (dBm)	3	-1	10	11	13	-2	0	5
RF-IF isolation (dB)	N/A	36	10	20	13	N/A	30	20
LO-IF isolation (dB)	50	50	10	30	20	47	33	35
LO-RF isolation (dB)	30	41	25	30	20	N/A	23	35
Input referred P1dB	-6.1	N/A	N/A	11	10	N/A	-6.3	-16.7
IIP3 (dBm)	4.4	-2	N/A	18	21	N/A	N/A	-5.5
Power (mW)	8	6.9	2500	0	0	53	90	40
Chip area (mm^2)	0.47	0.53	4	0.48	1.38	0.34	1	1.3
Process	0.13μm CMOS	0.13μm CMOS	0.1μm InP HEMT	GaAs MESFET	GaAs MESFET	SiGe HBT	GaAs HBT	0.13μm CMOS

a good CMRR, but now the system voltage V_d needs to be increased from 1.5 to at least 2 V.

III. MEASURED RESULTS OF THE 8.7–17.4-GHz MIXER

Figs. 12 and 13 show the schematic and photograph of the mixer fabricated using commercial 0.13-μm RF-CMOS process. By lifting the source and drain biases of the four mixing transistors from zero to the gate bias V_g of the IF differential pair, the dc blocking capacitors between the mixing core and the output IF stage can be removed to increase the mixer's conversion efficiency. The LO balun has also been optimized at 17.4 GHz. Among the four dc bias pads in this mixer, the system voltage V_d is for the active transistors' drain bias (1.5 V and 26 mA), V_g is for their gate bias (0.5 V and negligible current), and the two V_{LO} are for the core mixing transistors' gate bias (1 V and negligible current). This mixer takes an area of 1.3 mm^2 and has a total power consumption of around 40 mW.

Fig. 14(a) shows the mixer's conversion gain at both 9 and 13 GHz for -30-dBm RF input, where the 17.4-GHz LO power is sweeping from -20 to 10 dBm. As long as LO is larger than 5 dBm, a large and almost constant conversion gain can be obtained. Fig. 14(b) shows the mixer's conversion gain versus RF frequency, with the 17.4-GHz LO fixed at 5 dBm. The solid curve is the measured result, and the closely following dotted curve is the simulated counterpart where all the metal ground has been taken into consideration. Conversion gain larger than 10 dB can be achieved in the 8.7–17.4-GHz RF frequency range. Though there is an equalizer for each IF band in our receiver array, flat conversion gain will be among the top priorities in our next design iteration. Fig. 15 shows the measured fundamental frequency and the two-tone third-order intermodulation output signals for both 9- and 13-GHz RF input signals. The input referred P1 dB is -17.5 dBm at 9 GHz, and -16 dBm at 13 GHz. The third-order input intercept point (IIP3) is -6 dBm at 9 GHz, and -5 dBm at 13 GHz, and it can be improved by employing the technique of multiple gated transistors [29], [30].

Fig. 16(a) shows the return loss of the RF, IF, and LO ports where the testing power is set to -30 dBm; all ports have return loss better than -10 dBm in their respective frequency range (RF: 8.7–17.4 GHz, IF: dc–8.7 GHz, LO: 17.4 GHz). Fig. 16(b) shows the measured LO-IF, LO-RF, and RF-IF port isolation. The 35-dB LO-IF isolation at 17.4 GHz indicates that a low-pass or notch filter may be needed to further suppress the 17.4-GHz residual LO signal at the IF port. However, given the large separation of the LO frequency and IF band, designing this 17.4-GHz filter will be straightforward. The LO-RF port isolation is better than 35 dB at 17.4 GHz. Regarding the RF-IF port isolation, though nothing to do with the mixing process itself, the adding of an ideal amplifier into the mixer circuit does decrease its measured RF-IF port isolation while increasing its overall conversion gain by the same amount. Therefore, a more adequate measure should be adding the conversion gain in decibels to the RF-IF port isolation in decibels. In this respect, our mixer is better than other wide-IF-band mixers by at least 10 dB. By incorporating high-impedance current sources in both the RF and IF differential pairs, further improvement of RF-IF port isolation can be expected, though at the cost of larger system voltage. At this moment, the 10-dB conversion gain and 20-dB RF-IF port isolation of our mixer means the intended down-converted signal will always be 30 dB larger than the leakage one if their corresponding RF power are the same, and that is more than enough for our application. Fig. 17 shows the measured noise figure and gain of the mixer using a noise figure analyzer. The noise figure is 7 dB for 9-GHz RF, and it is 12.6 dB for 13-GHz RF.

Fig. 18 shows the measured output spectrum where the two -30-dBm input RF signals of 9 and 9.375 GHz are injected into the mixer and down-converted to the two intended IF signals. The very small 375-MHz spurious signal is due to the self mixing of the two intended IF signals at the output-stage common-source transistor, and it can be suppressed if that transistor is removed or replaced by a more robust circuit. Fig. 19 shows the measured results where the two -30-dBm input RF signals are at 16 and 16.375 GHz. A comparison with other mixers is tabulated in Table II.

IV. CONCLUSION

In this paper, a comprehensive analysis of the mixer has been carried out, which explains why the resistive double-balanced

mixer is preferred for wide-IF-band applications. The mathematical formulation for calculating the core mixing circuit's conversion resistance is then derived, which allows a better understanding of the underlying principles of mixing. Using a commercial 0.13-μm RF-CMOS process, an 8.7–17.4-GHz mixer where its RF bandwidth equal to its IF bandwidth is then designed and characterized.

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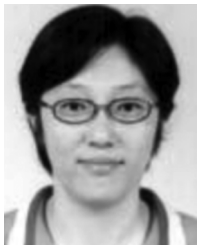

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