A Novel Method of MOSFET Series Resistance Extraction Featuring Constant Mobility Criteria and Mobility Universality

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***Abstract*—A method of MOSFET series resistance extraction is established in this paper. The core of this method relies on the constant mobility criteria, while for different gate lengths, it preserves the shape of universal mobility curves in the high-vertical-field regime. Consequently, the series resistance of a MOSFET can be extracted in an analytical and self-consistent manner, achieved without the knowledge of the gate oxide thickness, channel length, channel doping, or channel stress. Reasonable values of extracted series resistance are demonstrated in a wide range of gate length. Technology computer-aided design simulation further corroborates the validity of the proposed method, particularly for devices with heavily doped source/drain extensions. The constant mobility criteria with respect to the bulk charge linearization coefficient are also verified.**

***Index Terms*—MOSFET, series resistance, universal mobility.**

I. Introduction

MOSFET series resistance (R_{sd}), as shown in Fig. 1, leads to a voltage drop within source and drain diffusion regions, reducing the voltage across the intrinsic device and degrading drive capability. It constitutes an increasing portion of total resistance as gate length ($L_{\rm gate}$) shrinks due to reduced intrinsic channel resistance. Hence, the degradation of drive current becomes most serious in short-channel devices. In integrated circuit technology development, R_{sd} extraction remains one of the most critical tasks during device characterization and simulation. Many R_{sd} extraction methods [1]–[3] have one assumption in common: both the channel dopant concentration and carrier mobility are independent of $L_{\rm gate}$. However, the significance of the halo ion implantation and mechanical-stress-dependent dopant diffusion [4], as encountered in modern MOSFETs, renders this model inadequate. Recently, a constant mobility criterion in the high-surface-electrical-field regime was proposed [5], which can not only considerably improve R_{sd} extraction precision but also eliminate the disadvantages of conventional methods [1], [2], [6] such as requiring multiple I–V measurements over different channel lengths and/or sophisticated C–V measurements for short-channel devices.

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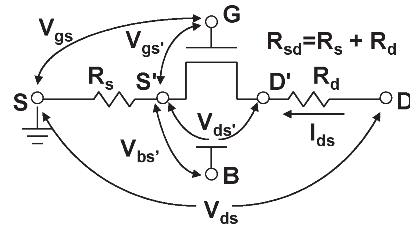

Fig. 1. Schematic of the equivalent circuit of the device used in R_{sd} extraction.

Contrary to the drain current model used in the literature [1]–[3], [5], [6], a bulk charge linearization coefficient (α) is adopted in this paper. This leads to a cancellation of the debiasing effect and the threshold voltage change induced by IR drop. Hence, an exact and compact drain current formulation results. In addition, a self-consistent algorithm is established by combining the constant mobility criterion [5] and an updated method of effective surface electrical field ($E_{\rm eff}$) extraction. In contrast to [5], which uses a constant η in the analytic expression of $E_{\rm eff}$, this empirical factor is treated as a fitting parameter ($\eta_{\rm ana}$) in this work. The values of R_{sd} and $\eta_{\rm ana}$ are determined by using an iterative procedure. With the constant mobility criterion taken into account, the R_{sd} can be more accurately extracted for a certain short-channel device by matching the shape of its universal mobility curve with that of a long-channel device. The procedure is conducted without requiring knowledge of the effective channel length ($L_{\rm eff}$), substrate doping concentration ($N_{\rm sub}$), or channel stress. With this unique feature in mind, the proposed method is particularly suitable for the short-channel devices for which unambiguous definition of $L_{\rm eff}$ is often hard to make. Reasonable values of extracted R_{sd} are successfully demonstrated in a wide range of gate lengths. The validity of the constant mobility criterion is addressed as well.

The device samples used in this work are fabricated using the 40-nm low-power process technology of Taiwan Semiconductor Manufacturing Company. This technology features abrupt and heavily doped ultra shallow junction for source/drain extensions (SDEs). Millisecond annealing is implemented to enhance

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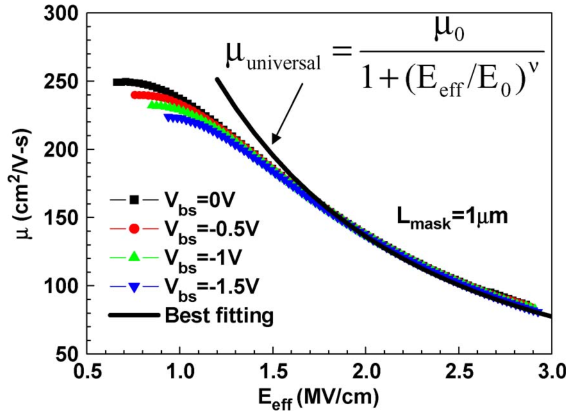

Fig. 2. Measured inversion carrier mobility (μ) versus effective surface electric field (E_{eff}) under different V_{bs} bias conditions of a long-channel NMOSFET. The inversion carrier mobility converges to the same trend when E_{eff} is sufficiently high. The curve of "best fitting" is obtained with $\mu_0 = 720\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, $E_0 = 0.82$ MV/cm, and $\nu = 1.63$ for the long-channel device used in this work.

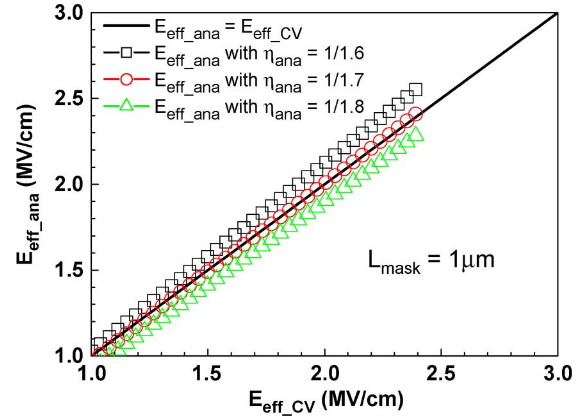

Fig. 3. Comparison between the effective surface electric field obtained from analytical equation $(E_{\mathrm{eff_ana}})$ and split C–V measurement $(E_{\mathrm{eff_}CV})$. $\eta_{\mathrm{ana}} = 1/1.7$ provides the best fitting result.

the dopant activation level. Aggressive strain engineering is used to boost device performance.

II. Universal Mobility and Analytic E_{eff} With η_{ana} as a Fitting Parameter

The universality of carrier mobility in the high-electrical-field regime is demonstrated in Fig. 2 for a long-channel MOSFET. The effective silicon vertical electrical field (E_{eff}) at the $\mathrm{SiO_2/Si}$ interface can be expressed as a function of the depletion charge (Q_d) and inversion layer charge (Q_i). The charge components Q_d and Q_i can be obtained via split C–V measurements [7], [8]. The E_{eff} formula can read as

$$E_{\mathrm{eff_}CV} = \frac{1}{\varepsilon_{\mathrm{Si}}}\left(|Q_d| + \eta|Q_i|\right) \tag{1}$$

where $\varepsilon_{\mathrm{Si}}$ is the silicon permittivity, and η is an empirical factor with common values of ∼1/2 and ∼1/3 for electrons and holes at room temperature, respectively [9]–[13]. Note that in this paper, η, which is the reciprocal of that in [5], follows the convention in existing publications [9]–[13]. In order to obtain accurate carrier mobility, split C–V and I–V measurements are performed on a long-channel MOSFET in which fringing capacitance and R_{sd} are insignificant as compared with intrinsic gate capacitance and channel resistance, respectively. As shown in Fig. 2, under various back bias (V_{bs}) conditions, carrier mobility appears to converge toward a universal mobility $(\mu_{\mathrm{universal}})$ curve in the high-E_{eff} region. This means that if the device is operated in the high-E_{eff} region, a constant mobility is achieved at a given E_{eff}, regardless of the varying impurity scattering element. At sufficiently high E_{eff}, carrier mobility is well described by [14]–[16]

$$\mu_{\mathrm{universal}} = \frac{\mu_0}{1 + (E_{\mathrm{eff}}/E_0)^{\nu}} \tag{2}$$

where μ_0, E_0, and ν are process-specific constants. Best fitting result, also shown in Fig. 2, is obtained with $\mu_0 = 720\ \mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, $E_0 = 0.82$ MV/cm, and $\nu = 1.63$ for the long-channel device used in this work.

To further investigate (1), it is transformed into the following analytical form:

$$E_{\mathrm{eff_ana}} = \frac{V_{\mathrm{gs}} + \left(\frac{1}{\eta_{\mathrm{ana}}} - 1\right)V_{\mathrm{th}} - \frac{1}{\eta_{\mathrm{ana}}}V_{\mathrm{FB}} - \frac{2}{\eta_{\mathrm{ana}}}\psi_B}{\frac{3}{\eta_{\mathrm{ana}}}T_{\mathrm{OX}}}. \tag{3}$$

The parameters associated with (3) have the usual meanings [5]. The threshold voltage V_{th} in (3) is extracted using a maximum transconductance method under a low drain bias (25 mV), ensuring a linear operation mode. In the derivation of (3), a constant N_{sub} is presumed. However, aggressive engineering of channel doping profile, such as retrograded channel and/or heavy halo ion implantation, is commonly used in modern MOSFETs. In addition, a nonuniform doping profile caused by mechanical-stress-dependent diffusion is also evident. These factors make the constant N_{sub} assumption problematic, and a specific treatment is needed.

In this paper, η_{ana} in the analytic expression (3) is treated as a fitting parameter in order to accommodate the error introduced by the constant N_{sub} assumption, as mentioned above. Similar to the method described in [15], the $E_{\mathrm{eff_ana}}$ values acquired through (3) are compared to those of split C–V method. A long-channel NMOSFET $(L_{\mathrm{mask}} = W_{\mathrm{mask}} = 1\ \mu\mathrm{m})$ is used to examine the consistency between the two methods. One should note that the value of η used for split C–V is set at 1/2 for NMOSFETs fabricated on wafers with (100) surface orientation. As shown in Fig. 3, in order to match the E_{eff} values between both methods, $\eta_{\mathrm{ana}} = 1/1.7$, instead of 1/2, is suggested when applying the analytic expression (3).

III. Methodology of R_{sd} Extraction: Constant Mobility Criterion

The R_{sd} extraction method based on a constant mobility criterion is first described in [5]. Here, to testify to the validity of the constant mobility criterion, an extra parameter is introduced: the bulk charge linearization coefficient denoted as α.

First, for the intrinsic MOSFET (Fig. 1) operated in linear region, drain current can be expressed as [17], [18]

$$I_d = \frac{C_{\rm ox} W_{\rm eff} \mu}{L_{\rm eff}} \left(V'_{\rm gs} - V'_{\rm th} - \frac{\alpha}{2} V'_{\rm ds} \right) V'_{\rm ds} \tag{4}$$

where $V'_{\rm th} = V_{\rm th} - (\alpha - 1)V'_{\rm bs}$, and $V'_{\rm bs} = -R_s I_d$. $V_{\rm th}$ is the threshold voltage measured without IR drop on the source side. Under the assumption of $R_s = R_d = R_{\rm sd}/2$ for a symmetric MOSFET and to account for the debiasing effect at the terminals, (4) can be expressed in terms of the externally applied voltages as follows:

$$\begin{aligned} I_d = \frac{C_{\rm ox} W_{\rm eff} \mu}{L_{\rm eff}} \Bigg[\left(V_{\rm gs} - \frac{R_{\rm sd}}{2} I_d \right) - \left(V_{\rm th} + (\alpha - 1) \frac{R_{\rm sd}}{2} I_d \right) \\ - \frac{\alpha}{2} (V_{\rm ds} - R_{\rm sd} I_d) \Bigg] (V_{\rm ds} - R_{\rm sd} I_d) \\ = \frac{C_{\rm ox} W_{\rm eff} \mu}{L_{\rm eff}} \left(V_{\rm gs} - V_{\rm th} - \frac{\alpha}{2} V_{\rm ds} \right) (V_{\rm ds} - R_{\rm sd} I_d). \end{aligned} \tag{5}$$

The above derivation process clearly demonstrates that cancellation of the debiasing effect and the threshold voltage change induced by IR drop takes place. As a result, the term in the first parentheses of (5) reduces to $(V_{\rm gs} - V_{\rm th} - \alpha V_{\rm ds}/2)$, thus constituting an exact and simple formulation for the drain current. By incorporating the criterion described in [5], a constant mobility can be achieved at the following two sets of bias conditions: 1) $(V_{\rm gs}^{(1)}, V_{\rm th}^{(1)})$ and 2) $(V_{\rm gs}^{(2)}, V_{\rm th}^{(2)})$, where $V_{\rm gs}^{(2)} = V_{\rm gs}^{(1)} + (1/\eta_{\rm ana} - 1)(V_{\rm th}^{(1)} - V_{\rm th}^{(2)})$. Again, using the same derivation procedure in [5] with the incorporation of α, series resistance can be written as

$$R_{\rm sd} = \left(\frac{B}{I_d^{(2)}} - \frac{A}{I_d^{(1)}} \right) \frac{\eta_{\rm ana} V_{\rm ds}}{\left(V_{\rm th}^{(1)} - V_{\rm th}^{(2)} \right)} \tag{6}$$

where $A = V_{\rm gs}^{(1)} - V_{\rm th}^{(1)} - 0.5\alpha V_{\rm ds}$, and $B = V_{\rm gs}^{(1)} + (1/\eta_{\rm ana} - 1) V_{\rm th}^{(1)} - V_{\rm th}^{(2)}/\eta_{\rm ana} - 0.5\alpha V_{\rm ds}$.

The expression of $R_{\rm sd}$ in (6) shows no dependency on $C_{\rm ox}$, $L_{\rm eff}$, and $W_{\rm eff}$. Therefore, this method is particularly suitable for modern MOSFETs with small geometries in which accurate measurements of $C_{\rm ox}$, $L_{\rm eff}$, and $W_{\rm eff}$ are hard to achieve.

For a modern MOSFET with thin gate oxide, α is close to 1, as will be explained later. In the following discussion, α is presumed as 1, and the error caused by this assumption will be further examined.

IV. Algorithm of Self-Consistent $R_{\rm sd}$ and $\eta_{\rm ana}$ Calculation

As device feature size shrinks, fringing capacitance and $R_{\rm sd}$ become no longer negligible. It is difficult to extract carrier mobility and $E_{{\rm eff}_CV}$ by using simple split C–V and I–V measurements. Thus, at small feature sizes, analytical derivations for μ and $E_{\rm eff}$ become necessary. Once $R_{\rm sd}$ has been extracted by using (6), an analytical expression of mobility $\mu_{\rm ana}$ can be written as

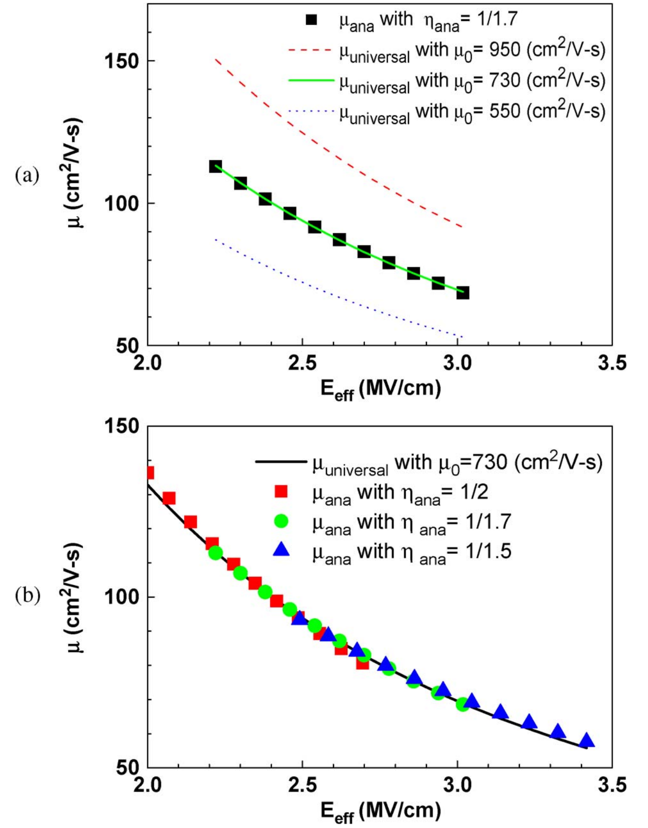

Fig. 4. (a) Fitting parameter μ_0 dominating the magnitude of $\mu_{\rm universal}$ versus $E_{\rm eff}$ behavior. (b) Fitting parameter $\eta_{\rm ana}$ dominating the slope of $\mu_{\rm ana}$ versus $E_{\rm eff}$ behavior.

$$\mu_{\rm ana} = \frac{L_{\rm eff}}{W_{\rm eff} C_{\rm ox}} \frac{I_d}{\left(V_{\rm gs} - V_{\rm th} - \frac{\alpha}{2} V_{\rm ds} \right) (V_{\rm ds} - R_{\rm sd} I_d)}. \tag{7}$$

Because $R_{\rm sd}$ is a function of $\eta_{\rm ana}$, as described in (6), $\mu_{\rm ana}$ is consequently also a function of $\eta_{\rm ana}$. For a given $\eta_{\rm ana}$, corresponding $E_{{\rm eff}_{\rm ana}}$, $R_{\rm sd}$, and $\mu_{\rm ana}$ are generated analytically. Moreover, a series of $E_{{\rm eff}_{\rm ana}}$ and $\mu_{\rm ana}$ can be defined for bias conditions in the vicinity of the specific $V_{\rm gs}$, where $R_{\rm sd}$ is extracted. It is worth noting that $V_{\rm gs}$ should be sufficiently high, as mentioned in Section III. In a sense, $V_{\rm gs}$ of ~2.5 V is typically used in this work.

Process-induced strain and intensive strain engineering are pervasive in modern MOSFETs. These may lead to significant variability in carrier mobility [19]–[22] and changes to $\mu - E_{\rm eff}$ behavior. The difference in $\mu - E_{\rm eff}$ behavior in a high-$E_{\rm eff}$ regime between strained and unstrained MOSFETs approaches a constant ratio, as mentioned in the literature [16], [23]–[25]. This implies that only μ_0 in (2) is sensitive to strain engineering in the high-$E_{\rm eff}$ regime. Consequently, the $\mu - E_{\rm eff}$ behavior in the high-$E_{\rm eff}$ regime extracted using long-channel MOSFETs is valid for shorter channel devices by simply modifying it with a constant ratio. μ_0 is therefore regarded as a fitting parameter for shorter channel MOSFETs in this work. In addition, determining $L_{\rm eff}$ for short-channel MOSFETs remains one of the most challenging issues in the industry. Without explicitly assigning a value to $L_{\rm eff}$, mask

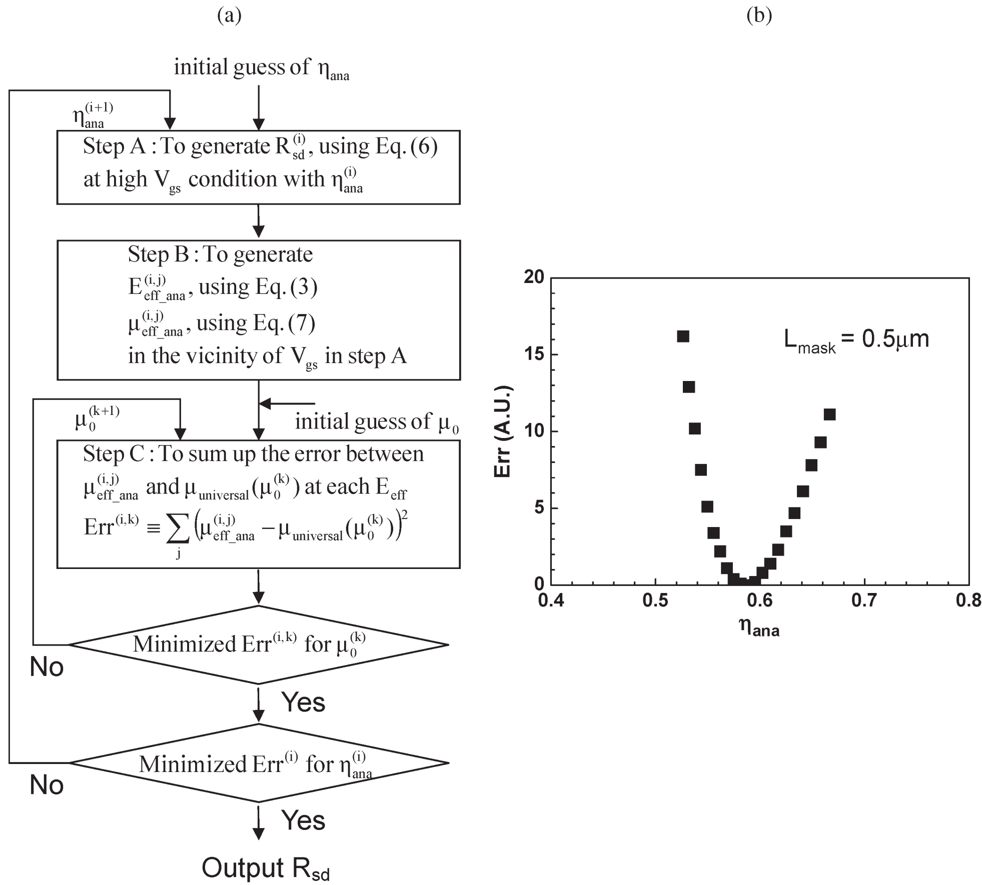

Fig. 5. (a) Self-consistent method of $R_{\rm sd}$ extraction using both μ_0 and $\eta_{\rm ana}$ as fitting parameters in order to minimize the difference between $\mu_{\rm universal}$ and $\mu_{\rm ana}$. (b) Summation of $(\mu_{\rm ana} - \mu_{\rm universal})^2$ over a wide range of $E_{\rm eff}$ in the vicinity of $V_{\rm gs}$, where $R_{\rm sd}$ is extracted. NMOSFET with 0.5 μm $L_{\rm mask}$ is used as an example. $\eta_{\rm ana}$ = 1/1.7 provides the lowest error.

length $(L_{\rm mask})$ is used in this work. The difference between $L_{\rm mask}$ and $L_{\rm eff}$ of a given short-channel MOSFETs is also absorbed by μ_0. As shown in (6), no information about $L_{\rm eff}$ is necessary for $R_{\rm sd}$ extraction, as mentioned in Section III. Therefore, the ambiguous definition of $L_{\rm eff}$ does not lead to erroneous $R_{\rm sd}$ extraction [5]. In the vicinity of the $V_{\rm gs}$ where $R_{\rm sd}$ is extracted, μ_0 is a fitting parameter accounting for the difference introduced by long- to short-channel mobility shifts as well as the constant ratio between $L_{\rm eff}$ and $L_{\rm mask}$ of a given shorter channel MOSFET. As shown in Fig. 4(a) and (b), μ_0 dominates the magnitude of $\mu_{\rm universal} - E_{\rm eff}$ behavior, while $\eta_{\rm ana}$ changes the slope of $\mu_{\rm ana} - E_{\rm eff}$ for a shorter channel device in which significant effects from strain engineering may take place. The most important task in this work is to determine a set of $\eta_{\rm ana}$ and μ_0 that minimizes the difference between $\mu_{\rm ana}$ and $\mu_{\rm universal}$.

An iterative method to determine $R_{\rm sd}$, $\eta_{\rm ana}$ and μ_0 is detailed in Fig. 5(a). For a given $\eta_{\rm ana}$, the summation of the square of the difference between $\mu_{\rm ana}$ and $\mu_{\rm universal}$ at each $E_{\rm eff}$ with modified μ_0 is plotted in Fig. 5(b). By using the MOSFET with a 0.5-μm gate length as an example, it is obvious that a minimum exists at $\eta_{\rm ana}$ = 1/1.7 (∼0.59). This is consistent with the value obtained in Section II, which exhibits a good correlation between $E_{{\rm eff}_CV}$ and $E_{\rm eff_ana}$. For state-of-the-art MOSFETs, localized doping profiles introduced by halo ion implantation from both source and drain sides are not strongly overlapped for a gate length longer than 100 nm. As a result, the substrate doping profile should not change significantly for the MOSFETs with a gate length longer than 100 nm. A consistent value of $\eta_{\rm ana}$ is therefore extracted by using the analytical method described in Section II and by using the iteration introduced in this section for devices having similar substrate doping profiles.

V. Experimental Results

The algorithm introduced in Section IV has been applied to a series of test devices, and the extracted $R_{\rm sd}$ values are shown in Fig. 6(a). Similar $R_{\rm sd}$ values are observed for long- and short-channel devices. This result is expected because all devices are located on a single wafer and share the same process conditions. As also shown in Fig. 6(a), μ_0 increases as $L_{\rm mask}$ shrinks from 1 μm and reaches a peak at 0.1 ∼ 0.2 μm. Below 0.1 μm, μ_0 decreases. This implies that the effects of strain engineering in these devices are more pronounced at $L_{\rm mask}$ values around 0.1 ∼ 0.2 μm. The root cause of the decreasing μ_0 needs more theoretical study.

The gate length dependency of $\eta_{\rm ana}$ is shown in Fig. 6(b). It stays at a constant value for gate lengths longer than 0.1 μm and starts to roll off gradually for shorter gate lengths. As gate length shrinks, substrate doping concentration changes because of overlap of halo ion implantation from the source

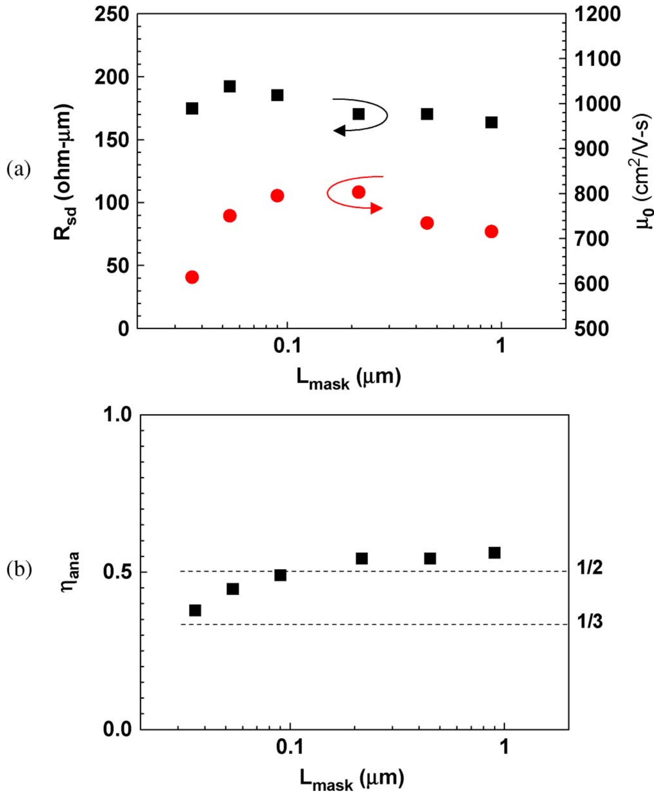

Fig. 6. (a) $R_{\rm sd}$ and μ_0 extracted using the method proposed in this paper. Similar $R_{\rm sd}$ values are extracted over a wide range of $L_{\rm mask}$. μ_0 increases from $L_{\rm mask} = 1\ \mu$m down to $L_{\rm mask} \sim 0.1$ um and then decreases toward the short-channel regime. (b) Extracted $\eta_{\rm ana}$–$L_{\rm mask}$ behavior. $\eta_{\rm ana}$ keeps at a constant level for long-channel devices and then decreases for $L_{\rm mask}$ shorter than 0.1 μm.

and drain sides. Consequently, the value of $\eta_{\rm ana}$ may deviate from that of the long-channel devices. In addition, $\eta_{\rm ana}$ itself is also a function of subband occupancy [26]. When gate length shrinks, 2-D charge sharing from source and drain junctions leads to a reduction in charge confinement in the channel region [27], [28]. This reduction in confinement reduces the subband separation. As a result, η decreases due to higher probability of carriers occupying high-level subbands [26]. The trend of decreasing $\eta_{\rm ana}$ with decreasing gate length supports this argument.

In this section, a self-consistent algorithm has been successfully demonstrated for the extraction of $R_{\rm sd}$ from long-channel to sub-100-nm devices. The extracted $R_{\rm sd}$ shows weak dependency on gate length. The reason for the gate length dependence of each parameter has also been proposed and discussed. This algorithm can easily be implemented with aforementioned analytical equations, and no C–V measurement for short-channel devices is required. These features avoid unnecessary error caused by fringing capacitance and therefore result in an accurately extracted $R_{\rm sd}$.

VI. Discussion

A. Technology Computer-Aided Design (TCAD) as Corroborating Evidence

Based on calibrated TSUPREM and Medici [29] (also used in [4] and [5]), the net doping concentration near the gate edge of a typical NMOSFET ($L_{\rm mask} = 0.1\ \mu$m) used in this work is shown in Fig. 7(a). In a state-of-the-art MOSFET, the doping concentration inside the SDE region is higher than 10^{20} cm^{-3}. It takes only several nanometers to change the doping polarity in the transition region from SDE to channel

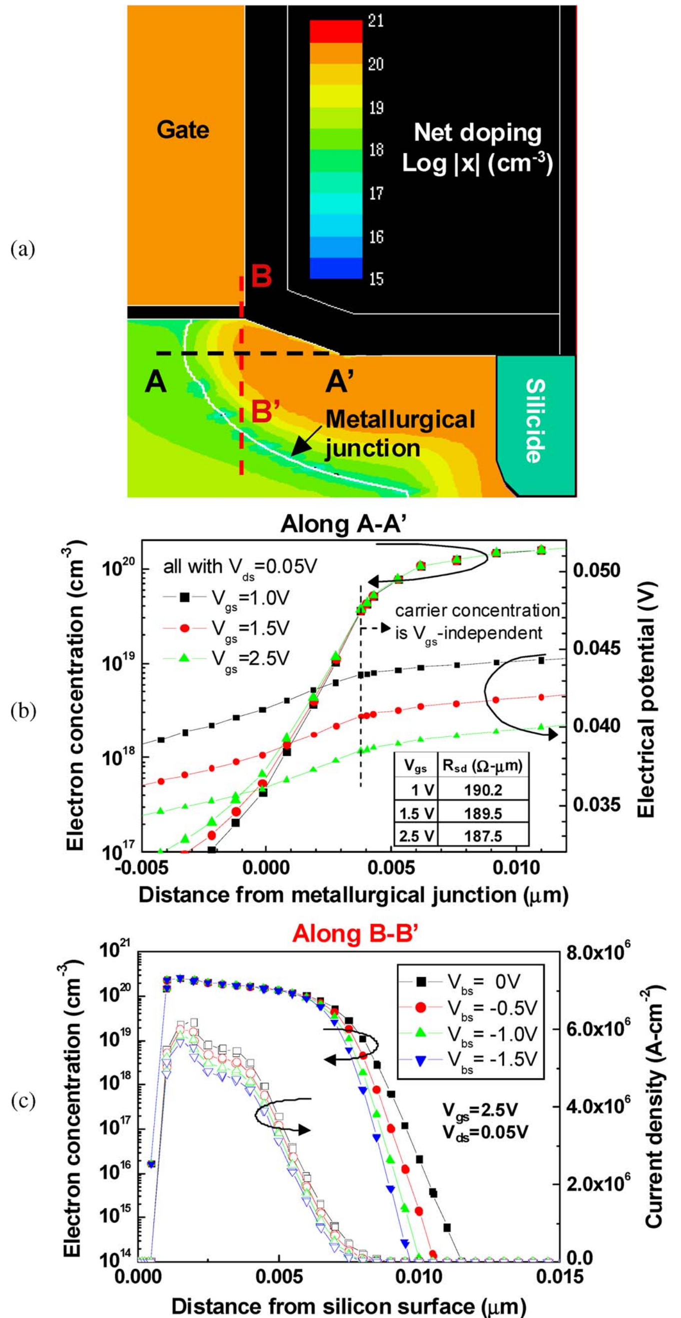

Fig. 7. (a) TSUPREM-4 simulated 2-D doping concentration in the vicinity of gate edge of the NMOSFET used in this work. (b) Carrier concentration on the drain side along the horizontal direction (A−A′), as shown in Fig. 7(a), under various $V_{\rm gs}$ conditions. $V_{\rm gs}$ shows little effect on modulating the carrier concentration inside source/drain extension regions. The inset table provides an example of TCAD-simulated $R_{\rm sd}$ values based on the potential drop between two characteristic points on the drain and the source sides of a 0.1-μm-$L_{\rm mask}$ MOSFET. The $R_{\rm sd}$ values are reasonably consistent with the extracted ones shown in Section V. (c) Carrier concentration along the vertical direction (B−B′), as shown in Fig. 7(a), under various $V_{\rm bs}$ conditions. The current flow in the source/drain extension is mainly located in a region where the carrier concentration is insensitive to $V_{\rm bs}$.

(lateral transition) and SDE to substrate (vertical transition). Fig. 7(b) illustrates the electron concentration on the drain side along the lateral direction A–A′ defined in Fig. 7(a). Over a wide range of bias conditions, $V_{\rm gs}$ shows little effect on modulating the electron concentration inside highly doped SDE region, while the modulation of carrier concentration in the channel region is obvious. In addition, the current flow in SDE is mainly located in a region where the carrier concentration is insensitive to $V_{\rm bs}$, as shown in Fig. 7(c), which is plotted along the vertical direction B–B′ defined in Fig. 7(a). It is obvious that the applied bias shows little effect on modulating both the carrier concentration and current flow inside the highly doped SDE region. Therefore, the $R_{\rm sd}$ values extracted under high-$V_{\rm gs}$ and high-$V_{\rm bs}$ bias conditions well represent the $R_{\rm sd}$ values under regular operating bias conditions for devices with highly doped and abrupt SDE.

On the other hand, when the carrier concentration is lower than a critical value (4×10^{19} cm^{-3} for the device used in this work based on TCAD simulation), it is sensitive to $V_{\rm gs}$ bias conditions, as shown in Fig. 7(b). $R_{\rm sd}$ should comprise the regions (on both source and drain sides) where electrical conductivity is $V_{\rm gs}$ independent. Therefore, $R_{\rm sd}$ can be estimated by subtracting the $V_{\rm gs}$-dependent resistance from total resistance: $R_{\rm sd} = V_{\rm ds}/I_d - \Delta V_c/I_d$, where ΔV_c is the potential drop ($V_{c_{\rm drain}} - V_{c_{\rm source}}$) between two characteristic points where the carrier concentration meets the critical value at the drain and source sides. Based on this method, $R_{\rm sd}$ values are calculated under various bias conditions, and the results are summarized in the inset of Fig. 7(b). The $R_{\rm sd}$ values obtained by using this simulation study are reasonably consistent with the extracted $R_{\rm sd}$ values shown in Section V.

B. On the Bulk Charge Linearization Coefficient α

Bulk charge linearization coefficient (α) is treated as unity in previous sections. The error caused by this assumption is discussed in this section. By definition, $\alpha = 1 + 3T_{\rm ox_inv}/W_D$ [17], where W_D is the channel depletion width. Based on TCAD simulation, W_D is about 43 nm for a 0.1-μm-$L_{\rm mask}$ NMOSFET operated in the linear region ($V_{\rm gs} = 1.5$–2.5 V, $V_{\rm ds} = 0.05$ V, and $V_{\rm bs} = 0$ V), as shown in Fig. 8(a). W_D is much thicker as compared to $T_{\rm ox_inv}$, which is 2.4 nm in this work. As a result, the value of α is 1.17 under this bias condition. When a negative $V_{\rm bs}$ is applied, the value of α further decreases because W_D further increases. A table of values of α under different bias conditions is shown in the inset of Fig. 8(a). As shown in Fig. 8(b), the impact of different values of α, from 1 to 1.4, on the extracted $R_{\rm sd}$ is minor. The assumption of "$\alpha = 1$" is adequate for the proposed $R_{\rm sd}$ extraction method.

VII. CONCLUSION

$R_{\rm sd}$ extraction is realized by using a self-consistent algorithm, combining the constant mobility criterion and an updated analytic calculation of the effective surface electrical field. By matching the shape of universal mobility curves of short- and long-channel devices using an iterative procedure, reasonable $R_{\rm sd}$ values have been obtained for a wide range of gate lengths without requiring information about $L_{\rm eff}$, $C_{\rm ox}$, and $W_{\rm eff}$. Even in the presence of process-variation-induced uncertainty, the proposed method has proved promising for short-channel devices with heavily doped SDE.

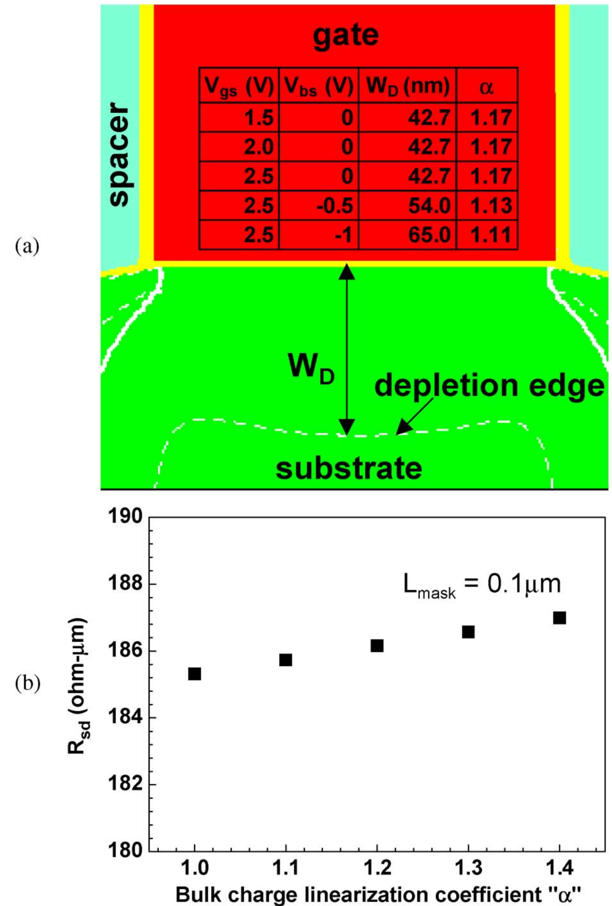

Fig. 8. (a) Schematic plot of depletion width under gate area of a 0.1-μm-$L_{\rm mask}$ NMOSFET. A table of values of bulk charge linearization coefficient "α" under various bias conditions is shown in the inset. The values of "α" are typically lower than 1.2. (b) Extracted $R_{\rm sd}$ shows negligible sensitivity on the bulk charge linearization coefficient. Therefore, the assumption of "$\alpha = 1$" is adequate in this extraction procedure.

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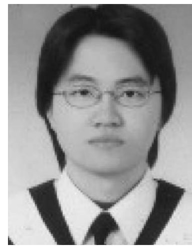

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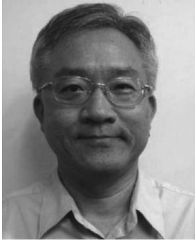

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