An Interconnecting Technology for RF MEMS Heterogeneous Chip Integration

Tzu-Yuan Chao, Chun-Hsing Li, Yang Chuan Chen, Hsin-Yu Chen, Yu-Ting Cheng, *Senior Member, IEEE*, and Chien-Nan Kuo

***Abstract*—An interconnecting technology using a Au–Au thermocompressive bond has been successfully developed for microelectromechanical system (MEMS) heterogeneous chip integration in this paper. The Daisy chain and RF transition structures are both designed and fabricated for the electrical characterization of the interconnect scheme. Measured dc contact resistance is about 14 ± 5 mΩ for the bonding interface of Ni (1 μm)/Au (0.4 μm)/Au (0.4 μm)/Ni (1 μm) with a pad size of 40 μm in diameter. The electrical transition between two chips, which have coplanar waveguides (CPWs) and microstrip lines, respectively, can be well interconnected with less than −15 dB return loss and −1.8 dB insertion loss up to 50 GHz without implementing complex structure designs and extra impedance matching networks in the transition by employing this technology. Meanwhile, it is found that the mechanical strength for the interconnecting bond can be as large as 100 MPa. A low-power RF low-noise amplifier has been successfully designed, fabricated, and utilized in this paper to demonstrate the feasibility of the interconnecting technology for RF MEMS heterogeneous chip integration by integrating a Taiwan Semiconductor Manufacturing Corporation 0.18-μm RF complimentary metal–oxide–semiconductor chip with a silicon carrier, where high Q MEMS inductors are fabricated and utilized for good circuit performance in terms of excellent impedance matching, power gain, and gain flatness.**

***Index Terms*—Au–Au thermocompressive bonding, bumpless interconnecting, flip chip (FC), heterogeneous chip integration, high Q microelectromechanical system (MEMS) inductor, low-noise amplifier (LNA).**

I. Introduction

PROCESS integration is a critical research topic in the development of micromechanical circuitry for wireless communication applications [1]–[4]. From surface, bulk, to CMOS-microelectromechanical system (CMOS-MEMS) micromachining processes, the tradeoff among device performance, material selection, process compatibility, and manufacture cost is required in design consideration while the machining techniques are employed for MEMS fabrication. For example, Nguyen and Howe [1] presented the first integrated high Q MEMS CMOS oscillator showing the potential of RF MEMS for low-power wireless communication applications. The work must utilize all tungsten interconnects for surviving in a post-CMOS poly-Si surface micromachining process with a processing temperature up to 835 °C. The nonstandard CMOS interconnect material with high electrical resistivity makes the approach not practical for the technology continuation of CMOS scaling. Weigold *et al.* [2] developed a merged process to integrate thick single-crystal Si resonators with a bipolar CMOS (BiCMOS) circuit for having high intrinsic Q factor performance. Deep silicon doping, i.e., 15 μm in depth, which is not an economical BiCMOS process, is required for etching stop in the ethylenediamine pyrochatechol release process. Although Lakdawala *et al.* [3] and Oz and Fedder [4] demonstrated a series of monolithic RF integrated circuits using MEMS-type passives fabricated by a standard CMOS process, only the backend aluminum and aluminum-oxide layers can be utilized as structural materials of RF MEMS components. Inevitable stress compensation and material property limitation would complicate the device design. In comparison with the integration approaches, post-CMOS electroforming techniques [5], [6] might be an ultimate integration solution of RF CMOS-MEMSs with several process advantages, including flexible material choice, low process temperature, and high manufacturing throughput. Mechanical deficiencies of metal-based materials, such as fatigue, aging, and low stiffness, still need to be resolved as the structural material of MEMS devices [7]–[9]. Therefore, it is critical to develop an integration scheme with the least tradeoff design for RF CMOS-MEMS fabrication.

Meanwhile, Si-based system-on-a-package (SOP) schemes have been proposed for microsystem fabrication in recent years [10]–[13]. Instead of building everything on a single chip, discrete components are designed and fabricated on separate chips and then fully integrated onto a silicon substrate to form a microsystem. A compact microsystem can be realized with the design flexibility without having any material and process limits for better performance. In addition, using silicon instead of ceramic or a printed-circuit-board (PCB) material as the packaging substrate can ensure the SOP scheme to be suitable for high-density interconnects due to a perfect coefficient-of-thermal-expansion match, which will not induce thermal stress to cause reliability problems in chip assembly. The contact size of the chip-to-silicon substrate can be reduced to several tens of micrometers in diameter [10]. Thus, a heterogeneous chip integration scheme, as shown in Fig. 1, is presented in this paper by adapting the SOP concept to integrate a CMOS circuit chip

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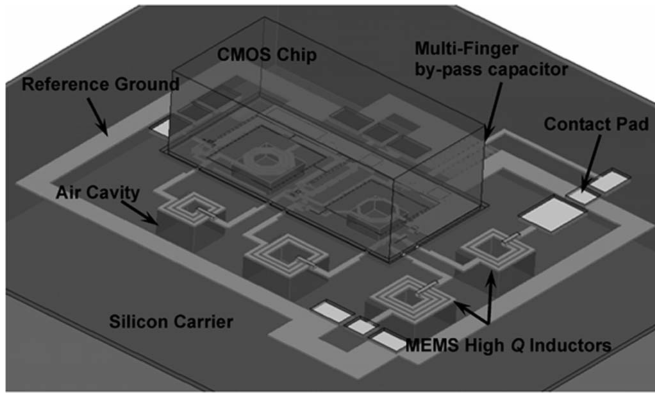


Fig. 1. MEMS heterogeneous chip integration.

with a micromachined silicon carrier, where high-performance RF MEMS components are fabricated.

Previously, Carchon *et al.* [13] successfully demonstrated a similar silicon-based multi chip module-deposited (MCM-D) technology for the integration of 0/1-level packaged RF-MEMS devices at millimeter-wave frequencies. Although this paper had shown excellent RF characteristics in the integration of a silicon substrate with an RF MEMS chip, most of research works were merely concentrated in the performance study of connected RF passive components without involving in any active CMOS circuit, which is, however, the most critical component in the development of RF MEMSs for wireless transceiving system applications. In comparison with the MCM-D technology using Au-stub interconnects, better system performance with more design flexibility can be further expected in the realization of RF CMOS-MEMSs since the scheme proposed here for multiple chip integration is aimed at a system structure with the interconnect configuration similar to that of a system-on-a-chip (SOC). Nevertheless, in the heterogeneous chip integration scheme, a flip-chip (FC) bonding technique is the key to achieve chip assembly with better interconnect performance. The conventional FC technology like Carchon *et al.*'s approach has been widely utilized for microelectronic packaging applications because it can enable the electrical interconnects between chips to have high-density and low parasitic reactance characteristics. However, large solder bumps for the interconnects still exhibit no negligible parasitic effects. While the device size continues to shrink, the parasitic effect can cause large sensitivity reduction of devices. While the frequency of the electrical signal transmitted within chips is greater than 10 GHz or even higher, the parasitic effect will result in the drastic increase in return loss in the interconnecting transition. Therefore, a bumpless bonding technique must be developed and implemented in the proposed integration scheme to further reduce the bump size effects for having an interconnection with low loss, wide bandwidth, high speed, and ultrafine pitch characteristics [16]–[18].

Previously, several bumpless interconnecting and microbumping concepts have been developed and implemented in the FC technology [14]–[18]. Saito *et al.* [16] utilized the surface activated bonding (SAB) [14], [15] to realize high-density bumpless interconnection from a Si chip to a polyimide substrate in which a pad loss at 20 GHz will be about 1/20 of that of wire bonding. In 2006, the same group also demonstrated Si-to-Si bumpless ultrafine pitch interconnects using the Cu SAB technique in which about 0.1-μm bump height and less than 10-μm pitch can be achieved [17]. The mechanism of SAB is based on the adhesive force formed by two atomically clean surfaces with intimate contact. The clean surfaces must be formed by a chemical–mechanical planarization process combined with the Ar fast atom beam (Ar-FAB) or Ar plasma irradiation treatment in an ultrahigh vacuum environment. Since the SAB has the characteristics of low process uniformity tolerance, long activation time ($\sim$30 min), and special customized tool requirement, it is difficult to be implemented for mass production. IBM Research demonstrated a controlled collapse chip connection (C4) microbump interconnect technique, which can provide conventional Pb and Pb-free solder bumps with $\sim$10 μm bump height, 25 μm in diameter, and 50 μm pitch size at the wafer level (200 mm) by an electroplating method [18]. The contact resistance can be achieved as low as several milliohms depending on the type of the solder material used for the microjoint. However, the microsolder bumping process requiring electroplating is generally the last process step that could raise the process integration problem for most of MEMS chips.

In this paper, a bumpless interconnecting technique is presented based on a self-interlocking design with a Au–Au thermocompressive bond for realizing the proposed heterogeneous chip integration scheme. A low-power RF low-noise amplifier (LNA) is designed, fabricated, and utilized to demonstrate the technology feasibility by integrating a TSMC 0.18-μm RF CMOS chip with a silicon carrier where high Q MEMS inductors are designed and fabricated in-house. In comparison with the aforementioned interconnecting technologies, a near-zero bump height and a post-CMOS compatible process without solder bumping on the CMOS chip can provide a total solution not only to the characteristic impedance matching problem raised in electromagnetic (EM) signal transmission between RF circuits but also to the heterogeneous chip integration of RF MEMS fabricated by different fabrication processes.

II. Bumpless Interconnect Design and Fabrication

A. Bumpless Interconnecting Scheme

Fig. 2 shows a typical FC transition from one interconnect line on a chip to another on a PCB and the corresponding equivalent circuit model, respectively [19]–[21]. The lump elements L_S, R_S, C_M, C_C, G_M, and G_C are the bump inductance, the radiation loss resistance in bump [20], the discontinuity capacitance at the PCB and the one at the chip, and the substrate loss conductance of the PCB and that of the chip, respectively. In general, series resistance R_S and shunt conductance G_M (G_C) are small enough to be neglected; the effective bump impedance can be calculated as follows:

$$z_{\text{bump}} = \sqrt{\frac{L_S}{C_M + C_C}}. \quad (1)$$

In the FC transition, the structure geometry and parasitic discontinuity capacitance C_M and C_C would lead the transition with a capacitive dominant characteristic, which results in a low bump impedance smaller than the system characteristic

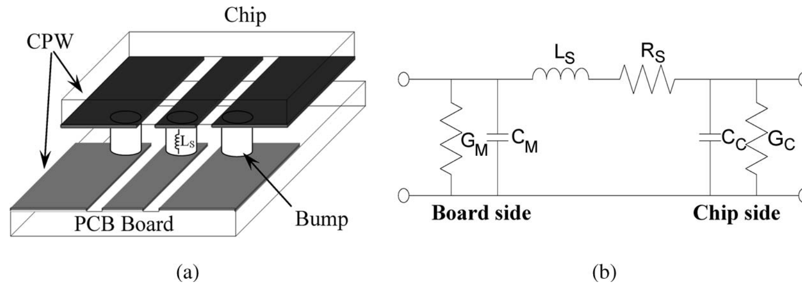


Fig. 2. (a) Typical FC transition structure and (b) corresponding equivalent circuit model.

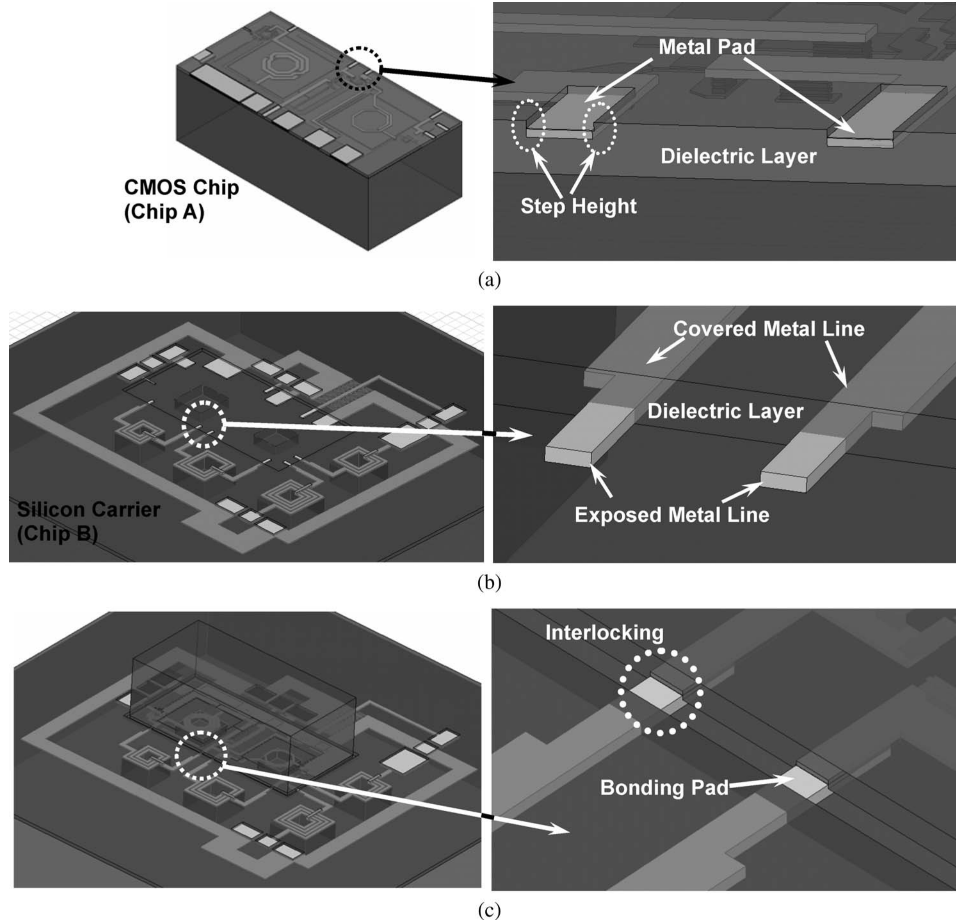


Fig. 3. Self-interlocking bumpless interconnecting technology proposed for heterogeneous chip integration. (a) CMOS chip after blade dicing. The enlarged view of a diced CMOS chip near bonding pads shows a step height between the top surface of the bonding pad and the passivation. (b) Silicon carrier is fabricated using a standard CMOS backend process and a MEMS process. The backend process is utilized to fabricate interconnect lines and bonding pads for the CMOS chip assembly, and a MEMS process is utilized to etch silicon, which is underneath the inductors for the purpose of substrate loss reduction. The thickness of the exposed metal line should be thicker than the step height on the CMOS chip. (c) CMOS chip is integrated with the carrier using the bumpless interconnecting technology. The inset shows that the concave pad on the chip will be self-interlocked with the metal line on the carrier during the chip integration.

impedance of 50 Ω. Wang and Wu [19] estimated that the effective bump impedance of a typical FC structure with 127 μm in bump height, 160 μm in bump diameter, and 200 μm in pad size is about 32 Ω, where series inductance L_S and shunt capacitance C_M (C_C) are 68.67 pH and 34.91 fF, respectively. To solve the 50-Ω matching problem resulted by the FC transition, several compensation structures like the staggered structure [22], high impedance line [23], and ground retreat [19] have been applied to reduce excessive capacitance of the transition and to make the FC transition with a 50-Ω impedance for lowering return loss. On the other hand, bumpless interconnecting is an alternative approach enabling the FC transition to have almost zero bump height and tiny bump pad size that can be reduced down to several micrometers. L_S and C_M (C_C) can be further neglected by the reduction of inductance and fringing capacitance, and the impedance of the FC transition will become negligible in the two connected 50-Ω transmission lines at a low frequency. To minimize the transition impact to the two connected transmission lines, the bumpless interconnecting can also simply reduce the return loss of the transition without adapting the complex compensation structure requiring customized design.

Fig. 3 shows the scheme of the proposed self-interlocking bumpless interconnecting technology. As aforementioned, the

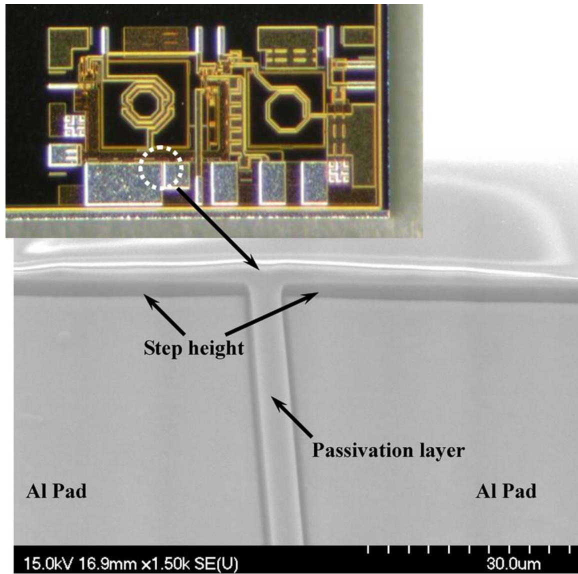


Fig. 4. SEM photograph of the enlarged view on the corner of an Al pad shows a step height between the top surfaces of the Al contact pad and the passivation in a standard CMOS chip. (Inset) Optical micrograph of the TSMC 0.18-μm mixed signal CMOS chip.

silicon carrier can be fabricated using either the same as or different from standard CMOS processes for having good process design flexibility in terms of the performance consideration of MEMS devices. For a standard CMOS chip, Si_3N_4 or polyimide will be deposited last on the top of CMOS circuitry as a passivation layer to prevent possible contamination, damage, and corrosion. For example, a TSMC 0.18-μm mixed signal CMOS chip has a 1-μm altitude difference between the top surfaces of the Al contact pad and the passivation, as shown in Fig. 4. Concave pad structures with the same step height generally form on the top of the chip, and solder balls are, conventionally, put inside the pads and utilized as metallurgical and electrical connection for chip assembly. This paper presents an alternative joint scheme, as shown in Fig. 3, where one end of the concave pad structures is removed first (chip A), the signal line, i.e., the electrical interconnect line, on the other chip (chip B) is opened, and then the electrical joint is achieved by mechanically interlocking and bonding the pads with the lines using a Au–Au thermocompressive bond to make two chips become a "single" chip. The interlocking mechanism can effectively prevent the metal interconnect line from the horizontal shift to be blocked by the edge of the concave pad, particularly when two chips are bonded on an unleveled bonder stage. Thus, the design rule for the interconnect line in a silicon carrier and the contact pad on a CMOS chip is determined based on the alignment accuracy provided by an FC bonder. For instance, the width of the contact pad is larger than the width of the interconnect line by 2 μm, which is two times larger than the maximum misalignment distance of the bonder used in this paper. Because the metal lines on a chip can be directly connected with the contact pads, the characteristics of almost zero bump height and similar signal line width between chips can allow a high-frequency EM signal to directly pass through the metal joint with the lowest power loss due to

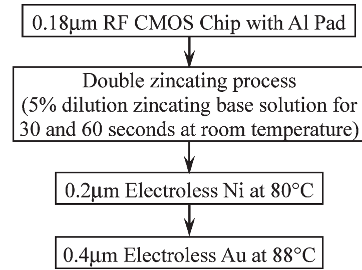


Fig. 5. Process flow of maskless metallization to the CMOS chip.

diminutive characteristic impedance mismatch and parasitic effects resulted by the minute structure discontinuity.

Several issues need to be addressed in the proposed bumpless interconnecting technology. First, all contact pads of the CMOS chip should be designed and located on the periphery of the chip. Second, either a blade or laser dicing process must be employed to remove the edge of the chip, so that one end of the contact pads can be opened. Third, because the contact pad and the metal line of a CMOS chip are either made of Cu or Al determined by the process node chosen for the CMOS chip fabrication, a metallization process and related electrical characterization must be developed for the chip assembly. At last, a Au–Au thermocompressive bond and related metallization processes must be developed and utilized as the last processing step in this paper to realize the proposed interconnecting technology.

B. Bonding Metallization and the Carrier Fabrication Process

In this paper, an ultrawideband (UWB) tunable LNA will be demonstrated for verifying the bumpless interconnecting technology for RF MEMS heterogeneous chip integration. The process for the metallization of contact pads is described as shown in Fig. 5. The metallization for the bonding is a maskless process. First, double-zincating processes on the Al pads of the CMOS chip are performed in a 5% diluted zincating-based solution for 30 and 60 s, respectively, at room temperature. Before starting the secondary zincating process, the Al pads should be put into a 10% diluted nitric acid for 30 s to remove the first Zn layer formed on the top of the pads. The purpose of double zincating is to deposit a uniform Zn layer on the Al pad for being a catalytic and adhesion layer for following electroless Ni deposition [24]. After the zincating process, serial electroless plating processes of 0.2 μm Ni and 0.4 μm Au are performed at 80 °C and 88 °C, respectively. Finally, blade dicing is performed on the CMOS chip to remove the edge of bonding pads. Once the contact pads are opened, the chip is ready for following Au–Au thermocompressive bonding.

It is noted that because several advanced CMOS processes have used Cu instead of Al as the material of metal interconnects and contact pads, the metallization will be slightly different from the previous one. Instead of double zincating, the chip is firstly put into a Pd catalyst solution for 30 s to activate the surface of Cu pads. In the process step, Pd is deposited on Cu pads as the catalyst seed for following electroless Ni plating.

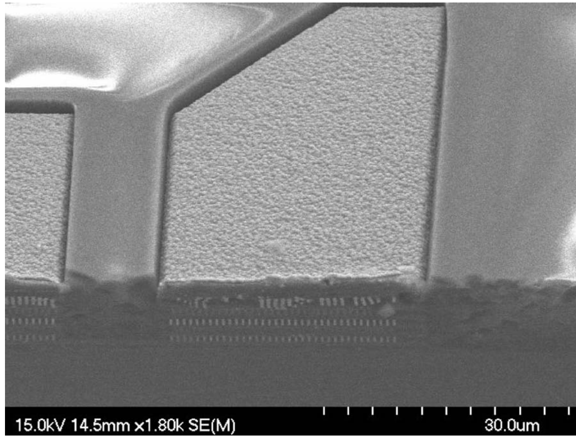


Fig. 6. SEM photograph of the enlarged view on the diced edges of the CMOS chip.

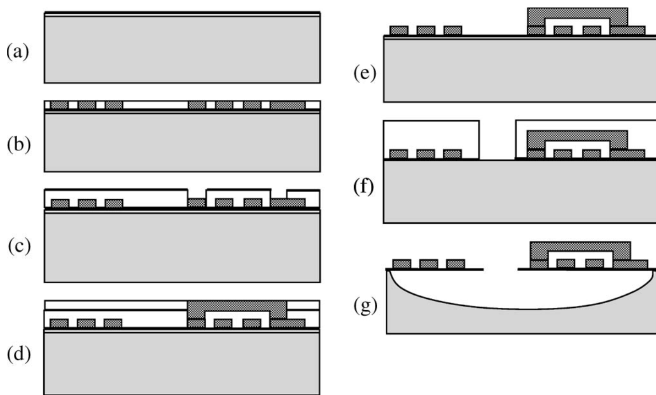


Fig. 7. Silicon carrier fabrication processes: (a) $SiO_2/Si_3N_4/SiO_2$ membrane and Ti/Cu seeding layer deposition, (b) first Cu plating, (c) via patterning and air-bridge seeding layer deposition, (d) air bridge and via plating, (e) photoresist and seeding layer removal, (f) membrane patterning by reactive ion etching, and (g) silicon substrate removal using XeF_2 gas followed by a photoresist strip.

After seeding, the Ni and Au electroless deposition processes, same as the aforementioned one, are performed for having a layer of 0.2 μm Ni/0.4 μm Au on the Cu pads for the following bonding process. Fig. 6 shows the enlarged view of contact pads on the CMOS chip right after Ni/Au metallization and blade dicing. The SEM picture shows that the contact pads are uniformly coated with a Ni/Au layer and have smooth surface morphology for following bonding.

For the verification of the UWB tunable LNA using the bumpless interconnecting technology, a silicon carrier will be designed and fabricated with high Q MEMS inductors [25], bypass capacitors, reference ground, and signal pads. Fig. 7 illustrates the fabrication processes of the silicon carrier. The fabrication begins with 0.7 μm wet oxidation on a p-type Si wafer, followed by 0.7 μm low-pressure chemical vapor deposition (CVD) Si_3N_4 and 0.7 μm plasma-enhanced CVD tetraethoxysilane SiO_2 deposition as an electrical insulation layer. A layer of Ti (10 nm)/Cu (90 nm) is then sputtered onto the silicon substrate as a seeding layer for Cu electroplating, as shown in Fig. 7(a). Fig. 7(b) shows that a 6 μm-thick AZ-4620 photoresist is coated and patterned on the top of the electrical insulation layer as a mold structure for 5 μm-thick electroplated Cu to make the coil part of the spiral inductor. After the first layer of Cu plating, a 10 μm AZ-4620 is coated, patterned, and sputtered with another 120 nm Cu seeding layer, as shown in Fig. 7(c), for the air-bridge Cu via filling. Fig. 7(d) shows that another 10 μm AZ-4620 is then utilized to be the mold for 5 μm Cu plating for the air-bridge fabrication of the inductor. The fabrication of the spiral inductor is done after stripping the photoresist and the seeding layer by acetone, CR-7T, and buffered oxide etchant, respectively, as shown in Fig. 7(e). Once the inductor is fabricated, the bonding pads will be metallized by serial electroplating processes of 1 μm Ni and 0.4 μm Au as described in the previous Cu pad metallization for bonding. For high Q performance, the Si under the inductors is removed to reduce eddy current loss. Fig. 7(f) shows that the $SiO_2/Si_3N_4/SiO_2$ membrane in the center of inductors is reactive ion etched to expose Si for following XeF_2 isotropic etching. Finally, the photoresist mask is stripped by acetone, as shown in Fig. 7(g).

III. Results and Discussion

A. Bumpless Interconnect Bonding

For most of the RF SOP schemes, it is a common feature to bond a circuit chip with a substrate carrier in which high-performance passives, including capacitors, inductors, and filters, are fabricated [26]–[28]. To electrically bridge the two chips, a transition structure from a CPW to a microstrip line and related RF characteristics are critical to the design of the RF SOP. Therefore, an electrical transition from CPWs to microstrip lines, which are designed and fabricated on a silicon carrier substrate and a TSMC 0.18-μm RF CMOS chip, respectively, is utilized to verify the effectiveness of the proposed bumpless interconnecting technology.

Regarding the substrate carrier part, probing pads and CPWs are designed and fabricated on a silicon substrate using the aforementioned Cu electroplating technique for RF characterization. Here, CPWs and microstrip lines are both designed with the same characteristic impedance and signal line width, which are 50 Ω and 10.5 μm, respectively. The structure design is based on the assumption of 10 S/m substrate conductivity. Fig. 8 shows the micrographs of the CMOS chip before and after being diced and the as-fabricated silicon carrier, respectively. The dashed lines in Fig. 8(a) indicate the dicing traces that are cut for bonding, as shown in Fig. 8(b). The reference plane is defined at the edge of contact pads using thru-reflect-line (TRL) calibration [29] for RF characterization, as shown in Fig. 8(c). The air bridge between two grounds is used to inhibit odd-mode excitation in the CPW. The CMOS chip and the Si carrier, which contain microstrip lines and CPWs, respectively, are bonded together under the conditions of 300 °C at the carrier, 180 °C at the chip, and 50 MPa applied pressure for 3 min.

Fig. 9 shows the SEM photographs of the chip-to-carrier assembly. An enlarged view of the SEM picture on the bonding interface shows that there is about 2-μm misalignment. The misalignment is caused by the malfunction of interlocking

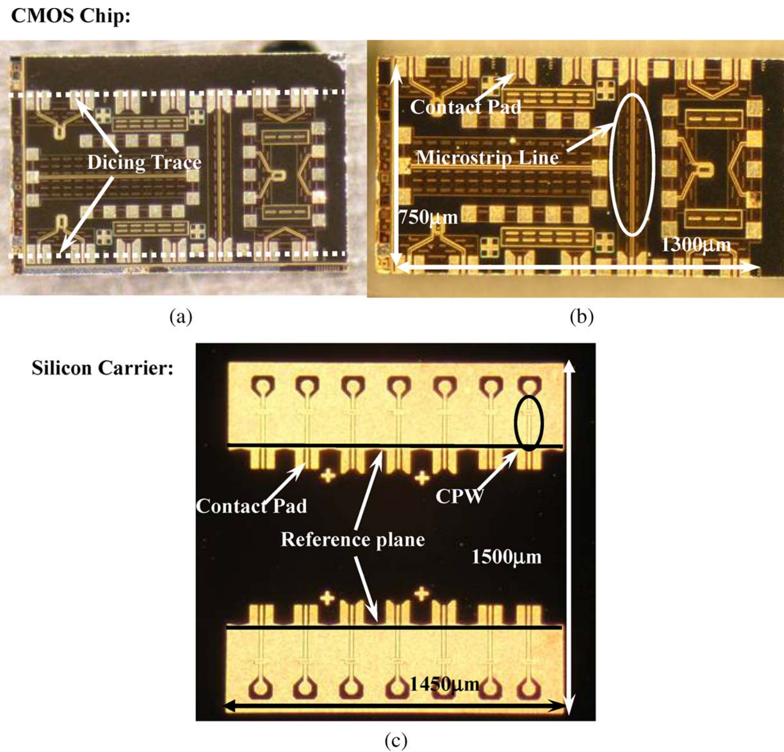


Fig. 8. Optical micrographs of (a) before, (b) after a blade dicing the CMOS chip, and (c) as-fabricated silicon carrier.

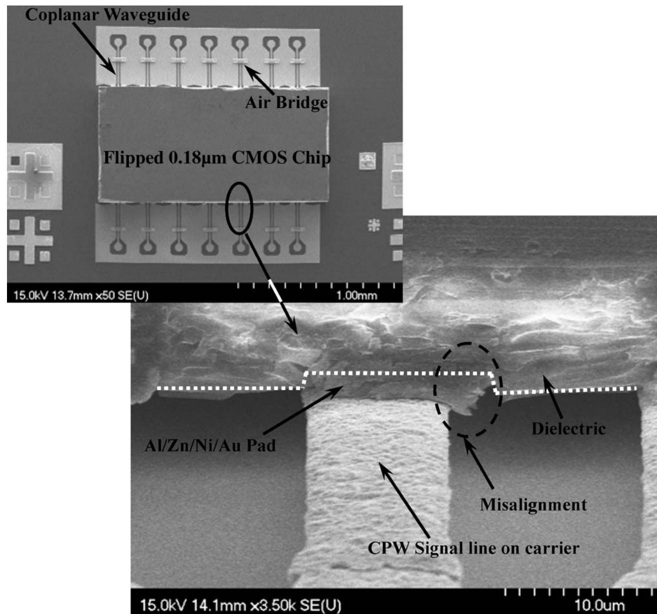


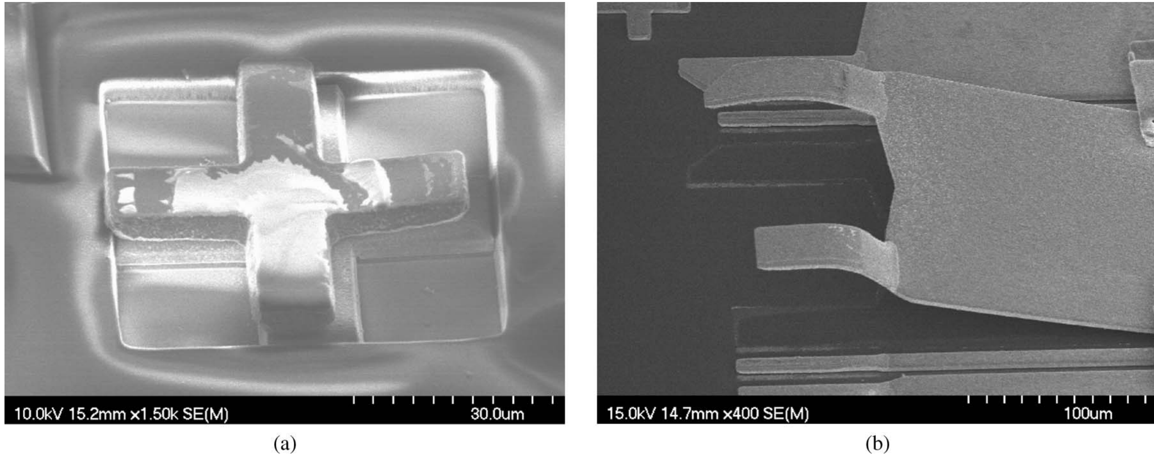
Fig. 9. (Top) SEM photograph of the chip-assembly result and (bottom) an enlarged view at the bonding area.

resulted by the overplating of Zn/Ni/Au layers on the Al pad. Such a malfunction can be further resolved by a better process control. After forcefully pulling the bonded CMOS chip away from the Si carrier, it is found that a cross-alignment mark on the carrier is totally transferred and attached onto the CMOS chip [Fig. 10(a)], or the Cu line deposited on the carrier can be lifted [Fig. 10(b)]. The results indicate that the Au–Au thermocompressive bond is strong enough to break the interface between Ti and SiO_2, which is about 100 MPa [30].

B. Electrical Characterizations of the DC Contact and the RF Transition Structure

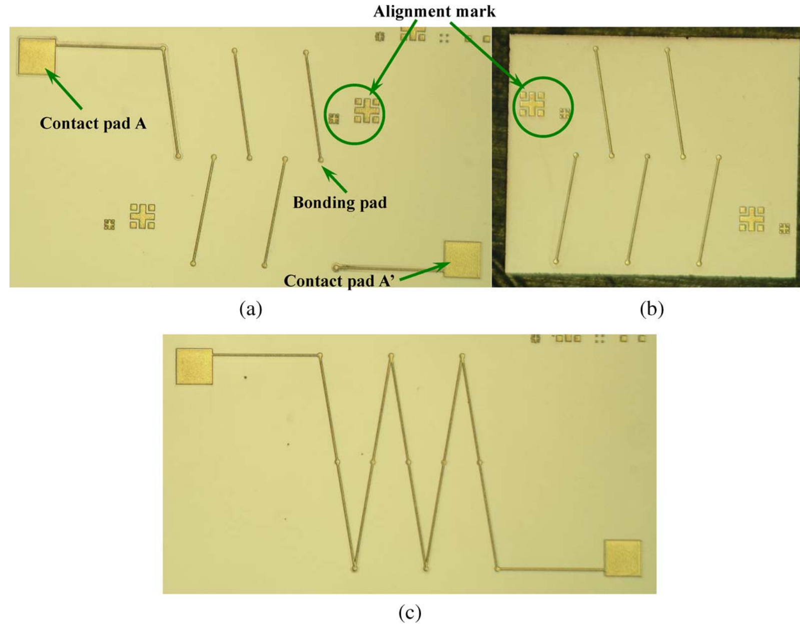
The electrical contact resistance of the Au–Au thermocompressive bonding is characterized using the test structure, i.e., the Daisy chain, as shown in Fig. 11. The Daisy chain is fabricated using the aforementioned Cu-plating and metallization processes. Ten corresponding bonding pads with complementary conducting lines are both designed on two separate chips [Fig. 11(a) and (b)]. Thus, the total contact resistance can be obtained by subtracting the resistance of the line pattern [Fig. 11(c)] from the resistance measured from two contact pads, A and A′, once the two chips are bonded. The contact resistance for each bonding pad can be derived by dividing the total contact resistance by the total number of bonding pads. The contact resistance is about 14 ± 5 mΩ for each circular bonding pad of 0.4 μm Au/1 μm Ni with a radius of 20 μm.

Two-port S-parameters of the transition structure are measured using Agilent E8364B PNA and Cascade Infinity GSG probe in the frequency range from 10 to 50 GHz, as shown in Fig. 12. The measured S-parameters have excluded the parasitic effect from measurement pads and have a reference plane to the edge of the bonding pad via TRL calibration. The assembly technique provides about -1.7 dB insertion loss and -15 dB return loss at 40 GHz, including the transmission loss of the microstrip line. The high-frequency structural simulation at 75 S/m silicon conductivity shows comparable S11 and S21



(a) (b)

Fig. 10. Enlarged SEM photographs of (a) alignment mark on the CMOS chip transferred onto the silicon carrier and (b) lifted Cu line on the silicon carrier after forcefully separating the bonded transition structure.



(a) (b)

(c)

Fig. 11. Optical micrographs of dc contact resistance test structures, i.e., the Daisy chain, including two separate chips (a, b), and a line pattern (c) for de-embedding.

values as compared with the measurement result. The discrepancy between the measurement and the simulation could be attributed to the aforementioned bonding misalignment and process variation. Nevertheless, the measurement result has revealed that the low loss and wide bandwidth characteristics of the bumpless interconnecting technology have the potential for RF chip integration.

C. UWB LNA With MEMS Inductors

In the present RF receiver architecture, an LNA is usually the first signal processing circuit right after an antenna receives an RF signal. The implementation of high Q inductors in the LNA can greatly improve the circuit performance like low power, low noise, high gain, and high tuning range [31], [32]. Previous investigations have shown that MEMS inductors can also exhibit high Q characteristics on a silicon substrate using a silicon micromachining technique to effectively reduce ohmic and eddy current losses [25], [33]. Thus, a low-power RF LNA is designed, fabricated, and utilized to demonstrate the heterogeneous chip integration technology by integrating a TSMC 0.18-μm RF CMOS chip with a silicon carrier, where high Q MEMS inductors are designed and fabricated in-house as aforementioned. The conductivity of the silicon carrier used in the RF LNA is 5 S/m rather than the aforementioned 75 S/m conductivity. Fig. 13 shows the scheme of the LNA circuit where four high Q MEMS inductors, i.e., L_1, L_2, L_g, and L_{d1}, are employed to improve the circuit performance. On the input side, the three inductors L_1, L_2, and L_g are used for broadband input impedance matching to decrease the thermal noise due to small parasitic resistance. Another inductor L_{d1} at the tunable LC resonator is used to provide high power gain and to maintain good gain flatness as a result of the wideband performance in terms of a high Q factor. Fig. 14 shows the SEM picture of the as-fabricated LNA circuit using the proposed bumpless chip-assembly technique. Circuit simulation shows

(a) (b)

(c) (d)

Fig. 12. Simulation and measurement results of (a) return loss and (b) insertion loss of the EM signal propagating through the transition design with the transmission lines, a CPW, and a microstrip line, and corresponding measurement results of (c) return loss and (d) insertion loss shown in Smith charts.

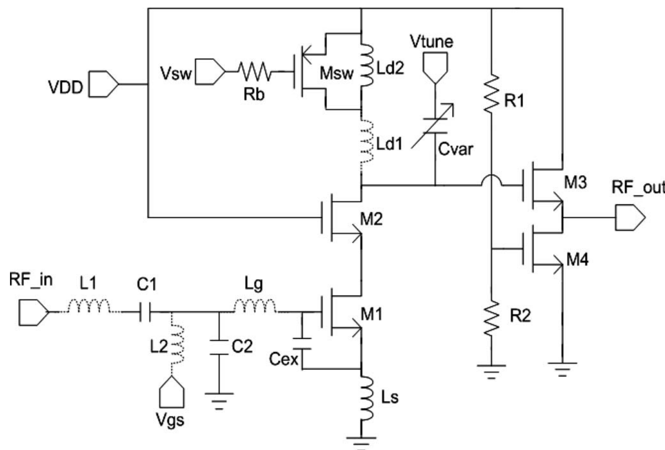


Fig. 13. Tunable LNA circuit. Four high Q MEMS inductors (as shown in dashed lines) are utilized to improve the circuit performance.

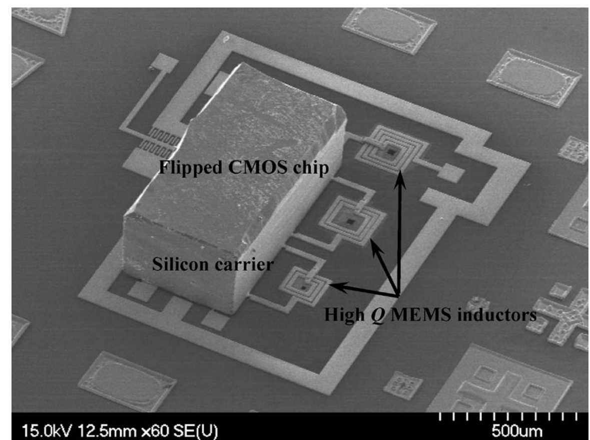


Fig. 14. SEM photograph of the UWB tunable LNA with high Q MEMS inductors. The rectangular holes located in the center of inductors provide a path for XeF_2 vapor isotropic etching.

that the LNA can have about 50% power savings and 50% tuning range enhancement in comparison with the LNA circuit using the conventional CMOS inductors [34].

Fig. 15 shows the comparison between simulated [Fig. 15(a)] and measured [Fig. 15(b)](Table I) S11 and S21 with a different tuning voltage in the LNA circuit. There are discrepancies in

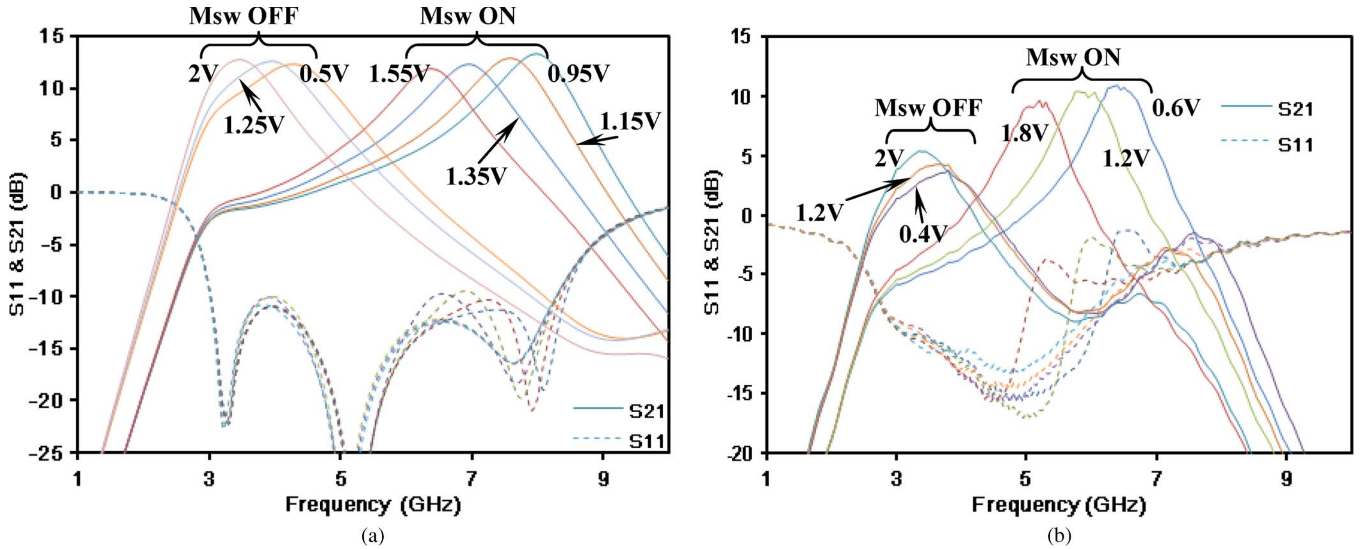


Fig. 15. (a) Simulation and (b) measurement results of the return loss and gain with a different tuning voltage of the UWB LNA circuit.

TABLE I
COMPARISON OF AU BUMP, AU STUD BUMP, AND NI/AU BUMPLESS PROCESSES [35], [36]

Bump type	Au bump	Au stud bump	Ni/Au bumpless (This work)
Process Technique	Electroplating	Wire bumping	Electroless deposition
Advantages	● Flexible bump shape ● High throughput in a batch process	● Cost-effective for low bump counts ● Rapid prototyping	● Maskless metallization and a typical process in packaging house ● Flexible bump geometry and pitch size ● Almost zero bump height ● High throughput in a batch process
Disadvantages	● Lithography process required for bump formation ● Not a typical metallization process in foundry and packaging house ● Large pitch size due to the lateral flow of bumps	● Low throughput for bump formation ● Large pitch due to the lateral flow of the bumps	● Bond pads limited to the periphery of a chip ● High chip dicing accuracy required on bump pads

S11 and gain degradation. The bandwidth of measured S11 is narrower than that of the simulation one and varied with the tuning voltage. The discrepancy could be caused by EM field coupling within inductors, which would result in input mismatch. The effect, in fact, can be resolved by adding guard rings around the inductors for the enhancement of EM signal isolation and by removing more Si underneath the inductors for Q enhancement to realize higher gain performance.

Although the function of self-interlocking was not fully demonstrated in this experiment due to the overplating of the Zn/Ni/Au layer on the CMOS chip, it can be resolved by process optimization. Nevertheless, it is noted that Ni, in the bonding scheme, not only plays a role as a seeding layer for following Au plating but also acts as a diffusion barrier to Au. In this paper, the Au–Au thermocompressive bond is chosen to realize bumpless interconnecting unlike the under-bump metal (UBM) of the packaging, where the Au layer is only used as a wetting layer to the solder for FC bonding. Thus, to effectively prevent Au from diffusing into a CMOS chip, to have a strong Au–Au bond, and to maintain self-interlocking mechanism, further process characterizations, including the thickness control of the Ni/Au metallization and related bonding quality and reliability investigation, are required for having an optimal process condition for manufacture applications. In fact, in comparison with the other two kinds of Au–Au thermocompressive bonding techniques proposed for FC applications, i.e., the Au bump and the Au stud bump, as listed in Table I [35], [36], the presented Ni/Au bumpless metallization for Au–Au thermocompressive bonding has shown a great potential in chip integration with the characteristics of high throughput, flexible bump geometry and pitch size, low cost without a lithography process, and almost zero bump height for high-frequency signal transition. In addition, the previous study has shown that the electromigration of a typical Pb-free solder using Ni-P/Au UBM is mainly caused by the movements of Sn atoms against the electron flow [37]. Since there is no Sn solder required in the bonding scheme, a better electromigration characteristic can be expected. Nevertheless, the long-term reliability investigation regarding our proposed assembly scheme is still undergoing.

The bumpless interconnecting technology can provide low parasitic capacitance and small contact resistance for chip assembly and make the electrical joint behave like a simple

interconnect line, which can reduce IC design complexity, provide process flexibility, and make the whole system perform like the SOC. Thus, in addition to MEMS inductors, RF MEMS components, such as switches, tunable capacitors, inductors, antennas, and BAW resonators, can be easily implemented for RF microsystem fabrication based on the heterogeneous chip integration scheme with the bumpless interconnecting technology. Although this paper only demonstrated an integration of a CMOS chip to a silicon carrier, the scheme can be utilized for a CMOS chip to a CMOS chip, a MEMS chip, or a III–V chip integration, and to provide an alternative technique for heterogeneous integration applications without modifying the existed chip design. Owing to the intrinsic characteristic of heterogeneous chip integration, the scheme can further ensure a cost-effective CMOS-MEMS fabrication process without sacrificing system performance as the scaling of CMOS technology is down to 90 nm or even further.

IV. Conclusion

A bumpless interconnecting scheme has been presented for MEMS heterogeneous chip integration based on the developed Au–Au thermocompressive bonding. The scheme can fully integrate a CMOS chip with another chip, which can be another CMOS, MEMS, III-V, or silicon carrier chip. The dc and RF electrical behaviors of the bumpless interconnect have been characterized and have shown good broadband transition performance. A low-power broadband LNA circuit has been realized using the bumpless interconnecting technology to fully integrate a TSMC 0.18 μm RF CMOS chip with a silicon carrier where high Q MEMS inductors and CPWs are fabricated in-house. With a better layout design and process optimization, the technology has shown its great potential for RF MEMS heterogeneous chip integration applications.

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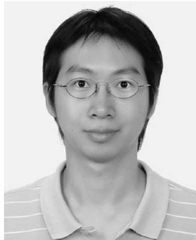

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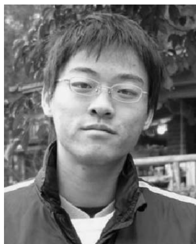

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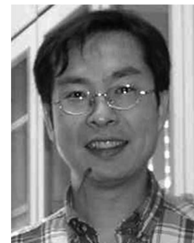

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