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Asymmetric gate capacitance and dynamic characteristic fluctuations in 16 nm bulk MOSFETs due to random distribution of discrete dopants

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Abstract

Characteristic variability of a transistor is a crucial issue for nanoscale metal-oxide-semiconductor field-effect transistors (MOSFETs). In this study, we explore the asymmetric sketch of the random dopant distribution near the source end and the drain end in 16 nm MOSFETs. Discrete dopants near the source and drain ends of the channel region induce rather different fluctuations in gate capacitance and dynamic characteristics. Based upon the observed asymmetry properties, a lateral asymmetry channel doping profile engineering is then proposed to suppress the random-dopant-induced characteristic fluctuations in the examined devices and circuits. The results of this study indicate that the fluctuations in average gate capacitance, circuit gain, 3 db bandwidth and unity-gain bandwidth for the cases with dopants near the drain side could be simultaneously reduced by 62.6%, 22.2%, 63.1% and 41.4%, respectively. Consequently, such a lateral asymmetry channel doping profile could be considered to design intrinsic parameter fluctuation resistant transistors.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The gate lengths of scaled metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the sub-30 nm for 45 nm node high-performance circuit design [1]. Moreover, the devices with sub-10 nm gate lengths have been currently investigated [2–5]. For the radio-frequency/mixed-signal applications, a cutoff frequency higher than 200 GHz has been also reported [6, 7]. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, etc, are known as indispensable components of the circuit design methodology [8–12].

As geometries of MOSFET shrink, the intrinsic device parameter variations such as line edge roughness [13], the granularity of the polysilicon gate [14, 15], random discrete-dopant effects [16–32] have brought significant impacts on device characteristic fluctuations; it is imperative to model and mitigate them in silicon technology. Furthermore, various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion and thermal annealing, have induced significant fluctuations in the electrical characteristics in nanometer scale (nanoscale) MOSFETs. The number of dopants is of the order of tens in the depletion region of a nanoscale MOSFET whose influence on device characteristic is large enough to be distinct [16]. Various random dopant effects have been recently studied in both experimental and theoretical approaches [16–32]. Fluctuations in characteristics are caused not only by a variation in an average doping density, which is associated with a fluctuation in the number of impurities, but also with

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a particular random distribution of impurities in the channel region. Diverse approaches have recently been reported to study fluctuation-related issues in semiconductor devices [16–30] and a digital integrated circuit [31–35]. So far, the attention is mostly drawn on the fluctuations in threshold voltage and dc characteristics. However, the investigation of intrinsic fluctuation in gate capacitance and dynamic characteristics due to random dopant placement is still not clear.

In this study, a large-scale 3D 'atomistic' device-circuit-coupled simulation is performed on a parallel computing system [36–41] to analyze the discrete-dopant-induced gate capacitance and dynamic characteristic fluctuations for the tested 16 nm MOSFET and circuit. Based upon the asymmetric sketch of the random dopant distribution near the source end and the drain end, it is found that discrete dopants near the source and drain ends of a channel region induce rather different fluctuations in gate capacitance and dynamic characteristics. This asymmetry property is utilized to design a lateral asymmetry channel doping profile for the reduction of random-dopant-induced characteristic fluctuations. Consequently, fluctuations in average gate capacitance, circuit gain, 3 db bandwidth and unity-gain bandwidth for the cases with dopants near the drain side are reduced by 62.6%, 22.2%, 63.1% and 41.4%, respectively. The lateral asymmetry channel doping profile could be considered to design intrinsic parameter fluctuation resistant transistors. Notably, the statistically sound analyzing methodology was quantitatively verified with the experimentally measured data of 20 nm CMOS [22–26] for the best accuracy.

The paper is organized as follows. In section 2, we brief the analyzing technique for studying the random dopant effect in a nanoscale device and circuit. In section 3, we examine the discrete-dopant-induced characteristic fluctuations in the 16 nm MOSFET devices and circuits. Finally, we draw conclusions and suggest future work.

2. The computational procedure

The original channel doping concentration of a device is 1.48×10^{18} cm^{-3}. It has a 16 nm gate, a silicon oxide gate thickness of 1.2 nm and a mid-gap metal gate with a workfunction of 4.4 eV. The generation approach for discrete-dopant cases follows our previous work [21–27]. Outside the channel, the doping concentrations in the source/drain and background in silicon are 1.1×10^{20} cm^{-3} and 1×10^{15} cm^{-3}, respectively. Inside the channel region, to consider the effect of random fluctuation in discrete channel dopants, 758 dopants are first randomly generated in an (80 nm)^3 cube, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in figures 1(*a*)–(*d*). The generation of a dopant distribution is totally randomly from computer simulation program. This completely randomized dopant generation of three dimensions can ensure the nominal doping concentration to be 1.48×10^{18} cm^{-3} (=758 dopants/(80 nm)^3). Then the (80 nm)^3 cube is partitioned into 125 sub-cubes of (16 nm)^3, where the dopants may vary from 0 to 14 (the average number = 6) within its sub-cubes. We define the channel doping profile in the (16 nm)^3 cube only, as shown in the cube of figure 1(*b*). For the channel dopant distribution outside the (16 nm)^3 sub-cube, definitely, the channel dopants will appear outside the defined (16 nm)^3 sub-cube. However, since the operation of MOSFET is through surface conduction, the influence of such channel dopants should be not significant in random dopant fluctuation. These sub-cubes are then equivalently mapped into the three-dimensional (3D) device channel region, shown in figure 1(*e*). All statistically generated discrete dopants are incorporated into the large-scale 3D 'atomistic' simulation under parallel computing system [39]. The quantum mechanically corrected transport simulation is performed by solving a set of 3D density-gradient equation coupling with drift-diffusion equations. Figure 1(*f*) shows the tested circuit for exploring the discrete-dopant-fluctuated high-frequency characteristics. To properly estimate the discrete-dopant-fluctuated high-frequency characteristics, due to lack of a well-known compact model of 16 nm MOSFET for circuit simulation, a 3D device- and circuit-coupled simulation with discrete dopants is conducted. Notably, only channel dopants are treated discretely: the doping concentrations remain continuous in the source/drain region because the volume of source/drain dopants is significantly larger than that of channel region [26]. This approach allows us to focus on the study of characteristic fluctuations induced by the random-dopant number and position in the channel simultaneously.

As for the generation of lateral asymmetry doping, the adapted near-drain-end and near-source-end channel doping profiles are shown in figure 1(*g*). Only half of the channel is doped and 758 dopants are randomly generated in a large rectangular solid (gate width, source–drain direction, channel depth: 40 nm × 80 nm × 80 nm). Therefore, the effective channel doping concentration is still 1.48×10^{18} cm^{-3}. Then the large cube is partitioned into 125 sub-cubes ((8 nm) × (16 nm) × (16 nm)) and mapped into the drain end of a channel region for discrete-dopant simulation. Similarly, the dopants in sub-cubes may vary from 0 to 14 (the average number is 6) within its sub-cubes, as shown in figure 1(*h*). To estimate the device characteristics on the same basis, the threshold voltage for both the original MOSFETs and the asymmetric MOSFETs are calibrated.

3. Results and discussion

In this section, the discrete-dopant-induced threshold voltage (V_{th}), gate capacitance (C_g) and high-frequency circuit characteristics fluctuations are first analyzed. Then 500 discrete-dopant-fluctuated transistors are classified into the cases of the near-source end and near-drain end for the studying of the asymmetry sketch of characteristics fluctuations. Then a lateral asymmetry doping profile is implemented to examine the associated fluctuation suppression technique.

3.1. Asymmetric device characteristic fluctuations

Figure 2(*a*) shows the total gate capacitance ($C_{g,total}$) versus the drain bias (V_D) for all discrete-dopant-fluctuated devices,

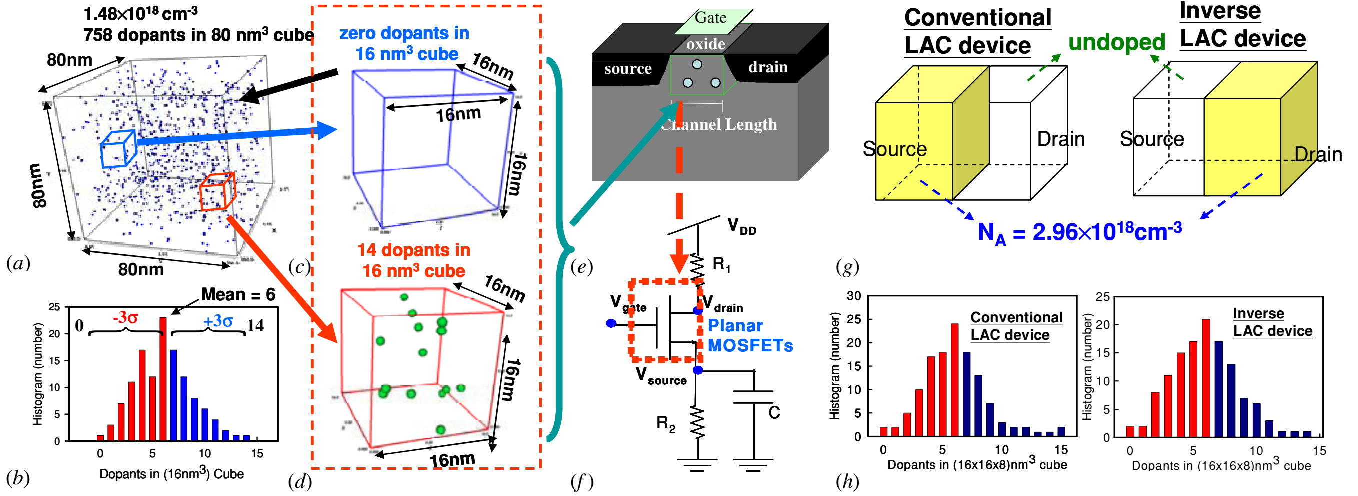

Figure 1. (*a*) Discrete dopants randomly distributed in the (80 nm)^3 cube with the average concentration of 1.48×10^{18} cm^{-3}. There will be 758 dopants within the cube, but dopants may vary from 0 to 14 within its 125 sub-cubes of (16 nm)^3, ((*b*)–(*d*)). The sub-cubes are equivalently mapped into the channel region for device and device-circuit-coupled simulation as shown in (*e*) and (*f*). The doping profile and distribution of discrete dopants for the LAC and inLAC structures are illustrated in (*g*) and (*h*).

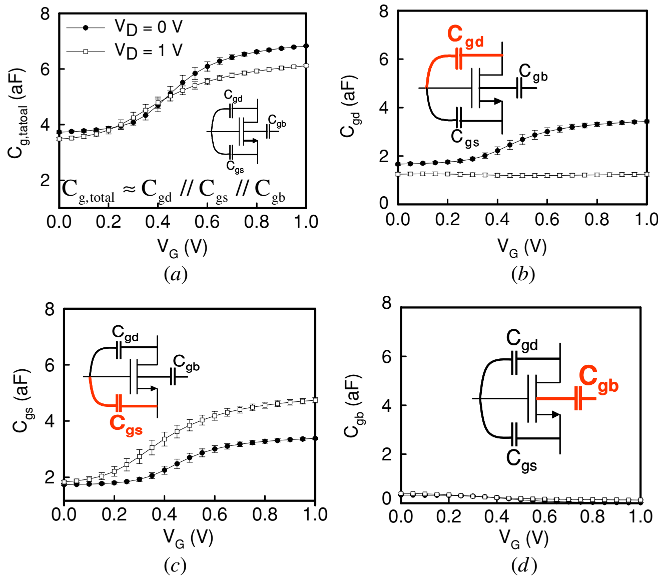

Figure 2. (*a*) The total gate capacitance ($C_{g,\text{total}} = C_{gd} \mathbin{//} C_{gs} \mathbin{//} C_{gb}$), where aF = 10^{-18} F; (*b*) gate-drain capacitance (C_{gd}); (*c*) gate-source capacitance (C_{gs}); (*d*) gate-bulk capacitance (C_{gb}) of all discrete-dopant-fluctuated 16 nm-gate planar MOSFETs, where the symbol and error bar denote the characteristics of normal case and fluctuation, respectively.

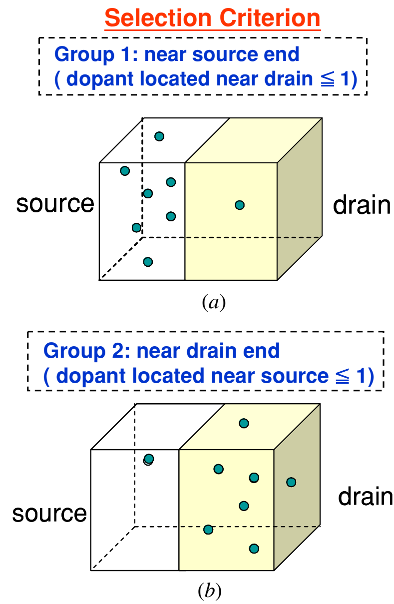

Figure 3. The discrete-dopant-fluctuated devices are then classified into two groups: (*a*) devices with dopants near the source end and (*b*) devices with dopants near the drain end.

where the symbol and error bar denote the characteristics of normal case and fluctuation, respectively. $C_{g,\text{total}}$ results from the shunt of the gate-drain capacitance (C_{gd}), the gate-source capacitance (C_{gs}) and the gate-bulk capacitance (C_{gb}). Figures 2(*b*)–(*d*) show the components of C_{gd}, C_{gs} and C_{gb}; as V_D changes from 0 V (open circles) to 1 V (fill-in circles), C_{gd} and the fluctuation of C_{gd} (σC_{gd}) are decreased due to the widerness of the depletion layer near the drain junction and the effect of channel pinch-off, as displayed in figure 2(*b*). Then C_{gs} and its fluctuation are increased, as shown in figure 2(*c*). As for C_{gb}, the fluctuation is small enough to be neglected, as shown in figure 2(*d*). The drain bias-induced different variations in C_{gd} and C_{gs} are observed, and the dependence of C_g on different V_D motivates the design of a lateral asymmetry doping profile along the source-drain direction.

We generate 500 discrete-dopant-fluctuated transistors exploiting similar approach, as shown in figures 1(*a*)–(*e*), and classify them into two groups according to the random distribution of discrete dopants: the cases of dopants near the source end and the drain end, as shown in figure 3, where the inset describes the selection criteria. To strengthen and make the phenomenon clear, the difference between dopant numbers near the source end and the drain end must be larger than 2. There are 105 and 122 cases correspond to the cases of

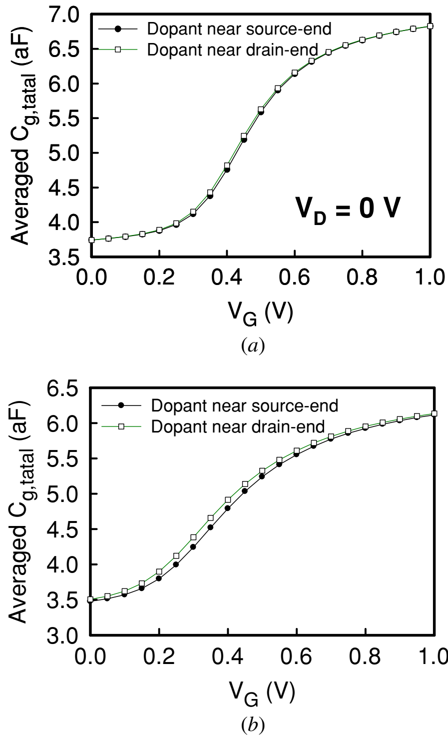

Figure 4. (*a*) Average of total gate capacitance ($C_{g,\mathrm{total}}$) at (*a*) $V_D = 0$ V and (*b*) $V_D = 1$ V.

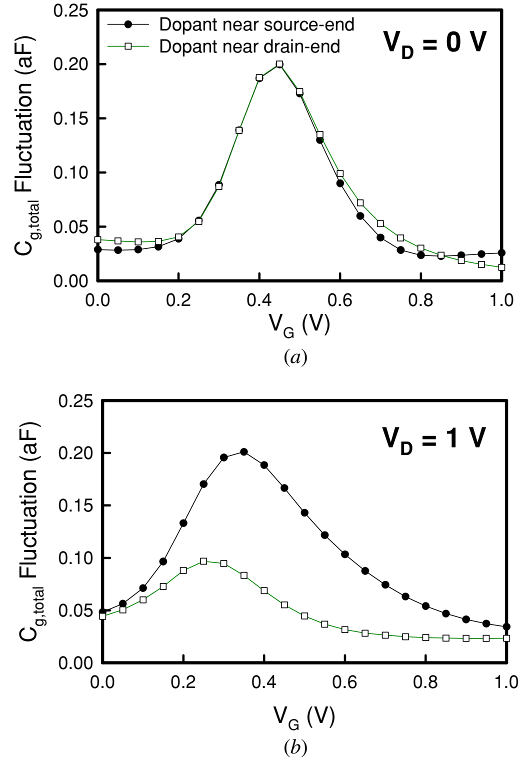

Figure 5. Fluctuations of total gate capacitance at (*a*) $V_D = 0$ V, (*b*) $V_D = 1$ V.

dopants near the source end and the drain end. For the cases of the near-source end, the selection criterion is that a device has more than three dopants in the near-source-end channel but with zero or one dopant locating near the other end. The cases of the near-drain end are then selected accordingly. The effects of discrete dopants near the source end and the drain end on fluctuations in gate capacitances and high-frequency characteristics are then examined. For the devices with $V_D = 0$ V, figure 4(*a*) presents the average total gate capacitance versus the gate bias for the discrete dopants near the source end and the drain end, respectively. Both the cases of dopants near the source end and the drain end exhibit a quite similar *C–V* characteristics under $V_D = 0$ V and $V_D = 1$ V, as shown in figure 4(*b*). Though the total *C–V* characteristics of the two groups are very similar, the fluctuation in the total *C–V* curves is outright different, as shown in figures 5(*a*) and (*b*). For devices with $V_D = 0$ V, as shown in figure 5(*a*), both the cases of dopants near the source end and the drain end exhibit resembling characteristic fluctuation. However, for devices at the bias of $V_D = 1$ V, as shown in figure 5(*b*), $\sigma C_{g,\mathrm{total}}$ of the cases of dopants near the source end show a significantly large fluctuation, compared with the cases of dopants near the drain end. Therefore, the corresponding σC_{gd} and σC_{gs} of devices with $V_D = 0$ V and 1 V are further calculated. σC_{gd} and σC_{gs} of devices with $V_D = 0$ V, as shown in figure 6, indicate that σC_{gs} is more pronounced and becomes a major source of fluctuation for the devices with the cases of dopants near the source end. Similarly, σC_{gd} dominates the fluctuation in gate capacitance for the devices with the cases of dopants near the drain end. The random dopants located near the source end or the drain end in the devices' channel exhibit different C_{gd} and C_{gs} characteristics in spite of the same $C_{g,\mathrm{total}}$ and $\sigma C_{g,\mathrm{total}}$. Notably, the drain bias will induce different characteristics in C_{gd} and C_{gs}, as discussed in figure 2. The fluctuations in C_{gd} and C_{gs} for devices with $V_D = 1$ V are calculated, as shown in figure 7; for a device under a strong drain bias, the fluctuation in C_{gd} is significantly reduced, as shown in figure 7(*a*), compared with the result of figure 6(*a*). In contrast, the fluctuation in C_{gs}, as shown in figure 7(*b*), is increased, in contrast with the result of figure 6(*b*). We observe that the fluctuation in C_{gd} is below 0.1 aF, as shown in figure 7(*a*). Therefore, for the devices with the cases of dopants near the drain end, since the major source of fluctuation is contributed by C_{gd}, $\sigma C_{g,\mathrm{total}}$ is well controlled. However, for the devices with the cases of dopants near the source end, the major source of fluctuation, that is the fluctuation in C_{gs}, could not be reduced.

Besides the fluctuation of various components in gate capacitance, we further compare the discrete-dopant-induced threshold voltage fluctuation (σV_{th}) of the conventional lateral asymmetric channel (LAC) device which has high channel concentration near the source end [42] and the inverse lateral asymmetric channel (inLAC) device which has high channel concentration near the drain end, as shown in figure 8. '*x*' and '*o*' indicate the distribution of threshold voltage versus the dopant number for the conventional LAC and inLAC devices, where the doping profiles of the conventional LAC and inLAC devices have been illustrated in figures 1(*g*) and (*h*). The calculation of threshold voltage here is determined from a current criterion for the drain current larger than 10^{-7} (W L^{-1})

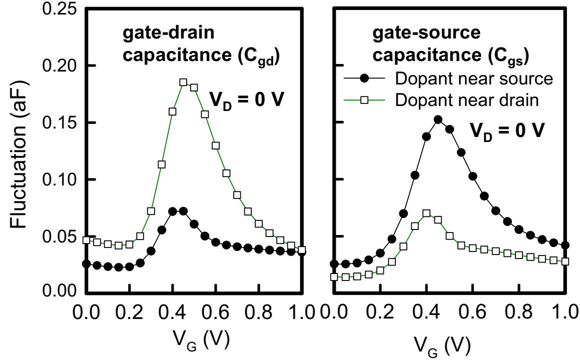

Figure 6. Fluctuations in C_{gd} and C_{gs} at $V_D = 0$ V. The major sources of fluctuation in dopant-near-drain and dopant-near-source devices are contributed from C_{gd} and C_{gs}, respectively.

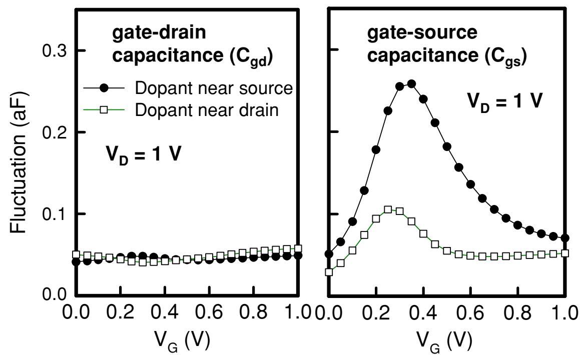

Figure 7. Fluctuations in C_{gd} and C_{gs} at $V_D = 1$ V, where the C_{gd} fluctuations are well controlled.

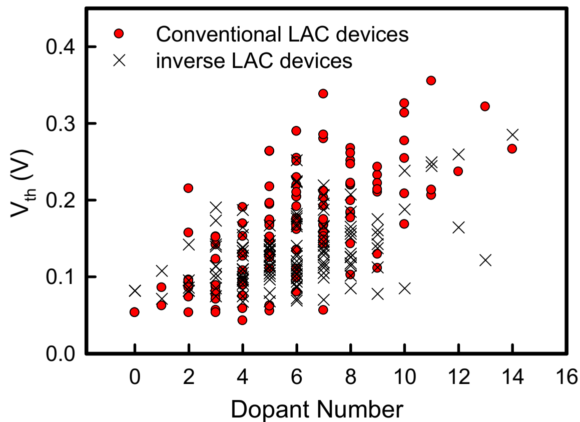

Figure 8. Comparison of the σV_{th} fluctuations for the LAC and inLAC structures.

A. σV_{th} of the proposed inLAC device is 1.6 times smaller than the conventional LAC device because of the smaller current variation for dopants near the drain end of channel. Therefore, an analog circuit, as shown in figure 1(*f*), using the proposed inLAC device is implemented and compared with planar MOSFETs (where the MOSFETs are with symmetric channel doping) to estimate the dynamic characteristic fluctuations.

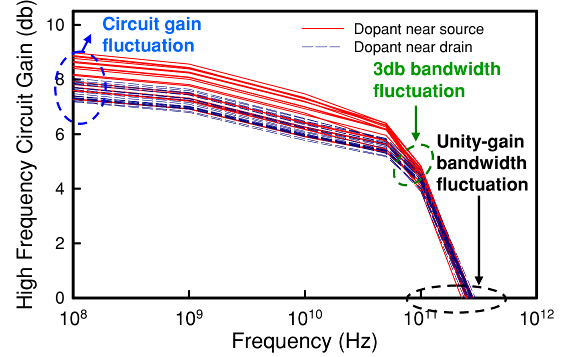

Figure 9. High-frequency response of the studied devices. The solid lines are due to the results of devices with random dopants near the source side and the dash lines are due to the results near the drain side.

Table 1. DC and high-frequency characteristic fluctuations for devices with the original doping profile.

V_{th} (mV)	I_{on} (*A*)	I_{off} (*A*)	$g_{m,\max}$ (*S*)
58.5	6.7 × 10^{-7}	9.5 × 10^{-9}	2.1 × 10^{-7}
C_g (×10^{-3} fF)	Gain (dB)	3dB bandwidth (Hz)	Unity-gain bandwidth (Hz)
0.24	0.465	9.63 x10^{9}	2.93 × 10^{10}

3.2. Dynamic characteristic fluctuations in circuit

This subsection presents the implication of device variability in a common source amplifier. At first, we have compared the devices with dopants near-drain end and with dopants near-source end in figure 9. The near-drain end case exhibits better immunity against RDF. The high-frequency characteristic fluctuation in circuit gain, 3 db bandwidth and unity-gain bandwidth for the device with dopants located near the source end are 1.7, 1.9 and 1.1 times larger than those with dopants near the drain end. Therefore, the dc, gate capacitance and high-frequency characteristic fluctuations in the inLAC device and original planar device are further explored. As listed in table 1, the discrete-dopant-induced dc and high-frequency characteristics' fluctuations for device with the original doping profile are summarized [4]. The fluctuations in threshold voltage, gate capacitance and circuit gain is 58.5 mV, 0.24 fF and 0.465 dB, respectively. Figures 10(*a*) and (*b*) explores the I_D–V_G and C_g–V_G characteristics of the discrete-dopant-fluctuated inLAC (dashed lines) and the original (solid lines) devices, respectively. The spreading range of the lateral asymmetry doping profile is reduced, which implies the suppression of the dc and C_g characteristic fluctuations. Figure 11(*a*) shows the V_{th} fluctuations of the studied devices, where '*x*' and '*o*' indicate the cases of the inLAC and original devices, respectively. The scattering range of V_{th} for the proposed inLAC devices is significantly smaller than original cases. V_{th} fluctuation is reduced by 21.8%. Figures 11(*b*)–(*d*) show the on-state current (I_{on}), off-state current (I_{off}) and maximum transconductance ($g_{m,\max}$) versus the dopant number, respectively. The fluctuations of I_{on} and $g_{m,\max}$ are reduced by 32.3% and 25.4%, due to the less injection current fluctuation induced by near-source dopants.

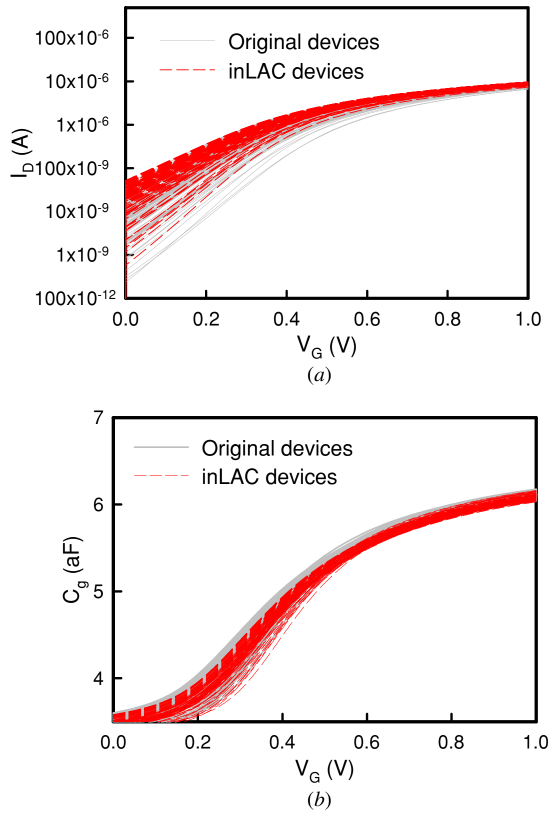

Figure 10. Comparison of (*a*) I_D–V_G and (*b*) gate capacitance fluctuations in the discrete-dopant-fluctuated 16 nm gate cases generated from the proposed inLAC devices (dashed line) and devices with the original doping profile (solid line).

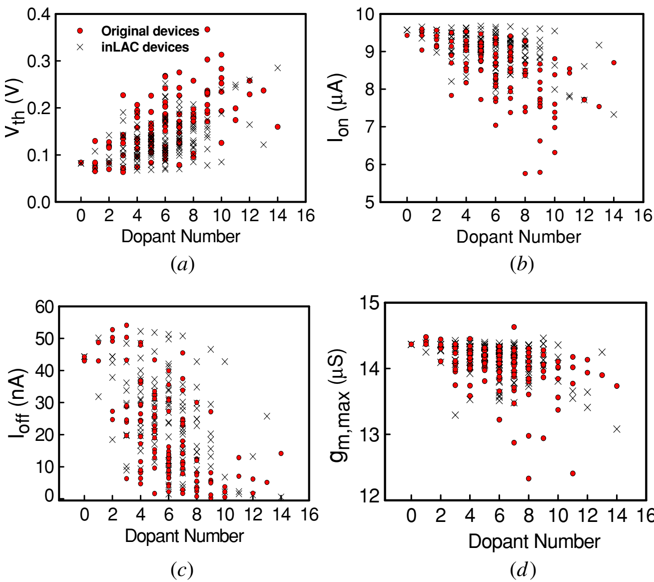

Figure 11. Fluctuations in (*a*) V_{th}, (*b*) I_{on}, (*c*) I_{off} (*d*) and $g_{m,\max}$ of the 125 discrete-dopant-fluctuated 16 nm gate planar MOSFETs, where '*x*' and '*o*' indicate the cases of the inLAC and original devices, respectively.

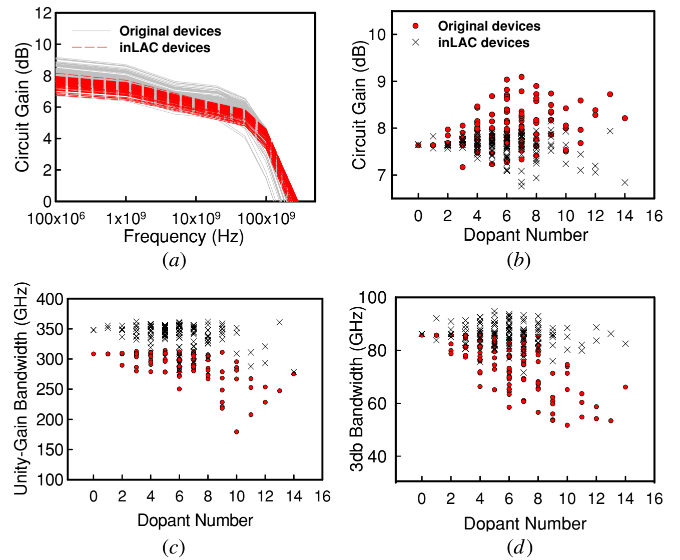

Figure 12. Comparison of (*a*) frequency response fluctuations, (*b*) circuit gain, (*c*) 3 db bandwidth (*d*) and unity-gain bandwidth fluctuations in the 125 discrete-dopant-fluctuated 16 nm gate planar MOSFET circuit with inLAC and original devices.

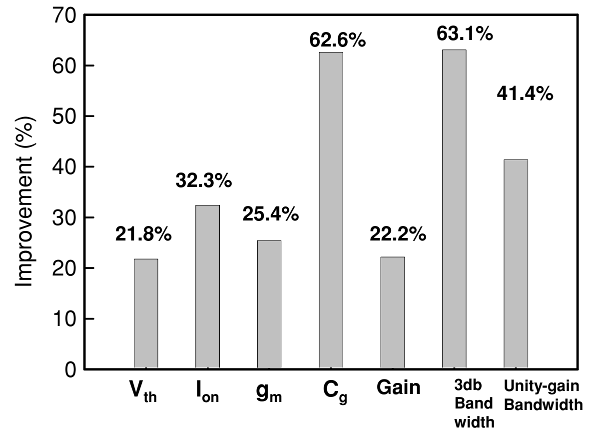

Figure 13. The effectiveness of the fluctuation suppression in both the 16 nm device and the common source amplifier circuit, compared with the results of the original device and circuit.

The high-frequency response of the nano-MOSFET circuit is then studied in figure 12(*a*), where the solid lines show devices with the original doping profile and the dashed lines show the inLAC devices. The spreading range of the inLAC devices is reduced significantly. As shown in figures 12(*b*)–(*d*), the high-frequency characteristic fluctuations, the circuit gain, the 3dB bandwidth and the unity-gain bandwidth are reduced by 22.2%, 63.1% and 41.4%, respectively for the inLAC devices. The effectiveness of fluctuation suppression on the explored inLAC devices and circuits is summarized in figure 13. Notably, since the 3dB bandwidth is proportional to C_g [27], the 3 dB bandwidth and C_g have similar fluctuation suppression. We have discussed several advantages of the proposed inLAC devices in dc and dynamic characteristics and their associated fluctuation suppression; however, the fluctuation of I_{off} is still large, as shown in figure 11(*c*), due to the weakened channel controllability, compared with the device with the original doping profile.

4. Conclusions

In this paper, the asymmetric scenario of random dopants distributed near the drain end of a channel in a 16 nm MOSFET has been advanced using a statistically sound 3D device-circuit-coupled 'atomistic' simulation. The device with dopants near the drain end exhibits less characteristic fluctuations due to the well-controlled major fluctuation source of C_{gd}. The fluctuations of average gate capacitance, circuit gain, 3dB bandwidth and unity-gain bandwidth for the cases of dopants near the source end are substantially larger than those near the drain end. Moreover, in contrast to the device with the original doping profile, the fluctuations of V_{th}, I_{on}, g_m, C_g, circuit gain, 3dB bandwidth and unity-gain are simultaneously reduced by 21.8%, 32.3%, 25.4%, 62.6%, 22.2%, 63.1% and 41.4%, respectively. According to comparative examinations and discussions throughout this study, the proposed inLAC device demonstrates very different fluctuation behaviors of dc and dynamic characteristics, compared with the conventional LAC device and original planar device, which may be used for the design of novel sub-20 nm MOSFETs. This study provides an insight into the design of a doping profile to suppress the random-dopant-induced characteristic fluctuations and shows the design trade-off between performance and fluctuation. The gate leakage is extremely important for a MOSFET with the silicon oxide gate and we will study the gate leakage fluctuation in our future work. Moreover, we believe that the mismatch of threshold voltage in the larger circuit such as two-stage amplifier and LNA circuits will significantly impact the performance in the future. We are currently studying doping profile optimization for the proposed inLAC devices to reduce the fluctuation in I_{off}.

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